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Simple and Performing Temperature-Compensated Voltage References

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Abstract – The paper proposes four new reference voltage sources (VR) based on the cross-connected current mirrors. The temperature coefficient of the two of proposed VR is smaller than 3 ppm/°C over the temperature range of 0…100ºC and the total transistor count is reduced. These performances result by using the first- and second-order temperature compensation techniques and resistors having a particular temperature coefficient. The process and temperature variations of the reference voltage were minimized by optimal design of resistors width; thus, for a CMOS 0.35-µm process, one gets less than 1% variation.
Keywords: CMOS voltage reference, cross-connected current mirrors, process and temperature variation

I. INTRODUCTION

The basic schematics of the CMOS simple voltage reference (VR) using cross-connected (i.e. self-biased) current mirrors are shown in Fig.1 [1]. The bottom mirror, transistors M_1, M_2 and resistor R_1, is either a modified Wilson or a Widlar one. The temperature coefficient (*TC*) of these VR is rather poor [2]. The use of these schemes remained in the current reference (CR) domain [2], [3].

This paper is focused on performance improvement, keeping the complexity of the circuit low. To this end we use a circuit technique applied previously for first- and second-order temperature compensation (FOTC, respectively SOTC) of the branch current of a CR, see Fig.2 [4]. This CR uses a modified-Widlar bottom mirror and a "reverse"-Widlar upper one; the resistors are designed based on the FOTC and SOTC conditions of the I_1 branch current. Similar temperature compensation technique has been used for CR with modified Wilson-type bottom mirror [5] and "total" (I_1+I_2) CR [6].

Table 1 lists the performance and circuit complexity of the several reported in literature references, for comparison. The bracketed values were estimated by authors through graph analysis and/or conversion.

The implementation given in [9] uses a cross-connected peaking current source and a simple current mirror, a weak inversion operation, and temperature compensation by resistor-ratio method. This represents the VR simplest solution (4 transistors and 2 resistors) which has excellent *SR* and *PSRR* parameters but its *TC* is rather poor (62 ppm/ºC).

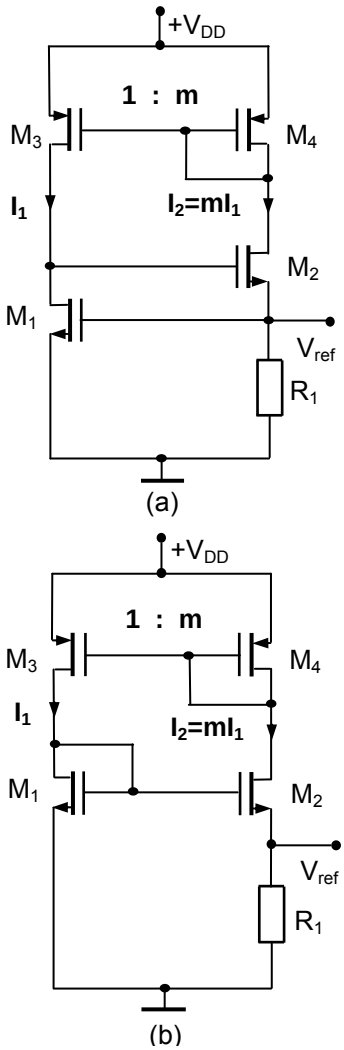

Fig.1. Self-biased VRs using (a) a Wilson mirror, and (b) a Widlar mirror.

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Table 1. Performances of some reported VR

Reference	CMOS process	Component total number	Reference voltage	Equivalent temperature coefficient (TC)	Temperature range	Process and temperature (P&T) total variation	Supply regulation SR	Low frequency PSRR
	[μm]		[mV]	[ppm/°C]	°C	[%]	[ppm/V]	[dB]
[3]	0.35	>41	800	2.1	−50...120			
[7]	0.6	>25	1140	5.3 (trim.)	0...100		(2180)	47
[8]	0.5	>43	631	17 (trim.)	−40...125	7 0.25 (trim.)		
[9]	0.35	6	580	62	0...70		(118)	84
[10]	0.35	13	670	10	0...80	(18.6)	(2700)	52
[11]	0.35	17	1211	3	6...90	(34)	4400	
[12]	0.18	31	657	10	0...150		(2700)	55
[13]	0.18	18	1012	4	−25...100		(176)	75
[14]	0.16	>80	1087	12 (trim.)	−40...125	1.6 0.28 (trim.)	(290)	70

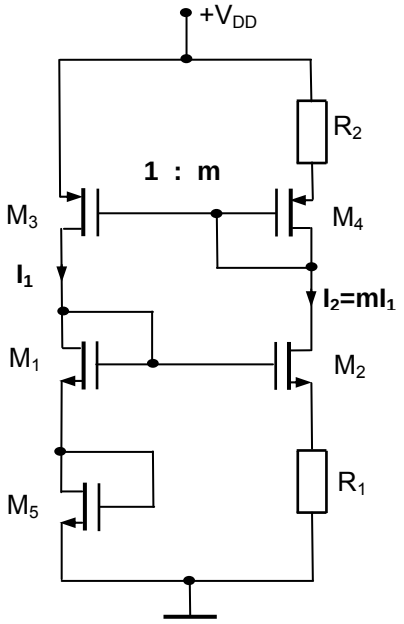

Fig.2. Fiori-Crovetti CR [4].

In our work the FO and SO temperature compensation technique introduced in [4] is applied to the VR source simple circuits in Fig.1. The use of a peaking current source for the upper current mirror is also proposed and discussed.

The main characteristics of the VRs proposed in this paper are: a) circuit simplicity – 4-5 transistors and 2 resistors, b) *TC* low value and c) small *P&T* total variation (see Table 2).

The analytic treatments in this paper suppose that all transistors operate in saturation, their output resistance is infinite and the drain current is given by the square-law dependency. Thus, for transistor M_k one can write

$$I_{Dn,p} = \beta_{n,p}\alpha_k \left(V_{GSk} - V_{Tn,p}\right)^2 \qquad (1)$$

where $\beta_{n,p} = \mu_{n,p}C_{ox}/2$, $\alpha_k = W_k/L_k$.

II. VR1 BASED ON MODIFIED WILSON MIRROR

The proposed VR1 circuit is presented in Fig.3a where the output reference voltage represents the voltage drop on the R_1 resistance. A similar topology is described in [5] for a CR with FO and SO temperature compensation.

Without the resistor R_3 one gets only FOTC and medium level performances. The use of the resistor R_3 is needed only for a SOTC and a good-performance design.

A. VR1 First-Order Temperature Compensation (VR1-FO)

In this case R_3=0 and the upper mirror is a simple one. The output is the drop voltage on the Wilson mirror resistance:

$$V_{ref} = I_2R_1 = mI_1R_1 = V_{GS1} \qquad (2)$$

The V_{ref} equation results after some algebra:

$$mR_1\mu_nC_{ox}\alpha_1V_{ref}^2 - 2\left(1+V_{Tn}mR_1\mu_nC_{ox}\alpha_1\right)V_{ref} + V_{Tn}^2mR_1\mu_nC_{ox}\alpha_1 = 0 \qquad (3)$$

Writing the left part of (3) as a five variable temperature function

$$\mathrm{f}(T) = \mathrm{f}\left(V_{ref}, V_{Tn}, \mu_n, R_1, m\right), \qquad (4)$$

the relative *TCs* for these five variables, defined as

$$k_v = (dv/v)/dT, \qquad (5)$$

are related by the following equation:

$$\frac{\partial \mathrm{f}}{\partial V_{ref}}V_{ref}k_{Vref} + \frac{\partial \mathrm{f}}{\partial \mu_n}\mu_nk_{\mu n} + \frac{\partial \mathrm{f}}{\partial V_{Tn}}V_{Tn}k_{VTn} + \frac{\partial \mathrm{f}}{\partial R_1}R_1k_{R1} + \frac{\partial \mathrm{f}}{\partial m}mk_m = 0 \qquad (6)$$

The condition for a FOTC of V_{ref} is equivalent to $k_{Vref} = 0$.

The reference voltage, $V_{ref\,\mathrm{VR1\text{-}FO}}$, if the FOTC condition is fulfilled, results from (6) by inserting the corresponding partial derivatives of (4):

$$V_{ref\,\mathrm{RV1\text{-}FO}} = V_{Tn}\left[1 + 2k_{VTn}\Big/\left(k_{\mu n} + k_{R1} + k_m\right)\right]. \qquad (7)$$

The R_1 value results from equations (1) and (6), for given values of the current I_1 and the branch-current ratio m.

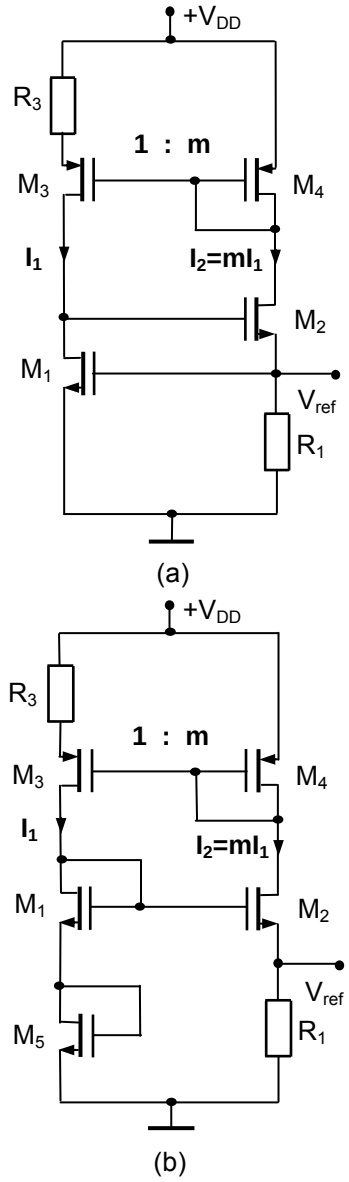

Fig.3. a) VR1 schematic (bottom mirror: modified Wilson mirror), b) VR2 schematic (bottom mirror: modified Widlar mirror).

A 0.35µm process provides TC_s k_{VTn} and $k_{\mu n}$ of negative value. In the case of FOTC only k_m is positive but of negligible value (of the order of 0.0275×10^{-3}/ºC). A reduced V_{ref} is desired, when the supply voltage V_{DD} is reduced too. This situation is attained with a resistor R_1 of negative TC (k_{R1}<0), the same sign as $k_{\mu n}$. In this case the quantities in numerator and nominator are both negative and V_{ref} will be positive and minimal. The resistor R_1 value is also significantly reduced, needing smaller chip area.

For the TC values in the considered process [5], [6]: $k_{VTn}=-1.83\times10^{-3}$/°C, $k_{\mu n}\approx-6.05\times10^{-3}$/°C, $k_{R1}=-2.84\times10^{-3}$/°C (poly n+ resistor) and for V_{Tn}=0.82 V it results V_{ref}=1.16 V.

B. VR1 Second-Order Temperature Compensation (VR1-SO)

The SOTC of VR1 can be obtained by modifying the upper current mirror by insertion of the resistor R_3. This method was previously used for CR source [5], to realize SOTC of the branch current I_1. To the same goal [4], a reverse-Widlar mirror (with R_2, Fig.2) has been used. This method makes it possible to get a convenient negative value for the TC k_m, of the branch-current ratio m. k_m is given [5], by

$$k_m = \left(1 - \sqrt{\alpha_4\Big/\left(m\alpha_3\right)}\right)\left(k_{\mu p} + 2k_{R3}\right). \qquad (8)$$

Since $k_{\mu p}\approx-5\times10^{-3}$/°C, $k_{R3}=1.6\times10^{-3}$/°C (for n+ diffused resistor) and fulfilling the condition $m\alpha_3>\alpha_4$ [5], k_m becomes negative, resulting in SOTC reference voltage. The TC value of the k_m parameter depends on α_3/α_4 ratio and m, while m on α_1 and R_3.

The above discussion is also valid for the proposed VR1. The analytical approach developed in [4], and applied in [5] and [6], for the CR branch or "total" current SOTC, can be used to get the VR1-SO (by evaluation of the second-order TC of m (k_{mm}). However, because of the imprecise values of the second-order TC_s of V_{Tn}, μ_n, μ_p, R_1, R_3 and m, the analytical approach provides a rather inaccurate result.

Consequently it is more convenient to optimize the design for SOTC by simulation, by iteratively adjusting the α_1, the α_3/α_4 ratio and the value of the resistance R_3, and checking up the reference voltage versus temperature. The initial state of the iteration process is the FOTC VR. There is only some iteration needed to complete the optimization process. The optimization criterion is the final form of the voltage-temperature diagram, given in Fig. 4, which assures the minimum total variation of the reference voltage across the temperature range.

The equivalent TC of the output voltage V_{ref} of the VR1-FO results, by simulation, of the order of 22 ppm/°C.

The simulation of the V_{ref} versus temperature dependence of the VR1-SO was based on the following values: α_1=0.5 µm/ 8.13 µm, α_2=24 µm/5 µm, α_3=24 µm/5 µm, α_4=20 µm/0.5 µm, R_1=80 kΩ (NTC type with $k_{R1}=-2.84\times10^{-3}$/°C), R_3=35 kΩ (PTC type with $k_{R3}=1.6\times10^{-3}$/°C), V_{DD}=3.3 V.

The optimized simulated V_{ref} versus temperature (branch-current ratio m=33) of the VR1-SO is presented in Fig.4. The VR1-SO total variation of V_{ref} over the specified temperature domain is 0.028%, corresponding to an equivalent TC of only 2.8 ppm/°C, see Table II.

The $P\&T$ total variation was measured between the V_{ref} values in BC (best case) and WC (worst case) process corners. The $P\&T$ total variation was minimized by iteratively sequential adjustment of the width of R_1 and R_3 resistors with the additional bonus

of minimizing the resistors' chip-area.
The VR1 minimum supply voltage is 2.7 V and the supply current is 15.8 µA. The *SR* parameter value of 2430 ppm/V (measured at V_{DD}=3.3 V) is acceptable.

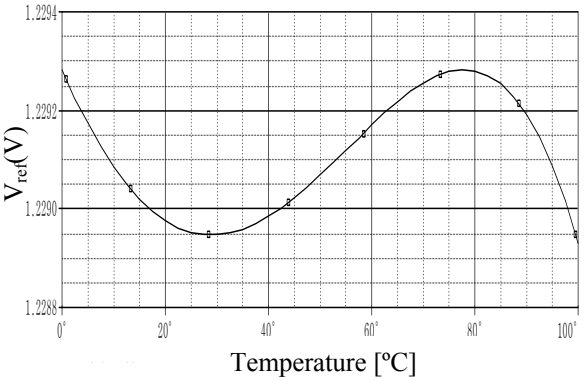

Fig.4. VR1-SO output voltage, V_{ref} versus temperature.

III. VR2 BASED ON MODIFIED WIDLAR MIRROR

The voltage reference source VR2, see Fig. 3b, is derived from CR source with SOTC of the branch current I_1 (Fig.2) [4], by replacing the upper current mirror by a normal Widlar one; the output voltage is the voltage drop on the resistor R_1.
If R_3=0, only FOTC is possible; this case corresponds to a known circuit [4]. A much better performance can be obtained by using the resistor R_3; in that case the SOTC of the reference voltage V_{ref} becomes possible.

A. VR2 First-Order Temperature Compensation (VR2-FO)

The upper mirror is a simple one (R_3=0). For the circuit lower loop (Fig.3b) one can write:

$$V_{ref} = I_2 R_1 = mI_1 R_1 = V_{GS1} + V_{GS5} - V_{GS2} \qquad (9)$$

and, following [4]:

$$V_{ref} - V_{Tn} - \sqrt{I_1/\beta_n}\left[1/\sqrt{\alpha_1} + 1/\sqrt{\alpha_5} - \sqrt{m/\alpha_2}\right] = 0 \; . \qquad (10)$$

Substituting $I_1=V_{ref}/mR_1$ we get after some algebra:

$$mR_1\mu_n C_{ox} V_{ref}^2 - 2\left(x^2 + V_{Tn} mR_1 \mu_n C_{ox}\right) V_{ref} + V_{Tn}^2 mR_1 \mu_n C_{ox} = 0 \qquad (11)$$

where

$$x = 1/\sqrt{\alpha_1} + 1/\sqrt{\alpha_5} - \sqrt{m/\alpha_2} \; . \qquad (12)$$

The equation (11) is similar to (3). It can be written, as in Section II, in the form (6) because x is a function of m.
Following the same approach as in the case of $V_{ref\,\text{VR1-FO}}$ in Section II, the FOTC reference voltage $V_{ref\,\text{VR2-FO}}$ results as:

$$V_{ref\,\text{VR2-FO}} = V_{Tn}\left[1 + \frac{2k_{VTn}}{k_{\mu n} + k_{R1} + \left(1 + \sqrt{m/\alpha_2}/x\right)k_m}\right] . \qquad (13)$$

The Section II analysis, related to R_1 and k_{R1} are valid too.
Using the same parameters values as for $V_{ref\,\text{VR1-FO}}$ one gets $V_{ref\,\text{VR2-FO}}$=1.15 V because of the small value of the k_m parameter for FOTC and the factor

$$1 + \sqrt{m/\alpha_2}/x \approx 1.8 \ldots 2.2 \; . \qquad (14)$$

B. VR2 Second-Order Temperature Compensation (VR2-SO)

The SOTC is realized using a Widlar mirror for the upper current mirror ($R_3 \neq 0$ in Fig.3b). The use of resistor R_3 allows one to get a convenient negative value for k_m (k_m depends on α_3/α_4 ratio and m, while m on α_1 and R_3).
The mathematical analysis of the SOTC is rather laborious and complex (it is similar to the one presented in [4], [5] and [6] for the RC branch or "total" current). It requires the knowledge of the second-order *TC* of the variables V_{Tn}, μ_n, μ_p, R_1, R_3 and m, which has imprecise numerical values. Thus, the SOTC α_5, α_3/α_4 and R_3 values, resulted by manual analysis, will differ much from the values established by simulation.
Consequently these parameters will be optimized by iteratively simulation of the circuit, targeting the $V_{ref}=V_{ref}(T)$ total variation minimization over the specified temperature range as in Fig.4.
The equivalent *TC* of the output voltage, V_{ref}, of the VR2-FO results, by simulation, close to 25 ppm/ºC.
The simulation of the V_{ref} versus temperature dependence of the VR2-SO was based on the values: α_1=6.4 µm/5 µm, α_2=20 µm/5 µm, α_3=24 µm/5 µm, α_4=40 µm/5 µm, α_4=0.5 µm/2.07µm, R_1=80 kΩ (*NTC* type with $k_{R1}=-2.84\times10^{-3}$/°C) and R_3=79 kΩ (n^+ diffused, *PTC*, $k_{R3}=1.6\times10^{-3}$/°C), V_{DD}=4 V.
The optimized simulated V_{ref} versus temperature of the VR2-SO (branch-current ratio m=8.65) has a form as that in Fig.4. The total variation of V_{ref} over the specified temperature domain is 0.016%, corresponding to an equivalent *TC* of only 1.6 ppm/ºC, see Table 2.
The *P&T* total variation was measured between the V_{ref} values in BC (best case) and WC (worst case) process corners and is smaller than 4%. The *P&T* total variation was minimized using the same approach as in Section II, by iteratively sequential adjustment of the resistors' width.
The VR2 minimum supply voltage is 2.8 V and the supply current is 15.8 µA. The *SR* parameter, measured at V_{DD}=3.5 V, has a satisfactory value of 2650 ppm/V.

IV. VR3 BASED ON PEAKING AND WILSON MIRRORS

The proposed VR3 (Fig.5a) is another new cross-connected-mirror voltage reference where the upper mirror is a peaking current one, and the bottom mirror

Table 2. Performances of proposed VR variants

This work version	CMOS process	Component total number	Reference voltage	Equivalent temperature coefficient (*TC*)	Temperature range	Process and temperature (P&T) total variation	Supply regulation SR
	[µm]		[mV]	[ppm/°C]	°C	[%]	[ppm/V]
VR1-SO	0.35	6	1229	2.8	0…100	18.2	2430
VR2-SO	0.35	7	1133	1.6	0…100	<4	2650
VR3-SO	0.35	6	628	6.75	0…100	<1.1	790
VR4-SO	0.35	6	632	47	0…100	0.9	2000

is a modified-Wilson one. The peaking current mirror was previously used [11] as bottom current mirror, cross-connected with a simple current mirror. But, his reference-voltage variation with temperature (Table 1) is too large for precision applications.

The VR3 FOTC is realized by the design of the transistor M_1 and resistor R_1 of the bottom mirror, using the approach described in Section II.

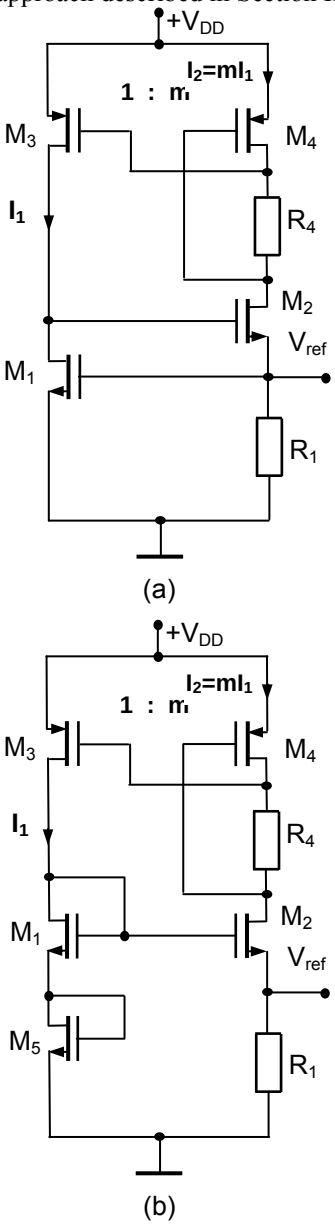

Fig.5. a) VR3 based on peaking and modified Wilson mirrors
b) VR4 based on peaking and modified Widlar mirrors

The mathematical analysis of the VR3-FO (with R_4=0, see Fig.5a) is similar to the VR1-FO and VR2-FO analysis performed in Section II, respectively III.

By using the upper peaking mirror it is possible to achieve a "partial" SOTC (unlike the optimal compensation in Sections II and III) and the transistors in the left branch of VR3 are operating in the weak-inversion, at very small drain current. The analysis of VR3-SO (with $R_4 \neq 0$) is not presented, being too complex and imprecise. This is similar to the CR analysis performed in [4], [5] and [6].

The simulation of the dependence V_{ref} versus temperature of the VR3-SO was based on the values: α_1=0.55 µm/5 µm, α_2=25 µm/5 µm, α_3=8 µm/5 µm, α_4=40 µm/5 µm, R_1=60 kΩ, R_4=40 kΩ (both of *NTC* type), V_{DD}=3.5 V. The $V_{ref}(T)$ dependence of the VR3-SO is presented in Fig.6. Because of the dome shaped dependence the SOTC is considered "partial". Here, the full optimization (this means a shape of the $V_{ref}(T)$ like in Fig.4) is not possible. The total variation of V_{ref} over the specified temperature domain is 0.0675%, corresponding to an equivalent *TC* of 6.75 ppm/°C.

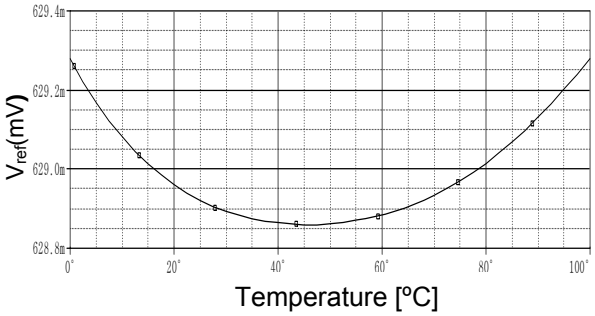

Fig.6. VR3-SO output voltage, V_{ref} versus temperature.

It is important to underline the small value of the *P&T* total variation better than 1.1%. It was measured between the V_{ref} values in BC (best case) and WC (worst case) process corners. This value corresponds to particular resistor widths and is so small thanks to the strong negative feedback realized in the peaking-mirror loop. Surely, the weak inversion operation of some transistors contributes to this performance.

The minimum supply voltage of the VR3-SO is 1.9 V, V_{ref}=628 mV, and the supply current is 10.5 µA. The SR parameter has a very good value of 790 ppm/V (measured at V_{DD}=3.5 V) and of 1050 ppm/V (measured at V_{DD}=2.5 V), promising a good PSRR at low frequency too.

V. VR4 BASED ON PEAKING AND WIDLAR MIRRORS

The VR4 has a bottom modified-Widlar current mirror (Fig.5b). The VR4 FOTC, is realized by the design of the transistor M_1 and resistor R_1 of the bottom mirror. The upper peaking mirror can accomplish only a partial SOTC. The RV4 left branch transistors operate at the limit of weak-inversion.

The simulation of the V_{ref} versus temperature dependence of the VR4-SO was based on the values: α_1=10 µm/5 µm, α_2=20 µm/5 µm, α_3=20 µm/5 µm, α_4=40 µm/5 µm, α_5=1.42 µm/5 µm, R_1=80 kΩ, R_4=40 kΩ (both of *NTC* type), V_{DD}=3.5 V.

The temperature dependence of the VR4-SO is similar as the presented in Fig.6 one, showing a partial SOTC. The VR4-SO total variation of V_{ref} over the specified temperature range is 0.47%, resulting in an equivalent *TC* of 47 ppm/°C.

The *P&T* total variation is only 0.9%, which constitutes an excellent performance. The minimum supply voltage is 1.9 V, V_{ref}=632 mV and the supplied current is 8 µA. The SR parameter, measured at V_{DD}=3.5 V, attains 2000 ppm/V.

VI. CONCLUSIONS

This work introduced four new simple and performing RVs based on cross-connected current-mirror combinations where, the bottom mirror is a modified-Wilson or a modified-Widlar type, while the superior mirror is a Widlar or a peaking type.

The FOTC, good enough for some applications, is implemented by the bottom current mirror by conveniently design its transistors and resistor.

The SOTC (fully optimized for VR1 and VR2, but only partially for VR3 and VR4) is implemented by means of the upper mirror (M_3 and M_4) by conveniently design of the transistors' size ratio α_3/α_4, the resistor R_3 or R_4, and re-designing the size of the bottom mirror transistors (α_1 or α_5).

An analytic derivation of the FOTC condition is presented for the VR1 and VR2. This derivation can be used with appropriate changes for VR3 and VR4.

The SOTC optimization for the described VRs is realized by simulation. The sequence of SOTC finding is rather simple and expedient. The used optimization criterion [6] targets the realization of close to cosine shape of the $V_{ref}(T)$ dependency, extended (1+0.25) "periods" over the proposed operating temperature range. Thus, the total reference-voltage variation becomes minimal.

The performance level that can be obtained even with simple circuits are in some cases spectacular (see Table 2 in comparison with Table 1). For example, the VR2 exhibits an excellent equivalent *TC* (1.6 ppm/°C) together with a reduced reference-voltage *P&T* total variation (<4%) and VR3 provides a good equivalent *TC* (6.75 ppm/°C) together with a spectacular reference-voltage P&T total variation (<1.1%) and a good SR parameter.

A small reference-voltage *P&T* total variation is also important from the point of view of the complexity of the trimming circuitry (a reduced *P&T* translates in fewer trimming bits).

But, at this small P&T variation, the component-mismatching effect must be considered too and thus, a Monte Carlo simulation becomes important.

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