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Novel Nonlinear Digital Controller for a Buck Converter with Dead Beat Characteristic

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Abstract – The static and dynamic characteristics of buck converters are well known for a long time. An easy approximation results in a first order transfer function in discontinuous conduction mode (DCM). Based on the description in DCM in time domain the controller is designed to compensate a load step using a nonlinear algorithm for the calculation of the duty cycle. The result is a controller with dead beat characteristic. Because in theory the controller needs only one clock cycle for compensation the controller is a member of the one-cycle controllers.

Keywords: nonlinear control, dead beat controller.

I. INTRODUCTION

The static and dynamic characteristics of buck converters are well known for a long time. Usually the controller design can be subdivided into several steps: modeling the converter, calculation of small signal transfer function and controller design using bode plots [1], [2]. Doing this buck converters are controlled using second a order controller with one operational amplifier. A good controller design is based on the K-factor method [3], [4].

Additionally, there are some controller design procedures based on the time domain characteristics. There are different types of current mode control like peak current mode or sliding mode control [5], [6].

In this paper a new approach of the controller design is proposed for the discontinuous conduction mode of a buck converter. Unlike the controllers mentioned above the control law is nonlinear. This is a result of the nonlinear characteristic in discontinuous conduction mode (DCM). Based on the time-domain description the control law is derived in a way that a load step is compensated in one clock cycle.

II. TIME-DOMAIN CHARACTERISTICS IN DISCONTINUOUS CONDUCTON MODE

For the controller design the knowledge of the time-domain waveforms is essential. The power circuit of a buck converter is shown in Fig. 1. The components of the circuit are assumed to be ideal.

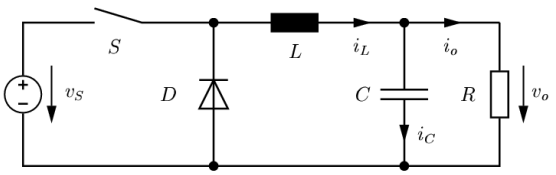

Fig. 1: Power circuit of a buck converter

In DCM the output voltage v_o of a buck converter depends on the input voltage v_s, the duty cycle d, the clock frequency f_c, the inductor L and the load current i_o or the load resistor R. Fig. 2 shows the waveforms of the inductor voltage and current. Furthermore, the dynamic depends on the load, because the main time constant is RC, where C is the output capacitor and R is the load resistance.

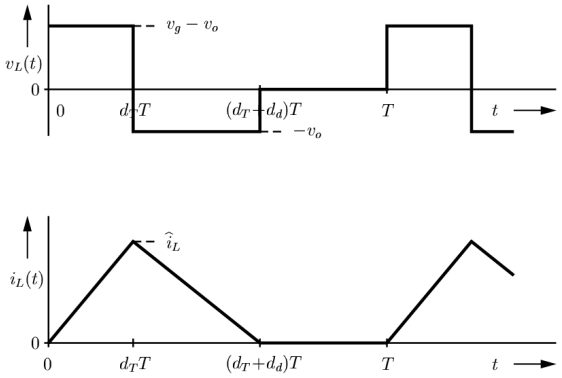

Fig. 2: Inductor current and voltage waveforms in DCM.

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The slopes of the inductor current correspond with the inductor voltage. The inductor voltage is

$$v_L(t) = \begin{cases} v_s - v_o & for \quad 0 \le t \le d_T T \\ -v_o & for \quad d_T \le t \le (d_T + d_d)T \\ 0 & for \quad (d_T + d_d)T \le t \le T \end{cases}$$

In this equation $d_T T$ is the on-time of the switch S and $d_d T$ the conducting time of the diode D in a clock period. Every clock period begins with switching on the switch under the condition $i_L = 0$. So the peak value of the inductor current can be calculated using the integral of the inductor voltage.

$$\hat{i}_L = \frac{1}{L} \cdot (v_s - v_o) \cdot d_T \cdot T$$

Under steady state conditions the average value of the inductor current (voltage second balance) is zero. Therefore we can derive that

$$\frac{1}{L} \cdot (v_s - v_o) \cdot d_T \cdot T = \frac{1}{L} \cdot v_o \cdot d_d \cdot T \quad .$$

Solving this equation for the relative conducting time of the diode after canceling the clock period T and the inductance L gives

$$d_d = d_T \cdot \frac{v_s - v_o}{v_o} \quad .$$

So the charge transferred to the output can be calculated quite simple because of the triangular waveform.

$$Q_L = \int_0^T i_L(t)\, dt = \frac{1}{2} \cdot \hat{i}_L \cdot (d_T + d_d) \cdot T$$

Inserting the peak value of the inductor current and the relative conducting time of the diode yields:

$$Q_L = \frac{1}{2L} \cdot (v_s - v_o) \cdot d_T \cdot T^2 \cdot \left(d_T + d_T \cdot \frac{v_s - v_o}{v_o} \right)$$

Finally the expression is simplified resulting in:

$$Q_L = (d_T \cdot T)^2 \cdot \frac{v_s - v_o}{2L} \cdot \frac{v_s}{v_o} .$$

So the charge can be calculated using the input voltage, the output voltage and the duty cycle with the clock period respectively the transistor on time without measuring currents.

III. CONTROLLER DESIGN

Measuring the output voltage and the input voltage the controller can calculate the difference between the load current at the actual clock cycle and the last clock cycle. In Fig. 1 the current law is

$$i_L(t) = i_C(t) + i_o(t) \quad .$$

Integrating this equation over one clock period yields

$$Q_L = \Delta Q_C + Q_o \quad ,$$

where Q_L is the charge transferred by the inductor to the output circuit, ΔQ_C is the change of the capacitor charge and Q_o is the charge transferred to the load resistor. Under steady state conditions all signals are periodic. Because of the charge balance in the capacitors the average values of capacitor currents are zero. So under steady state conditions the value of ΔQ_C is zero, too. The voltage across the output capacitor is calculated by

$$Q_C = C \cdot v_o \quad .$$

As a consequence the voltage change is

$$\Delta v_o = \frac{1}{C} \cdot \Delta Q_C = \frac{1}{C} \cdot (Q_L - Q_o) \quad .$$

In every cycle the charge transferred from the source to the load is known, as shown before, if the source voltage is measured. The remaining values, namely the output voltage, the duty cycle, the clock period and the inductance are known anyway. The charge transferred through the inductor is Q_L. An output voltage variation is also caused by a change of the load charge Q_o. So the new load resistance can be calculated without measuring the current. The new charge transferred via the inductor in the next clock cycle is calculated via the new load resistance, respectively the new load charge (corresponding to one clock cycle), adding the charge necessary to bring the output voltage exactly to the required value.

$$Q_o = Q_L + \Delta Q_C = Q_L + C \cdot \Delta v_o \quad ,$$

$$Q_{L,new} = Q_o + C \cdot (v_{ref} - v_o) \quad ,$$

where v_{ref} indicates the reference value of the output voltage. So the new duty cycle is:

$$d_{T,new} = \frac{1}{T} \cdot \sqrt{Q_{L,new} \cdot \frac{2L}{v_s - v_o} \cdot \frac{v_o}{v_s}} \quad .$$

This formula results from the last equation of section II, if the equation is solved for the duty cycle.

Knowing the load charge Q_o, the load current and the load resistance can be estimated as:

$$i_o^* = \frac{Q_o}{T}$$

$$R^* = \frac{V_o}{I_o^*} = \frac{V_o \cdot T}{Q_o}$$

The calculations above do not consider the voltage drop of the diode, transistor and inductor or any other losses.

IV. SIMULATION RESULTS

The theory in the previous section was tested using a simulation in MATLAB/SIMULINK. The model is shown in Fig. 3. The straightforward calculation of the controller routine is shown in Fig. 4. The model is based on the state-space description of the buck converter. The model contains a very easy pulse width modulator. The diode in the buck converter was modeled by a saturation of the integrator, which integrates the inductor voltage. This causes a limitation of the inductor current at zero.

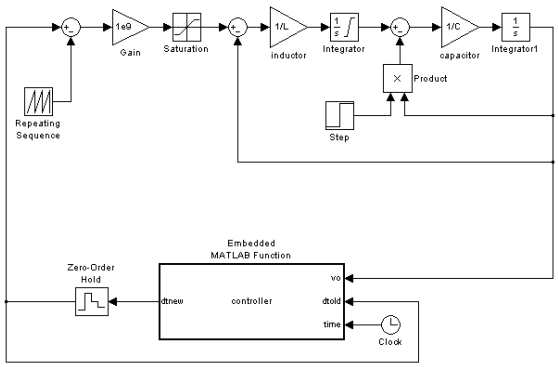

Fig. 3: Simulink model of the simulation.

The components and parameters were:

$L = 24\ \mu H,$

$C = 40\ \mu F,$

$f_T = 100\ kHz,$

$v_s = 20\ V,$

$v_{ref} = 12\ V.$

Fig. 5 shows the waveforms of the inductor $i_L(t)$, the output voltage $v_o(t)$ reduced by 10 V and the duty cycle d_T. The simulation shows a load step from a load resistance of $R = 50\ \Omega$ to $R = 30\ \Omega$ at $t = 0$.

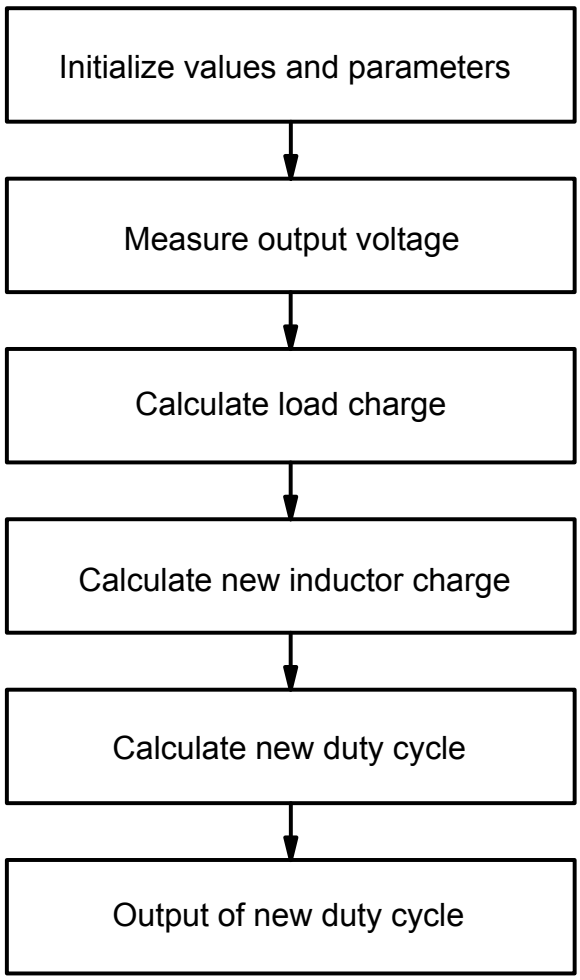

Fig. 4: Controller routine

The load step is corrected within one clock cycle. One clock cycle is needed to notice the load step due to a voltage decreasing. At $t = T$ the controller sets the duty cycle to a higher value for one clock cycle to take into account the higher output current and to correct the decreased output voltage. In the following clock cycle, beginning at $t = 2\ T$, the duty cycle is constant with an increased value according to the higher output current. Fig. 6 shows the estimated value of the load resistance.

The calculated duty cycles were:

before load step:	0.294
compensating clock period:	0.449
steady state duty cycle after load step:	0.379

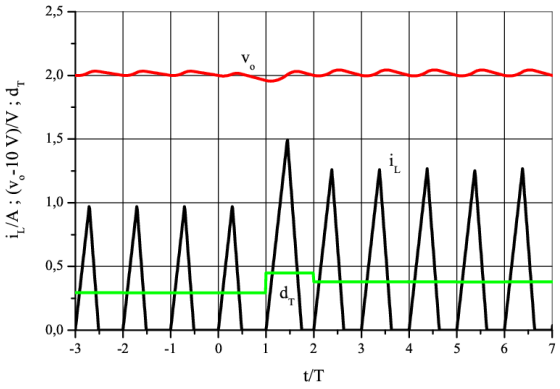

Fig. 5: Simulation of a load step in DCM.

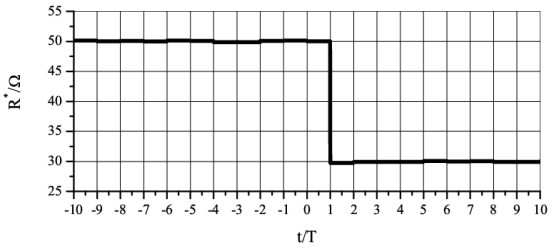

Fig. 6: Estimated load resistance

V. CONCLUSION

A novel nonlinear controller was introduced, based on the time-domain description of the DCM operating mode of a buck converter.

The advantages of the proposed controller are:

- very fast response time: within one clock period a load step is compensated.
- dead beat characteristic: as an advantage of a digital controller the converter has no exponential transients.
- transferable strategy to other converter types, like boost converter or buck-boost converters.
- the algorithm is based on a straightforward calculation without iterations or similar procedures.
- feed forward of the source voltage: because of taking into account the source voltage while calculating the duty cycle, a feed forward of the source voltage is automatically included.
- voltage measurement: the calculation of the duty cycle for the actual clock cycle only requires the measurement of the voltages. So current probes for current measurements are not needed. This simplifies the circuit, and, which is more important, reduces costs.

The disadvantages of the proposed controller are:

- nonlinear algorithm: if the microcontroller is not powerful enough, the duty cycle can be stored in a two dimensional array.
- unsynchronized load step: if the load step occurs not at the beginning of a clock cycle, the controller needs two clock cycles for compensation, because the load charge calculation, or the load resistance calculation respectively, will be wrong one clock cycle after the load step.
- DCM: the controller works best in discontinuous conduction mode, before and after the load step and during the compensation clock cycle.

The simulation verifies the controller design approach. A load step is compensated within one clock period. Future activities can optimize and extend the controller performance. Possible key points could be:

- application of the design to other converter types, like boost or buck-boost.
- consideration of the voltage drop of the diode and other losses.
- implementation of the algorithm using a microcontroller or DSP.

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