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CMOS Multiplier Circuit with Improved Linearity

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Abstract-An original voltage multiplier circuit will be presented. The circuit is implemented in $0.35\mu m$ CMOS technology and, in order to improve its frequency response, it is based exclusively on MOS transistors working in saturation region. The utilization of a FGMOST (Floating Gate MOS Transistor) for replacing the classical MOS devices allows obtaining an important reduction of the circuit complexity and, as a result, of the silicon occupied area. The SPICE simulation using the previous mentioned technological parameters confirms the theoretical estimated results, showing an excellent linearity of the new proposed CMOS voltage multiplier circuit.

Keywords: equivalent FGMOS device, linearization technique, multiplier circuit, second-order effects

I. INTRODUCTION

COMPUTATIONAL circuits and particularly multiplier circuits are important building blocks for telecommunication applications, medical equipments, hearing devices and disk drives [1], [2].

In the bipolar technology, the multiplication function could be easily obtained from the logarithmical characteristic [3] of the bipolar transistor. Important errors still remain because of the nonzero values of the base currents, especially for pnp transistors and of the temperature dependence of the bipolar transistor parameters (the thermal voltage is linear increasing with temperature and the saturation current has an exponential dependence on temperature).

In order to respond to the low-power requirements of the newest CMOS designs, the subthreshold operation of the MOS transistor is an interesting choice. Based on the logarithmical law of a MOS transistor in weak inversion, the implementation of a CMOS current-mode multiplier/divider becomes very simple (even with respect to the bipolar version) and, in consequence, with the result of a smaller silicon area consumption, making the circuit compatible with low-power VLSI designs.

For obtaining an important increasing of the circuit frequency response, many analog signal processing functions can be achieved by employing the square-law model of MOS transistors. Analog circuits based on the square-algebraic identity can be easily realized from the well-known square-law model of the MOS transistors in the saturation region. Based on this principle, several basic building blocks, such as multipliers, active resistors and transconductors have been developed [4] – [6]. The linearity of the basic multiplier still remains poor because of the fundamental nonlinear characteristic of the MOS transistor. Thus, it results the possibility of achieving a relatively good linearity only for a restricted input voltage range, the amplitude of the input voltages being restricted below a few hundreds of mV .

Consequently, it is obviously the necessity of implementing a linearization technique for decreasing the superior-order nonlinearities of the MOS multipliers and for increasing the available range for the input voltage amplitudes. It exists in literature many circuit techniques used to improve the linearity of the MOS differential amplifier (the basic cell of the CMOS multiplier). It was presented in [7] a third and fifth-order harmonics cancellation with good results and a relatively simple circuit implementation. A constant-sum of the gate-source voltages circuit connection was described in [8] and it allows an important reduction of the total harmonic distortions coefficient of the circuit. In [9], it was presented and implemented in CMOS technology a simple technique based on square-root circuits for improving the CMOS differential stage linearity, which compensate the quadratic characteristic of the MOS transistor working in saturation.

An original approach of a CMOS voltage multiplier will be presenting, having the important advantages of an excellent linearity (as a result of compensation the circuit linearity degradation caused by the second-order effects by implementing an original design technique) and of an extreme simplicity achieved by replacing classical MOS devices by a FGMOS transistor. The frequency response of the proposed multiplier circuit will be strongly improved by operating all MOS active devices in the saturation region.

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I. THEORETICAL ANALYSIS

A. *The CMOS implementation of the voltage multiplier circuit*

The original proposed voltage multiplier circuit exploits the well-known quadratic characteristic of the MOS transistor working in saturation. In order to obtain a linear characteristic of the circuit, a perfect symmetrical structure with respect to the two input potentials will be described in Fig. 1a, while the equivalent symbol of the multiplier is presented in Fig. 1b.

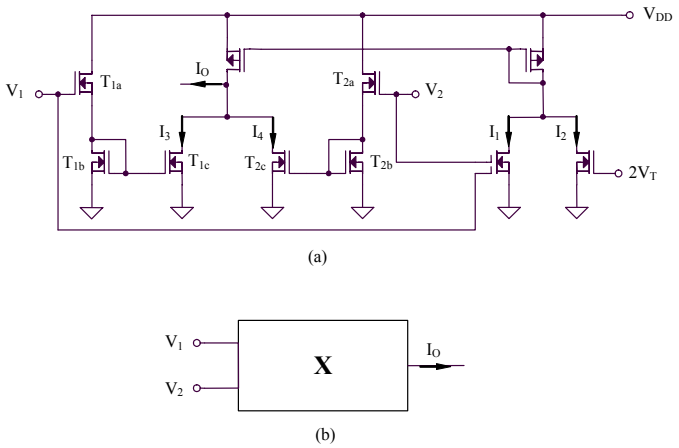

Fig. 1. (a) The CMOS implementation of the multiplier circuit; (b) The equivalent symbol of the multiplier circuit

B. *The FGMOS transistor*

The FGMOS transistor is a MOS transistor whose gate is floating (Fig. 2a), while the symbolical representation of this device is shown in Fig. 2b. The first silicon layer over the channel represents the floating-gate and the second polysilicon layer, located over the floating-gate implements the multiple input gates. This floating-gate is capacitive coupled to the multiple input gates.

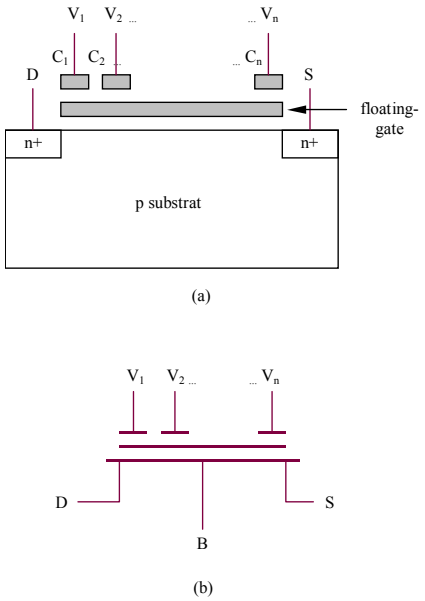

Fig. 2. (a) The basic structure of a n-channel FGMOS transistor; (b) symbolic representation

The drain current of a FGMOS transistor with n-input gates in the saturation region is given by the following relation:

$$I_D = \frac{K}{2}\left[\sum_{i=1}^{n} k_i (V_i - V_S) - V_T\right]^2 \qquad (1)$$

where $K = \mu_n C_{ox}(W/L)$ being the transconductance parameter of the transistor, μ_n is the electron mobility, C_{ox} is the gate oxide capacitance, W/L is the transistor aspect ratio, $k_i, i = 1,...,n$ are the capacitive coupling ratios, V_i is the i-th input voltage, V_S is the source voltage and V_T is the threshold voltage of the transistor. The capacitive coupling ratio is defined as:

$$k_i = \frac{C_i}{\sum_{i=1}^{n} C_i + C_{GS}} \qquad (2)$$

C_i are the input capacitances between the floating-gate and each of the i-th input and C_{ox} is the gate-source capacitance which is equal to $(2/3)C_{ox}$ for operation in the saturation region. All the overlap capacitances are assumed to be considerably smaller than capacitances summation $\sum_{i=1}^{n} C_i + C_{GS}$. Equation (1) shows that the FGMOS transistor drain current in saturation is proportional to

the square of the weighted sum of the input signals, where the weight of each input signal is determined by the capacitive coupling ratio of the input.

C. *The multiplier circuit operating*

Considering a strong inversion (saturation) operation of all MOS devices for improving the circuit frequency response, the output current could be expressed as:

$$I_O = (I_1 + I_2) - (I_3 + I_4) \tag{3}$$

where:

$$I_1 = \frac{K}{2}\left(\frac{V_1 + V_2}{2} - V_T\right)^2 \tag{4}$$

$$I_2 = \frac{K}{2}V_T^2 \tag{5}$$

$$I_3 = \frac{K}{2}\left(\frac{V_1}{2} - V_T\right)^2 \tag{6}$$

$$I_4 = \frac{K}{2}\left(\frac{V_2}{2} - V_T\right)^2 \tag{7}$$

For the previous mathematical relations it results a perfect linearity of the output-computed function:

$$I_O = \frac{K}{2}V_1V_2 \tag{8}$$

D. *Design technique for reducing the circuit complexity*

Strongly and repetitively used in neural networks, the multiplier circuit cell imposes an important part of the entire circuit complexity. Thus, a reduction of the multiplier circuit complexity will be concretized in an approximately equal reduction of the neural network complexity. For this reason, a new method for replacing three classical MOS devices by a FGMOS transistor will be presented in Fig. 3.

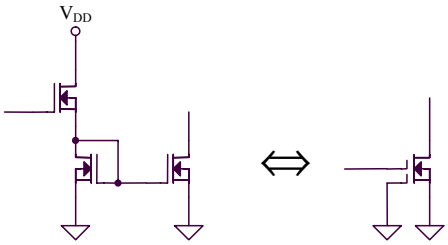

Fig. 3. The replacing of three MOS devices by a FGMOS transistor

E. *The implementation of the threshold voltage extractor circuit*

In order to obtain the linear characteristic (8) of the multiplier, it is necessary to implement a circuit for obtaining a voltage equal to the double threshold of the MOS devices. The circuit, named "threshold voltage extractor circuit", is presented in Fig. 4.

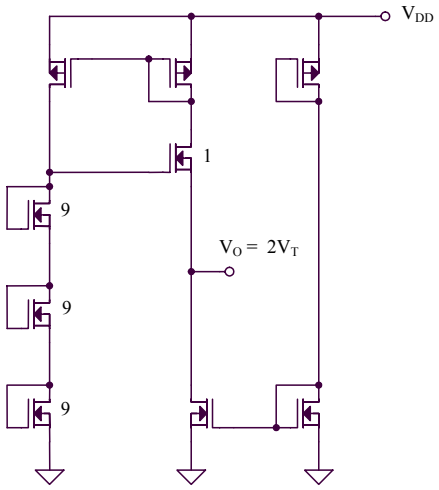

Fig. 4. The CMOS implementation of the voltage extractor circuit

The proposed implementation of the previous circuits presents the important advantage of using exclusively MOS devices, so relative small silicon area consumption could be achieved.

F. *The linearity improvement technique for the multiplier circuit*

The operation of the circuit presented above is affected by the second-order effects that degrade the quadratic law of the MOS transistor. These undesired effects are modeled by the following relations (channel length modulation (9) and mobility degradation (10)).

$$I_D = \frac{K}{2}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \tag{9}$$

$$K = \frac{K_0}{[1 + \theta_G(V_{GS} - V_T)](1 + \theta_D V_{DS})} \tag{10}$$

Considering that the design condition $\lambda = \theta_D$ is fulfilled, the expression (8) of the output current will be affected by superior-order nonlinearities, quantitative evaluated by the following expression:

$$I_O = \frac{K}{2}V_1V_2 + a_1V_1V_2^2 + a_2V_1^2V_2 + a_3V_1V_2 + a_4 \tag{11}$$

where $a_1 - a_4$ are constants with respect to the input voltage variations: $a_1 = -3K\theta_G/16$,

$a_2 = -3K\theta_G / 16$, $a_3 = 3K\theta_G V_T / 4$ and $a_4 = -K\theta_G V_T^3$.

The original idea for reducing the nonlinearity of the multiplier circuit introduced by the second-order effects is based on an anti-parallel connection of two quasi-identical circuits opposite excited. In this case, it is possible to demonstrate that the linearity error could be strongly reduced (with about an order of magnitude). The remaining nonlinearities will be given by the fifth-order errors, neglecting in the previous analysis and having much smaller amplitudes.

I. SIMULATED RESULTS

The SPICE simulation $I_O(V_1,V_2)$ based on $0.35\ \mu m$ CMOS technology parameters for the anti-parallel connected circuit is presented in Fig. 5, showing a linearity error of only $0.5\ \%$ for an extended input range.

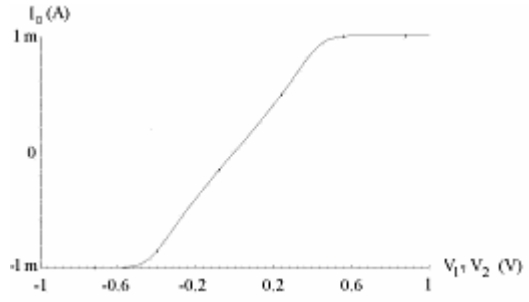

Fig. 5. The SPICE simulation $I_O(V_1,V_2)$

The circuit layout implemented in the same technology is presented in Fig. 6.

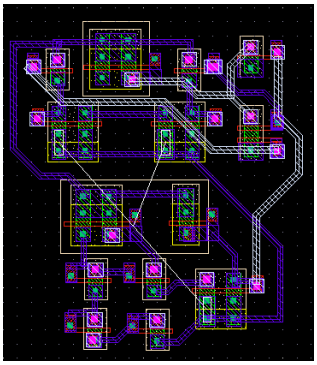

Fig. 6. The layout of the multiplier circuit

IV. CONCLUSIONS

An original voltage multiplier circuit has been presented. The circuit was implemented in $0.35\mu m$ CMOS technology and, in order to improve its frequency response, it was based exclusively on MOS transistors working in saturation region. The utilization of a FGMOST (Floating Gate MOS Transistor) for replacing the classical MOS device allows obtaining an important reduction of the circuit complexity and, as a result, of the silicon occupied area. The SPICE simulation using the previous mentioned technological parameters confirms the theoretical estimated results, showing an excellent linearity of the new proposed CMOS voltage multiplier circuit.

ACKNOWLEDGEMENT

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