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The Micropower Translinear Network Implementation of Rational Approximated and Partial Fractions Decomposed Functions

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Abstract – In this paper is presented a translinear topology suitable for static and dynamic analog signal processing at very low supply voltage. The one variable objective functions, firstly are rational approximated, then decomposed in partial fractions and finally implemented with CMOS translinear networks. Such functions processing have small computational time and leads to the implementations with controllable errors. This topology will be used in structural synthesis program, named TLSS, for automate synthesis of translinear circuits.

Keywords: analog signal processing circuits, translinear circuits, CMOS integrated circuits, low power circuits.

I. INTRODUCTION

Nonlinear objective-functions are widely applied in practical VLSI electronic systems and there are many cases in which the translinear networks are the best solutions of implementation of these. The synthesis of nonlinear networks is a heavy task. However a systematic procedure for the synthesis of translinear circuits was developed by Evert Seevinck [1]. The proposed synthesis method consists in three parts: objective-function approximation, approximate-function decomposition and realization of translinear network for the function obtained after decomposition.

Using at starting point the Seevinck synthesis method in period 199-2004 we developed the algorithms and we realized a few programs in C++ code which permit the automatic synthesis of translinear circuits but only whit bipolar transistors, named TLSS, [2], [3], [4]. From 2006 we analyzed the possibility to improve and extended the program so to be able to automatic syntheses the translinear circuits with MOS transistors. In some papers we already present some types of generic TL networks for objective functions which were rational approximated and decomposed in continued fractions, [5], and polynomial approximated and continued products decomposed, [6]. The reasons for that we decide to develop algorithms and generic networks with MOS transistors is presented in the next paragraph.

In practical CMOS VLSI mixed signal electronic systems the power supply voltage continues to scale down. Future analog circuits will have to operate successfully at supply voltages slightly higher than the MOS threshold voltage. The suitable topologies for signal processing at such low values of supply voltages are the translinear circuits because are operating in current domain and in this way the very small voltage swings are avoided. More, the tranlinear circuits provide insensitiveness to processing and temperature variation, high functional density and well suitability to monolithic fabrication. MOS transistors have exponential current-voltage characteristics in weak inversion (or sub-threshold) region. Therefore in these circuits the MOS transistors will operate in this region. The main problems of this operating region are the relatively low speed capability and inferior matching. But these problems are relatively solved in sub-micron technology.

In this paper is presented a CMOS translinear topology that implements one variable objective functions which was rational approximated and decomposed in partial fractions. Such functions processing have small computational time and leads to the implementations with relatively low number of devices, controllable errors and good stability.

II. THE MOS TRANSISTORS IN WEAK INVERSION

In above section was argued that the MOS transistor in low-voltage translinear circuits will operate in weak inversion.

It is well known the general expression of drain current of MOS transistor [7]:

$$I_D = I_S \cdot \exp\left(\frac{V_P}{V_T}\right) \cdot \left[\exp(-V_S / V_T) - \exp\left(-V_D / V_T\right)\right] \quad (1)$$

or in terms of V_{GS} and V_{GD} as follows

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$$I_D = I_S \cdot \exp\frac{V_P - V_G}{V_T} \cdot \left(\exp\frac{V_{GS}}{V_T} - \exp\frac{V_{GD}}{V_T} \right), \quad (2)$$

where I_S is specific current (limit of weak inversion). The specific current is proportional to W/L, follows explicitly shown

$$I_S \cdot \exp[(V_P - V_G)/V_T] = (W/L) \cdot I_\Diamond(V_G), \quad (3)$$

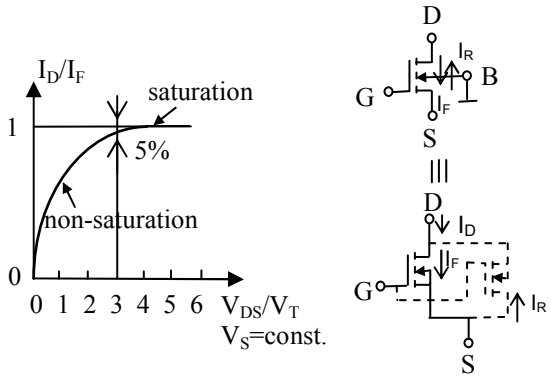
with $I_\Diamond(V_G)$ the zero-bias ($V_{GS} = 0$) current for a square transistor, which represents the body effect. So, the forward and reverse currents become:

$$\begin{aligned} I_F &= (W/L) \cdot I_\Diamond(V_G) \cdot \exp(V_{GS}/V_T) \\ I_R &= (W/L) \cdot I_\Diamond(V_G) \cdot \exp(V_{GD}/V_T) \end{aligned} \quad (4)$$

If $I_R << I_F$, then the MOS transistor is saturated, otherwise the MOS transistor is non-saturated.
In figure 1.a are shown the two operation regions for weak inversion, which are defined by the ratios I_D / I_F and V_{DS} / V_T [7].
Therefore, each of the drain current components (expressed by (4)) of a non-saturated transistor may be relate to an equivalent saturated transistor with gate-source voltage V_{GS} and V_{GD} respectively and the non-saturated transistor may be decomposed into two identical saturated transistors connected anti-parallel [8]. This is symbolically shown in figure 1.b. The transistor that corresponds to reverse current component is shown in dashed line, and represents the effect of the non-saturated operation of the real transistor. This equivalence may be also applied to bipolar transistors, based on the Ebers-Moll model, but it is impractical because of asymmetry of real bipolar transistors

III. THE CMOS TRANSLINEAR IMPLEMENTATION OF RATIONAL APPROXIMATED AND DECOMPOSED IN PARTIAL FRACTIONS FUNCTIONS

The objective-functions are first normalized, so that theirs variables to take values only in interval [-1, 1]. Then the one variable normalizes functions are approximated by using *Padé approximation* or *Chebyshev rational approximation* so that the maximum relative error of approximation to be $0.01\% \div 0.1\%$. Finally, it is changed the x variable of the rational function in auxiliary variable $y = y(x)$ so that $y > 0$, $\forall x \in [-1;1]$.
The result of these processes must be manipulated into products of linear terms in the input and output variables. These linear terms have real coefficients and they must always remain positive for all combinations of input variable values.



a) b)

Figure 1. a) The operation regions in weak inversion of the MOS transistor; b) Non-saturated MOS

In conformity with decomposition algorithm developed by us and presented in [3], the general final form of partial fraction that incorporates all cases that can be encountered in the decomposition process is:

$$\begin{aligned} & f_{ar}(x) = f_{ar0}(x) + f_{ar1}(x) \\ & f'_{ar1}(x) = \frac{p_1 + q_1 \cdot x \pm f_{ar1}(x)}{p_1 + q_1 \cdot x \mp f_{ar1}(x)} \\ & f'_{ar1}(x) = f'_{ar10}(x) + f'_{ar2}(x) \\ & \ldots \\ & f'_{ari}(x) = \frac{p_i + q_i \cdot x \pm f_{ari}(x)}{p_i + q_i \cdot x \mp f_{ari}(x)} \\ & f'_{ari}(x) = f'_{ari0}(x) + f'_{ar,i+1}(x) \\ & \ldots \\ & f'_{ar,n-1}(x) = f'_{arn-1,0}(x) + f'_{arn}(x) \\ & f'_{arn}(x) = \frac{p_n + q_n \cdot x \pm f_{arn}(x)}{p_n + q_n \cdot x \mp f_{arn}(x)} \end{aligned} \quad (5)$$

The functions $f_{ar0}(x), f'_{ari0}(x), i = 1,\ldots,n-1$ and $f'_{arn}(x)$ are functions that have denominator polynomials with real roots only positionated out of variation range of input variable, x. The form of these decomposition functions is:

$$\begin{aligned} z_{i0} = & \frac{(A_{11})_i}{(x - x^*_{i,1})^{\alpha^*_{i,1}}} + \frac{(A_{12})_i}{(x - x^*_{i,1})^{\alpha^*_{i,1}-1}} + \frac{\left(A_{1\alpha^*_{i,1}}\right)_i}{(x - x^*_{i,1})} + \\ & + \frac{(A_{21})_i}{(x - x^*_{i,1})^{\alpha^*_{i,2}}} + \ldots + \frac{\left(A_{2\alpha^*_{i,2}}\right)_i}{(x - x^*_{i,2})} + \ldots + \\ & + \frac{\left(A_{n^i_r,1}\right)_i}{(x - x^*_{i,n^i_r})^{\alpha^*_{n^i_r}}} + \ldots + \frac{\left(A_{n^i_r,\alpha^*_{n^i_r}}\right)_i}{(x - x^*_{i,n^i_r})^{\alpha^*_{n^i_r}}} = \sum_{k=1}^{n^i_r} \sum_{j=1}^{\alpha^*_{i,k}} z_{kj} \end{aligned} \quad (6)$$

$$z_{kj} = \left(A_{kj}\right) \Big/ \left(h_{i,k}\right)^{\alpha^*_{ik} - j + 1}$$

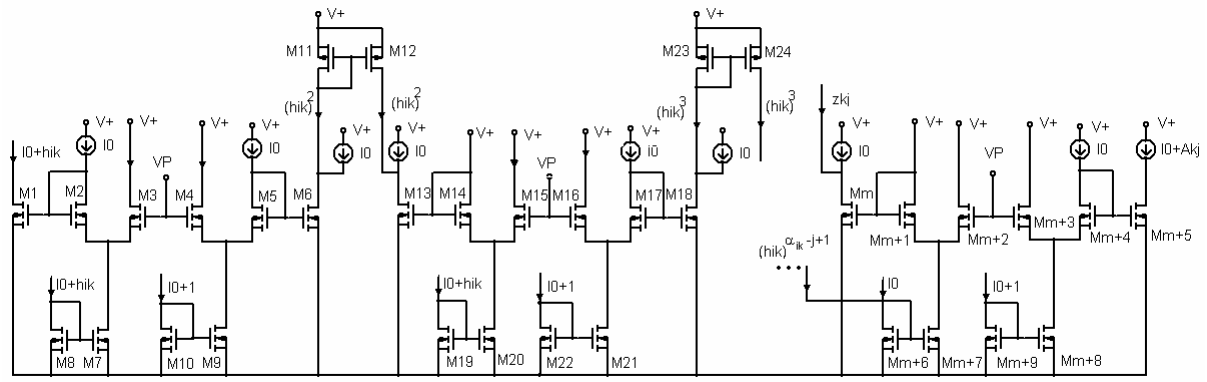


Figure 2. The network that implements the function z_{kj}.

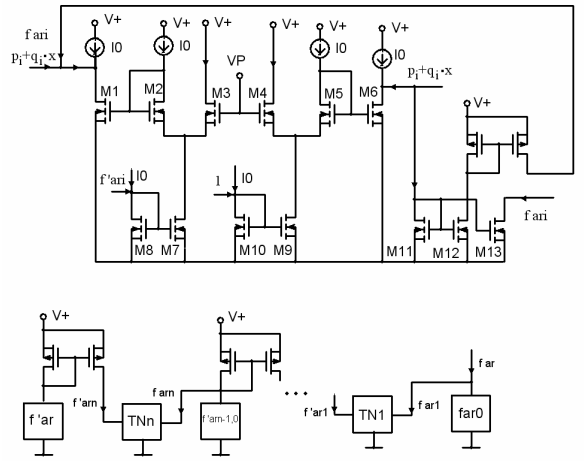


Figure 3. The network that assure the obtaining of $f_{ar,i}(x)$ from $f'_{ari}(x)$, TN, and the general network that gives the function $f_{ar}(x)$

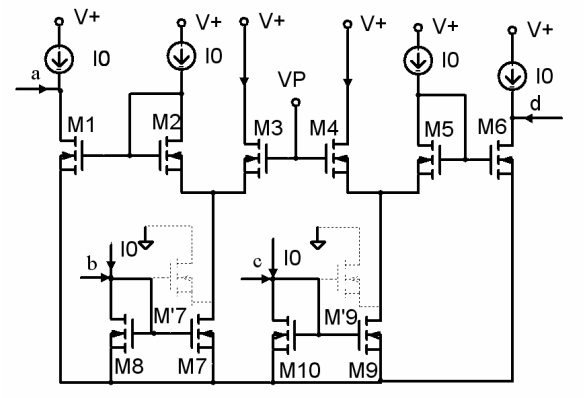


Figure 4. The base cell of networks presented in figures 2 and 3.

The TL network that implements the function z_{kj} is presented in figure 2. The TL network that implements the approximated function $f_{ar}(x)$, using the above presented networks and the network that assure the obtaining of functions $f_{ar,i}(x)$ from $f'_{ari}(x)$, is presented in figure 3.

For a minimum supply voltage, the current-source n chanel transistors will be non-saturated. Therefore, in accordance with decomposition technique described in section two (see figure 1.b.), the fictitious transistors can be added in order to account the non-saturation of these transistors. These fictitious transistors was noted with the same number like the real non-saturated transistors but was aded the simbol prim " ' ". From those presented in previous section, it follows that all shown network transistors can now be regarded as saturated.

From figures 2 and 3 one can see that the networks use the same base cell. So, we analyse this base cell, shown in figure 4. This network are three translinear loops: $M_1 - M_6$, next M_1, M_2, M'_7 and M_8 and finally M_6, M_5, M'_9 and M_{10}, which are immune from the body effect. It can see that the oppositely connected transistor pairs $M_1 - M_2$, $M_3 - M_4$, $M_5 - M_6$, $M_8 - M'_7 -$ M_7 and $M_9 - M'_9 - M_{10}$ have the same gate voltage. It is follows that:

$$\begin{aligned} &I_{\Diamond}(V_{G1}) = I_{\Diamond}(V_{Gi2});\ \ I_{\Diamond}(V_{G3}) = I_{\Diamond}(V_{G4}) \\ &I_{\Diamond}(V_{G5}) = I_{\Diamond}(V_{G6}) \\ &I_{\Diamond}(V_{G7}) = I_{\Diamond}(V'_{G7}) = I_{\Diamond}(V_{G8}) \\ &I_{\Diamond}(V_{G9}) = I_{\Diamond}(V'_{G9}) = I_{\Diamond}(V_{G10}) \end{aligned} \qquad (7)$$

Assuming equal-sized transistors for the translinear loops and applying the Kirchoff low to TL loops it is obtained the following expressions:

- for the first loop

$$(a + I_0)\cdot I_{D3}\cdot I_0 = I_0 \cdot I_{D4}\cdot(d + I_0), \qquad (8)$$

- for the second loop

$$(b + I_0)\cdot I_0 = (a + I_0)\cdot I'_{D7}, \qquad (9)$$

with

$$I'_{D7} = I_0 + b - I_{D3} - I_0 = b - I_{D3}, \qquad (10)$$

- for third loop

$$I_0 \cdot (c + I_0) = I'_{D9} \cdot (d + I_0), \quad (11)$$

with

$$I'_{D9} = c + I_0 - I_{D4} - I_0 = c - I_{D4}, \quad (12)$$

Eliminating I_{Di1} and I_{Di2} yields:

$$a \cdot b = c \cdot d, \quad (13)$$

The expressions for the drain currents of transistors M_3 and M_4 are:

$$\begin{aligned} I_{D3} &= \frac{a \cdot b - I_0^2}{a + I_0} \\ I_{D4} &= \frac{c \cdot d - I_0^2}{d + I_0} \end{aligned}, \quad (14)$$

and relive that

$$\min |a \cdot b| > I_0^2, \quad (15)$$

for a well operating of network.
Using these results we obtain for the first cell of the network of figure 2 the relation:

$$h_{ik} \cdot h_{ik} = 1 \cdot (I_{D6} - I_0), \quad (16)$$

By repeting the using of relation (13) to all cells of network, finaly we obtain the relation:

$$z_{kj} \cdot h_{ik}^{\alpha_{ik} - j + 1} = 1 \cdot A_{kj}, \quad (17)$$

similary with (6).
Appling the result (13) to the transform network presented in the first part of figure 3 one obtains:

$$(f_{ari} + p_i + q_i \cdot x) \cdot f'_{ari} = (p_i + q_i \cdot x - f_{ari}) \cdot 1, \quad (18)$$

similary with

$$f'_{ari}(x) = \frac{p_i + q_i \cdot x - f_{ari}(x)}{p_i + q_i \cdot x + f_{ari}(x)}. \quad (19)$$

In this way one obtains the implementation of all relations (5) and (6). The minimum supply voltage at these networks can operate is around $2 \cdot V_P$. For verify the network operation we use the SPICE simulator.
One must pointed that the current-mode signals are natural for translinear circuits, but in the real-word systems voltage-signals are generally used and therefore voltage-current interfacing will be needed in practice.

IV. CONCLUSION

The existing CMOS technologies provide ample opportunity to integrate entire systems on to a single integrated circuit. To date, the ability to integrate large digital systems has far outweighed the ability to integrate the analog systems. Future analog circuits will have to operate successfully at supply voltages slightly higher than the MOS threshold voltage. So, the suitable topologies for signal processing at such low values of supply voltages are the translinear circuits because are operating in current domain and in this way the very small voltage swings are avoided.
In this paper are presented some translinear topologies suitable for static and dynamic analog signal processing in mixed-signal chips, fabricated in digital CMOS technology and operated at very low supply voltage. These topologies implement the rational approximated and partial fraction decomposed functions. The minimum supply voltage at these networks can operate is around $2 \cdot V_P$.

For the previous presented network will be developed algorithms so these to can be integrated in our TLSS synthesis program.

ACKNOWLEDGMENT

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