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Log-Domain multipliers for VLSI architectures

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Abstract – We propose new modular configurations for one-, two-, and four quadrant multipliers in order to be used in large dimension circuits, like analog support vector machines or neural networks. Some investigations on these structures are made taking into account the real configurations and parameters of transistors in BiCMOS technology. We also underline the advantage of using such modular structures for high frequency large dimension circuits.
Keywords: Log-Domain, analog multiplier, VLSI architecture

I. INTRODUCTION

In analog computation and signal processing there are many cellular architectures that have to perform weighted sums with controllable or adaptive weights or sums of products of signals. Such examples are artificial neural networks, cellular nonlinear networks or support vector machines whose decision function is based on vector products. All of these circuits have to perform a large amount of calculations, therefore demands in area, power and high frequency operations usually appear.
As example for a SVM classifier [6] a test vector

$$\mathbf{x} = [x_1, \ldots, x_N]^T \tag{1}$$

and M support vectors

$$\mathbf{x}_i = [x_{i1}, \ldots, x_{iN}]^T, i = 1 \ldots M \tag{2}$$

are given. Using kernels based on vector products a decision function has to be determined:

$$y = \operatorname{sgn}\left(\sum_1^M a_i y_i \left(\sum_1^N \mathbf{x}_{ij} \mathbf{x}_j \right) + b \right) \tag{3}$$

Coefficients a_i and the bias term b are known from the learning process and y_i are the positive or negative labels of SV's i. Resulted label y corresponds to the test vector of features, which is positive classified if $y \geq 0$. A possible structure of such a classifier is given in Fig. 1 [1].

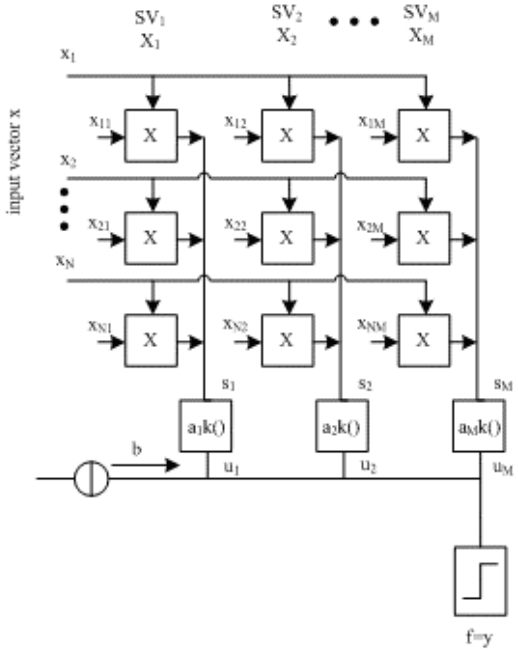

Fig. 1 Block diagram of a cellular SVM classifier with multiplying law: (x_k x_{kj})
k = 1,…,N; j = 1,…,M;
N – vector length M – SV number

The main cell in this schematic type is the multiplier. For summation we preferred to use current mode circuits and in the following we consider currents at input and output of multiplying cells.
Because the implementation of SVM classifiers needs high power, high speed, high densities, we thought to extend log-domain design [4] in this area because it is very appropriate for such requirements.
The very simple structure and the possibility of controlling their parameters are also very attractive for using this design.
Until now the log-domain was used for linear circuits [2] [3] [4] [5]. We have realized a modular nonlinear cell library for such tasks [4]. The principial architectures proposed in this paper for one-, two- and four quadrant multipliers were proved by simulations taking into account bipolar and BiCMOS technology. In this paper BiCMOS schematics are considered because they give the best results.

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II. ONE QUADRANT MULTIPLIER/DIVIDER

The function

$$i_{out} = \frac{i_x i_y}{i_{REF}} \tag{4}$$

can be simply obtained with a log-domain amplifier if the two signals are one-directional [4].

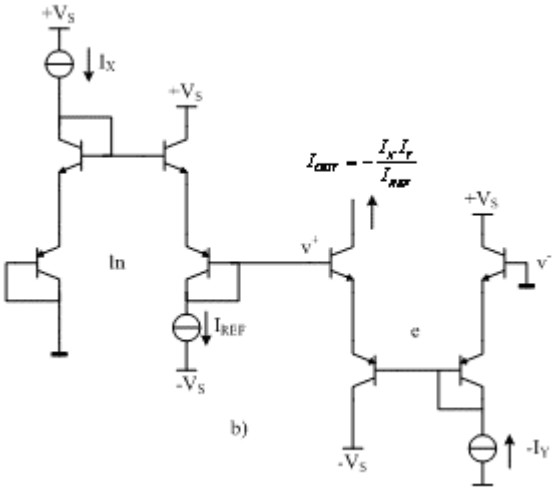


Fig. **2** a) and b) show such structures.

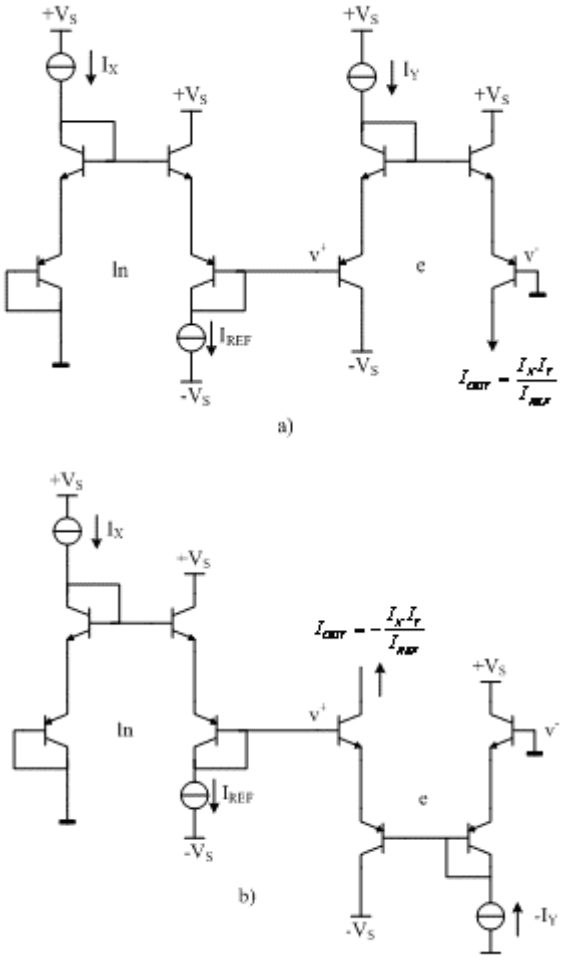


Fig. 2 One quadrant log-domain amplifiers: a), b) schematics

Modules **ln** in Fig. 2 accept a positive input I_X and a reference current I_{REF}. The inputs in the **e** cells can be either positive I_Y (Fig. 2, a) or negative ($-I_Y$) (Fig. 2, b). We took as reference the positive input and output directions as the arrow show in Fig. 2, a) and b). Multipliers operate in one quadrant. For Fig. 2, a) as an example we can write:

$$v^+ = V_A \ln \frac{I_X}{I_{REF}}; I_{out} = I_Y e^{\frac{v^+}{V_A}}; V_A = 2V_T \tag{5}$$

$$\Rightarrow I_{out} = \frac{I_X}{I_{REF}} I_Y \tag{6}$$

For Fig. 2 a) the simulated dc transfer characteristics and the time diagrams are shown in Fig. 3.

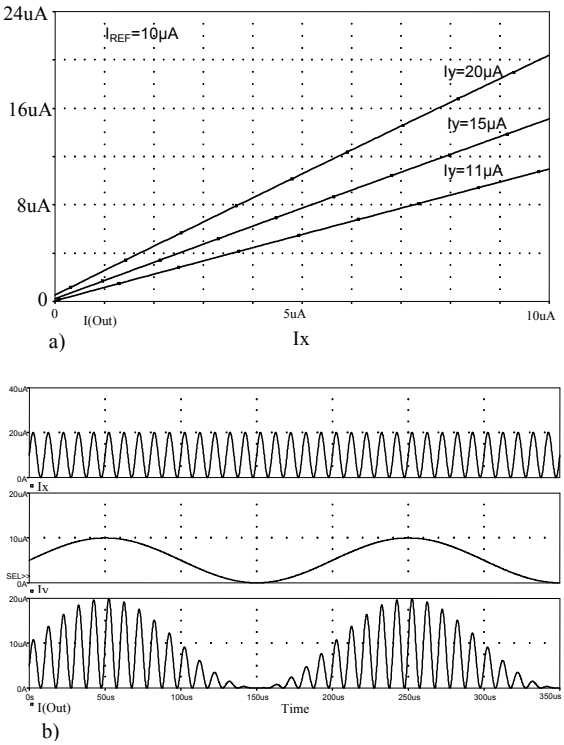


Fig. 3 a) DC transfer characteristic of one quadrant multiplier; b) time diagram for I_{REF}=10μA, I_X=(10+10sin2π100kt)μA, I_Y=(5+5sin2π5kt)μA

For Fig. 3 a), current I_X is positive [0,10uA], current I_Y is also positive and takes the values 11uA, 15uA, 20uA, I_{REF} is equal to 10uA.
Fig. 4 a) and b) show the symbols of each module **ln** and **e** respectively.

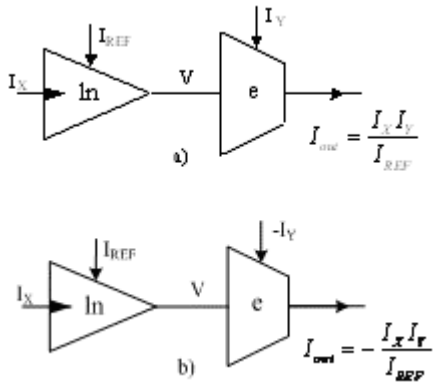


Fig. 4 One quadrant modular log-domain multiplier symbols: a) Ix>0, Iy>0; b) Ix>0, Iy<0

It is worth to put relation (6) in the form

$I_{out} = I_X \frac{I_Y}{I_{REF}} = A(I_Y) I_X$ so it can be seen why this circuit can also be considered as a current controlled current amplifier (Fig. 3, a).

III. TWO QUADRANT MULTIPLIERS

Fig. 5 shows the proposed two-quadrant multiplier. The input I_X is one-directional, the input i_y is bidirectional.

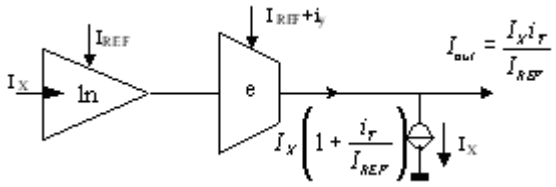


Fig. 5 Two quadrant multiplier

$$\left|i_y\right| < I_{REF}; I_{REF} > 0; A\left(i_y\right) = \frac{\left(I_{REF} + i_y\right)}{I_{REF}} \qquad (7)$$

$$I_{out} = A\left(i_y\right) I_X - I_X = \frac{I_X i_y}{I_{REF}} \qquad (8)$$

We simulated the circuit. The dc transfer characteristics of this multiplier is shown in Fig. 6 a) and a time diagram in Fig. 6 b):

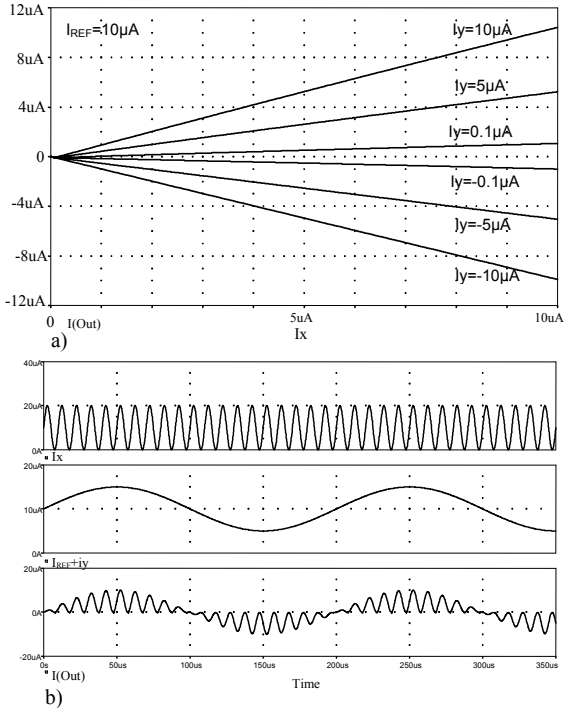


Fig. 6 a) DC transfer characteristics of the two-quadrant multiplier; b) time diagram for I_{REF}=10μA, I_X=(10+10sin2π100*10^{3}t)μA, i_Y=(5sin2π5*10^{3}t)μA

IV. FOUR QUADRANT MULTIPLIERS

For this type of multiplying cell we proposed the circuit given in Fig. 7.

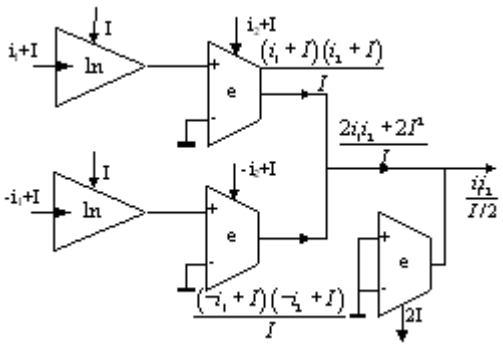


Fig. 7 Four-quadrant multiplier

The input signal i_1 is applied in opposite direction over a biasing current I at the input of two current amplifying paths, having the gains $(i_2+I)/I$ and $(-i_2+I)/I$ respectively. Current i_2 is the second bidirectional signal.

These currents, i_1+I and $-i_1+I$ (i_2+I, $-i_2+I$) were obtained by the circuit from Fig. 8:

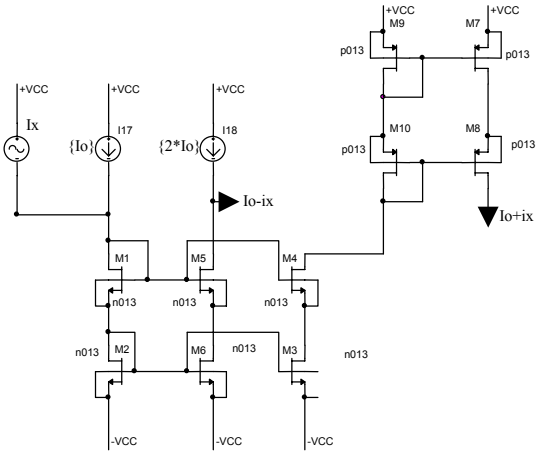


Fig. 8 Circuit for sum and difference

The input and output signals are presented in Fig. 9:

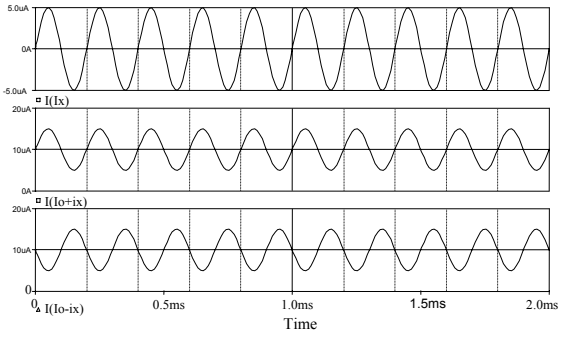


Fig. 9 Input and output signals from Fig. 8

The constant component of the sum of the output currents is cancelled by a current sink also realized with an **e** cell.

For proving the validity of the circuit some time diagrams resulted in simulations are given in Fig. 10. The simulated circuit is given in Fig. 15. Each input signal is a sinusoidal one, $i_1=(5\sin 2\pi 5*10^3 t)\mu A$ and $i_2=(5\sin 2\pi 100t)\mu A$, $I_{REF}=10\mu A$.

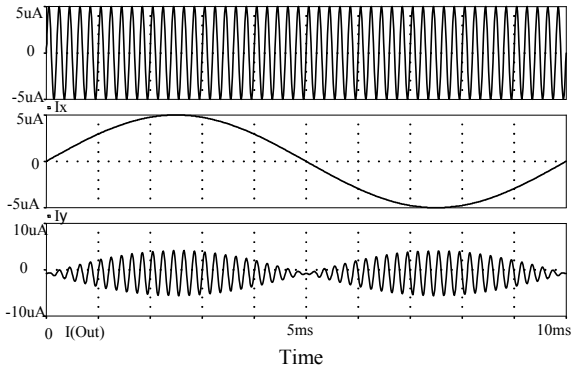


Fig. 10 Time diagrams for the four-quadrant multiplier

In Fig. 11 the magnitude spectrum of the output current signal for the proposed four-quadrant multiplier shown in Fig. 7 is presented.

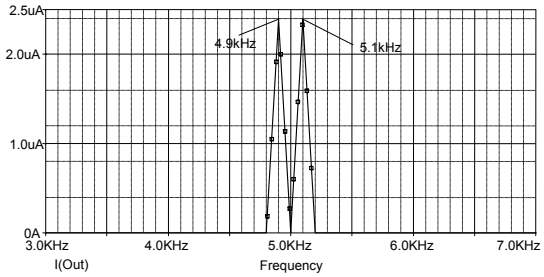


Fig. 11 Magnitude spectrum of the output current for the four-quadrant multiplier

The output current is of the form:

$$i_{out} = \frac{2i_x i_y}{I} \qquad (9)$$

Fig. 12 gives the dc transfer characteristic for: $i_x \in (-9\mu A, 9\mu A), I_{REF} = 10\mu A,$

$i_y \in \{-9\mu A, -5\mu A, -1\mu A, 1\mu A, 5\mu A, 9\mu A\}$

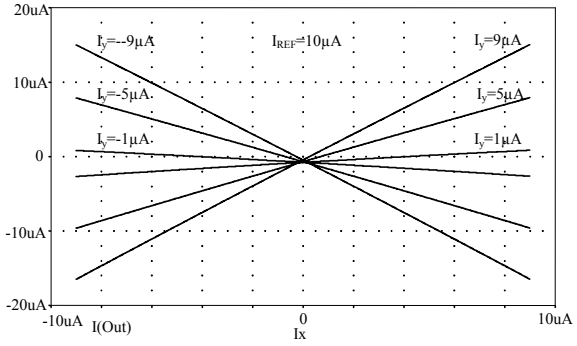
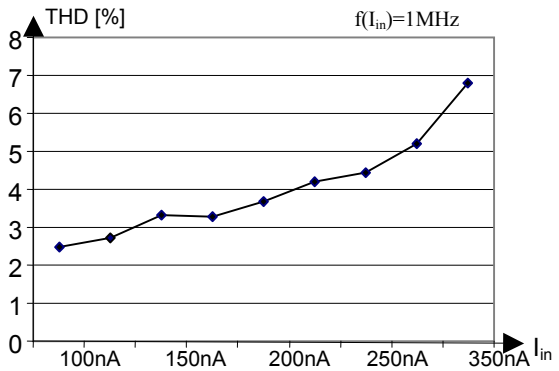


Fig. 12 DC transfer characteristics for the four-quadrant multiplier

We made also some THD computing and the results are shown in Fig. 13,a,b,c for different bias currents: 1μA (Fig. 13, a), 10μA (Fig. 13, b) and 100μA (Fig. 13, c). We compared the results with the THD results obtained for a classical Gillbert cell (Fig. 14, a). For the log-domain multiplier cell we consider three bias current values because for log-domain circuits the bias current is used for changing the cut-off frequency of the circuit. For higher bias current we have higher cut-off frequencies of the multiplier.



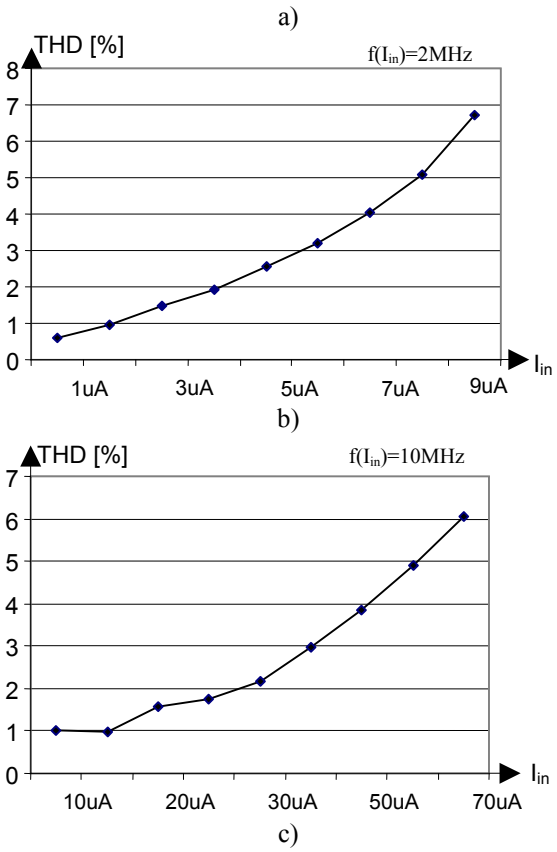
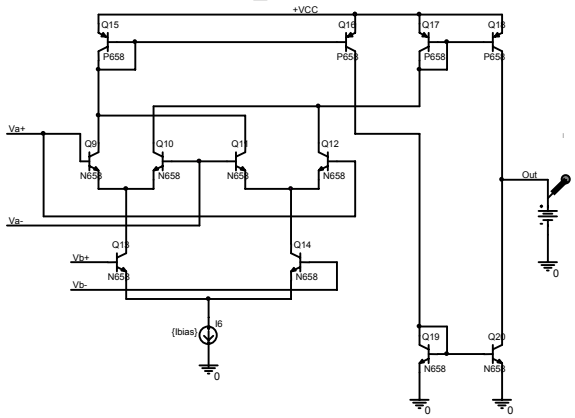


Fig. 13 THD characteristics for different bias currents: a) I_{REF}=1μA , b) I_{REF}=10μA, c) I_{REF}=100μA

The diagrams show that for a THD ≤ 5% we can increase the input current to about 30% I_{REF} if I_{REF}=1μA, 80% I_{REF} for I_{REF}=10μA and 60% I_{REF} for I_{REF}=100μA. In the case of Gillbert cell as Fig. 14, b shows the input voltage can reach only about 50% V_T in order to have a THD ≤ 5%.



a)

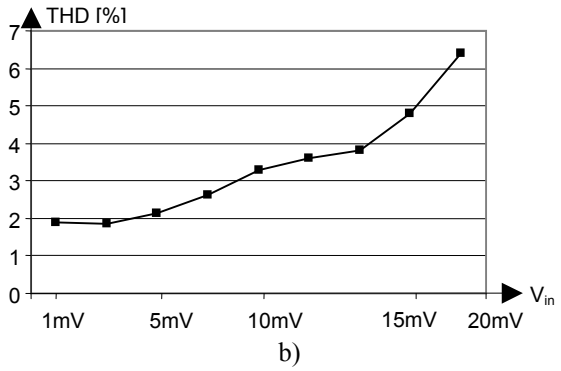


Fig. 14 Gillbert cell: a) Schematics b) THD characteristics

In Fig. 15 we have the simulated circuit in SPICE. All circuits were simulated in SPICE using BiCMOS transistor models from National Instruments.

V. REMARKS

The proposed multiplying cells open new directions of applications of log-domain design. We proposed this modular structure in order to be used in analog SVM classifiers and also in neural networks. This analog cells offer simplicity, low area, low voltage and high frequency and can be a good alternatives in VLSI analog modular design.

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