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Hardware Implementation of the Linguistic Decomposition Technique in the FPGA–FIS System

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Abstract – The hardware cost of the FATI relational fuzzy inference system can be reduced using the decomposition technique. In the paper has been proposed a modified Gupta's decomposition method expanded on linguistic level. It allows reducing hardware cost of the implementation of the FITA or FITA/FATI fuzzy inference systems. It can be implemented as a hardware unit in an FPGA structure to decrease an initialization time of the FPGA–FIS system.

Keywords: Fuzzy Rule, Fuzzy Relation, Relational Decomposition, Linguistic Decomposition, Fuzzy Inference Algorithm, FPGA, Decomposition Management Unit.

I. INTRODUCTION

The general structure of the MISO (*Multiple Inputs Single Output*) FIS (*Fuzzy Logic Inference System*) is shown in fig. 1. It consists of the following components: a fuzzification block, a knowledge base, an inference block and a defuzzification block [2], [7].

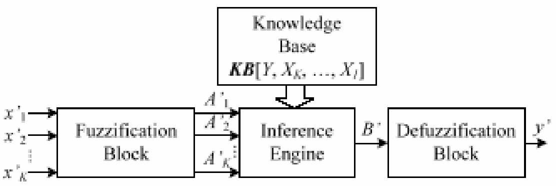

Fig. 1. General structure of the Fuzzy Logic Inference System

The knowledge base $\boldsymbol{KB}[Y, X_K, \ldots, X_1]$ comprises a collection of linguistic rules and definitions of linguistic variables. The fuzzy system is characterized by the linguistic description in the form of fuzzy rules

$$\text{If } X_K \text{ is } \underline{A}_{Kj_K} \text{ and } \ldots \text{ and } X_1 \text{ is } \underline{A}_{1j_1} \text{ then } Y \text{ is } \underline{B}_{j_K \cdots j_2 j_1}, \text{ also} \ldots \quad (1)$$

where $X_K, \ldots, X_2, X_1$ are input variables; Y is an output variable; $\underline{A}_{Kj_K}, \ldots, \underline{A}_{2j_2}, \underline{A}_{1j_1}, \underline{B}_{j_K \cdots j_2 j_1}$ are linguistic values defined by fuzzy sets $A_{Kj_K}, \ldots, A_{2j_2}, A_{1j_1}, B_{j_K \cdots j_2 j_1}$ on the corresponding universes of discourse $\mathsf{X}_K, \ldots, \mathsf{X}_2, \mathsf{X}_1$ and Y respectively ($j_K=1\ldots N_K, \ldots, j_2=1\ldots N_2, j_1=1\ldots N_1$, where N_k ($k=1\ldots K$) denotes the number of the linguistic values for the k^{th} input variable).

The general inference process usually encompasses four (or three for a system with exclusively fuzzy outputs) steps:

1) Fuzzification; actual input values $x'_K, \ldots, x'_2, x'_1$ are converted into fuzzy sets $A'_K, \ldots, A'_2, A'_1$. The most popular method is singleton fuzzification (systems with no fuzzy inputs).
2) Inference; the membership functions defined on the input variables $X_K, \ldots, X_2, X_1$ are applied to their actual values $A'_K, \ldots, A'_2, A'_1$ to determine the degree of truth for each rule premise (the if-parts of the rules) and then applied to the conclusion part of each rule (the then-parts of the rules).
3) Aggregation; all of the fuzzy subsets obtained in the previous step are combined together to form a single fuzzy set B' for output variable Y (fuzzy output).
4) Defuzzification; converts the fuzzy output set B' to a crisp number y'.

The output fuzzy set $B'_{j_K \cdots j_2 j_1}$ for rule $R_{j_K \cdots j_2 j_1}$ (1) can be expressed by means of the formula [2], [7]

$$B'_{j_K \ldots j_2 j_1} = \boldsymbol{A'} \circ \mathfrak{R}_{j_K \ldots j_2 j_1} \quad (2)$$

where the symbol $\circ$ denotes the compositional rule of inference operators (e.g. sup-min, sup-prod), $\mathfrak{R}_{j_K \cdots j_2 j_1}$ represents the relation between antecedent and consequent part of $R_{j_K \cdots j_2 j_1}$ rule, and $\boldsymbol{A'} = A'_K \times \ldots \times A'_2 \times A'_1$. The relation $\mathfrak{R}_{j_K \cdots j_2 j_1}$ defined in the cartesian product $\mathsf{X}_K \times \ldots \times \mathsf{X}_2 \times \mathsf{X}_1 \times \mathsf{Y}$ can be expressed by the formula (Mamdani) [2], [7]

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$$\mathfrak{R}_{j_K \dots j_2 j_1} = \mathbf{A}_{j_K \dots j_2 j_1} \wedge B_{j_K \dots j_2 j_1} \quad (3)$$

where $\wedge$ denotes the MIN operator and

$$\mathbf{A}_{j_K \dots j_2 j_1} = A_{Kj_K} \times \dots \times A_{2j_2} \times A_{1j_1} \quad (4)$$

The single output fuzzy set *B'* for a collection of rules can be computed on the basis of two approximate reasoning methods:

Method 1
The fuzzy sets $B'_{j_K \dots j_2 j_1}$ are combined together to get a single fuzzy set by using the aggregate MAX ($\vee$) operator

$$B' = \bigvee_{j_K=1}^{N_K} \cdots \bigvee_{j_1=1}^{N_1} B'_{j_K \dots j_2 j_1} \quad (5)$$

Method 2
A global relation $\mathfrak{R}$ for all rules is determined

$$\mathfrak{R} = \bigvee_{j_K=1}^{N_K} \cdots \bigvee_{j_1=1}^{N_1} \mathfrak{R}_{j_K \dots j_2 j_1} \quad (6)$$

and then the output fuzzy set is computed according to the formula

$$B' = \mathbf{A}' \circ \mathfrak{R} \quad (7)$$

where the symbol $\circ$ denotes the compositional rule of inference operators (e.g. sup-min, sup-prod).

II. HIERARCHICAL AND CLASSICAL FUZZY INFERENCE SYSTEM

In [3], [4] the theory of the relational decomposition technique has been described. It is based on projection operation defined for fuzzy relation [2]. For *K*-th dimensional fuzzy relation $\mathfrak{R}$ the results of this operation are *K*-th two-dimensional fuzzy relations $\mathfrak{R}_K \dots \mathfrak{R}_1$ [6]. The fuzzy relation is represented as a FLUT (Fuzzy Lookup Table). The dimension of the table and hardware cost of the system depends on dimension of fuzzy relation. The logical architecture of the MISO (Multiple Inputs Single Output) classical and decomposed relational FATI (First Aggregate Then Inference) [1] fuzzy inference system has been presented in fig. 2a and 2b respectively.
The first one consists only one element – memory module. It stores the fuzzy relation $\mathfrak{R}$ represented as a binary matrix. The second one consists *K*-th SISO (Single Input Single Output) subsystems. There are memory modules smaller sizes and stories subrelations $\mathfrak{R}_K \dots \mathfrak{R}_1$. To compute fuzzy inference result an additional fuzzy arithmetic component has been used. It realizes a MIN operation on partial results (fuzzy sets $B'_1 \dots B'_K$).

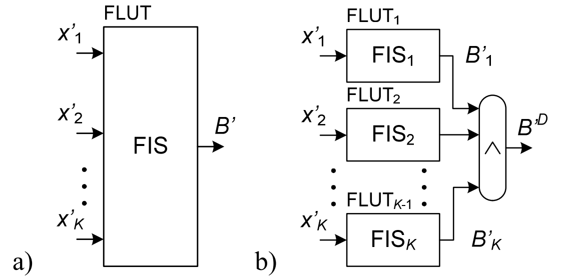

Fig. 2. Logical architecture of the classical (a) and hierarchical (b) fuzzy inference systems

The estimated hardware cost of the fuzzy inference system depends on the hardware cost of the memory modules, connections and components used in the system. To compare the two structures a hardware cost reduction coefficient has been defined

$$\upsilon_H[\%] = \frac{H - H^D}{H} \cdot 100 \quad (8)$$

where *H* and H^D are hardware costs of the classical and decomposed fuzzy system. Theoretically, the computed hardware cost reduction coefficient has been presented graphically in fig. 3. For practically implemented systems the decomposition method leads to the lowering of hardware costs.

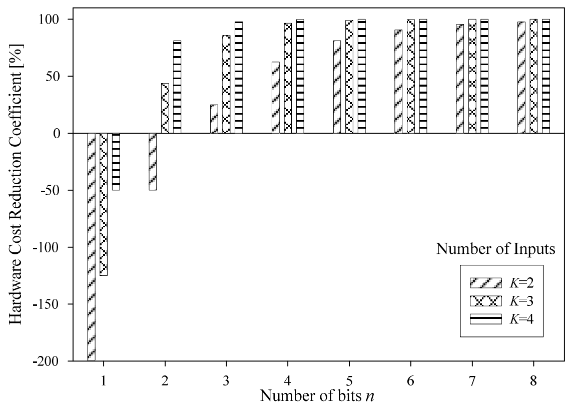

Fig. 3. Hardware cost reduction coefficient vs. number of bits of input and output values and number of inputs for FATI systems

III. LINGUISTIC DECOMPOSITION TECHNIQUE

The fuzzy relation $\mathfrak{R}$ of the FATI inference system is computed based on information stored in knowledge base ***KB***[*Y*, X_K, …, X_1] (where *Y*, X_K, …, X_1 are output and inputs linguistic variables) of the FITA (First Inference Then Aggregate) inference system [1]. The flow diagram of creating subrelations $\mathfrak{R}_K \dots \mathfrak{R}_1$ proposed by M. M. Gupta is shown in fig. 4 (left path of the diagram). A lot of time is required to compute a global relation $\mathfrak{R}$ and a large memory to store it. These disadvantages can be eliminated if decomposition is used for knowledge base ***KB***[*Y*, X_K, …, X_1] (in fig. 4 right path of the diagram) [8].

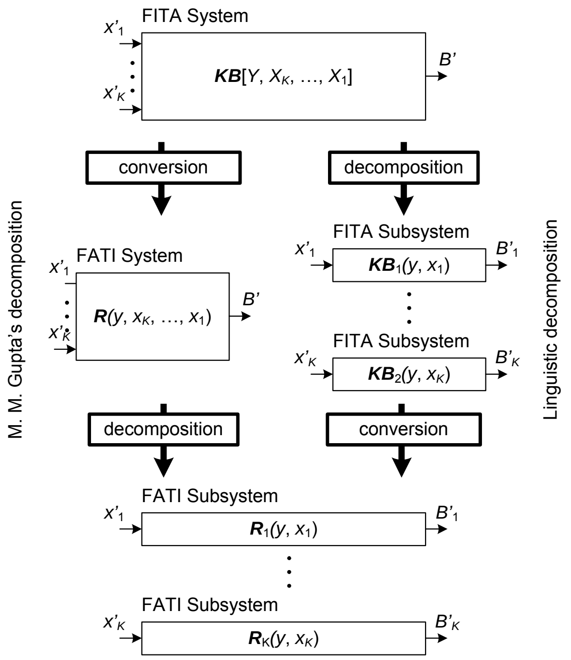

Fig. 4. Flow diagram of creating subrelations based on relational and linguistic decomposition technique

The proposed methodology needs a transform classical projection of fuzzy relation into linguistic projection of knowledge base. It can be expressed by the formula

$$\boldsymbol{KB}_i\left[Y, X_i\right] = \underset{X_K,\ldots,X_{i+1},X_{i-1},\ldots,X_1}{Proj} \boldsymbol{KB}\left[Y, X_K, \ldots, X_1\right] \quad (9)$$

This operation combines conclusion parts of the all rules in **KB**[Y, X_K, …, X_1] to get conclusion part (fuzzy set $B^D_{ij_i}$) of the rule in **KB**$_i$[Y, X_i] according to

$$B^D_{ij_i} = \bigvee_{j_K=1}^{N_K} \cdots \bigvee_{j_{i+1}=1}^{N_{i+1}} \bigvee_{j_{i-1}=1}^{N_{i-1}} \cdots \bigvee_{j_1=1}^{N_1} B_{j_K,\ldots,j_1} \quad (10)$$

where N_K, …, N_1 are number of linguistic values defines for each variable X_K, …, X_1, and $\vee$ denotes a MAX operator [7]. The linguistic projection of three-dimensional knowledge base has been graphically depicted in fig. 5 (the dimension of the knowledge base is equal to number of linguistic variables [3], [4]).

The obtainment knowledge bases **KB**$_1$[Y, X_1] and **KB**$_2$[Y, X_2] can be afterwards converted into fuzzy relations stored in memories in hierarchical system presented in fig. 1b or can be used to implementation of the FITA hierarchical system. In this way the FIS$_i$ (i=1, …, K) modules are SISO FITA systems and has logical architecture presented in [5], [8].

Proposed method has following advantages:

1) It is no need a lot of time to compute a global fuzzy relation $\mathfrak{R}$ and a large memory to store it,
2) Results of decomposition the primary knowledge base can be used to implement FITA inference system as a hierarchical structure, estimated hardware cost is also lower, but it is the highest than FATI system.

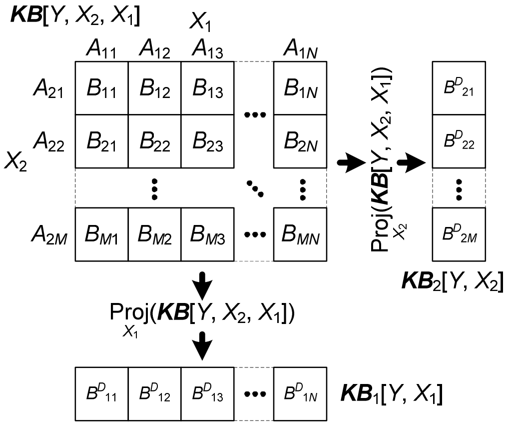

Fig. 5. Projection of the two dimensional knowledge base of the primary inference system into two one dimensional knowledge bases of the subsystems

IV. HARDWARE ARCHITECTURE OF THE RULE/RELATIONAL FUZZY INFERENCE SYSTEM

General architecture of the digital fuzzy logic inference system is shown in fig. 6.

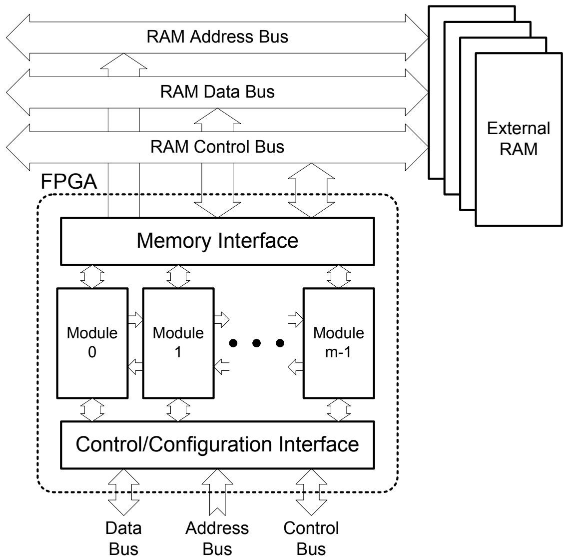

Fig. 6. General architecture of the digital fuzzy logic inference system

It consists of two main components: external SRAM and an FPGA chip (Xilinx Spartan II XC2S200 [9]). The RAM is used to store configuration data e.g. knowledge base (FITA systems), relation as a form of FLUT (FATI systems) or both structures (FITA/FATI systems). It is connected to the FPGA via an 8–bit bidirectional data bus, 20–bit address bus and 6–bit control bus. In the FPGA chip are implemented two interfaces: memory and control/configuration. The first provides a communication between memory and internal modules of the FPGA, second allow external device (e.g. microprocessor) to configure the fuzzy system and then to control the inference process.

The modules, implemented in the FPGA chip, perform various tasks: fuzzy operations control the inference process, configuration of the system etc. They are provided communication via internal buses, but at the same time only one of them is the master and has direct access to the RAM buses to control the behavior of the system.
It has been designed various components gathered in IP Core library. All of them have been described in Verilog HDL [10]. In the FPGA chip are implemented only selected modules to create desirable FITA, FATI or FITA/FATI system [8].

V. DECOMPOSITION MANAGEMENT UNIT

The DMU (Decomposition Management Unit) module allows the decomposing of the knowledge base of the primary system into knowledge bases of the SISO subsystems (fig. 1b). The linguistic decomposition process is performed in two steps:

1. Decomposition the primary base rule into base rules of FITA subsystems of the hierarchical architecture (fig. 5),
2. Creation a new linguistic values of the output linguistic variable (formula 10).

All parameters of the inference system (knowledge base e.g. base rule and definitions of linguistic variables) are stored in the first 64kB of the external SRAM.
In fig. 7 is shown a hardware configuration of the fuzzy inference system FPGA-FIS in configuration mode. It has been presented only necessary modules for performing linguistic decomposition.

VI. REMARKS

Some modules implemented in FPGA-FIS system are used only during inference process, some during initialization process after power up. If it is implemented FITA, FATI or FITA/FATI system then initialization process takes two main steps: decomposition primary knowledge base and conversion knowledge subbases into subrelations (only for FATI, FITA/FATI systems). It has been designed a hardware DMU module to decrease this time. The time of decomposition step is in the worst case equal 2,5ms (225 rules in primary knowledge base, membership functions are represented as a binary matrix, arguments and values of membership functions are represents as 8 bits unsigned number, system clock is 12MHz). This time is limited by memory SRAM access time (55ns) and can be still decreased.
The hardware cost of the DMU module are presented in Table 1. It can be noticed, that the DMU module occupies around 1% resources of the Spartan II XC2S200 FPGA chip.

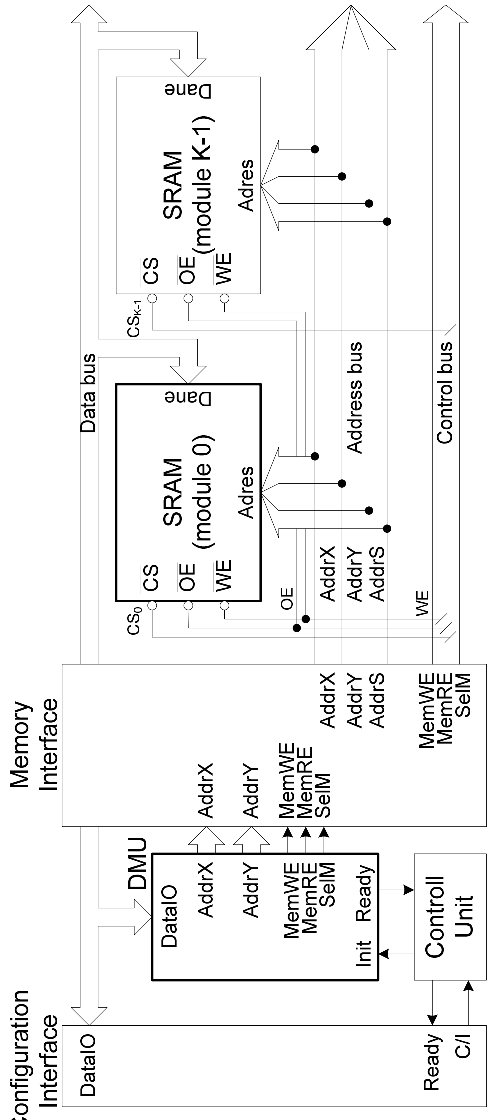

Fig. 7. Hardware configuration of the FPGA-FIS during linguistic decomposition step

Table 1. Hardware cost of the DMU module

Number of			Total equivalent gates count for design
Slices	Flip-Flops	LUTs	
112	65	207	1831

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