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A Quadratic Boost Converter with PFC Applications

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Abstract – A novel quadratic boost converter capable of delivering a high output voltage is introduced. Dc-dc operation in continuous conduction mode (CCM) and discontinuous inductor current mode (DICM) are analyzed. A simple and versatile feedforward (FF) circuit is proposed in order to be used with the new converter when operated in CCM. Another application is the use of the converter as a power factor correction (PFC) circuit. At low power levels DICM operation is chosen because of the converter natural capability of emulating a resistor at low frequency. Design equations, simulation results and merit parameters are presented for all the investigated topologies.

Keywords: converter synthesis, quadratic converters, feedforward, power factor correction, simulation.

I. INTRODUCTION

It is known that in high-voltage/low current applications such as TV-CTR's, lasers, X-ray systems, ion pumps, electrostatic systems, etc. a capacitor-diode voltage multiplier is preferable to a transformer. The solution of a BUCK converter followed by a push-pull multiplier has the drawback of using three active switches and therefore a complex control. Moreover, as the input current is discontinuous an input filter is invariably required.

In dc-dc converters applications operating with a wide range of input and/or output voltages, conventional PWM converters must operate at very small or very large values of the duty cycle. These operation modes are severe restricted by the transistors on-time (t_{ON}) or off-time (t_{OFF}) minimum values. These drawbacks are eliminated by the quadratic converters [1], having the static conversion ratio M ($M = Vo/Vg$) as a rational function of two polynomials, at least one of them being of second order.

The novel single-stage high voltage converter proposed in the paper is suitable to provide a high voltage. Converter topology is derived and CCM operation is analyzed in Section II. Converter operation in DICM mode is investigated in Section III, while its power factor correction capability is revealed in Section IV. The theoretical concepts are verified by simulation in Section V while Section VI is devoted to conclusions.

II. THE NEW QUADRATIC BOOST CONVERTER

It is known [1], [4] that quadratic converters cannot be realized with less than two capacitors, two inductors and four switches, but the number of transistor switches can be reduced to one. The technique based on rotating basic switching cells [2] is employed here for deriving the new BOOST topology. Namely, assuming the input source and the load share a common terminal, as Fig. 1 presents, a three-terminal switching cell is connected between the terminals *g*, *l* and *c* in all the six possible ways and for each topology switch synthesis [4] is performed. The basic

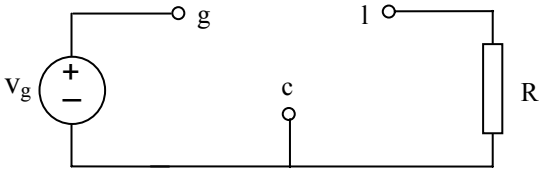

Fig. 1. The supply voltage and the load sharing the same ground terminal.

cell used here is drawn in Fig. 2. Switches S_1 and S_3 are synchronously driven, while S_2 and S_4 are complementary driven to S_1 and S_3. This is denoted by the negation sign accompanying them. The duty cycle D is related to switches S_1 and S_3.

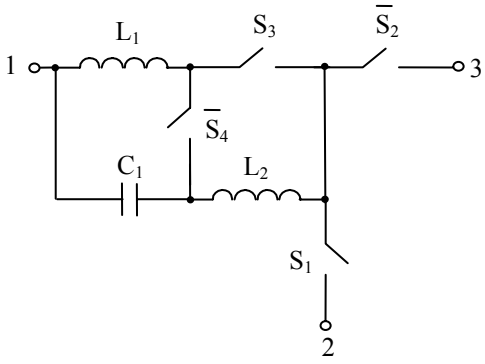

Fig. 2. The basic switching cell.

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The new converter topology corresponds to the connection $1 \to l, 2 \to c, 3 \to g$ and after switch implementation the resulting structure is that shown in Fig. 3.

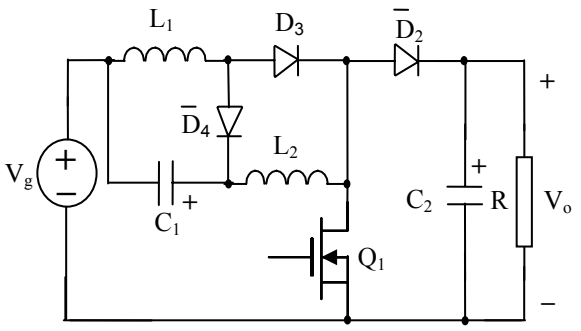

Fig. 3. The new BOOST converter topology.

Assuming ideal components and CCM operation, during the first topological state, when Q_1 and D_3 are on and D_2 and D_4 are off, the input voltage is applied across inductor L_1, while the voltage across L_2 equals $V_{C1}+V_g$. In the second topological state V_{C1} is opposite applied across L_1, while $V_{C1}+V_g-V_{C2}$ is applied across L_2. Imposing volt-second balance over L_1 and L_2 one obtains:

$$DV_g + (1-D)(-V_{C_1}) = 0 \quad (1)$$

$$D(V_{C_1} + V_g) + (1-D)(V_{C_1} + V_g - V_{C_2}) = 0 \quad (2)$$

From (1) and (2) the static conversion ratio is:

$$M = \frac{V_o}{V_g} = \frac{1}{(1-D)^2} \quad (3)$$

Given the output power, the output voltage and the input voltage the average semiconductor currents and voltage stresses are presented in Table 1. The stresses are computed in CCM assuming that ac ripples of the inductor currents and capacitor voltages are negligible. For comparison, the same stresses in the classical BOOST converter operating under the same conditions are provided in Table 2.

Comparing the results in the two tables it can be easily seen that for Q_1 and D_2 the current and voltage stresses are the same as the transistor and diode stresses in the classical BOOST converter, while for D_3 and D_4 the voltage stresses are lower than in the classical converter.

III A FEEDFORWARD CIRCUIT FOR CCM OPERATION OF THE NEW CONVERTER

For switching converters feedforward compensation is effective in reducing effects of source disturbances on converter outputs and improving steady-state and dynamic responses. A converter with FF behaves at low frequencies as a linear power amplifier with constant gain, independent of operating conditions.

In deriving the FF controller let us impose the average output voltage V_o to be equal to the control voltage v_m

Table 1.

	Proposed BOOST quadratic converter
V_{Q1}	V_o
I_{Q1}	$P_o\left(\frac{1}{V_g}-\frac{1}{V_o}\right)$
V_{C1}	$V_g\left(\sqrt{\frac{V_o}{V_g}}-1\right)$
V_{C2}	V_o
I_{L1}	$\frac{P_o}{V_g}$
I_{L2}	$\frac{P_o}{V_o}\sqrt{\frac{V_o}{V_g}}$
V_{D2}	V_o
I_{D2}	$\frac{P_o}{V_o}$
V_{D3}	$V_o\left(1-\sqrt{\frac{V_g}{V_o}}\right)$
I_{D3}	$\frac{P_o}{V_g}\left(1-\sqrt{\frac{V_g}{V_o}}\right)$
V_{D4}	$\sqrt{V_o V_g}$
I_{D4}	$\frac{P_o}{V_o}\sqrt{\frac{V_o}{V_g}}$

Voltage and current stresses in the proposed quadratic BOOST converter.

Table 2

	Classical BOOST converter
V_Q	V_o
I_Q	$P_o\left(\frac{1}{V_g}-\frac{1}{V_o}\right)$
V_C	V_o
I_L	$\frac{P_o}{V_g}$
V_D	V_o
I_D	$\frac{P_o}{V_o}$

Voltage and current stresses in the classical BOOST converter.

multiplied by the constant gain A:

$$V_o = A \cdot v_m \quad (4)$$

On the other side, the input and output voltages are related by the static conversion ratio given by (3). From (3) and (4) it results that:

$$v_m(1-D)^2 - \frac{v_g}{A} = 0 \quad (5)$$

As it is known [6], trailing-edge, leading-edge or both-edge pulse width (PWM) modulators can be used. For the proposed converter a leading-edge (LE) modulator is proposed. Although a trailing-edge modulator could also be used, this choice is more convenient because it is much simpler. In a LE modulator the falling edge of the output logic-level function coincides with the short-pulse constant frequency clock, while the rising edge corresponds to the zero crossing of the modulator function. The modulator function is found from (5) if we let $D \to 1 - \frac{t}{T_s}$, resulting in:

$$v_m\left(\frac{t}{T_s}\right)^2 - \frac{v_g}{A} = 0 \qquad (6)$$

It can be seen that in the modulator function (the right hand side of (6)) the term $v_m\left(\frac{t}{T_s}\right)^2$ occurs. This term can be implemented without fast multipliers or relatively complex nonlinear elements. The implementation makes use of integrators with reset, just as in conventional PWM controllers and is based on the observation that the control voltage v_m is a slow varying signal compared to the switching frequency. Practically, in open loop operation v_m is constant. Mathematically, we can use the following approximation:

$$v_m\left(\frac{t}{T_s}\right)^2 \cong \frac{1}{\frac{T_s}{2}}\int_0^t\left(\frac{1}{T_s}\int_0^t v_m(u)du\right) \qquad (7)$$

Relationship (7) clearly suggests that the implementation of the term $v_m\left(\frac{t}{T_s}\right)^2$ consists of a cascade of two integrators with reset having the time constants equal to the switching period T_s and half of the switching period respectively. The practical implementation is shown in Fig. 4. Beside the two integrators only a comparator and a flip-flop are needed. The FF circuit can be easily constructed as an integrated circuit or with general-purpose components such as comparators, flip-flops and operational amplifiers. One can easily derive that in case of the architecture in Fig. 4 the output voltage is:

$$V_o = \left(1 + \frac{R_1}{R_2}\right)\cdot\frac{1}{2R_3C_3R_4C_4f_s^2}\cdot v_m \qquad (8)$$

IV OPERATION IN DISCONTINUOUS INDUCTOR CURRENT MODE AND AS A POWER FACTOR CORRECTION CIRCUIT

As three passive switches are present in the converter, theoretically DCM modes can be related to any of the diodes. However, only D_2 and D_4 can induce discontinuous inductor current operation (DICM) as the current through D_3 has a positive slope during the

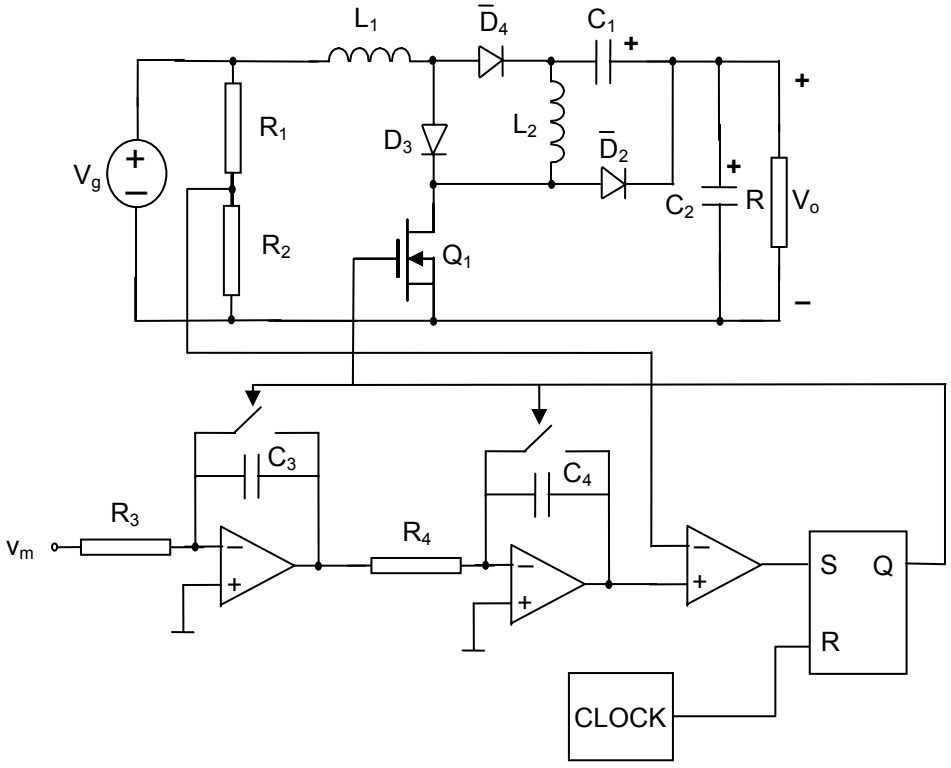

Fig. 4. The new quadratic BOOST converter and the feedforward circuit.

first topological state. It can be demonstrated that the DICM operation induced by D_4 is quantitatively given by the condition:

$$\frac{2L_1 f_s}{R} \le D(1-D)^4 \tag{9}$$

In case of DICM operation because of D_2, the condition becomes:

$$\frac{2L_2 f_s}{R} \le D(1-D)^2 \tag{10}$$

Because during its on state the averaged input current equals i_{L1}, it becomes obvious that in DICM due to D_1 the averaged input current shape is the same as in the conventional boost converter. The inductor current i_{L1} waveform is presented in Fig. 5.

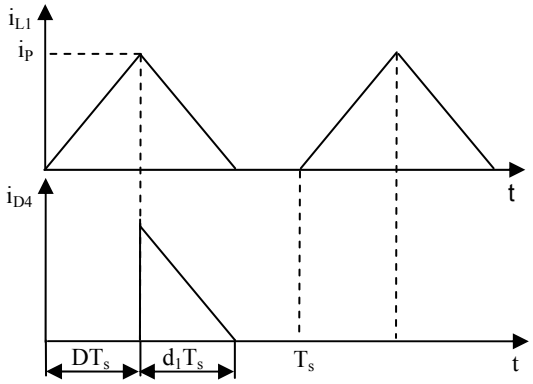

Fig. 5. Input inductor and diode D_4 waveforms.

The operation in DICM due to D_4 and the waveforms in Fig. 5 suggest the possibility to use the converter as an "automatic" or "natural" current shaper when operating in DICM. This is similar and "inherited" from the classical BOOST converter, being a simple solution at low power levels. Keeping in mind that v_g is now the output of a full wave uncontrolled rectifier fed by a sinusoidal voltage of angular frequency ω and amplitude V_M, we have

$$v_g = V_M \left|\sin \omega t\right| \tag{11}$$

Quasi steady state operation related to the line frequency and constant voltage on C_1, are assumed [6]. Therefore we can admit that $\overline{i_{C_1}} = 0$ and $\overline{i_g} = \overline{i_{L_1}}$

Volt-second balance on L_1 provides:

$$Dv_g + d_1(-V_{C_1}) = 0 \tag{12}$$

resulting in:

$$d_1 = D\frac{v_g}{V_{C_1}} \tag{13}$$

On the other side, i_P is given by:

$$i_P = \frac{v_g}{L_1} DT_s \tag{14}$$

The averaged value of the input current is given by:

$$\overline{i_g} = \overline{i_{L_1}} = \frac{1}{T_s}\frac{1}{2}(D + d_1)T_s i_p \tag{15}$$

In (15) if d_1 is replaced from (13) and i_P from (14), it follows that:

$$\bar{i}_g = \frac{v_g}{R_e} \cdot \left(1 + \frac{V_M}{V_{C_1}}\left|\sin \omega t\right|\right) \tag{16}$$

where the emulated resistance is:

$$R_e = \frac{2L_1 f_s}{D^2} \tag{17}$$

From (16) the power factor (PF) and the total harmonic distortion coefficient (THD) can be evaluated as:

$$PF = \sqrt{\frac{2}{\pi}} \frac{\int_0^0 \sin^2\theta(1 + a\sin\theta)d\theta}{\sqrt{\int_0^\pi \sin^2\theta(1 + a\sin\theta)^2 d\theta}} \tag{18}$$

$$a = \frac{V_M}{V_{C1}} \qquad THD = \sqrt{\frac{1}{PF^2} - 1} \tag{19}$$

These two merit parameters are represented in Fig. 6 as a function of the ratio V_{C1}/V_M. It can be seen that very good PF and THD can be obtained when V_{C1}/V_M >0.5, which in practice can be easily achieved.

Inductor L_1 design equation is obtained imposing DICM operation over the whole line half cycle when operated as a PFC circuit. This condition will significantly differ from that of DICM operation as a dc/dc converter given by (9). The design equation can be derived as in [4] and finally results in:

$$L_1 \le \frac{V_M^2}{4P_o f_s}\left(1 - \sqrt{\frac{V_M}{V_o}}\right) \tag{20}$$

V SIMULATION RESULTS

All simulations were performed using the CASPOC package (Simulation Research) [7]. First the new quadratic BOOST converter with feedforward, similar to the architecture presented in Fig. 4, was simulated. Converter parameters were:

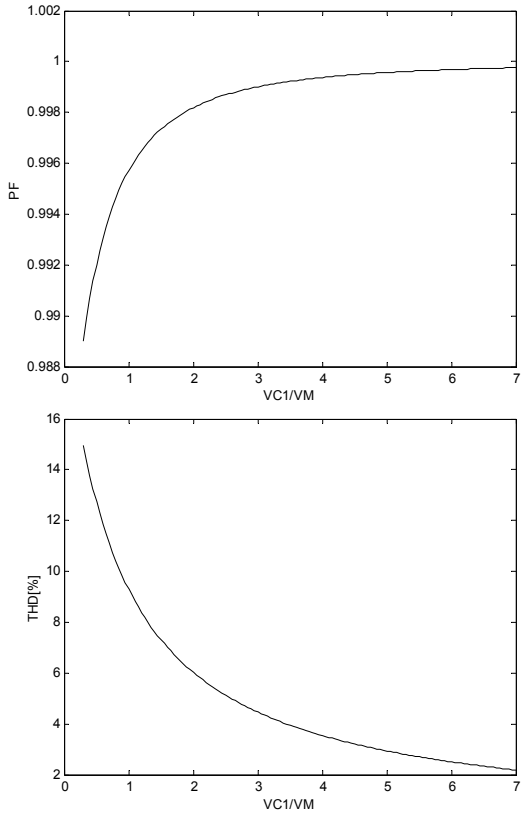

Fig. 6. Power factor and input current TDH as a function of the ratio V_{CI}/V_M in DICM.

$$L_1 = 237\mu H;\ L_2 = 415\mu H;\ C_1 = C_2 = 10\mu F;$$
$$R = 100\Omega;\ f_s = 40kHz;$$
$$v_m = 3V;\ R_1 = 90k\Omega;\ R_2 = 10k\Omega;\ R_3 = R_4 = 2k\Omega;$$
$$C_3 = 12.5nF;\ C_4 = 6.25nF$$

The input voltage was forced to vary with a square waveshape between 8V and 14 V. The simulation results are shown in Fig. 7. It can be seen that after short transients the output voltage tightly follows the prescribed 30V value.

Then the converter was simulated in a PFC application with DICM operation. The parameters of the PFC circuit were:

$$V_M = 70V;\ L_1 = 30.6\mu H;\ L_2 = 0.5mH;\ C_1 = 1\mu F;$$
$$C_2 = 470\mu F;\ P_o = 40W;\ V_o = 400V;\ R = 100\Omega;$$
$$f_s = 40kHz;\ D = 0.2;$$

After the uncontrolled bridge supplying the converter, a small high frequency filter with L_F=80μH and C_F=2μH was used, in order to suppress the high frequency components from the input current which are large in DICM. In Fig. 8 the input voltage and current waveforms are presented. The expected output voltage of 400 V was confirmed by the simulation which provided an output voltage of 406 V. It can be seen that qualitatively the input current has a closely sinusoidal shape and tightly follows the input voltage. Harmonic analysis of the input current was performed. The input current spectrum is shown in Fig. 9. The input current total harmonic distortion (THD) coefficient was 2.52%, while unity

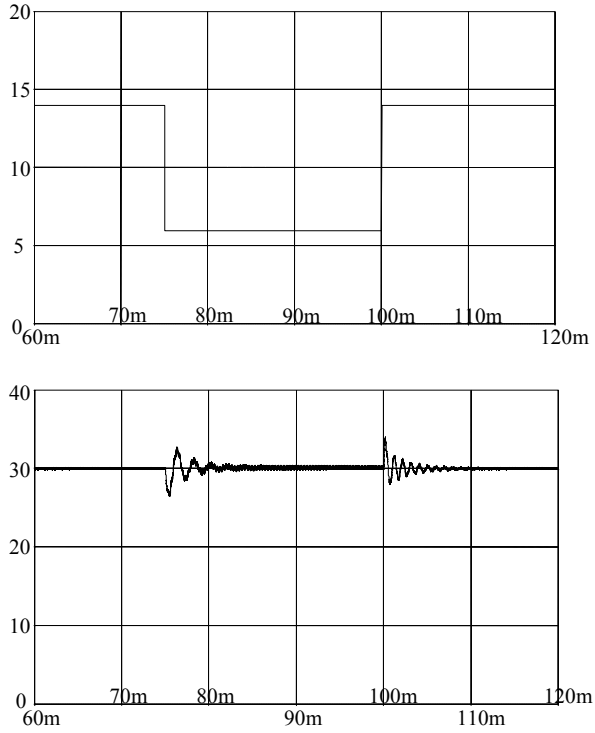

Fig. 7. Dynamic operation of the quadratic BOOST converter with FF. Input voltage (up) and output voltage (down).

displacement power factor was found. An excellent total power factor of 0.996 was achieved.

VI CONCLUSIONS

A novel quadratic BOOST converter is proposed. Containing only a single transistor and three diodes, the converter can be easily controlled. The proposed topology exhibits better efficiency compared to a two stage configuration. High output voltages can be obtained and because the minimum off-time is much less restrictive, the converter can operate at a relatively high frequency (500 kHz). A feedforward circuit is developed to be used with the proposed converter. It consists of only two integrators, one comparator and a flip-flop and therefore it can be implemented on an integrated circuit or with general-purpose components.

The proposed converter is well suited for PFC applications at low power levels. DICM operation of the converter can be exploited because its natural property to be an "automatic" current shaper. This solution leads to a very simple control, without a current loop. Design equations, and DICM operation conditions are provided both for dc/dc and for PFC operation in order to quickly design the required topology.

The simulation results confirmed all the theoretical predictions regarding the converter, the feedforward controller and the PFC applications.

Thus the new converter together with the proposed controller provides simple solutions for wide range dc/dc applications and for low power level power factor correctors.

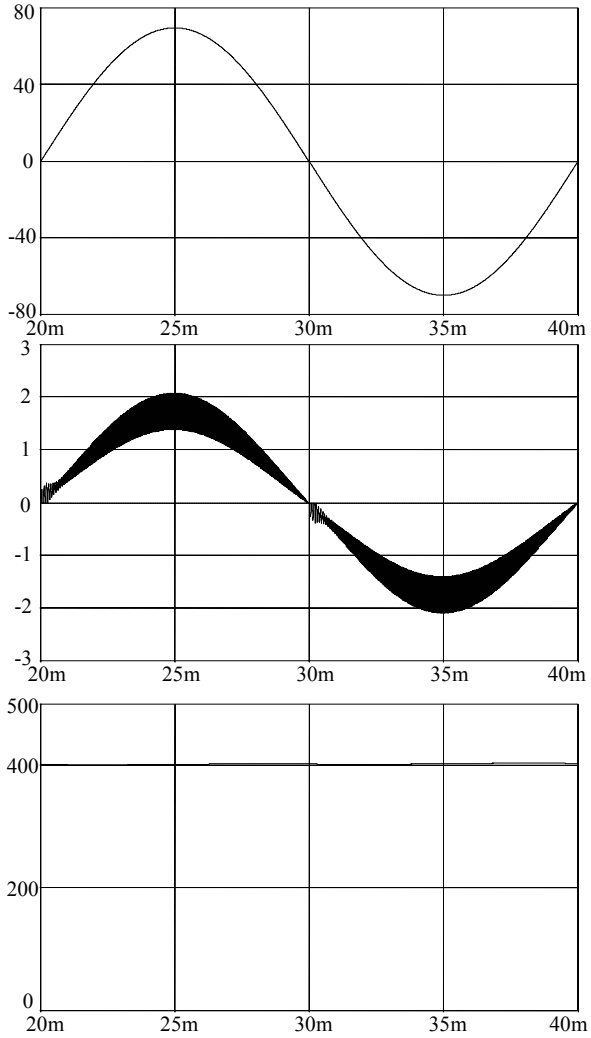

Fig. 8. PFC operation of the new converter in DICM mode. Input voltage, input current and output voltage (this up to down order).

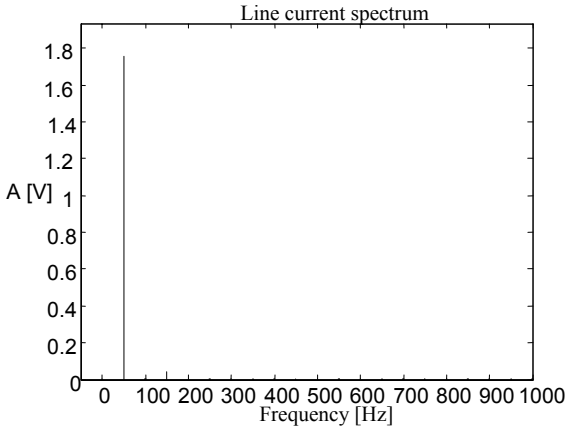

Fig. 9. Input current spectrum – first 20 harmonics.

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