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Improved Linearity Active Resistor with Negative Equivalent Resistance

Cosmin Popa[1]

Abstract - An original improved linearization technique for a CMOS active resistor will be further presented. The main advantages of the original proposed implementation are the improved linearity, the small area consumption and the improved frequency response. The new method for linearizing the $I(V)$ characteristic of the active resistor will be based on a parallel connection of two quasi-ideal circuits opposite excited and different biased, having the result of improving the circuit linearity with about an order of magnitude. Because of this original design technique, the circuit linearity is not affected by the second-order effects that alter the MOS transistor operation. The reduced complexity obtained by using a FGMOS transistor will be made maintaining the compatibility with classical technologies (the classical FGMOS device could be replaced by an original equivalent circuit using exclusively classical MOS devices). The frequency response of the circuit is very good as a result of operating all MOS transistors in the saturation region. In order to design a circuit having a negative equivalent resistance, an original method specific to the proposed implementation of the active resistor circuit will be presented. The circuit is implemented in $0.35\mu m$ CMOS technology, the SPICE simulation confirming the theoretical estimated results and showing a linearity error under a percent for an extended input range $(\pm 500mV)$ and for a small value of the supply voltage $(\pm 3V)$.

Keywords: active resistor circuit, linearity error, complementary functions, second-order effects

I. INTRODUCTION

CMOS active resistors are very important blocks in VLSI analog designs, mainly used for replacing the large value passive resistors, with the great advantage of a much smaller area occupied on silicon. Their utilisation domains includes amplitude control in low distortion oscillators, voltage controlled amplifiers and active RC filters. These important applications for programmable floating resistors have motivated a significant research effort for linearising their current-voltage characteristic.

[1] Faculty of Electronics, Telecommunications and Information Technology, E-mail: cosmin@golana.pub.ro

An important class of these circuits, referring to the active resistors with controllable negative equivalent resistance, covers a specific area of VLSI designs, finding very large domains of applications such as the cancelling of an operational amplifier load or the design of Deboo integrators with improved performances.

The first generation of MOS active resistors [1], [2] used MOS transistors working in the linear region. The main disadvantage is that the realised active resistor is inherently nonlinear and the distortion components were complex functions on MOS technological parameters.

A better design of CMOS active resistors is based on MOS transistors working in saturation [3], [4]. Because of the quadratic characteristic of the MOS transistor, some linearisation techniques were developed in order to minimize the nonlinear terms from the current-voltage characteristic of the active resistor. Usually, the resulting linearisation of the $I-V$ characteristic is obtained by a first-order analysis. However, the second-order effects which affect the MOS transistor operation (mobility degradation, bulk effect and short-channel effect) limits the circuit linearity introducing odd and even-order distortions, as shown in [4]. For this reason, an improved linearisation technique has to be design to compensate also the nonlinearities introduced by the second-order effects.

II. THEORETICAL ANALYSIS

The original idea for implementing a linear current-voltage characteristic of the active resistor, similar to the characteristic of a classical passive resistor is to use two complementary functions, the desired linearity being obtained by a mutual compensation of their nonlinearities. The proposed circuit presents the important advantage of a reduced silicon area with respect to classical implementations of an active resistors, based on symmetrical structures. Because of the requirements for a good frequency response, only MOS transistors working in saturation could be used. For this reason, the original choose is to use the quadratic and the square-root dependencies as complementary functions. So, square and square-root

circuits must be designed based exclusively on saturated MOS devices.

The application of a new method of inversing the current passing through the two pins of the active resistor allows to obtain a circuit having a controllable negative resistance.

In order to improve the circuit performances by using the FGMOS device and to maintain, also, the compatibility with classical CMOS technologies, an original equivalent FGMOS device will be proposed.

A. *The block diagram of the FGMOS active resistor*

The structure of the proposed active resistor is based on three important blocks:

- a voltage-current squarer X^2, implementing the function $I_{OUT} = K(V_X - V_Y)^2 / 4$;
- a current-pass circuit I;
- a current square-root circuit $\sqrt{\ }$, for obtaining $I_{XY} = 2\sqrt{I_{OUT} I_O}$;

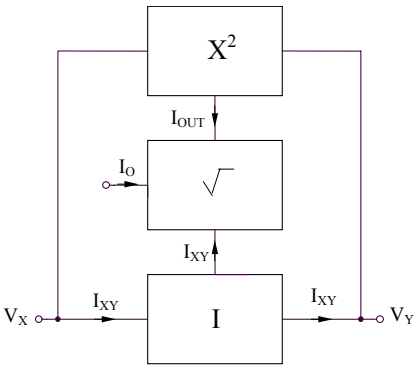

Fig. 1. The block diagram of the resistor

Because I_{XY} current is proportional to the square-root of I_{OUT} and I_O currents, while I_{OUT} current is proportional to the square of the differential input voltage $V_X - V_Y$, the result will be a linear relation between the differential voltage across the two pins, $V_X - V_Y$ of the active resistor and the current passing through it, I_{XY}. The great advantage of the proposed circuit is that, in a first-order analysis, no superior-order terms will appear in the $I(V)$ characteristic of the active resistor.

B. *The equivalent FGMOS transistor*

The FGMOS transistor is a MOS transistor whose gate is floating (Fig. 2a), while the symbolical representation of this device is shown in Fig. 2b. The first silicon layer over the channel represents the floating-gate and the second polysilicon layer, located over the floating-gate implements the multiple input gates. This floating-gate is capacitive coupled to the multiple input gates. The drain current of a FGMOS transistor with n-input gates in the saturation region is given by the following relation:

$$I_D = \frac{K}{2}\left[\sum_{i=1}^{n} k_i (V_i - V_S) - V_T\right]^2 \qquad (1)$$

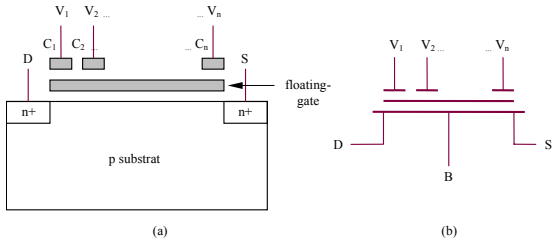

Fig. 2. (a) The basic structure of a n-channel FGMOS transistor; (b) symbolic representation

The great limitation of using FGMOS devices is that they are available only in few CMOS technologies, restricting the area of utilization of the circuits based on these transistors. The original idea for replacing the classical FGMOS device with two inputs by five MOS transistors is presented in Fig. 3.

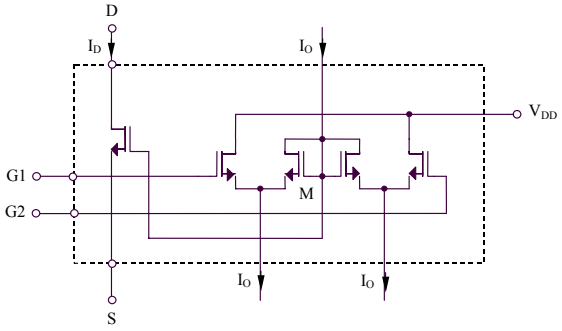

Fig. 3. The equivalent circuit of the FGMOST

The four pins of the equivalent FGMOS device are, respectively: D (drain), S (source), $G1$ and $G2$ (gates). Because of the connection of the four MOS transistors from the right part of the circuit, the M potential is equal to the arithmetic mean of the gates' potentials, $V_M = (V_{G1} + V_{G2})/2$. For this reason, the drain current of the entire equivalent FGMOS device from Fig. 3 will have the following expression:

$$I_D = \frac{K}{2}\left(\frac{V_{G1} + V_{G2}}{2} - V_S - V_T\right)^2 \qquad (2)$$

similar to the equation which characterizes the operation of the classical FGMOS transistor.

The original proposed implementation presents the great advantage of avoiding the utilization of any resistor for computing the arithmetic mean, with the result of reducing the circuit area and of improving the achieved accuracy. The circuit from Fig. 3 could replace, in the practical implementation, the FGMOS transistors, symbolic used in Figs 4 and 5.

C. *The voltage-current Squarer*

The new proposed squarer is based on the quasi - symmetrical structure from Fig. 4.

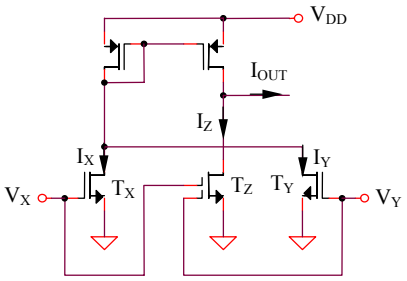

Fig. 4. The voltage-current squarer

The output current expression has a linear dependence on the drain currents of T_X, T_Y and T_Z transistors:

$$I_{OUT} = I_X + I_Y - I_Z \tag{3}$$

Considering a saturation operation of all MOS devices from Fig. 4 and supposing that the area of T_Z is twice that the T_X and T_Y areas, I_{OUT} will have the following dependence on the differential input voltage $V_X - V_Y$:

$$I_{OUT} = \frac{K}{4}(V_X - V_Y)^2 \tag{4}$$

D. *The square-root circuit*

The square-root circuit represents also a perfect symmetrical structure (Fig. 5), using MOS transistors and a FGMOS device (T) working in saturation for improving the circuit frequency response.

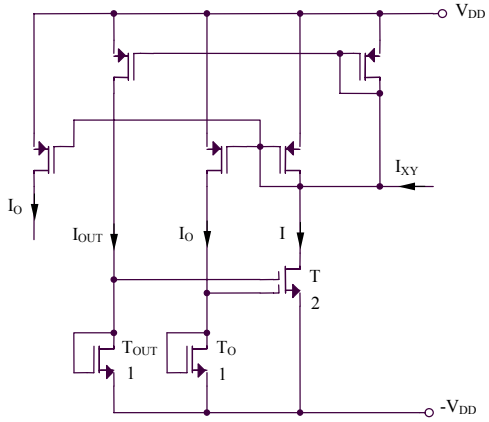

Fig. 5. The square-root circuit

Considering an aspect ratio of the FGMOS transistor fourth time greater than the aspect ratio of all the other devices from Fig. 5, the drain current I will have the following expression:

$$I = \frac{4K}{2}\left(\frac{V_{GS_{OUT}} + V_{GS_O}}{2} - V_T\right)^2 \tag{5}$$

where $V_{GS_{OUT}}$ and V_{GS_O} represent the gate-source voltages of T_{OUT} and T_O transistors. The output current expression is linearly dependending on the drain currents of T_{OUT}, T_O and T transistors:

$$I_{XY} = I - I_{OUT} - I_O \tag{6}$$

resulting a square-root dependence of the output current on the two input currents:

$$I_{XY} = 2\sqrt{I_{OUT} I_O} \tag{7}$$

E. *The current-pass circuit*

The necessity of designing this circuit is derived from the requirement that the same current to pass between the two output pins, X and Y. The implementation in CMOS technology of this circuit is very simple, consisting in a simple and a multiple current mirrors (Fig. 6).

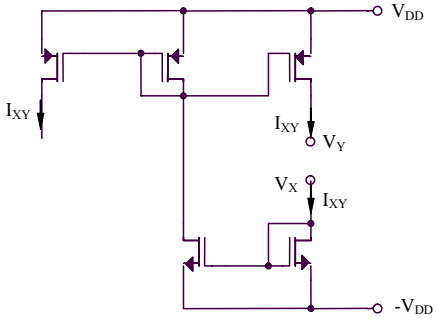

Fig. 6. The current-pass circuit

F. *The linear characteristic of the active resistor*

Because of the complementary characteristics (4) and (7) of the squaring and square-root circuits, the current-voltage characteristic $I_{XY}(V_X - V_Y)$ of the active resistor will be perfectly linear.

$$I_{XY} = \sqrt{KI_O}(V_X - V_Y) \tag{8}$$

being possible to define an equivalent resistance between X and Y pins as follows:

$$R_{ECH.} = \frac{V_X - V_Y}{I_{XY}} \tag{9}$$

It results $R_{ECH.} = 1/\sqrt{KI_O}$. The great advantage of the previous presented circuit is that the value of the equivalent active resistance could be very easily controlled by modifying the reference current I_O. For

usual values of K and I_O parameters, R_{ECH}. resistance covers about three decades $(1k\Omega - 1M\Omega)$, equivalent with an important reduction of the silicon occupied area, especially for large values of the active resistance simulated by the circuit from Fig. 1.

G. *The second-order effects*

The relation (8) of the current-voltage characteristic for the active resistor circuit having the block diagram presented in Fig. 1 is slightly modified by the second-order effects that affect the MOS transistor operation, modeled by the following relations: channel-length modulation (10) and mobility degradation (11)).

$$I_D = \frac{K}{2}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \tag{10}$$

$$K = \frac{K_0}{[1 + \theta_G(V_{GS} - V_T)](1 + \theta_D V_{DS})} \tag{11}$$

Taking into account these second-order effects and considering that the design condition $\lambda = \theta_D$ is fulfilled, the operation of the voltage-current squarer from Fig. 4 will be affected by a small error that will be quantitative evaluated by:

$$\varepsilon = -\frac{K\theta_G}{4}(V_X - V_Y)^2\left(\frac{V_{CM}}{2} - V_T\right) \tag{12}$$

V_{CM} being the common-mode input voltage of the current-voltage squarer. The great advantage of this implementation is that the additional error ε is proportional to the square of the differential input voltage $V_X - V_Y$, so no superior-order terms will appear in the $I - V$ characteristic of the CMOS active resistor as a result of the second-order effects. The only error introduced by these undesired effects will be a small changing of the equivalent resistance (no linearity degradation for the proposed circuit).

$$R_{ECH} = \frac{1}{\sqrt{KI_O}}\left[1 + \frac{\theta_G}{4}(V_{CM} - 2V_T)\right] \tag{13}$$

Small nonlinearities could be identified for large values of the active resistance, equivalent with small values of the reference current.

H. *The active resistor with controllable negative equivalent resistance*

The great advantage of the proposed implementation shown in Fig. 1 is that a circuit with a negative equivalent resistance could be very easily obtained by a minor change in the current-pass circuit presented in Fig. 6. The modified implementation of the current-pass circuit proposed for obtaining an active resistor with a negative equivalent resistance is presented in Fig. 7.

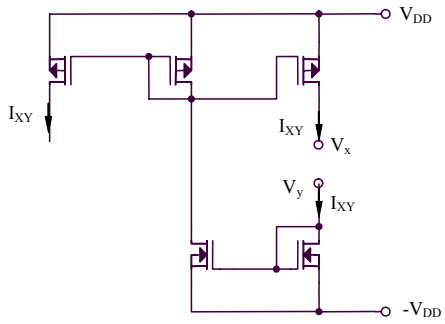

Fig. 7. The current-pass circuit for the active resistor with a negative equivalent resistance

The resulting expression of the active resistance will be $R'_{ECH} = -R_{ECH} = -1/\sqrt{KI_O}$. The advantage of the good controlability of R_{ECH} by the current I_O is still valuable, even for the negative resistance active resistor.

III. SIMULATED RESULTS

The low-power CMOS active resistor was implemented in $0.35\mu m$ CMOS technology. The SPICE simulation $I_{XY}(V_X - V_Y)$ of the active resistor is presented in Fig. 8. The maximum nonlinearity error of the active resistor for limited input voltage range ($|V_X - V_Y| \le 500mV$) is less than a percent.

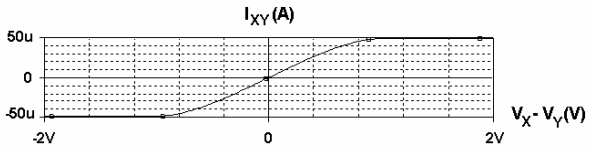

Fig. 8. The SPICE simulation $I_{XY}(V_X - V_Y)$

IV. CONCLUSIONS

A new active resistor circuit has been presented in this paper. The main advantages of the original proposed implementation are the improved linearity, the small area consumption and the improved frequency response. Because of an original design technique, the circuit linearity is not affected by the second-order effects that alter the MOS transistor operation. The reduced complexity obtained by using a FGMOS transistor was made maintaining the compatibility with classical technologies (the classical FGMOS device could be replaced by an original equivalent circuit using exclusively classical MOS devices). The frequency response of the circuit is very good as a result of operating all MOS transistors in the saturation region. The circuit was implemented in $0.35\mu m$ CMOS technology, the SPICE simulation confirming the theoretical estimated results and showing a linearity error under a percent for an

extended input range ($\pm 500mV$) and a small value of the supply voltage ($\pm 3V$). In order to design a circuit having a negative equivalent resistance, an original method specific to the proposed implementation of the active resistor circuit will be presented. In order to obtain a low-power operation of the proposed active resistors, the MOS active devices could be biased in weak inversion, while the complementary squaring/square-root functions must be replaced by logarithmical/exponential functions.

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