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Current-Steering Digital-to-Analog Converter/ Programmable Sub-Bandgap Voltage Reference with Split Input Code

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Abstract - In this paper we will offer a concrete solution of a DAC which will be used in high speed and medium resolution applications. This DAC presents an important innovation as the voltage reference does not represent a distinct block, but it overlaps the functional diagram of the converter. This was considered to be of current-steering type with MOS transistors in standard CMOS technology like in most of the recent works. The new solution also implies the splitting in two equal parts of the digital input code applied to the converter. This will drastically diminish the number of large dimension transistors used in the current sources of the converter.
Keywords: current-steering digital-to-analog converter, sub-bandgap voltage reference, split input code

I. INTRODUCTION

The recent tendency in the field of analog and mixed integrated circuit manufacturing is to use technological processes which are accessible in terms of price as the standard CMOS process. Furthermore the supply voltages become lower and lower to meet the growing request of portable equipments on the market. Most of the works which deal with the subject of Nyquist frequency DAC-s design suggest the use of a reference voltage source which must be able to work at these low supply voltages. Thus, sub-bandgap reference voltage sources have been developed [8], [9], [10] and obviously they provide an output voltage lower than 1.2V.
There are two premises as starting point of this paper:
1. The sub-bandgap voltage source is attached to DAC either as a distinct integrated circuit or it is integrated in the same chip next to the converter as it is presented in [1], [2], [3], [4].
2. The most widespread types of Nyquist frequency DAC-s are current-steering DAC-s, a statement sustained by recent works, such as [1], [2], [4], [5]. For these types of converters, exact theoretical models have been elaborated. These models allow an easy evaluation of the static and dynamic performances of the converter [5], [6].
Taking into consideration these two aspects, we will show along this paper how the sub-bandgap source and the DAC will be joined in a single, inseparable circuit which will benefit of the qualities of both circuit types.

II. SUB-BANDGAP VOLTAGE REFERENCE

It is known that the bandgap voltage has two components: the first is represented by the voltage across a directly biased junction and the second is proportional to absolute temperature (PTAT). The negative temperature coefficient of the first component (-2mV/K) is compensated by the positive coefficient of the second. If, in order to get the PTAT voltage, the thermal voltage $V_T=kT/q$ is used, this has to be multiplied with approximately n=23. In these terms the bandgap voltage is given by equation (1):

$$V_{BG}=V_{BE}+n\frac{kT}{q} \qquad (1)$$

and it is ≈1.2V. In equation (1) k is Boltzmann's constant, T is absolute temperature and q is electronic charge.
By using a low supply voltage (e.g. 1V) it is obvious that the 1.2V value can not be produced anymore. However a fraction of this voltage with the same thermal properties can be generated if we can produce currents proportional with both V_{BE} and V_T. These currents will be weighted, summed up and injected in a resistor to obtain the desired output voltage. Finally, the value of the reference voltage will be obtained as a fraction of bandgap voltage, established by a resistor ratio. This type of circuit was suggested by Banba and Malcovati in [8] and [9] and it is shown in fig.1.
Through the pnp-lateral transistors Q1 and Q2 connected as diodes and with the ratio of emitter junction areas equal to N_E, the same current will pass, imposed by current mirror M1, M2 (pMOS transistors). As the operational amplifier (OPAMP) forces the potentials Va and Vb to be equal, the voltage across the resistor R0 will be $U_{R0}=\Delta V_{BE}=V_T\ln(N_E)$ and so the currents through R1

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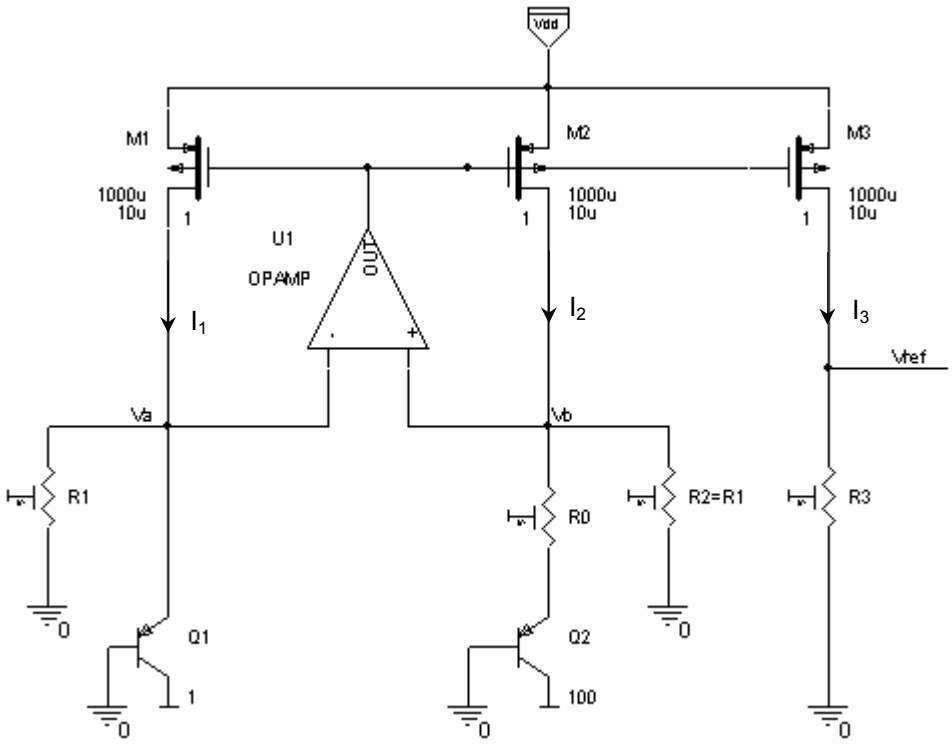

Fig.1 Sub-bandgap voltage reference

and R2, which are equal, will be proportional to V_{BEQ1} (i.e. they will have a negative temperature coefficient). Thus, the currents through M1, M2, M3 which are identical will have the following value:

$$I_1 = \frac{V_T \ln(N_E)}{R_0} + \frac{V_{BE}}{R_1} \tag{2}$$

The output voltage will be:

$$V_{out} = I_1 R_3 = V_T \frac{R_3 \ln(N_E)}{R_0} + V_{BE} \frac{R_3}{R_1} = \\ = \frac{R_3}{R_1}\left[\frac{R_1 \ln(N_E)}{R_0} V_T + V_{BE}\right] \tag{3}$$

The thermal compensation of the output voltage will take place only if :

$$\frac{R_1 \ln(N_E)}{R_0} = 23 \tag{4}$$

As we can see, the bandgap voltage of 1.2V can be weighted by the ratio R3/R1 and if R3 is small enough, very low value reference voltages can be obtained.

For example, imposing the value of the output voltage 0.5V, for N_E=100 the following values of the resistors resulted: R1=R2=80kΩ, R0=18.14kΩ and R3=34kΩ. Only R3 will change if we establish another value of the output voltage.

III. BLOCK DIAGRAM OF PROPOSED DAC

As it was shown in section II, the sub-bandgap reference taken into consideration allows us to obtain a current independent of temperature which is mirrored in the third branch of the circuit and injected in the resistor R3. This resistor must be made of the same kind of material as the other resistors from the circuit. We can say that the voltage reference becomes programmable if we can programme the value of R3.

Another way to obtain a programmable output voltage is to mirror the output current of the reference in more branches through which the currents are switched or not towards the resistor R3 of constant value. If, by using the unit element principle, like in [5], we add 2^N-1 unit current sources controlled by N switches which are supposed to lead or not a current through R3 we could obtain an N-bit DAC. Surely, the LSB will control a single unit current source, the next will control two unit current sources, while the MSB will control 2^{N-1} unit current sources.

As both the current sources block and the resistor R3 belong equally to the voltage reference and to the converter or, more precisely, because, in fact, the whole converter is included in the sub-bandgap mechanism, we obtained a single, inseparable circuit resulted from the overlapping of the two types of circuits.

In order to avoid a sudden current step on the switched current sources we must ensure dual, complementary current outputs. Thus, the currents corresponding to the digital input code as well as those which will not contribute to the output voltage manufacturing will be summed up in two distinct

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nodes and will be led through equal value resistors towards the ground.

The major disadvantage of this type of converter is that it used a very large number of pMOS transistors. The number of the transistors which make up the unit current sources (which have to be of large dimensions in order to ensure a perfect equality of unit currents) is 2^N-1. For example, if N=10, we must use 1023 transistors.

Our new solution implies the splitting into equal parts (for an even number of bits) of the digital input code applied to the converter. In these conditions, we will have two identical blocks. Each block will be controlled by N/2 bits and will contain $2^{N/2}$-1 unit current sources. In order to ensure the weighting of $2^{N/2}$:1 in the output voltage contribution, the nodes in which the currents of the two blocks will be summed up are connected as shown in fig.2. The ratio of resistor values R8 and R9 (which replace R3), respectively R10 and R11 (for the complementary output) must be $2^{N/2}$-1. This will drastically diminish the number of large dimension transistors used in unit current sources. For example, if N=10, we must use only $2\times(2^5-1)=62$ transistors.

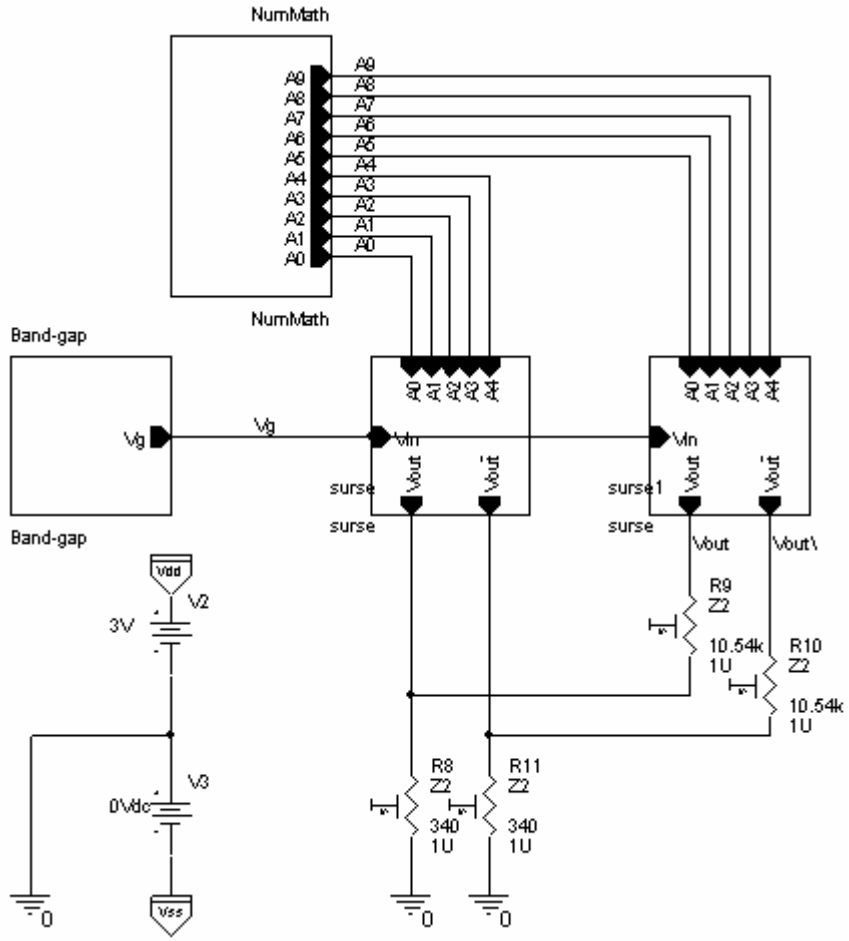

Fig.2 Block diagram of proposed DAC

The maximum number of bits of a converter that doesn't need trimming for the resistors mentioned above is given by the precision with which we can manufacture the ratio of the resistors and which is 0.1%, i.e. 1:1000 or roughly $1:2^{10}$. This limits the resolution of the converter to 10 bits.

In fig.2, the delimitation between the blocks "Band-gap" and "Surse" is purely formal and it was adopted for optimising and organising the block diagram of the converter on hierarchical blocks.

IV. DAC DESIGN AND SIMULATION

As mentioned in the previous section the ratio between R8 and R9 (which replaced R3 from fig.1) must be 1:31. As follows, we note the equal currents through the two first branches of the sub-bandgap block I_{BG} and the currents generated by the unit current sources I_u. The transfer function of the converter will be:

$$V_{out} = 1{,}2\frac{I_u}{I_{BG}}\left(\frac{R_8}{R_1}\sum_{i=0}^{4}A_i 2^i + \frac{R_8+R_9}{R_1}\sum_{i=0}^{4}A_{i+5}2^i\right) =$$

$$= 1{,}2\frac{I_u}{I_{BG}}\frac{R_8}{R_1}\left(\sum_{i=0}^{4}A_i 2^i + 32\sum_{i=0}^{4}A_{i+5}2^i\right) =$$

$$= 1{,}2\frac{I_u}{I_{BG}}\frac{R_8}{R_1}\left(\sum_{i=0}^{4}A_i 2^i + \sum_{i=0}^{4}A_{i+5}2^{i+5}\right) =$$

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$$= 1{,}2\frac{I_u}{I_{BG}}\frac{R_8}{R_1}\sum_{i=0}^{9}A_i 2^i = 1{,}2\frac{I_u}{I_{BG}}\frac{R_8}{R_1}2^{10}\sum_{i=0}^{9}A_i 2^{i-10}$$

[V] (5)

Imposing the resolution of the converter to be 0.5mV and $I_u/I_{BG}=1/10$ ($(W/L)_u/(W/L)_{BG}=1/10$) the resulting values of the resistors R8, R9, R10 and R11 are shown in fig.2. The maximum output voltage of the converter is 0.5mV×1023=511.5mV.

The structure of the "Surse" blocks which include 31 unit current sources each is presented in fig.3.

The structure of the "S_unitara" block from fig.3 and which includes a unit current source (M4) and the corresponding switch is shown in fig.4. .

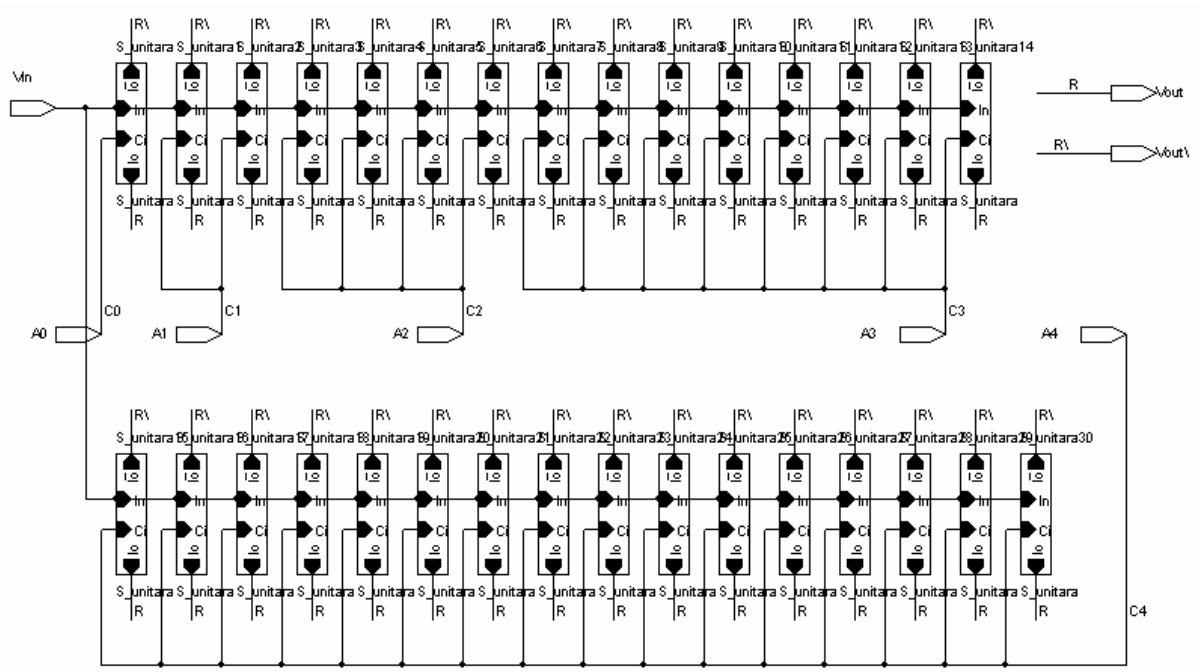

Fig.3 Structure of "Surse" blocks from fig.2

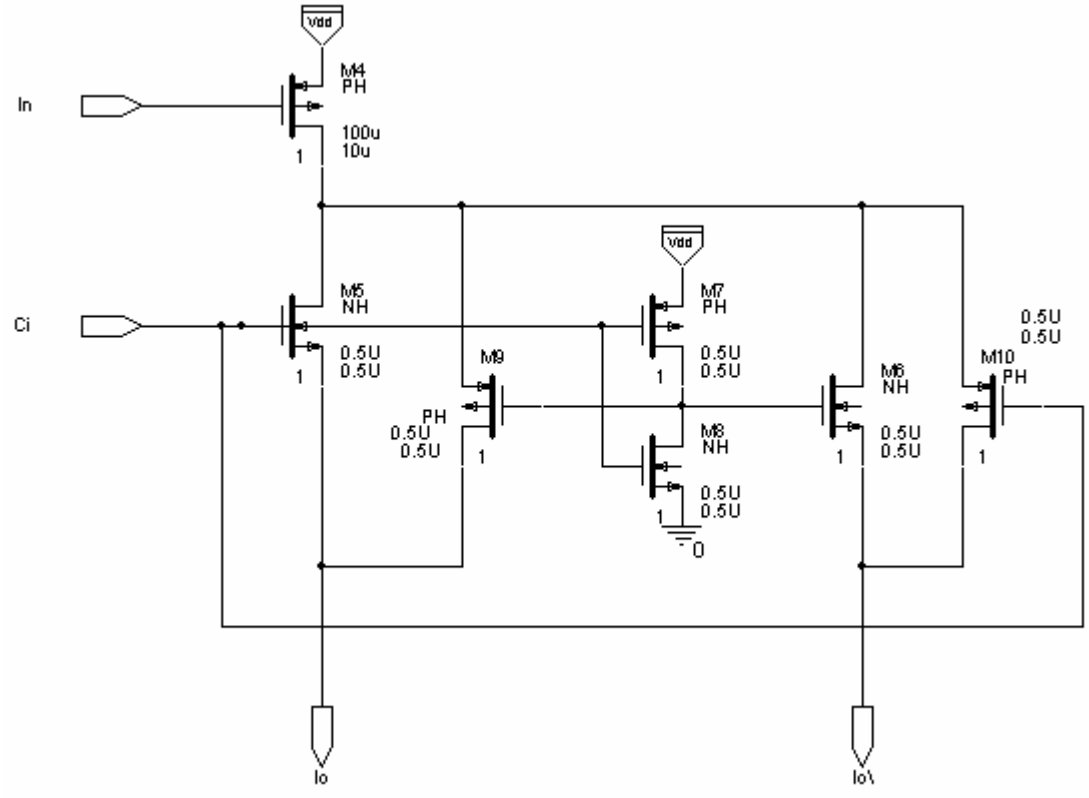

Fig.4 Structure of "S_unitara" block from fig.3 which includes a unit current source (M4) and the corresponding switch

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In order not to affect the control voltage V_{GS} of the transistor M4 through which the reference current is imposed, the current switch was placed in its drain and it was made with two transmission gates M5, M9 respectively M6, M10 controlled in opposite-phase conditions to ensure a permanent conduction for transistor M4. The use of transmission gates instead of simple transistors is compulsory because the circuit works with low supply voltage and because a variable potential can appear at the outputs Io and Io/. In this way at least one transistor (out of M5, M9) is perfectly "on" and M4 is maintained saturated.

At the same time, the control with opposite-phase signals minimises the clock feedthrough. On the other hand the charge injection is also minimised because of the small dimensions of the switch transistors. The opposite-phase control is ensured by the inverter M7, M8.

The necessary digital stimuli for the simulation of the converter are provided by the block "NumMath". This is a counter built with elements that present ideal mathematical models of some circuit functions and which allows the generation of consecutive binary sequences in which all the bits are switched simultaneously. This block was designed according to [7].

The converter was simulated using OrCAD programme version 10.3 in which the models of the components correspond to 0.35µm CMOS process.

In the sub-bandgap reference we used an ideal model of the operational amplifier, but in which the gain was set at 1000 that corresponds to a real case, easy to obtain in design using only two amplifier stages. To ensure the stability of the circuit it was necessary to integrate a capacitance of 2pF between the inverting input and the output of the operational amplifier. As we can see in fig.5 the output voltage is set to 0.5V and it vary with only 1mV if the temperature changes from -30°C to 100°C.

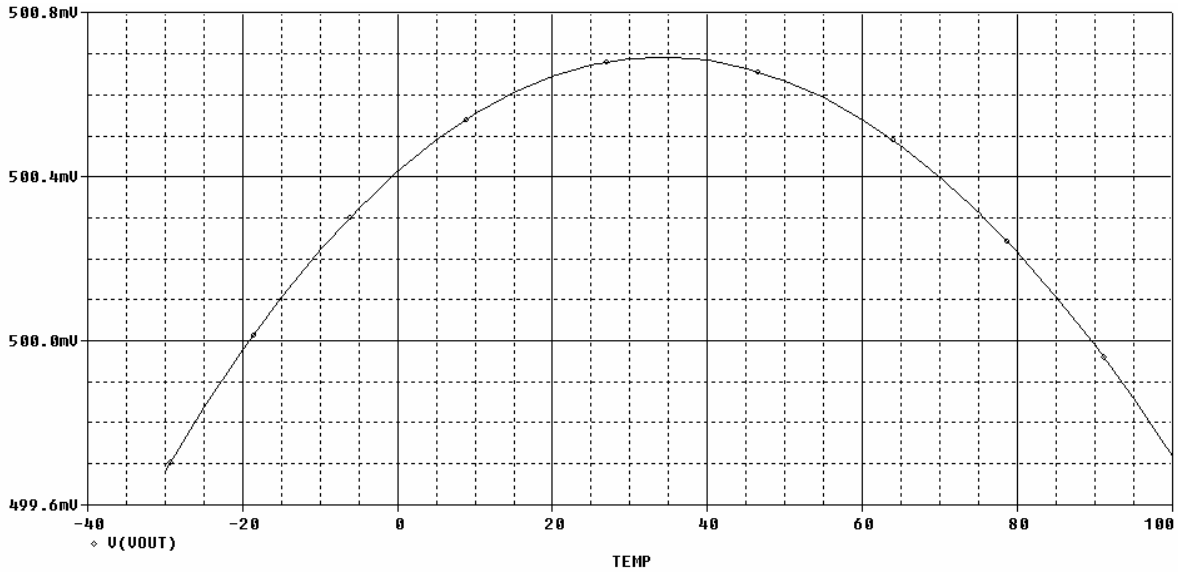

Fig.5 Simulation results of sub-bandgap voltage reference

The simulation of the whole converter was made by using a supply voltage of 3V, as we can see in fig.6, but similar results were obtained for lower supply voltages like 2V or 1V. This confirmed that the pMOS transistors of the unit current sources remained in the saturation region. As we can observe from fig.6.b the converter works very good at 10MHz because, despite the glitches that appeared, the settling time of the converter is not so much affected. If we examine the cursors, we can observe that the voltage step corresponds to the resolution of the converter and a DNL of about 15µV.

V. CONCLUSIONS AND PERSPECTIVES

In this paper we proposed a 10-bit current-steering DAC overlapping a sub-bandgap voltage reference. The converter is controlled by a split digital input code (2×5b) that allows a drastic diminishing of the number of unit current sources.

The solution presented here can be an excellent starting point to design a DAC with very good static and dynamic performances. Our future research will focus on:

-the second order correction for the sub-bandgap voltage reference for improving the thermal behaviour of the converter, as in [9];

-design of a high-speed operational amplifier that will be connected as follower with the inputs at the complementary outputs of the converter; this will diminish the effect of parasitic capacitance switching towards the nodes which don't have different potential anymore. We expect an important reducing of the glitches and an increasing of the converter speed;

-introducing a thermometer code (easy for the two 5-b sections of the digital input code) and a randomiser that would minimise the effect of the matching errors which affect the pMOS transistors of the unit current sources.

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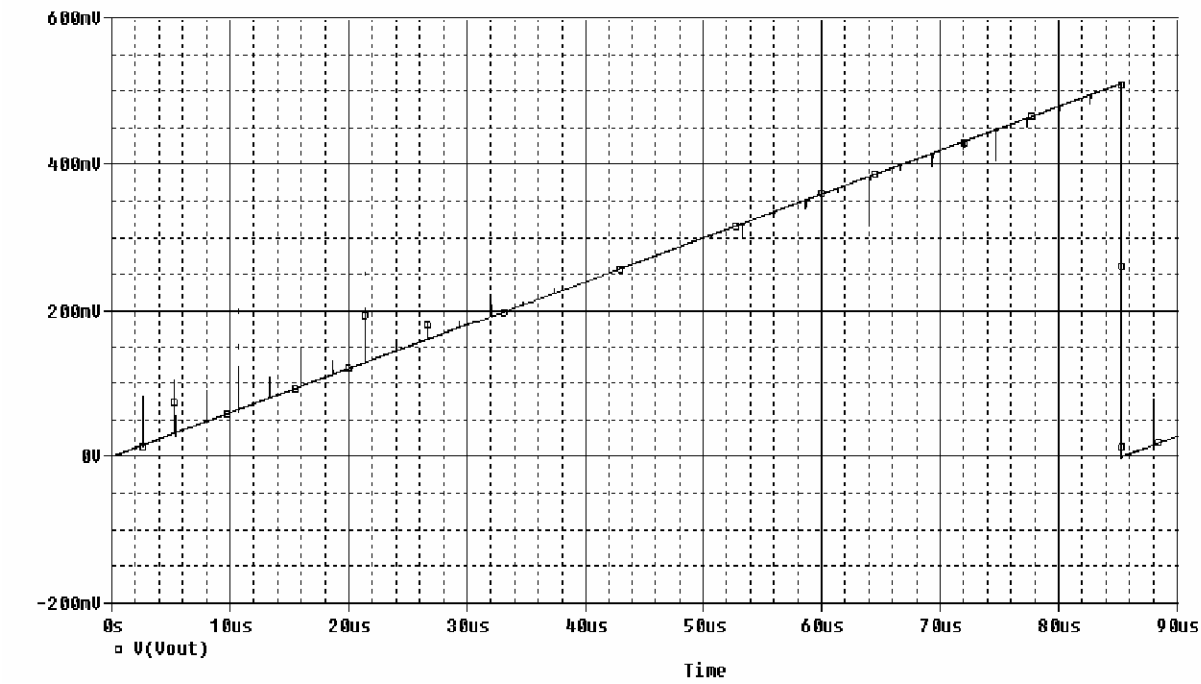

Fig.6.a Simulation results of DAC for all digital input combinations

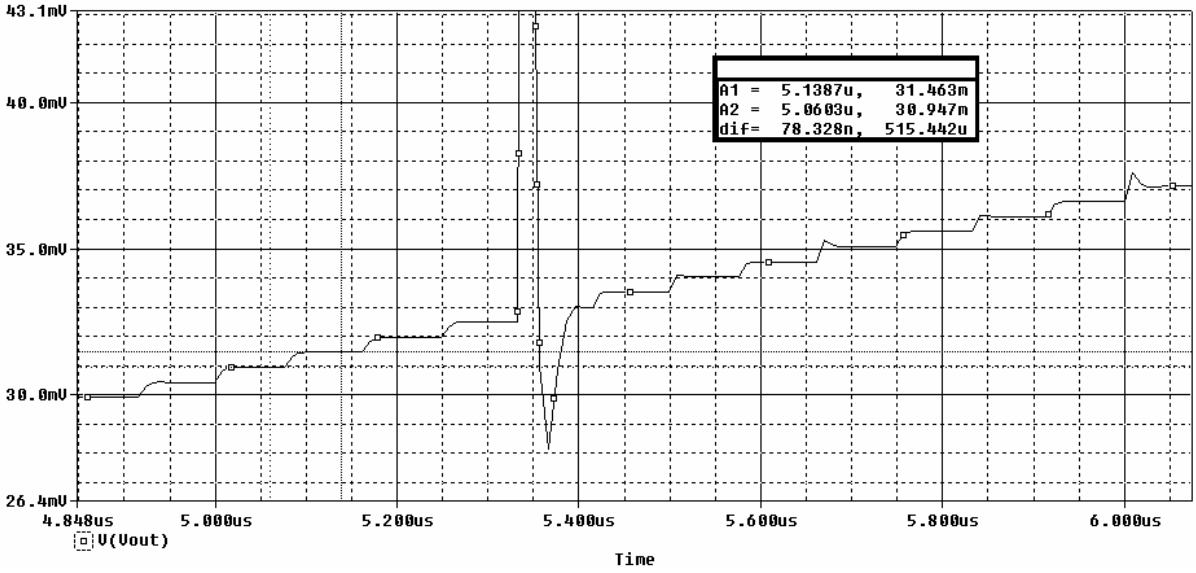

Fig.6.b Simulation results of DAC; detail of glitch

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