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Short-circuit power evaluation of deep submicrometer CMOS gates driving lossless transmission lines

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Abstract – In this paper the short-circuit power of a CMOS gate driving a inductive – capacitive (lossless) transmission line is investigated. The case of input signal transition time smaller than twice the transmission line propagation delay is considered. Closed-form expressions for the output voltage, short-circuit power and short-circuit to dynamic power ratio are derived. Also, a formula for calculating the transistor widths for the matched condition is obtained. The nth power law MOSFET model for short-channel devices is used. The analytical results are in very good agreement with SPICE simulations.

Keywords: submicrometer CMOS gates, interconnections, transmission lines, short-circuit power dissipation

I. INTRODUCTION

Nowadays, due to the continually scaling of CMOS technology and increasing chip size, the role of interconnections in determining circuit performance is growing in importance [1]. In addition, the inductive component of the interconnections is becoming more important with decreasing signal transition times and longer wire lengths [2], [3]. Therefore, more accurate RLC transmission lines models are necessary in the analysis of actual VLSI circuits. The RC and LC models can be seen as limiting cases of the RLC transmission lines models. These cases are well represented in the literature [4], [5]. The LC model approximates the low-loss lines encountered in multichip modules (MCMs) and printed circuit boards (PCBs). Although an on-chip interconnect has a non-negligible resistance, the LC analysis provides an upper limit for analyzing inductive effects in VLSI circuits.

On the other hand, the calculation of critical path delay or power dissipation in large VLSI systems using a transistor level simulator, like SPICE, can be very expensive in terms of storage and computation time. Hence, much of past research addressed the development of analytical models of propagation delay and power dissipation for CMOS gates, without the necessity of expensive numerical iterations [6], [7]. These analytical models can be incorporated in CAD tools optimizing the design verification procedure.

In this paper the short-circuit power of deep submicrometer CMOS gates driving lossless transmission lines is analyzed. The *n*th power low MOSFET model, which takes into account the carriers' velocity saturation effects of deep submicrometer CMOS technologies, is used for the transistors' current. This model is more accurate in the linear region and in determining the drain-to-source saturation voltage as compared to the α–power law MOS model, avoiding any discontinuity between the linear and saturation regions.

Firstly, analytical expressions for the output voltage of a CMOS inverter driving a lossless transmission line is obtained. The output voltage expressions are derived analyzing the reflections at the far end and the near end of the transmission line. A formula for calculating the transistor widths for the matched condition is, also, obtained.

Based on the analytical expressions of the output voltage, a formula of short-circuit power that occurs in the time interval when both the NMOS and PMOS transistors are in conduction is obtained. The short-circuit energy dissipated during an input transition is evaluated as a product between the power supply V_{DD} and the approximated area delimited by the short-circuiting transistor current and the current through its gate-to-source capacitance. Also, the dependence of the short-circuit power to dynamic power ratio on device and transmission line parameters is analyzed.

Finally, the analytical expressions are compared with circuit simulations for several submicrometer CMOS technologies, and for a wide range of input transition time, transistor sizes and transmission line parameters.. The experimental results show a very good agreement with SPICE simulations.

II. OUTPUT VOLTAGE ESTIMATION

In the following analysis consider the equivalent circuit of a CMOS inverter driving a lossless transmission line shown in Fig. 1. The output voltage derivation is for a falling input ramp

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$$V_{in} = \begin{cases} V_{DD} - (V_{DD}/\tau)\cdot t & 0 \le t \le \tau \\ 0 & t > \tau \end{cases} \quad (1)$$

where τ is the input transition time. The analysis for a rising input ramp is symmetrical.

Noting T_D the transmission delay of the line, in the time interval $0 < t < 2T_D$, the transmission line can be replaced by its characteristic impedance $Z_0 = \sqrt{L_l / C_l}$, where L_l and C_l are the total inductance and capacitance of the line, respectively.

The *n*th power law MOS model [8] which is assumed for the transistor currents is more accurate in the linear region and in determining the drain-to-source saturation voltage as compared to the α–power law model [9], avoiding any discontinuity between the linear and saturation regions. Thus, in the saturation region ($V_{DS} \ge V_{Dsat}$), the drain current is

$$I_D = I_{Dsat} = (W/L)B(V_{GS} - V_T)^n (1 + \lambda V_{DS}) \quad (2)$$

and in the linear region ($V_{DS} \le V_{Dsat}$), the current is

$$I_D = I_{Dsat}\left(2 - \frac{V_{DS}}{V_{Dsat}}\right)\frac{V_{DS}}{V_{Dsat}} \quad (3)$$

where $V_{Dsat} = K(V_{GS} - V_T)^m$. In these model equations, W and L are the geometric width and length, respectively, of the transistor channel, and V_T is the threshold voltage. n, m, B, K and λ are constants which describe the short-channel effects in an empirical manner. For instance, the parameter n models the carriers' velocity saturation effect taking values between 1 (for ultra-deep submicrometer devices) and 2 (for long channel devices). A comparison between the *n*th power law model and α–power law model is shown in Fig. 2.

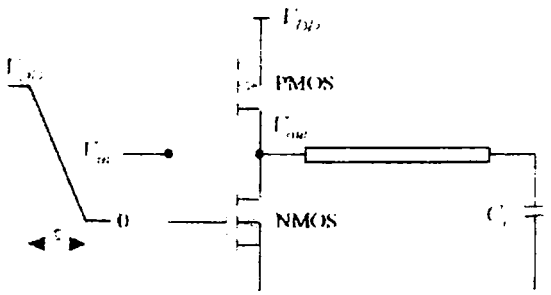

Fig. 1. CMOS inverter driving a lossless transmission line

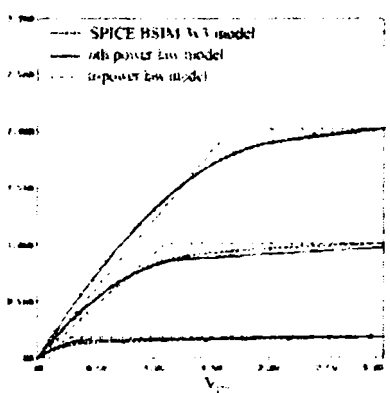

Fig. 2. Comparison between the *n*th power law MOS model, α-power law model and SPICE BSIM 3v3 model

For the equivalent circuit from Fig. 1, initially, the output voltage is 0. Ignoring the effect of the NMOS transistor for a falling input, after the time point $t = (V_{Tp}/V_{DD})\tau$, the PMOS transistor enters in conduction in saturation region and, consequently, the output voltage is given by the product of PMOS current and characteristic impedance of the transmission line:

$$V_{out} = Z_0 I_{psat} \quad (4)$$

Due to the fact that I_{psat} depends on both V_{in} and V_{out}, the expression for the beginning part $V_0(t)$ of the output voltage which results from (4) is

$$V_0(t) = \frac{\frac{W_p}{L_p} B_p \left(V_{DD} - V_{in} - |V_{Tp}|\right)^{n_p} (1 + \lambda_p V_{DD}) Z_0}{1 + \lambda_p \frac{W_p}{L_p} B_p \left(V_{DD} - V_{in} - |V_{Tp}|\right)^{n_p} \cdot Z_0} \quad (5)$$

At time $t = \tau$ when the input voltage reaches its final value of zero volts, the initial output voltage waveform reaches a maximum value V_1 given by

$$V_1 = \frac{I_{ps_1}(1 + \lambda_p V_{DD}) Z_0}{1 + \lambda_p I_{ps_1} Z_0} \quad (6)$$

where $I_{ps_1} = (W_p/L_p) B_p \left(V_{DD} - |V_{Tp}|\right)^{n_p}$. This initial output voltage signal, shown in Fig. 3, propagates across the line and reaches the load at time T_D.

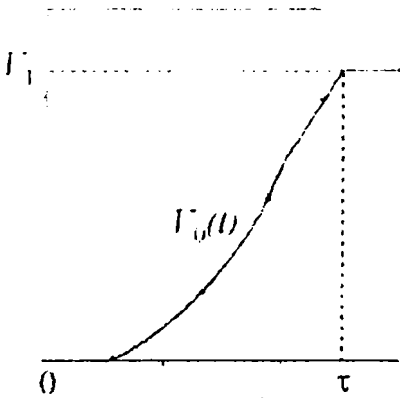

Fig. 3. The initial output voltage waveform generated by CMOS inverter during the falling input transition

Assuming the load is open or is a small capacitor, the signal reaches a steady-state value of $2V_1$ due to the reflection. The time required to reach this value depends on the time constant Z_0C_L. Typically, this time constant is in order of a few picoseconds and is sufficiently small to neglect the effects of the load p [3]. I v l $T_D < t < 2T_D$, reflected voltage wave with the magnitude V_1 propagates back toward the CMOS inverter. At time $2T_D$, this voltage wave is reflected again by the PMOS transistor being initiated a new voltage wave with the magnitude V_2. Thus, after the time $2T_D$ the output voltage of the CMOS inverter becomes $V_{out} = 2V_1 + V_2$, as can be seen in Fig. 4. The value of V_2 is given by he imp dan i Z_0 m ipli d by he current of the PMOS transistor with the source-to-

drain voltage $V_{SDp} = V_{DD} - 2V_1 - V_2$ and source-to-gate voltage $V_{SGp} = V_{DD}$. Assuming that the PMOS transistor is in the saturation region the value of V_2 is

$$V_2 = \frac{I_{ps_1}\left[1 + \lambda_p(V_{DD} - 2V_1)\right]Z_0}{1 + \lambda_p I_{ps_1} Z_0} \qquad (7)$$

For the period of time from $2T_D$ to $4T_D$ the cycle is repeated and a new voltage of magnitude V_3 is initiated at time $4T_D$. As long as the PMOS transistor is still in saturation, each new voltage wave which is initiated has a magnitude V_k calculated similar as V_2 replacing in (7) the voltage V_1 by the sum $V_1 + V_2 + \ldots + V_{k-1}$. If at the times $t = 2(k-1)T_D$ the condition $V_{DD} - 2\sum_{i=1}^{k-1} V_i - V_k \le K_p\left(V_{DD} - |V_{Tp}|\right)^{m_p}$ is satisfied, then the PMOS transistor is in its linear region and the magnitude V_k is obtained from the nonlinear equation

$$V_k = Z_0 I_{plin}(V_k) \qquad (8)$$

Neglecting the channel length modulation effect in the linear region and linearizing the equation (8) around the value of zero, the resulting solution is [12]

$$V_k = \frac{I_{ps_1}(2 - P_{k-1})P_{k-1}}{1 + \frac{4I_{ps_1}}{V_{dsp_1}}(1 - P_{k-1})} \qquad (9)$$

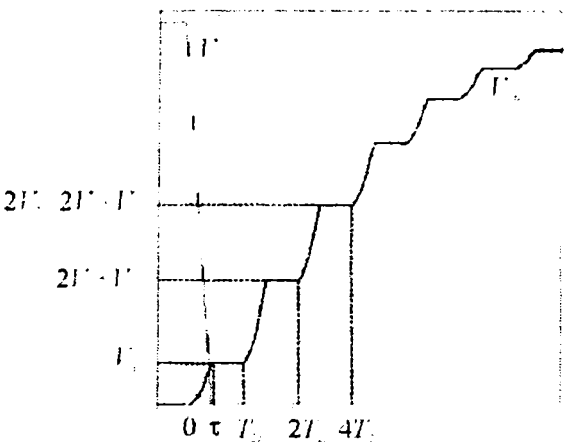

Fig. 4. Voltage waveform at the output of the PMOS transistor driving an open circuit transmission line

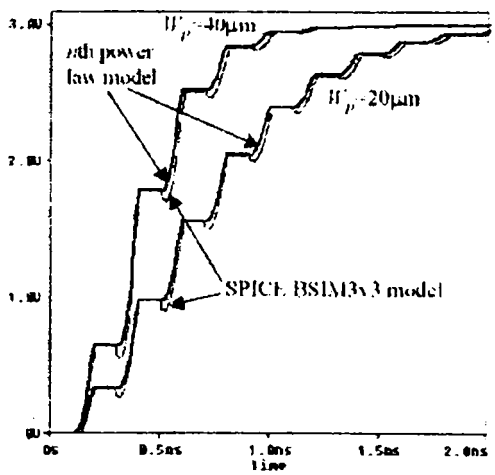

Fig. 5. Comparison between the analytical output voltage and SPICE simulations for two values of the PMOS channel width

where $P_{k-1} = \left(1/V_{dsp_1}\right)\left(V_{DD} - 2\sum_{i=1}^{k-1} V_i\right)$. The initiating process of the new wave repeats until the voltage at the output of the CMOS inverter reaches the steady state value of V_{DD}. Fig. 5 shows that the output voltage waveforms based on the analytical expressions, for two values of the PMOS channel width, are very close to the ones resulted from SPICE simulations.

On the other hand, as it can be seen in Fig. 6, while the input transition time increases with respect to T_D, the horizontal portions of output voltage become shorter. Thus, for $\tau > 2T_D$, the horizontal portions of the response does no longer exist and the lossless transmission line behaves as a single lumped capacitor equal to the input capacitance of the line.

Due to the fact that the signal transition times are decreasing in next generation VLSI circuits while wires are becoming longer, the most important region of interest when analyzing the effects of on-chip interconnections occurs when $\tau < 2T_D$.

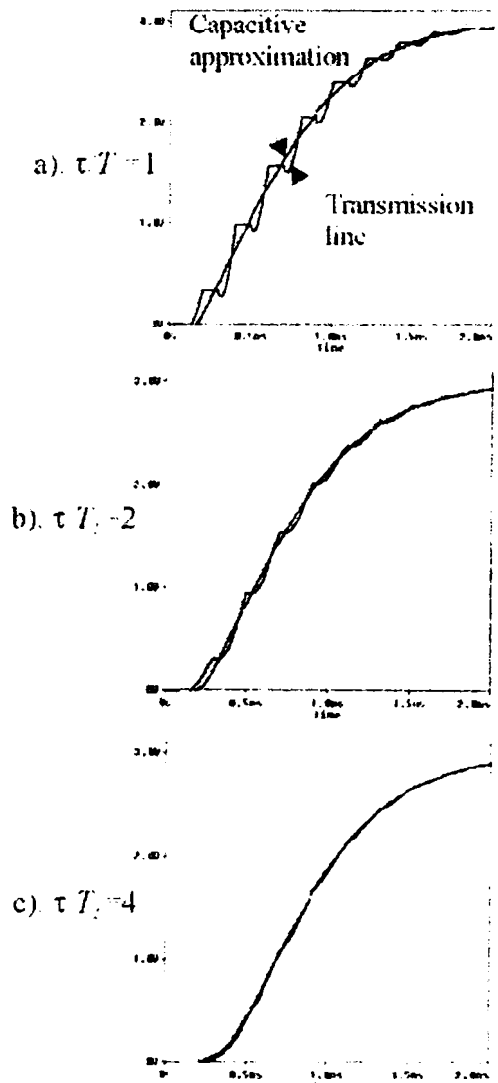

Fig. 6. Input transition time effect on the capacitive approximation of the transmission line for three values of the ratio τ/T_D.

III. MATCHING CONDITION

For a given lossless transmission line with the characteristic impedance Z_0 and the time delay T_D, the number of the generated voltage waves depends on the driving capability of the transistor. Thus, if the geometric width of the transistor is small, results a small magnitude V_1 of the initial voltage signal. Also, the magnitudes of the all reflected voltage at the output of the CMOS inverter are small. In this case, due to the great number of iterations in which the signals propagate across the line, the output voltage reaches its final value of V_{DD} after a long time. For greater values of the geometric width of the transistor, the magnitudes of the signal which propagate across the line become greater and, so, a smaller number of iterations are required until the output voltage reaches its final value.

If the width of the transistor is adjusted to a value so the magnitude V_1 of the initial voltage wave that is launched to the transmission line is $V_{DD}/2$, then at time $2T_D$ when the reflected wave reaches the transistor, the output voltage becomes V_{DD}.

Consequently, the drain-to-source voltage of the PMOS transistor becomes zero volts and the transistor no longer conducts any current. Thus, there is no any reflection and the output voltage reaches its final value in a single iteration. In this case, the CMOS inverter and the transmission line are said to be matched.

The width of the PMOS transistor that satisfies the matching condition can be determined from

$$I_p\left[V_{SG_p}=V_{DD}, V_{SD_p}=V_{DD}/2\right]=\frac{V_{DD}}{2Z_0} \qquad (10)$$

where $I_p\left[V_{SG_p}=V_{DD}, V_{SD_p}=V_{DD}/2\right]$ is the PMOS transistor current when the source-to-gate voltage is V_{DD} and the source-to-drain is $V_{DD}/2$. Due to early saturation phenomena of deep submicrometer devices [9], equation (10) is resolved considering the nth power law model of the transistor current for saturation region. Thus, the geometric width W_{p_M} of the PMOS transistor for the matched condition is

$$W_{p_M}=\frac{V_{DD}}{2Z_0\frac{B_p}{L_p}\left(V_{DD}-\left|V_{Tp}\right|\right)^{n_p}\left(1+\lambda_p\frac{V_{DD}}{2}\right)} \qquad (11)$$

The geometric width W_{n_M} of the NMOS transistor for the matched case is obtained in a similar manner. The CMOS inverter is full matched to a transmission line if both PMOS and NMOS transistors are matched to the line. In this case, the output impedance of the CMOS inverter is equal to the characteristic impedance of the line for both rising and falling input ramp.

The line is said to be underdriven if the widths of the transistors of the CMOS inverter driving the transmission line are smaller than the transistor widths in the matched case, such that the output impedance of the CMOS inverter is greater than the characteristic impedance of the line. If wider transistor are used, as compared to the matched widths, the output impedance of the CMOS gate is smaller than the value of Z_0 and the output response is overdriven with overshoots and undershoots.

Fig. 7.a. shows the SPICE simulations for the matched condition that demonstrate the accuracy of the equation (11), while Fig. 7.b. illustrates an underdriven case (the channel width is half of matching width).

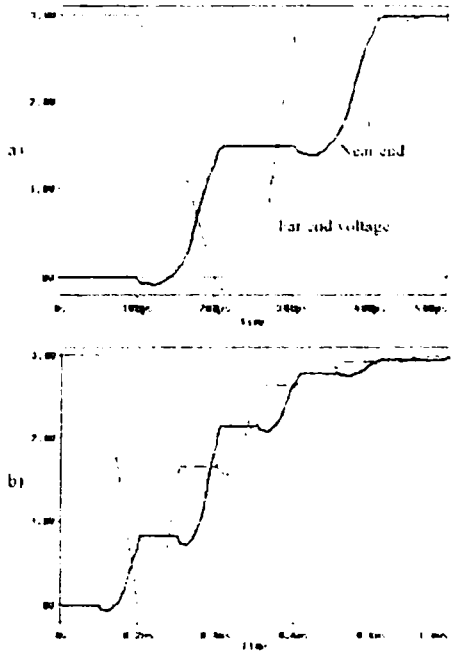

Fig. 7. SPICE simulation for a CMOS inverter driving a lossless transmission line a). matched case b). underdriven case

IV. SHORT-CIRCUIT POWER DISSIPATION

The power dissipated in a CMOS gate driving a transmission line consists of dynamic (or switching) power, leakage (or stand-by) power and short-circuit power components.

The short-circuit power is dissipated when both the NMOS and PMOS transistors conduct at the same time, namely during the time interval when the rising (falling) input voltage is between V_{Tn} and $V_{DD}-|V_{Tp}|$, where V_{Tn} is the threshold voltage of the NMOS transistor. This power is investigated below for the case when $\tau < 2T_D$. In this case, the reflections do not affect the short-circuit power because the initial output signal has reached its final value. Therefore, for the time interval 0 to τ, the transmission line appears as a resistance with a value of Z_0. Considering the case of rising input voltage $V_{in}=(V_{DD}/\tau)t$, the line is assumed to be charged to V_{DD}. The equivalent circuit used to determine the short-circuit power is shown in Fig. 8.

In order to obtain better results, the gate-to-source capacitance C_{GSp} of the PMOS transistor is taken into account. Thus, the short-circuit current I_{SC} is given by

$$I_{SC}=I_p-I_{GS} \qquad (12)$$

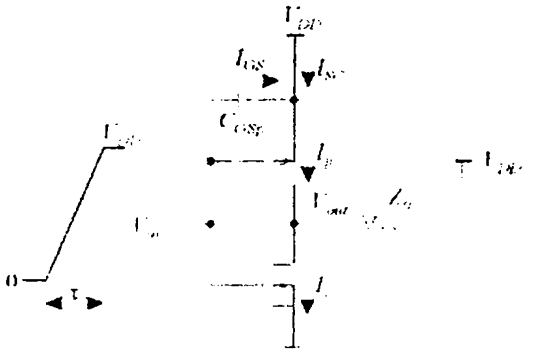

Fig. 8. The circuit used to determine the short-circuit power

where I_p is the source-to-drain current of the PMOS transistor and I_{SC} is the current trough capacitor C_{GSp}. During the first part of the rising input voltage, the PMOS transistor operates in the linear region and, after that, it enters in the saturation region. When the PMOS transistor operates in the linear region, the current I_p is given by

$$I_p = \frac{W_p}{L_p} B_p \left(V_{DD} - \frac{V_{DD}}{\tau} t - \left|V_{Tp}\right| \right)^{n_p} \left(2 - \frac{V_{DD} - V_{out}}{V_{DSAT_p}} \right) \left(\frac{V_{DD} - V_{out}}{V_{DSAT_p}} \right) \left[1 + \lambda_p \left(V_{DD} - V_{out} \right) \right] \tag{13}$$

where $V_{DSAT_p} = K_p \left(V_{DD} - \frac{V_{DD}}{\tau} t - \left|V_{Tp}\right| \right)^{m_p}$ and V_{out} is the output voltage of the CMOS inverter, expressed as $V_{out}=V_{DD}-V_0(t)$. Here, $V_0(t)$ is the initial voltage pulse with negative from equation (5), except the index p is replaced by n.

When the PMOS transistor is in the saturated region, the current Ip is

$$I_p = \frac{W_p}{L_p} B_p \left(V_{DD} - \frac{V_{DD}}{\tau} t - \left|V_{Tp}\right| \right)^{n_p} \left[1 + \lambda_p \left(V_{DD} - V_{out} \right) \right] \tag{14}$$

The current I_{GS} is given by

$$I_{GS} = C_{GSp} \frac{\mathrm{d}\left(V_{in} - V_{DD}\right)}{\mathrm{d}t} = C_{GSp} \frac{V_{DD}}{\tau} \tag{15}$$

Because C_{GSp} has different values in the linear and saturation regions, I_{GS} has the constant values I_{GS1} and I_{GS2} when PMOS transistor operates in the linear region and saturation region, respectively.

The short-circuit energy dissipated during an input transition can be evaluated as a product between V_{DD} and the area delimited by PMOS current I_p and capacitive current I_{GS}. This area can be evaluated simpler if a linear approximation of I_p current is used, as shown in Fig. 9. In this figure $t_n = (V_{Tn}/V_{DD})\tau$ and $t_p = \left(1 - \left|V_{Tp}\right|/V_{DD}\right)\tau$ define the times when NMOS transistor starts to conduct and PMOS transistor becomes off. Time t_s corresponds the moment when PMOS transistor enters in saturation region and is a solution equating the two expressions (13) and (14) of PMOS current for linear and saturation regions, respectively. Because t_s can not be obtained

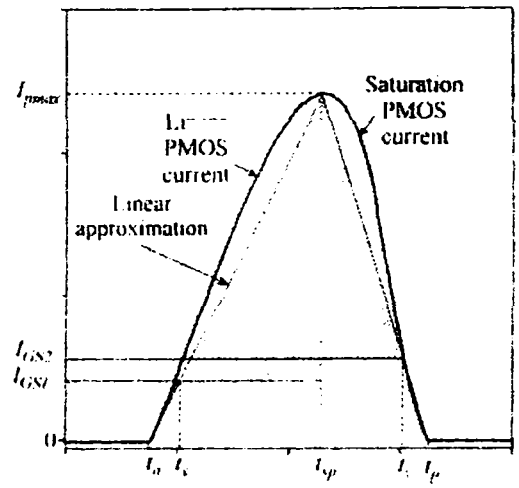

Fig. 9. Linear approximation of the drain-to-source PMOS current. Short-circuit energy is represented by dashed area.

analytically, it is expressed as

$$t_s = t_n + \theta \left(t_p - t_n \right) \tag{16}$$

where θ is a constant. From experiments, a good approximation for θ is 0.65.

At time t_s the PMOS current has a maximum value I_{pmax} that can be obtained evaluating any of the expressions (13) or (14) for $t=t_s$. Based on this approximations, the short-circuit energy is the product of V_{DD} and dashed area shown in Fig. 9 and is

$$E_{SCp} = K_{ap} \frac{V_{DD}}{2} \cdot \left[\left(t_{sp} - t_x \right) \left(I_{pmax} - I_{GS1} \right) + \left(t_y - t_{sp} \right) \left(I_{pmax} - I_{GS2} \right) \right] \tag{17}$$

where K_{ap} is a correction factor used to compensate the underestimation of the area due to linearization. The terms $t_{sp} - t_x$ and $t_y - t_{sp}$ can be evaluated from Fig. 9 geometrically. Thus, (17) becomes

$$E_{SCp} = K_{ap} \frac{V_{DD}}{2} \left(t_p - t_n \right) \cdot \left[\frac{\left(I_{pmax} - I_{GS1} \right)^2}{I_{pmax}} \theta + \frac{\left(I_{pmax} - I_{GS2} \right)^2}{I_{pmax}} (1 - \theta) \right] \tag{18}$$

Finally, the short circuit energy disipated in a cycle of the input signal is

$$E_{SC}/_{cycle} = E_{SCp} + E_{SCn} \tag{19}$$

where E_{SCn} is the short-circuit energy disipated during of the falling input.

Table 1 presents the results of the short-circuit energy dissipated in a cycle of the input signal evaluated by analytical expression (19) compared to SPICE simulations. The results are for three CMOS process technology and different values of the width to matched width ratio (W/W_M). As can be seen from this table, the errors are within 15% and are greater for smaller CMOS technology. The correction factors K_{ap} and K_{an} are determined in matched cases. That why, in matched cases the errors are zero. The results are obtained considering the transmision line parameters $Z_0 = 100\Omega$, $T_D = 400\text{ps}$ and the input transition time $\tau = 0.4\text{ns}$.

Table I. Analytical and SPICE results comparison of short-circuit energy for different lenght of transistors and different values of the width to matched width ratio (W/W_M).

Process L	W/W_M	$\frac{K_{ap}}{K_{an}}$	Analytical [fJ]	SPICE [fJ]	Error [%]
0.18μm	0.4	$\frac{1.194}{1.187}$	20.44	23.61	13.43
	0.6		57.55	61.11	5.83
	0.8		82.94	85.29	2.76
	1		124.01	124.01	0
	1.2		164.01	161.00	1.87
	1.4		205.67	199.12	3.29
0.25μm	0.4	$\frac{1.157}{1.150}$	101.16	112	9.68
	0.6		219.45	229	4.17
	0.8		363.69	373	2.56
	1		552	552	0
	1.2		690.00	681	1.32
	1.4		878.02	854	2.81
0.35μm	0.4	$\frac{1.126}{1.119}$	112.04	120.31	6.87
	0.6		274.90	282.18	2.58
	0.8		477.86	483.47	1.16
	1		702.86	702.86	0
	1.2		949.31	941.59	0.82
	1.4		1225.69	1193	1.73

V. SHORT-CIRCUIT TO DYNAMIC POWER RATIO

The short-circuit power is given by

$$P_{SC} = E_{SC} \Big/ _{cycle} \cdot f = \left(E_{SCp} + E_{SCn}\right) \cdot f \qquad (20)$$

The dynamic power is due to the energy stored in the capacitance of the line after a falling input transition. This energy is passed to ground in the next rising input transition as the line is discharged. Thus, the dynamic power is given by [11]

$$P_D = C_l V_{DD}^2 f = \frac{T_D}{Z_0} V_{DD}^2 f \qquad (21)$$

The short-circuit to dynamic power ratio is obtained dividing (24) by (25):

$$\frac{P_{SC}}{P_D} = \frac{Z_0}{T_D} \frac{E_{SCp} + E_{SCn}}{V_{DD}^2} \qquad (22)$$

From (21) and (18) it can be seen that the short-circuit to dynamic power ratio depends on the ratio between the rise time of the input signal to the transmission line time delay (τ/T_D) and the chanel width of the transistors. The dependence of the short-circuit to dynamic power on the transistors' width is shown in Fig. 10. It can be seen that this ratio is smaller in the underdriven case and it is greather in the overdriven case. Therefore, it is preferable to not overdrive the transmission line.

VI. CONCLUSIONS

The short-circuit power disipated by a short-channel CMOS gate driving a lossless transmission line was investigated. The case of input signal transition time less than twice of the transmission line propagation delay were considered. This is the case when the transmission line effects are significant. Based on the nth power law MOSFET model, a closed-form

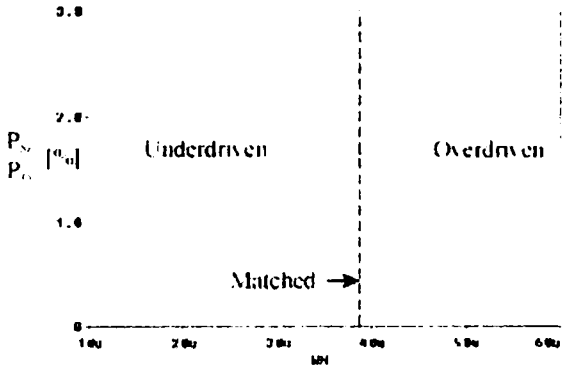

Fig. 9. The dependence of the short-circuit to dynamic power ratio on the CMOS transistor widths.

expression for the output voltage of a CMOS inverter driving a transmission line is derived. A formula for calculating the transistor widths for the matched condition is obtained. Finally, a close-form short-circuit power expression is derived. Also, the short-circuit to dynamic power ratio is investigated. Validations have been performed for different values of device widths, input transition times and parameters of transmission line. The results based on analytical expressions show very good agreement with SPICE simulations.

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