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Double-Simulation New Quadrature Sine Oscillator – the "Electronic Quartz"

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A stract - e aut ors aim particularly, to signa ze out the spectacular performances of this oscillator and to explain the occurring numerous theoretical and practical aspects. The new oscillator is made up of a resonant parallel LC circuit, including both simulated components, obtained with the help of operational amplifiers. Due to a variable resistance of the amplitude limiting device, the resonant circuit establishes itself automatically in an undamped regime, characterized by a quality factor Q = ∞. There are discussed the main equations giving the oscillation condition and frequency, the output voltage phase and amplitudes. This paper shows both the achieved simulations as well as the experiment results.

Key words: sine oscillator, LC simulation, quadrature oscillator, high [illegible]

I. INTRODUCTION

The new type of oscillator, proposed in [1, 2], is based on a resonant parallel circuit, consisting of equivalent inductance and capacity, L_{eq} and C_{eq}, as in Fig.1.

Here, the circuit with A1 represents a NIC whose inverting input simulates, in ideal conditions, a pure inductive impedance, given by

$$z_{i1} = -\frac{1}{j\omega C_1}\frac{R_1}{R_3} = j\omega L_{eq}$$

From this

$$L_{eq} = \frac{R_1}{\omega^2 C_1 R_3} \tag{1}$$

The circuit with A2 represents a NAIC (negative admittance / impedance converter) whose inverting input simulates, whit ideal conditions, a pure capacitive impedance, given by

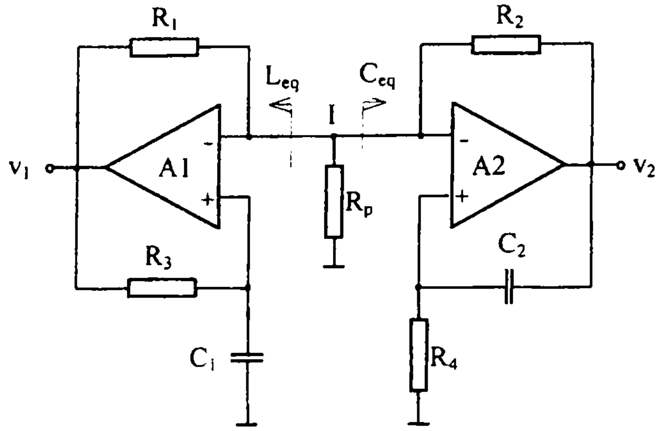

Fig.1. Oscillator departure form

$$z_{i2} = -j\omega C_2 R_2 R_4 = \frac{1}{j\omega C_{eq}}$$

From this

$$C_{eq} = \frac{1}{\omega^2 C_2 R_2 R_4} \tag{2}$$

Heaving in fact two capacitors with losses in the scheme (we note by R_C a parallel loss resistance of a capacitor) they both transfer a negative resistance in the node I (Fig.1). Thus, a certain value (positive) resistor R_p may compensate the negative resistance and may give an undamped resonant circuit (that is, with a $Q = \infty$ factor).

Because of a d.c. positive feedback to A1 amplifier, closed by R_3, the A1 output attains to saturation, so that the produced oscillations in the Fig.1 scheme outputs are not sinusoidal and cannot be used [1]. To achieve a d.c. negative feedback which keeps to zero both output d.c. voltages, considering that the OA inputs have, in ideal case, the same voltage, one reverses between them the non-inverting input connections of the two OAs (Fig.2). Thus the A2 d.c. feedback is negative.

The two voltages are now sinusoidal and, theoretically, without d.c. component. The oscillation frequency is given by the equation [1, 2]:

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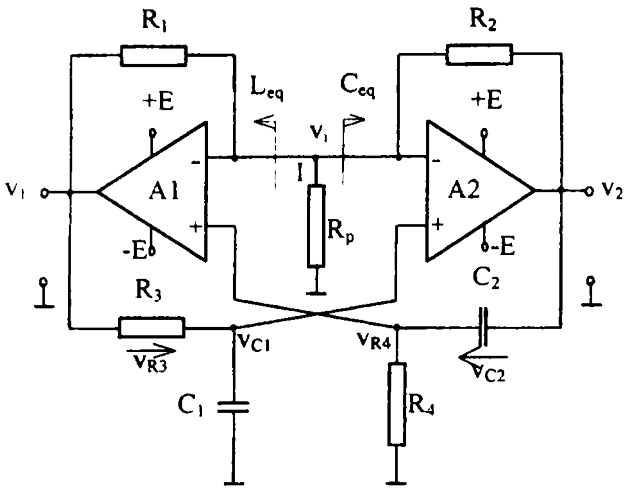

Fig.2 Oscillator principle scheme

$$f_0 = \frac{1}{2\pi\sqrt{L_{eq}C_{eq}}} = \frac{1}{2\pi}\sqrt{\frac{R_1}{R_2R_3R_4C_1C_2}} \qquad (3)$$

an , n t e case o comp ete symmetr ca sc eme (namely, for $R_1 = R_2$, $R_3 = R_4 = R$, $C_1 = C_2 = C$):

$$f_0 = \frac{1}{2\pi\ RC} \qquad (4)$$

If the R_1 and R_2 resistances are made unequal (by a potentiometer) the frequency results in:

$$f_0 = \frac{1}{2\pi\ RC}\sqrt{\frac{R_1}{R_2}} \qquad (5)$$

being in offing the frequency adjusting possibility, provided by R_1/R_2 ratio.

Omitting the R_p resistor in Fig.2 oscillator scheme a resonator circuit may be found including the C_1 capacitor in parallel with a simulated inductance (in the A2 non-inverting input node), discovered by A. Antoniou [5] and proposed as band-pass filter. It is the merit of the author of the paper [1] to point out the fact that this circuit may generate oscillations by itself. In fact, if this filter is supplied from a source with too small internal resistance, the circuit does not oscillate.

II. VOLTAGE PHASE-DIFFERENCE AND AMPLITUDES

In Fig.2 complete symmetrical scheme, the two output voltage amplitudes are limited by the OA supply voltages (that is ±E) in the neighbourhood of E-1 volts. On the R_3 - C_1 divider, considering $v_{C1} = v_i$, we have:

$$v_1 = v_i + v_{R3} = v_i + j\omega C_1R_3v_i = v_i(1 + j\omega C_1R_3)$$

and, with the (3) frequency equation:

$$v_1 = v_i\left(1 + j\sqrt{\frac{C_1R_2R_3}{C_2R_1R_4}}\right) \qquad (6)$$

On the C_2 – R_4 divider, cons er ng $v_{R4} = v_i$, one obtains:

$$v_2 = v_i + v_{C2} = v_i + \frac{v_i}{j\omega C_2R_4} = v_i\left(1 + \frac{1}{j\omega C_2R_4}\right)$$

and, with the (3) frequency equation:

$$v_2 = v_i\left(1 - j\sqrt{\frac{C_1R_1R_3}{C_2R_2R_4}}\right) \qquad 7)$$

Based on these relationships, it may construct the phase diagram of the two output voltages. Thus, in the case of complete symmetrical scheme, the phase diagram has the shape of Fig.3a.

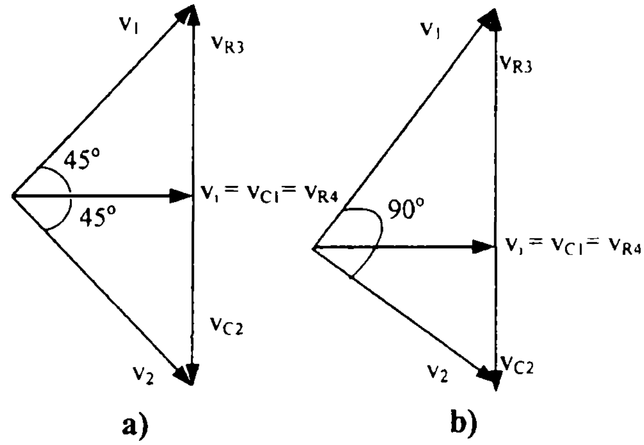

Fig.3. Phase diagrams of the voltages given in Fig.2 in two cases.

It may observe the two output voltages are in quadrature and they have the amplitude:

$$v_{1m} = v_{2m} = \sqrt{2}v_{im} \qquad (8)$$

For an unsymmetrical scheme, v_1 and v_2 voltages may be in quadrature too if (the Pitagora's theorem):

$$v_{1m}^2 + v_{2m}^2 = (v_{R3m} + v_{C2m})^2$$

with

$$v_{1m} = v_{im}\sqrt{1 + \frac{C_1R_2R_3}{C_2R_1R_4}}$$

$$v_{2m} = v_{im}\sqrt{1 + \frac{C_1R_1R_3}{C_2R_2R_4}}$$

$$v_{R3m} = v_{im}\sqrt{\frac{C_1R_2R_3}{C_2R_1R_4}}$$

$$v_{C2m} = v_{im}\sqrt{\frac{C_1R_1R_3}{C_2R_2R_4}}$$

This result in:

$$C_1R_3 = C_2R_4 \qquad (9)$$

Thus, for the partially symmetrical scheme ($C_1 = C_2 = C$, $R_3 = R_4 = R$) the two voltages are in quadrature regardless the R_1/R_2 ratio (Fig.3b) and have the amplitudes [1, 3]:

$$v_{1m} = v_{im}\sqrt{1+\frac{R_2}{R_1}}\ ,\quad v_{2m} = v_{im}\sqrt{1+\frac{R_1}{R_2}} \qquad (10)$$

Consequently, if the frequency is modified by the R_1/R_2 ratio the two amplitudes become unequal but they maintain themselves in quadrature [4].

We use $L^{\bullet}_{eq}$ for the Antoniou cell (with R_p) simulated inductance [5]. The presence of a second resonant circuit, namely $C_1 \| L^{\bullet}_{eq}$ (Fig.6), heaving the same resonance frequency, this time on the A_2 amplifier non-inverting input, may be exploited to achieve an easy amplitude limitation at wanted value (Fig.4).

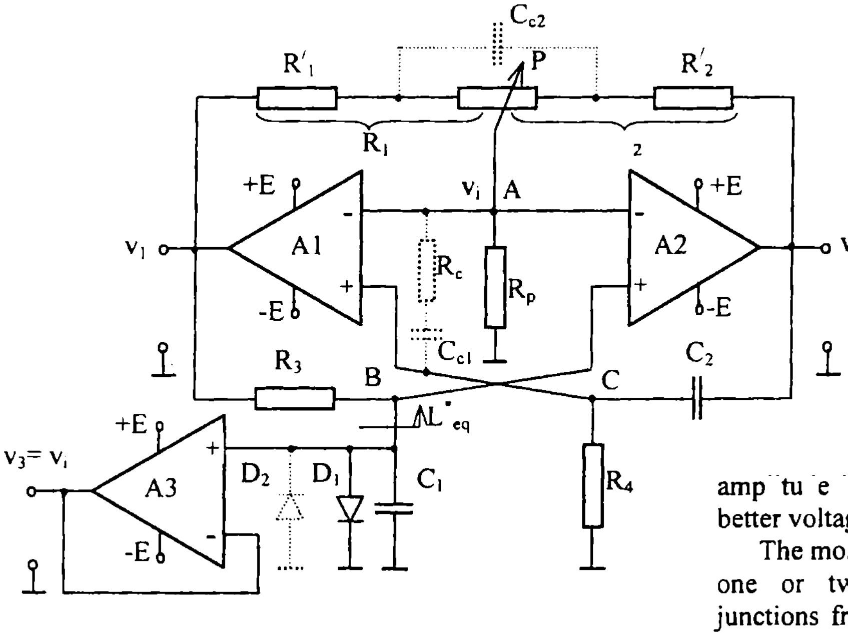

Fig.4. Application oscillator scheme

In fact, the simplest limitation may be obtained by means of one or two diodes (with counter-parallel connection) as shown in Fig.4. The symmetrical amplitude limitation using two devices assures better spectral purity. In accordance with [3] the diode (diodes) gives, in parallel with the resonant circuit C_1, a dynamic equivalent resistance:

$$r_{deq} \approx kQ^{*}r_{dp} \qquad (11)$$

where: - k is a coefficient which depends upon the limiting diode type and number; for a single diode k=2.2 and for two counter-parallel diodes k=0.5 ; for a limiting branch with a Zener and an ordinary diode in series, back to back, k=1 and for two this last type counter-parallel branches k=0.25;

- Q^{*} is the quality factor of the resonant circuit $C_1 \| Leq^{*}$ and it has a great value [3];

- r_{dp} is the dynamic "peak" resistance of a diode, defined as the v-i characteristic slope in the working point at v_i sine voltage amplitude (Fig.5).

One imposes a value of 1kΩ for the r_{dp} resistance if a single diode is being used, 2kΩ for two diodes and 3kΩ in the case of a Zener diode. This value assures a compromise between the output voltage limitation efficiency and spectral purity respectively. Due to the Q^{*} quality factor great value (as we will see it later) r_{deq} is great too, and the limiting diode slightly influences the output voltage THD factor. A 0.01% THD value has been obtained [3, 4]. Consequently, the output voltage form is extremely close to a sinusoidal one.

If we use a limiting branch with Zener and a simple diode in series, the v_{im} voltage amplitude is close to V_z voltage. So, we may obtain the wanted output voltage amplitude. It is also possible to use as a limiting device one or two LEDs , when the v_i voltage

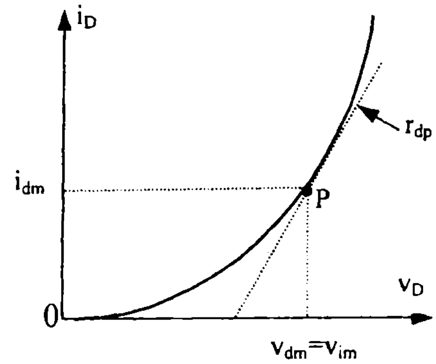

Fig.5. Diode "peak" resistance definition

amplitude is $v_{im}\approx 1.3V$. LED gives the advantage of a better voltage thermal stability

The most successful limiting solution is by using of one or two thermo-stabilized transistor collector junctions from µA726 (Fairchild) i.c. In this case the temperature influence on the output voltage amplitude and frequency is minimized.

A third voltage output, by A3 OA follower, as shown in Fig.4, is provided to deliver a $v_{3m}= v_{im}$ near invariable voltage amplitude at frequency adjustment (when the potentiometer is operated).

Certain OA types used in the oscillator require a lead-lag compensation, to remove a high frequency parasite oscillation. This frequency compensation is necessary only to A1 amplifier and is achieved by the C_{c1} and R_c components (with some tens of pF and a few kΩ respectively). Usually, the JFET input OAs does not claim this operation.

When a wide range frequency adjustment is expected (the P potentiometer value is greater than $R_1' = R_2'$) a second compensation capacitor is to be used. It will have such a value as to assure a shunting way throughout the potentiometer at the high frequency (MHz) parasite oscillation. This appears when the potentiometer is operated toward the extremities. Thus, C_{c2} assures the scheme symmetry at high frequency and the parasite oscillation disappears.

The R_p resistor optimal value will be discussed in the following section.

III. OSCILLATION CONDITION AND QUALITY FACTORS

Fig.4 (without the A3 OA follower and the frequency compensation components) can be redrawn in the form given in Fig.6 [4]. It shows the Antoniou cell which has a pure inductive (L_{eq}*) input impedance [5] (if ignores the capacitor's losses). The introduction of the resistor R_p and r_{deq} allows the oscillation of Antoniou's cell by the compensation of a negative resistance within the A node.

In the following calculus the operational amplifiers are assumed to be ideal. Thus, the sinusoidal voltage v_i, indicated in Fig.6, appears in the three nodes: A, B and C, of the circuit. So, the nodes may be equated in array type as follows [4]:

$$\begin{vmatrix} \frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_p} & -\frac{1}{R_1} & -\frac{1}{R_2} \\ \frac{1}{r_{deq}}+\frac{1}{R_3}+j\omega C_1 & -\frac{1}{R_3} & 0 \\ \frac{1}{R_4}+j\omega C_2 & 0 & -j\omega C_2 \end{vmatrix} \times \begin{vmatrix} v_i \\ v_1 \\ v_2 \end{vmatrix} = \begin{vmatrix} 0 \\ 0 \\ 0 \end{vmatrix} \qquad (12)$$

The oscillation condition is obtained by equalling to zero the coefficient array determinant. This gives the equation:

$$(j\omega)^2\frac{C_1C_2}{R_1}+(j\omega)C_2\left(\frac{1}{r_{deq}R_1}-\frac{1}{R_3R_p}\right)+\frac{1}{R_2R_3R_4}=0 \qquad (13)$$

Thus, the oscillation maintenance condition is:

$$\frac{R_p}{r_{deq}}=\frac{R_1}{R_3} \quad \text{or} \quad R_p=r_{deq}\frac{R_1}{R_3} \qquad (14)$$

and the oscillation frequency results the same as in the (3) formula.

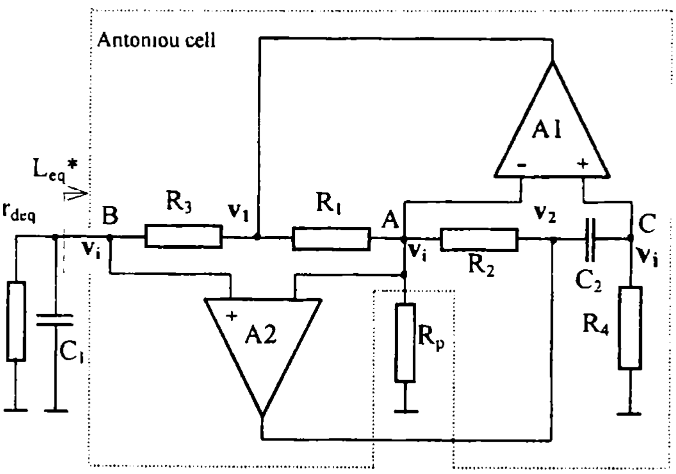

Fig.6 Antoniou cell in the proposed oscillator

In [4] the quality factor of the parallel resonant circuit $L_{eq}\|C_{eq}$ in node A (for complete symmetrical scheme) was deduced as:

$$Q^{-1}=R\left(\frac{1}{R_p}-\frac{1}{r_{deq}}\right) \qquad (15)$$

For the case when $R_1=R_2$, $R_3=R_4$, $C_1=C_2$ and considers the loss resistance of the capacitors, R_C,(in parallel with C and equal for all capacitors for simplicity) and the input resistance of the OAs (equal for all the OAs for simplicity), R_i , one may be demonstrate that:

$$Q^{-1}\cong\left(\frac{R_1}{R_p\|0.5R_i}-\frac{R_3}{r_{deq}\|0.5R_C}\right) \qquad (16)$$

It may be seen that Q is not dependent upon frequency. This fact allows reduce the oscillation frequency toward one Hz, maintaining the high quality factor!

The quality factor of the (16) formula can attain an ideal value $Q=\infty$ if :

$$\frac{R_1}{R_p\|0.5R_i}-\frac{R_3}{r_{deq}\|0.5R_C}\Rightarrow 0 \qquad (17)$$

or :

$$R_p\cong\frac{0.5R_i(R_1\ R_3)(r_{deq}\|0.5R_C)}{0.5R_i-(R_1\ R_3)(r_{deq}\|0.5R_C)} \qquad (18)$$

that must be positive. By using a very high input resistance OAs (with JFETs or MOSFETs in inputs) the formula is simplified as follows:

$$R_p\cong(R_1/R_3)(r_{deq}\|0.5R_C) \qquad (19)$$

Apparently this condition seems hard to carry out because of its lack of precision and the instability of some implicated resistances. But the [4] paper, which analyzed the oscillation maintenance condition (for $R_i=\infty$), has demonstrated that the equation of same form with (15) [illegible] oscillation condition. This being carried out if the oscillator is working, we may draw an important conclusion: the $L_{eq}\|C_{eq}$ resonant circuit operates with $Q=\infty$. For a given R_p precisionless value this situation is automatically carried out and maintained due to the fact that the r_{deq} resistance adapts its value (that is, v_i, v_1, v_2 voltages are modified little) to comply with the (14) or (17) condition. Consequently, the R_p value is by no means critical. On the contrary, it may be modified within a still large range. It should be noted that the (17) condition may be carried out (with an appropriate R_1/R_3 ratio) even in the case when OAs have a smaller input resistance (that is, for usual OAs) and when the capacitors have greater losses (smaller R_C). But, the frequency stability is higher when greater R_C is used.

It may be demonstrated that the Q* quality factor formula, encountered in the (11) equation, is similar to the Q one when r_{deq} is eliminated, that is:

$$Q^{*-1} = \frac{R_1}{R_p \| 0.5R_i} - \frac{R_3}{0.5R_C} \quad (20)$$

This means the Q* factor has a finite value which is still very high (of the order of hundreds even more) if R_1 and R_3 are small enough, because r_{deq} has a great value, comparable with $0.5R_C$.

IV. SIMULATIONS

The authors have performed simulations over complete symmetrical oscillators, by using Apollo workstations and the Accusim II software [3], [4]. An intermediate value of Q of 13000 has been obtained but the test is endless. In fact, this result confirmed the theoretical conclusion according to which the resonant circuit has, in ideal conditions, a quality factor $Q = \infty$.

Other band-pass filter simulations, with the R_p value a little modified in comparison with the calculated by (19) equation value, have been performed [4]. In this case, a finite value resulted for Q. It is not possible to establish by simulation or experiment the frequency characteristic for an amplitude limitation oscillator as its output voltage amplitude cannot vary.

Concrete oscillator schemes with real OAs and diodes (as that in Fig.4) have been simulated [3]. The phase differences as shown in the diagram given in Fig.3 have been verified. A very important test has been performed by modifying the R_p resistance value. One could observe the self-adapting mechanism of the r_{deq} value (to respect the 17 oscillation condition) revealed itself by a corresponding amplitude modification of v_i voltage (diode peak voltage).

V. REALISATIONS

The first experiments and measurements have been performed on complete symmetrical schemes of the form as given in Fig.4 [1, 3, 6], heaving a simple diode or thermo-stabilized junction (from μA726 integrated circuit) amplitude limiter. Small values of 1...15 kΩ (including the potentiometer) have been used for $R_1 \ldots R_4$.

The experimental results confirmed the conclusions of the theoretical study. Thus, it has been confirmed that modifying the R_p resistance value within a large range, the oscillation condition ($Q = \infty$) is maintained due to the self-adaptation. This mechanism revealed itself by the conservation of the same small THD (of the order of 0.01%) and by the expected little amplitude variation of v_i voltage on limiter device.

The best results have been obtained by using JFET input OAs, metallic film resistances, polystyrene capacitors and thermo-stabilized transistor junctions from μA726 i.c. Thus, the R and C components had contrary sign temperature coefficients which reciprocally compensated to a great extent. The frequency instability with temperature variation was:

$$\Delta f / f_0 \Delta T \approx 2 \cdot 10^{-6} /°C$$

which brings the exposed circuit near to usual quartz oscillators. This explains the name of "electronic quartz" given to the new oscillator by its inventor.

A small instability of the output voltage amplitudes has been obtained:

$$\Delta v_i / v_i \Delta T \approx 2 \cdot 10^{-4} /°C$$

Another oscillator scheme has been carried out with JFET amplitude limiter one [4]. This scheme is more complicated, needs a resistance adjustment and is recommended only for a fixed frequency. The experimentation of this scheme confirmed the very good frequency, amplitude and phase difference stabilities as well as the excellent spectral purity of outputs voltages. The third output voltage harmonic component attained to a level with 80dB smaller in comparison with the fundamental one.

A new quadrature oscillator interesting application was the realization, with the help of two additional OAs, of a three phase oscillator with special performances [6].

VI. CONCLUSIONS

The proposed new sine oscillator has surely the highest performance among all known quartzless oscillators. If carried out carefully, the attained frequency stability is close to that of the usual quartz oscillators.

The new oscillator distinguishes itself both by the output voltage amplitude stability as well as a very small THD. Being the best quadrature oscillator, it allows to easily carry-out a best three-phase one.

Future research work will provide with regard to the complete oscillator integration and to its perfection in view the equalization, even the overtaking, of the quartz oscillator performances.

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