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An Improved Design Method for the Rectifier with a Filter Capacitor

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Abstract – A simple and rather precise design method for a transformer-coupled input rectifier with a filter capacitor is proposed in this paper. It is based on the determination of the conduction angle of the rectifier diodes, by taking in account the transformer equivalent resistance and the rectifier diode voltage drops. This design method is based on a logarithmic equation and can replace the classical design procedure that is based on coefficients taken from nonlinear graphical diagrams.
Keywords: rectifier, filter capacitor, design method

I. INTRODUCTION

The classical electronic c reu ts power supp y cons sts on a transformer supplied from the ac line voltage, a full-wave bridge rectifier with a capacitor filter and a voltage regulator (usually an integrated circuit). The rectifier design consists of choosing the circuit elements for a given output voltage and current.
The diodes are chosen based on the maximum value of the medium current in the load and maximum voltage at the transformer output [1]. The ripple at the rectifier output depends mainly on the capacitor value and the load current. The smoothing capacitor value can be computed based on the diode conduction angle, by utilizing few coefficients that can be found from tables or nonlinear diagram [1].

II. THEORETICAL ANALYSIS

The classical diode-bridge rectifier with transformer and capacitor filter is presented in Fig.1. The load of the circuit, R is considered to be resistive.
Firstly, the circuit components will be considered to be ideal (with C finite) and then an infinite capacitor and ideal diodes in the bridge will be considered (with a non-zero transformer resistance) [2].

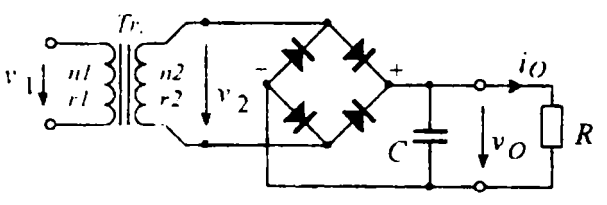

Fig 1. The diode-bridge rectifier with capacitor filter

For a sine input (ideal ac line voltage), the transformer output (and the rectifier input voltage) are:

$$v_2 = v_i = V_p \sin \omega t \,. \tag{1}$$

A. *Ideal rectifier with finite C*

The waveforms for a time constant much greater than the period at the output, $RC=5(T/2)$ in this case, are presented in Fig.2.

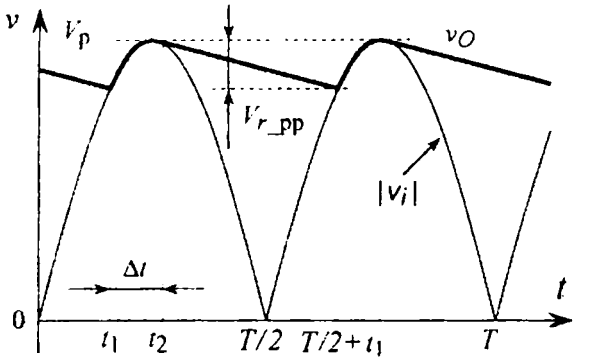

Fig 2. Rectifier waveforms for finite C (ideal Tr. and diodes)

For $RC \gg T/2$ the minimum output voltage is:

$$v_{O\min} \cong V_p \exp\left(-\frac{T}{2RC}\right). \tag{2}$$

The ripple voltage (peak-to-peak and rms values) and the average output voltage are determined by the circuit time constant RC, [2] and [3]:

$$V_{r\_pp} \cong V_p \frac{T}{2RC}. \tag{3}$$

$$V_r \cong \frac{V_{r\_pp}}{2\sqrt{3}} \cong V_p \frac{T}{4\sqrt{3}RC}. \tag{4}$$

$$V_O = V_p - \frac{V_{r\_pp}}{2} = V_p\left(1 - \frac{T}{2RC}\right). \tag{5}$$

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The ripple factor is:

$$r \cong \frac{V_r}{V_O} \cong \frac{T}{\sqrt{3}(4RC - T)} \left(\cong \frac{T}{4\sqrt{3}RC} \right). \quad (6)$$

The average output voltage and the ripple factor are important when the power supply doesn't have a voltage regulator. When a voltage regulator exists, the minimal capacitor voltage is important, because a liniar regulator can reduce its input voltage, only. These results can be used for very low internal resistance of the transformer (much lower than R), but this is not the case for most of the practical circuits.

B. *Ideal rectifier with finite R_i*

In the second analysis, an infinite capacitor and ideal diodes will be considered. The waveforms for these assumptions are presented in Fig.3.

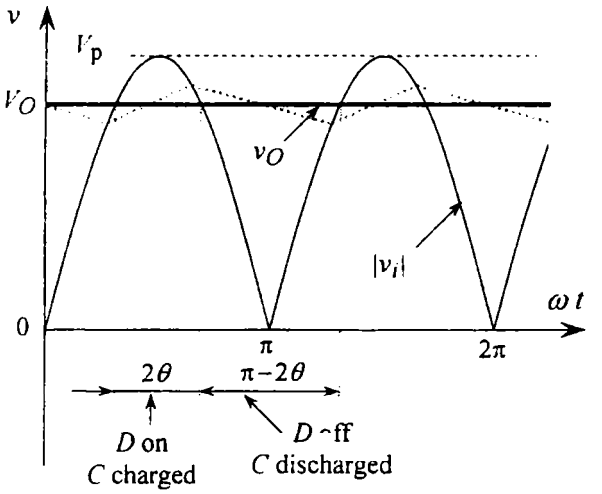

Fig.3. Rectifier waveforms for infinite C and finite R_i

The output waveform is a pure dc voltage, the ripple being zero (4), because of the infinite capacitor. With 2θ being the conduction angle (as in Fig.3.), the output voltage and current can be computed:

$$V_O = V_p \cos\theta, \quad I_O = \frac{V_p \cos\theta}{R}. \quad (7)$$

Fig.4 presents the equivalent circuit during the C charging time, R_i being the transformer equivalent resistance from the secondary point of view:

$$R_i \cong R_{tr} = r_2 + r_1 \left(\frac{n_2}{n_1} \right)^2, \quad (8)$$

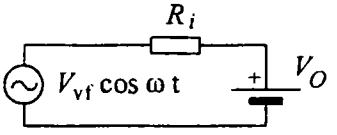

Fig.4. The equivalent schematic while C is charging

The charge conservation law can be used to find the conduction angle. The average current received by the equivalent voltage source V_O during one period (of the output signal) should be equal with the average current supplied by the equivalent voltage source during the same period:

$$Q_{ch} = I_{ch} T = Q_{dsc} = I_{dsc} T. \quad (9)$$

The average current that charges the capacitor can be calculated by integration (in the schematics in Fig.3):

$$I_{ch} = \frac{2}{\pi} \int_0^{\theta} \frac{V_p \cos\omega t - V_p \cos\theta}{R_i} d\omega t. \quad (10)$$

By replacing (10) and (7) in (9):

$$\frac{V_p}{\pi R_i} (\sin\theta - \theta\cos\theta) = \frac{p \cdots \theta}{R}, \quad (11)$$

the ratio between the internal resistance R_i and the load resistance R is expressed as a function of the conduction angle, $k_i(\theta)$:

$$\frac{R_i}{R} = \frac{tg\theta - \theta}{\pi} = k_i. \quad (12)$$

In order to compute the average output voltage (7), k g (s of k_i, for example). The function $\theta(k_i)$ can be found utilizing approximate analysis. The function (12) pp r appr xi...a.ely l.near w..en a l ga.it.mic scale for k_i is used and a linear approximation of it can be outlined for the usual domain of k_i, as in Fig.5 The approximate function expressed as:

$$\theta = a \lg k_i + b, \quad (13)$$

can be found considering two points of the line (the intercepts with k_i axes: θ=0, k_i=0.0031 and k_i=1, θ=69°). The constants expressed in degrees are:

$$b = 69°, \quad a = -\frac{69}{\lg 0.0031} = 27.5°. \quad (14)$$

and the function we are looking for (in degrees or in radians) is:

$$\theta \cong 27.5 \lg k_i + 69 \ [°], \quad (15)$$

$$\theta \cong 0.48 \lg k_i + 1.2 \ [\text{rad}]. \quad (16)$$

In Fig.5 the error (between the initial function and its approximation, expressed in %) is represented also. The approximate function can be used for k_i=0.05...1 with an error less than 1.5%.

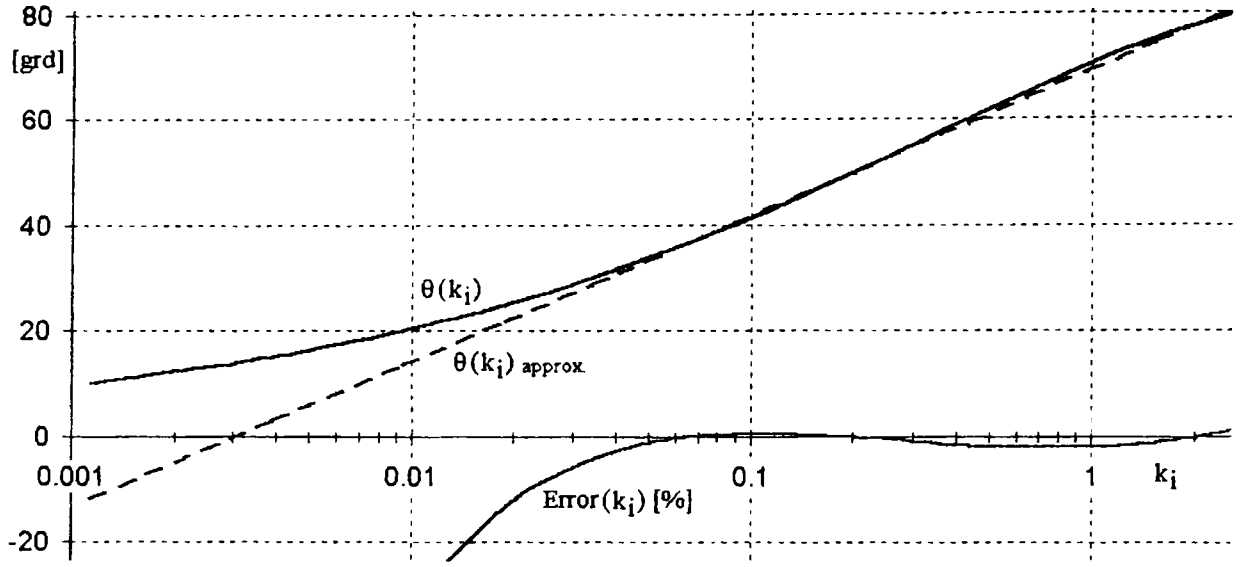

Fig.5. The graph of $\theta(k_i)$, its approximation (the dashed line) and the error between the two curves (in %).

The effect of the diodes voltage drop can be taken in account by subtracting a constant voltage from the input peak voltage (V_D=0.7...0.9V, for every diode connected in the current path). For the diode bridge rectifier the peak voltage should be replaced in all the previous equations with its reduced value:

$$V_p \leftarrow V_p - 2V_D. \qquad (17)$$

The analysis of the circuit with a finite capacitor and a non-zero transformer resistance leads to equations that can not be solved by hand. An analysis based on nonlinear graphs can be conducted [1], or a computer simulation of the circuit can be made.

C. *The ripple limits*

Another possible method is to determine the ripple limits (the minimum and maximum values for a given situation). The ripple voltage and factor computed for an ideal rectifier (with R_i=0) and a finite capacitor, equations (3)...(6), represents the maximum ripple.
Two reasons for that can be stressed: the capacitor discharging time is the maximum possible (10ms) and for a non-zero R_i, the R_i-C group introduces a supplementary filtering effect that reduces the ripple.
To compute the minimum ripple value, the conduction angle determined for the actual R_i and for an infinite capacitor can be considered.
The fact that this is the minimum ripple results from the graph in Fig.3 and will be experimentally verified. In Fig.3, where the waveform for a finite capacitor is sketched (with a gray dotted line), one can see that the time when the diode is off is the shortest one for an infinite capacitor (the black horizontal line is shorter than the gray one). The infinite capacitor case will gave the minimum capacitor discharging time and the minimum ripple. The ripple voltage and factor is proportional with time and can be computed (for θ expressed in radians) with:

$$V_{r\_min} \cong V_p \frac{T}{4\sqrt{3}RC}\left(\frac{\pi-\theta}{\pi}\right). \qquad (18)$$

$$r_{min} \cong \frac{T(\pi-\theta)}{4\pi\sqrt{3}RC} \cong r_{max}\left(\frac{\pi-\theta}{\pi}\right). \qquad (19)$$

III. THE RECTIFIER DESIGN

A. *The smoothing capacitor estimation*

Given the ripple factor r (the ac to dc output voltage ratio, in %) and the minimum load resistance R_{min} (in Ω), for a full wave rectifier, the minimum capacitor C_{min} (in F) can be computed from (6):

$$C_{min} = \frac{0.29}{r \cdot R_{min}}. \qquad (20)$$

The maximum limit of the ripple factor is considered and the result will cover all the possible cases (the capacitor will be overestimated).

B. *The transformer secondary voltage*

If the transformer is not given, its parameters should be estimated. For a normally loaded transformer it can be considered the ratio k_i=0.1...0.3. Replacing (15) in (7), for k_i=0.2 and V_D=0.8V, a first approximation of the rms transformer voltage in the secondary (in V) will be:

$$V_{2rms} \cong 1.1(V_O + 1). \qquad (21)$$

A transformer with a secondary voltage greater than (or at least equal with) the value in (21) should be chosen. If the transformer will be over-dimensioned a lower secondary voltage can be chosen.

For the actual transformer, the primary and secondary winding resistance can be taken from the transformer data-sheet or can be measured with an ohmmeter and the transformer equivalent resistance can be computed with (8). This result is enough precise for normal frequency and load, when the magnetizing and leakage transformer inductance can be neglected.
The actual k_i ratio, the diode conduction angle and the average output voltage of the rectifier can be computed with (12), (15) and (7) respectively. R in (12) will be the minimum load resistance computed by Ohm's law with the average output voltage and the maximum value of the average output current.
The transformer current (and power) and the diode-bridge (or diodes) are chosen in the classical manner, considering the average output current (and the peak voltage at the transformer secondary).

IV. VALIDATION OF THE THEORY

Some experiments in the laboratory were made to prove the formulas derived in the theoretical analysis section of this article.
A full-wave bridge (1PM1) rectifier with a (220/12V, 0,2A) transformer, two different capacitors (220μF and 1000μF) and a variable load (50...160Ω) were considered. The equivalent transformer resistance and the peak voltage in the secondary are:

$$R_i \cong R_{tr} = 10 + 1810\,(12.9/230) = 15.7\Omega.$$

$$V_p = \sqrt{2}\cdot 12.9 = 18.2\,V$$

The measurements, the theoretic calculations and the errors between these results are presented in table 1.

Table 1

	I_O (mA)		80	100	180
C = 220μF	V_O (Vdc)		12.8	11.9	9.5
	V_o (V ac)		0.69	0.83	1.22
	r_1		0.054	0.069	0.128
C = 1000μF	V_O (Vdc)		12.8	12	9.6
	V_o (V ac)		0.15	0.18	0.27
	r_2		0.018	0.015	0.028
Theory	R (Ω)		160	120	53.3
	k_i		0.098	0.131	0.295
	θ (°)		41.3	44.7	54.4
	V_O (Vdc)		12.5	11.8	9.66
	r_1	max	0.082	0.109	0.245
		min	0.045	0.055	0.098
	r_2	max	0.018	0.024	0.054
		min	0.001	0.012	0.022
Errors	V_O (%)		-2.3	-1.6	+0.6
	r_1 (%)	max	+52	+58	+91
		min	-17	-20	-23
	r_2 (%)	max	+50	+60	+93
		min	-18	-20	-21

The theoretical results are computed as follows:
- R with Ohm's law at the rectifier output,
- k_i from equation (12),
- θ (in °) from equation (15),
- V_O (V) from equation (7) and
- The ripple factor: - case "max", from (6) and
  - case "min" from (19).

For the ripple factor, the differences between theory and experiment are great; for the "max" case the theoretical r-s are greater than the experimental ones with 50 to 93%. The minimum r-s are lower than the experimental ones (with 17 to 23%), and closer to the experiment than the maximum approximations.
If one is interested in finding a precise ripple factor, he is recommended to use equation (19), but he must be aware that the result is somehow lower than in the practical circuit. Another observation is concerning the tolerance of the filter capacitor that is rather high, usually -10...+50% (in some cases ±20%). The high dispersion of the capacitor value does not justify very precise formulas when this capacitor is involved, such that typical results can be found with equation (19); the typical positive capacitor tolerance compensates the typical negative error given by formula (19).
On the other hand, the ripple factor can be computed by equation (6), the formula is much simpler, the result is covering all the cases, but the result is much greater than in the practical circuits. Equation (6) is appropriate for the worst case analysis.
A special remark should be made about the precision of computing the average output voltage. The error is lower than few percents and more important, it doesn't depend significantly on the capacitor value (for example, the minimum time constant, for C=220μF and R=53Ω, is almost equal with the period of the signal at the rectifier output, that is 10ms).

V. FINAL REMARKS

In this paper, the transformer-input, capacitor-filter, diode-bridge rectifier was analyzed and some original formulae were presented and justified.
These formulae can be used to compute the diode conduction angle, the ripple factor and the average voltage at the rectifier output.
A simple and enough precise procedure and formulas for choosing the capacitor and the secondary transformer voltage were presented.
The proposed formulas were theoretically justified and experimentally verified. The differences between theory and experiment were stressed and practical recommendations were made in the previous section.
Some supplementary simulations, not presented in this paper, validate the results also.

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Simulation based testing of complex electronic systems

Dan Simu[1]

Abstract – Complex electronic systems[3,21] are built of different electronic devices interacting between them. The devices are interacting using one or several common buses. The testing of each device is done as a functional testing but it doesn't prove the functioning of the hole system. Testing complex systems while simulating the environment with additional hardware could prove to be impossible. Simulating each device, assembling the system, generating the test program for the entire system and running the test while injecting errors and failures to some of the devices could be very useful for the assessment of the system reliability in time. This paper analyses the technical and the cost opportunities for the design of such a testing system.
Keywords: editing, Symposium, author

I. COMPLEX ELECTRONIC SYSTEMS

In our days the electronic devices could be found everywhere. The industry is building more and more complex systems. There are two sectors where complex systems are used on large scale: the aircraft industry and the automotive industry. Every year new devices are added to the previous architecture. An electronic complex system could be defined as a collection of electronic devices connected through one ore more buses performing together the tasks associated with the system. The system could have an hierarchical structure or could be only a collection of standalone devices performing different tasks at different moments. In the aircraft industry there are several subsystems (organized usually hierarchically) exchanging information on two or more buses (usually ARINC 429 or ARINC 629). In the automotive industry there are tens of devices using a CAN bus as a support for information exchange. Every device has its own functionality driven by an intelligent hardware running its own software. The usual testing procedure is to take each device and to verify it on a test bench. This type of verification is based on the ability of the test engineer to design the set of tests for a good coverage of the failures field of the specific unit. While the complexity of the systems is growing, the possibility of unforeseen situations becomes reality more often. For complex systems for economical reasons there are used Automatic Test Equipments with different Test Unit Adapters (interfaces between the standard equipment and the Unit Under Test) and different Test Program Software.

II. ATE BASED FUNCTIONAL TESTING[22,23,24,25]

The ATE based functional testing means that every stand alone device has a Test Requirement Definition designed by the manufacturer and based on this document, a suite of tests could be performed connecting the test equipment at the connector of the UUT. The device is seen as a black box and there is no access to the components inside. Usually the ATE is a collection of general purpose measurement and stimulus devices controlled by a computer. The computer is running the tests controlling all the measurement devices via a GPIB type bus or other common connections (serial, USB, parallel) . The functional testing represents a suite of tests organized to verify the complete functionality of the device. The testing design is based on the hardware architecture of the device. It verifies every block of the unit orderly, starting with the power block and continuing with the other blocs one by one. While this covers the entire hardware of the unit it assumes a reasonable functionality for the environment of the device. It means that the testing is more targeted to the hardware failures. Unfortunately for complex systems the verification of the software inside a device cannot be completely tested at the design stage. When the number of interacting devices is growing the number of possible situations is growing either. Using an ATE equipment to test several interconnected devices is almost impossible because of increasing costs.

III. COMPONENT MODELING AND SYSTEM SIMULATION[14]

Functional tests, because of their precise description are suitable for simulation. The UUT could be descript by a functional model. There is an open issue regarding the detail of modeling when simulating a device. The better and detailed model of the device means the more accurate and close to reality simulation. But a very detailed description could cost a lot of development time and also could

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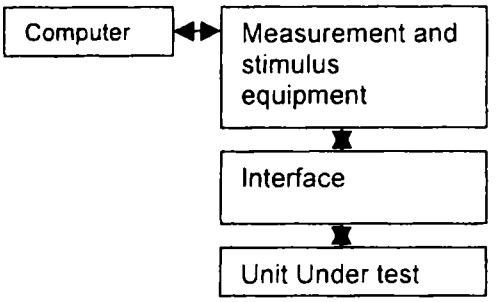
cost running time during testing. A functional description of the device based on the original testing requirements at least as the first testing iteration is convenient. The device could be descript using VHDL as a language. The new model will be easily tested based on the original functional test. Based on this modeling approach the entire system may be built as a library of models. The design of the VHDL models will have some supplementary features to enable the implementation of some new testing strategies and more important the error injection[13]. The model library is not enough to run the simulation. We have to add the model of the bus or busses used for information interaction and the model of the measurement and stimulus devices (the ATE models). The last component of the simulator will be the application running all the models. The application will have some important features. The models represents processes which are running simultaneously. The application like any VHDL simulator has to run all the models simultaneously based on a time sampling. None of the commercial software was built to run the VHDL models and to exchange data with other applications. But the ability to run test programs, to inject errors and create test reports is based on the possibility to exchange global data at specific moments with the simulator. The simulation environment will have an application running the models, an application running the test program and an application performing the error injection. All those applications will be able to exchange data and will be synchronized. A complete simulation will be very useful at the design stage of the system.

IV. OBJECTIVES OF THE SYSTEM LEVEL SIMULATION[5,2,3,7]

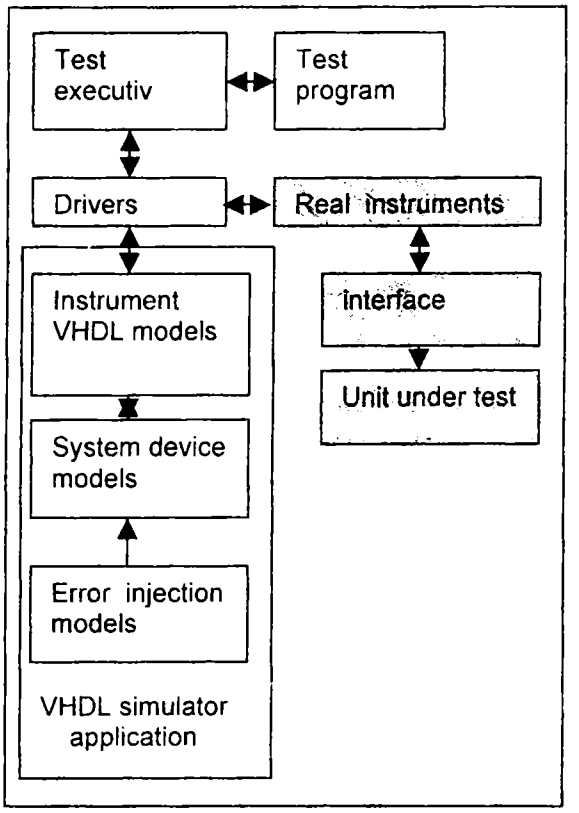
This paper presents the opportunity of the system simulation in connection with the system testing strategy. During the design stage, the possibility to simulate the system will improve the test requirement design of each component. It also will improve the verification of the software of each device and the implementation of a fault tolerant software. It also will allow the implementation for the hierarchical systems of a BIST (Built In Self Test) procedure[7] at the system level. During the service of the unit the testing is usually performed for maintenance reasons. In this situations the testing equipment is necessary to verify and diagnose if the unit is serviceable. For the complex systems the test design is never perfect. During service new scenarios are possible. While a standalone device could be available, the entire system is more difficult to have. In this cases a hybrid system partially simulated and partially hard implemented will prove very useful. For this reason the test program running application will be capable to control virtual instruments (real or simulated).

V. ENVIRONMENT ARCHITECTURE

The architecture of a testing environment for complex systems could have the following simple hardware structure:



and the following software structure:



VI. CONCLUSIONS

The simulation of the complex electronic systems together with the testing environment is improving the quality of test programs from the design stage. It also allows to implement fault tolerant systems and to better define the dependability of the system. The main inconvenient is the cost of model development. But avionic complex systems and automotive systems are using more standard units enabling general use library development. Also modeling at functional level will limit the complexity.

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