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Synthesis of controlled nonlinear simulated circuit elements based on a GIC-structure

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Abstract – In this communications the possibilities offered by the Antoniou's GIC structure to synthesize electrically controlled nonlinear (generalized) circuit elements are analyzed.

I. INTRODUCTION

Electrically controlled elements have found applications in many areas of electric and electronic engineering. Currently used techniques are based on semiconductor devices like diodes or transistors, analog multipliers, thermal, optical, electric or magnetic controlled devices etc. A method based on the use of multipliers has been reported in [1]. The controlled element was the so-called x-controlled scalor and had the property of electrically scaling any linear or nonlinear circuit element. Basically, the xcontrolled scalor is a 3-port for which, the characteristic "seen" at port 1 is a scaled version (on current or voltage) of the characteristic of the element connected at the output port, depending on the controlled signal applied at the third port.

The power scalor is a linear 2-port described by the transmission matrix

$$T_{\mu} = \begin{bmatrix} K, & 0\\ 0 & K_{\mu} \end{bmatrix}$$
(1)

and transforms a nonlinear resistive element u=f(i)connected at the output into a nonlinear resistive element of the form

$$u = K_u f(i/K_i)$$
⁽²⁾

An interesting class of controlled two-ports is that of mutators and generalized mutators [2-4]. They are two-ports having the property that the nonlinear

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element "seen" at port one has a similar characteristic compared to that of the element connected at the output port but of another type. As an example, a CR mutator transforms the nonlinear resistor described by an i(u) characteristic connected at the output port into a nonlinear capacitor described by a similar characteristic q(u) for an impedance converter and u(q) for an impedance inverter. More general, a mutator described by transmission matrices of the type

$$T_{\kappa} = \begin{bmatrix} as^{\omega} & 0\\ 0 & ds^{\sigma} \end{bmatrix}; \quad T_{\mu} = \begin{bmatrix} 0 & bs^{\omega}\\ cs^{\sigma} & 0 \end{bmatrix}$$
(3)

(s stands for derivative and s^{-1} for integration) for impedance converters and inverters respectively, transforms a nonlinear element described by one of the relations

$$s^{k}u = f(s^{k}i); \ s^{k}i = f(s^{k}u)$$
 (4)

into a nonlinear element described respectively by

$$s^{k-m}u/a = f(s^{k'-n}i/d); \ s^{k'-m}i/d = f(s^{k-m}u/a)$$

$$s^{k-m}i/c = f(s^{k'-m}u/b); \ s^{k'-m}u/b = f(s^{k-m}i/c)$$
(5)

The implementation of such elements is possible using OA's or other active elements.

II. THE GIC-TYPE CONTROLLED STRUCTURE

It has been previously shown [4] that Antoniou's GIC structure that has input impedance

 $Z_{in} = (Z_1Z_3Z_5)/(Z_2Z_4)$ (Fig. 1) represents a flexible way to simulate a large class of nonlinear (generalized) circuit elements and a similar structure has been used to synthesize tunable filters [5].

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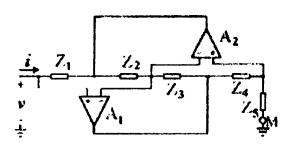


Fig. 1. Antoniou's GIC structure.

Using the above structure, it has been shown in [4] t at t e following scalor-type result can be of taine (Table 1)

On the other hand, most op-amp JFET structures for the realization of positive or negative voltagecontrolled impedances that have been reported use the technique of Nay and Budak. The equation describing the JFET drain current ID in the nonsaturated region is

Tab	e l			
Nr.	Output	Transmission matrix		Type of two - port
	port"	Nonlinear case	Linear case	
1	1	$\begin{bmatrix} (u_5 \circ i_4 \circ u_3 \circ i_2)(\bullet) & 0 \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} R_5 G_4 R_3 G_2 & 0 \\ 0 & 1 \end{bmatrix}$	voltage scalor
2	2	$\begin{bmatrix} 0 & (u_5 \circ i_4 \circ u_3)(\bullet) \\ i_1(\bullet) & 0 \end{bmatrix}$	$\begin{bmatrix} 0 & R_5 G_4 R_3 \\ G_1 & 0 \end{bmatrix}$	power scalor cascaded with ideal gyrator
3	3	$\begin{bmatrix} (u_5 \circ i_4)(\bullet) & 0\\ 0 & (i_1 \circ u_2)(\bullet) \end{bmatrix}$	$\begin{bmatrix} R_{5}G_{4} & 0\\ 0 & G_{1}R_{2} \end{bmatrix}$	power scalor
4	4	$\begin{bmatrix} 0 & u_5(\cdot) \\ (i_1 \circ u_2 \circ i_3)(\cdot) & 0 \end{bmatrix}$	$\begin{bmatrix} 0 & R_3 \\ G_1 R_2 G_3 & 0 \end{bmatrix}$	power scalor cascaded with ideal gyrator
5	5	$\begin{bmatrix} 1 & 0 \\ 0 & (i_1 \circ u_2 \circ i_3 \circ u_4)(\bullet) \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 0 & G_1 R_2 G_3 R_4 \end{bmatrix}$	current scalor

^{•)}input port = port 6

$$I_{\rm D} = \frac{I_{\rm DSS}}{V_{\rm P}^2} \Big[2V_{\rm DS} \left(V_{\rm GS} - V_{\rm P} \right) - V_{\rm DS}^2 \Big]$$
(6)

where I_{DSS} is the extended during the V_P is the threshold voltage. If the JFET gate-to-source voltage V_{GS} satisfies

$$V_{\rm gs} = \frac{V_{\rm DS} + V_{\rm C}}{2} \tag{7}$$

where V_{DS} is the drain-to-source voltage and V_C is a control voltage, then the drain current I_D will be linear in V_{DS} and

$$I_{\rm p} = \frac{I_{\rm DSS}}{V_{\rm p}^2} (V_{\rm C} - 2V_{\rm P}) V_{\rm DS}$$
 (8)

As the above equation is valid only for small values of V_{DS} , the extension of the linear range can be achieved by reducing the drain-to-source voltage of the JFET to a fraction a<<1 of the input voltage V to keep the JFET in the nonsaturated region, i.e., $V_{DS} = aV$.

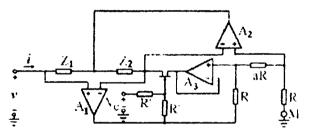


Fig. 2. The configuration proposed in [5]

Basically, the control of the input impedance value Z_{in} can be obtained by replacing any of the impedances Z_i , i = 1-5, with a JFET operating in the nonsaturated region. To fulfill the conditions for linear operation and wide dynamic range, a supplementary op-amp was embedded into the GIC structure, the impedances Z_4 and Z_5 were replaced by two resistances $R_4 = aR$ and $R_5 = R$, and the impedance Z_3 was replaced by the JFET drain to source as shown in Fig. 2. Straightforward analysis gives the following expression for the input impedance:

$$Z_{in} = \frac{Z_i R_{JFET}}{a Z_2}$$
(9)

where

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$$R_{IFET} = \frac{V_p^2}{I_{DSS}(V_C - 2V_p)}$$
(10)

is the drain-to-source resistance of the JFET.

The drain-to-source voltage is independent of Z_1 , Z_2 , and of the transistor parameters.

The main idea of this paper is to combine the results related to scalor-type configurations based on the GIC structure with the controlled architecture shown in Fig. 2. Thus, we allow in the above configuration nonlinear elements as well. The results presented in Table 1 can be easily particularized by considering that port 3 has the resistance R_{JFET}/a where R_{JFET} is controlled according to equation (10).

III. SIMULATION RESULTS

The above theoretical considerations have been verified by simulation as shown below. The characteristics shown in Fig. 3 have been obtained using resistances of 1K on all branches except the controlling one.

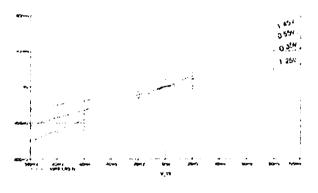


Fig. 3. Voltage controlled resistance.

The results of Fig. 4 represent scaled versions of two antiparallel connected diodes placed in branch 1.

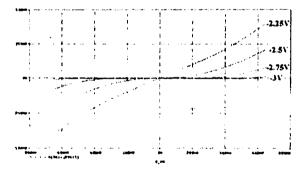


Fig. 4. Input characteristic for branch 1 consisting of two antiparallel connected diodes. All other branches except the controlling one are linear resistors.

The results in Fig. 5 have been obtained using two antiparallel connected diodes placed on branch 2. The GIC-type structure behaves like a controlled scalor cascaded with a gyrator (reflector).

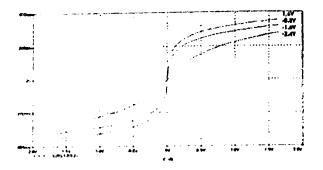


Fig. 5. Input characteristic for branch 2 consisting of two antiparallel connected diodes. All other branches except the controlling one are linear resistors..

The last two figures represent similar characteristics obtained with the antiparallel connected diodes on branch 4 and 5 respectively. The results are similar to those obtained with the nonlinear element connected on branches 2 and 1 respectively.

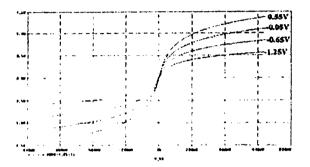


Fig. 6. Input characteristic for branch 4 consisting of two antiparallel connected diodes. All other branches except the controlling one are linear resistors.

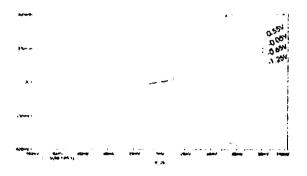


Fig. 7. Input characteristic for branch 5 consisting of two antiparallel connected diodes. All other branches except the controlling one are linear resistors.

The simulations have been performed within input and control voltage limits that did not lead to voltage and/or current saturations for the OA's.

IV. CONCLUDING REMARKS

It has been shown that using a FET controlled GICtype structure voltage controlled scalors and/or scalors cascaded with gyrator can be obtained. The structure is versatile and can be easily implemented. Moreover, using capacitors placed on various branches, C-R or L-R mutators can be obtained as well.

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