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Virtual Measurement of Op Amp Parameters

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Abstract: Circuit simulation by computer (*SPICE* simulation) has become a powerful and indispensable tool in both circuit analysis and design. This paper presents the identification of op amp parameters based on the *SPICE* model from libraries.
Keywords: op amp, model, *SPICE*

I. INTRODUCTION

The op amp is a differential single-ended amplifier implemented in a monolithic integrated circuit. The op amp amplifies the difference of the input port and produces a voltage on the output port (referenced to the ground).
As long as the op amps are operated at moderate frequencies and moderate gains there is generally remarkable agreement between actual behaviour and behaviour predicted by the ideal op amp model. Increasing frequency or gain, however, is accompanied by a progressive degradation in performance because various limitations come into play.
The static limitations are generally impervious to the curative properties of negative feedback. The most common ones are [1], [2]:

- the input offset voltage, V_{IO}
- the input offset current, I_{IO}
- the input bias current, I_{IB}
- the ac noise densities V_n and I_n
- the common-mode rejection ratio, CMRR

The dynamic op amp limitations have a profound impact on the closed-loop characteristics of a circuit: they affect both its frequency and transient responses, and also its input and output impedances. The most common dynamic limitations of op amps are [1], [2]:

- the differential input resistance, r_{id}
- the common-mode input resistance, r_{ic}
- the output resistance, r_o
- the differential voltage amplification, A_{VD}
- the unity gain-bandwidth, BI
- the pole frequencies; f_{p1}, f_{p2}
- the maximum peak output voltage swing, V_{OM}
- the slew rate, SR

Before using an op amp in an application it is useful to simulate the particular circuit. The most popular simulation tool is SPICE. The op amp can be described using a micromodel or a macromodel [3].
The micromodel is the actual transistor level model of the device and it is used in the design of the integrated circuit.
The micromodel can give a complete and accurate model of the circuit's behaviour; because of the large number of transistors with their multiple internal nodes, the simulation time is very long.
The macromodel is a functional circuit, which uses ideal elements to model the observed behaviour of the device.
The macromodel can be described in SPICE using a subcircuit. The macromodel comprises fewer elements than the micromodel, thus saving simulation time.
The accuracy or convergence of SPICE depends on the complexity of the macromodel. For instance, it is not enough to model just the gain, the input resistance and the output resistance because it is not possible this way to analyse the influence of the offset, of the common-mode signal or the frequency behaviour.

II. CHECKING THE MODELLED PARAMETERS

Both SPICE libraries and data sheet specifications offer op amp models, although their modeled parameters are not available.
Appropriate circuit design requires however the knowledge of these parameters.
The paper proposes a series of simple circuits, which allow determination of the modeled parameters using SPICE simulation. The developed circuits allow the knowledge of both static and dynamic op amp parameters.
The general circuit used to check the static and dynamic op amp limitations is presented in fig. 1.
The values for the resistances, the relations needed to calculate the parameters and/or the SPICE analysis types are given in Table 1 [4], [5].

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Table 1

R1	R2	R3	R4	Calculated and/or simulated parameters
∝	0	∞	0	V_{IO}
∞	1MΩ	∞	1MΩ	$I_{IO} = \frac{V_{OUT} - V_{IO}}{R2}$
∞	0	∞	1MΩ	$I_{IB} = \frac{V_{OUT} - V_{IO}}{R4} - \frac{I_{IO}}{2}$
10kΩ	10kΩ	10kΩ	10kΩ	$CMRR_{dB} = 20\log\left(\frac{V_{OUT}}{V_{CM}}\right)$
0	∞	0	∝	$r_{ic} = \frac{V_{IN}}{I(V_{IN})}$
0	∞	∞	0	$r_{id} = \frac{V_{IN}}{I(V_{IN})}$; r_o (.TF analysis)
				A_{VD}, B1, f_{p1},f_{p2} (.AC analysis)
				V_{OM}, SR (.TRAN analysis)

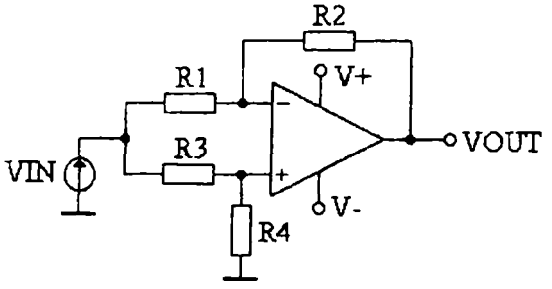

Fig. 1. Circuit for checking static and dynamic op amp limitations

III. EXPERIMENTAL RESULTS

The resistance values given in lines 2 to 7 from Table 1, allow the implementation of 6 circuits. Any SPICE model available in SPICE libraries or in data sheets, wen introduced in one of the 6 test circuits allows the measurement of the op amp modelled parameters.

Lines 2 to 5 from Table 1 correspond to the circuits allowing the determination of op amp static limitations. The last two lines of Table 1 correspond to the test circuits supporting the measurement of op amp dynamic parameters.

The 6 circuits are analysed one by one, subsequently writing the SPICE source file required to determine, by virtual measurement – simulation – the modelled op amp parameters.

Experimental determinations were carried out using the evaluation version of the MicroSim Pspice 6.0 program. The two op amp models: μA741 and LF411 were chosen from eval.lib. The first one is a bipolar widely used op amp whereas the second one has an input stage implemented with J-FETs.

The circuit used in determining the input offset voltage. V_{IO} results for the resistor combination given in line 2 of Table 1. The test circuit where the nodes are numbered according to SPICE is shown in Fig. 2.

The source file describing the test circuit is:

```
 R  UT NO.  -  O
X1      0  5  3  4  5  uA741;LF411;
.LIB    EVAL.LIB
V+      3        0        DC      15
V-      4        0        DC      -15
.END
```

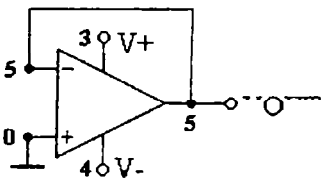

Fig. 2. Circuit for checking V_{IO}

From the output file (*.OUT) we keep the voltage in node5, V(5). This voltage is the input offset voltage. For the two op amp types the obtained values are:

- for the uA741: V(5)=20.74E-06
- for the LF411: V(5)=-3.301E-06

The obtained results show that the two op amps were modeled by disregarding the input offset voltage.

If high resistors are connected in series with the non-inverting input and included in the feedback loop of the op amp, the input bias currents will determine measurable voltage drops across the resistances. Thereby, information on the difference of the two input bias currents, representing the offset input current I_{IO} becomes available. The test circuit is as shown in Fig. 3.

The source file is written as:

```
CIRCUIT NO.2 - IIO
R2      2        5        1Meg
R4      1        0        1Meg
X1      1  2  3  4  5  uA741;LF411;
.LIB    EVAL.LIB
V+      3        0        DC      15
V-      4        0        DC      -15
.END
```

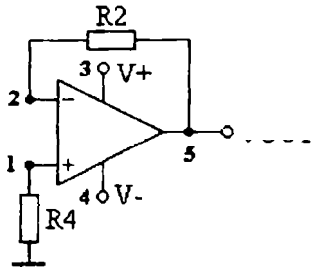

Fig. 3. Circuit for checking I_{IO}

The output voltages used in calculations are:

- for the uA741: V(5)= 65.48E-06
- for the LF411: V(5)= -3.298E-06

The calculated values of the I_{IO} are very small and in disagreement with the data sheet specifications of these op amps:

- for the uA741: IIO=44.7pA
- for the LF411: IIO=0.003pA

The only remarkable difference consists in the much lower I_{IO} current in J-FET op amps compared to the op amp equipped with bipolar transistors at the input. The difference between the I_{IO} values for the two op amps corresponds to the real case value but the values are by approximately three orders of magnitude lower then the real ones.

The 3-rd test circuit, presented in Fig. 4, allows the determination of the input bias current, I_{IB}. The source file is:

```
CIRCUIT NO.3 - IIB
R4      1       0       1Meg
X1      1  5  3  4  5  uA741;LF411;
.LIB    EVAL.LIB
V+      3       0       DC      15
V-      4       0       DC      -15
.END
```

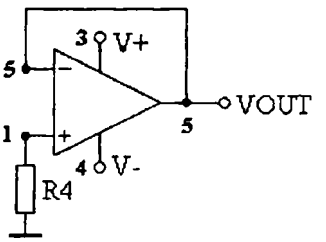

Fig. 4. Circuit for checking I_{IB}

The output voltages, which were determined for the two op amps lead to following input bias current values:

- for the uA741: I_{IB} =79.65nA
- for the LF411: I_{IB} =40.3pA

The test circuit shows the fact that, in modeling the two op amp types the input bias current was taken into account. The values of the I_{IB} are comparable with the real ones.

The test circuit, which allows the determination of the common-mode rejection ratio, CMRR is given in Fig. 5.

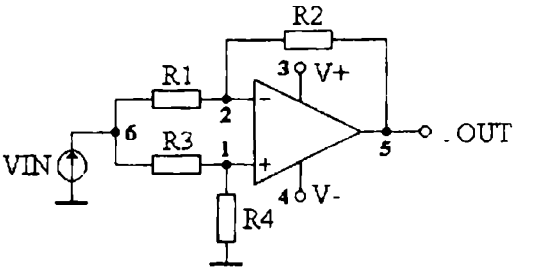

Fig. 5. Circuit for checking CMRR

The analyzed circuit is in closed loop, like the other 3 previously presented circuits. The SPICE description of this circuit is:

```
CIRCUIT NO.4 - CMRR
R1      6       2       10K
R2      2       5       10K
R3      6       1       10K
R4      1       0       10K
X1      1  2  3  4  5  uA741;LF411;
.LIB    EVAL.LIB
V+      3       0       DC      15
V-      4       0       DC      -15
VIN     6       0       AC      1
.AC     DEC     10      1       1G
.PROBE
.END
```

By contrast to the previous 3 circuits where dc analyses were carried out, reading the values of the steady-state operating point, the circuit used to determine the CMRR is subjected to an ac analysis. Thereby, we obtain the variation of the CMRR with frequency, which is represented in Fig. 6 for the uA741 op amp.

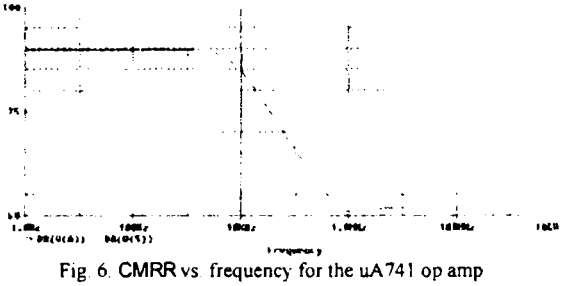

Fig. 6. CMRR vs. frequency for the uA741 op amp

The CMRR value at low frequency is 90dB, which is in agreement with the real case.

Similarly, we obtain a CMRR=106dB for the LF411 op amp.

From the dynamic parameters, the common mode input resistance is determined on the circuit in Fig. 7. The source file is written:

```
CIRCUIT NO.5 - ric
X1      1  1  3  4  5  uA741;LF411;
.LIB    EVAL.LIB
V+      3       0       DC      15
V-      4       0       DC      -15
VIN     1       0       AC      1
```

```
.AC     DEC    10     1      1G
.PROBE
.END
```

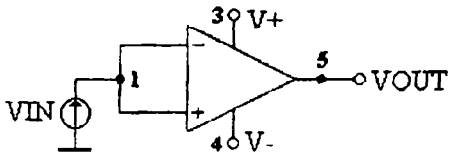

Fig. 7. Circuit for checking r_{ic}

The value of the common-mode input resistance can be determined by an ac analysis. For the uA741 op amp, the variation of r_{ic} with frequency is like the one in Fig. 8.

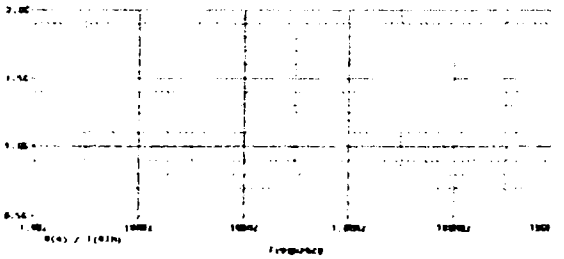

Fig. 8. Graphical determination of ric

The value of r_{ic} is 1.25GΩ for the uA741 op amp. Similarly, for the LF411 op amp we obtain $r_{ic} \cong 500G\Omega$.

The test circuit of Fig. 9, although more simple, allows the identification of a significant number of dynamic parameters. We thus can determine:

- $R_{in} = r_{id} \| 4r_{ic}$ and r_o by a transfer function-type analysis (.TF)
- A_{VD}, B1, f_{p1} and f_{p2} by an ac analysis (.AC)
- V_{OM} and SR by a time-domain analysis (.TRAN).

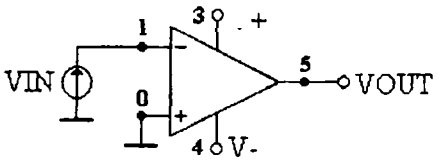

Fig. 9. Circuit for checking dynamic parameters

The circuit description is:

```
CIRCUIT NO.6 - rid, ro
*AVD, B1, fp1, fp2
*VOM, SR
X1      0  1  3  4  5  uA741;LF411;
.LIB    EVAL.LIB
V+      3      0      DC     15
V-      4      0      DC     -15
VIN     1      0      AC     10U
+SIN(0 1 1K)
.TF     V(5)   VIN
.AC     DEC    101    1      1G
.TRAN   1E-6   2M     0      1E-6
.PROBE
.END
```

The transfer function-type analysis leads to following results:

- for uA741:
  R_{in}=996.3kΩ
  = 5 .7Ω
- for LF411
  R_{in}=399.6GΩ
  ro=76.39Ω

Since on the input circuit of the op amp, r_{id} appears in parallel with $4r_{ic}$, after determining the value of r_{ic}, r_{id} is recalculated using the relation:

$$r_{id} = \frac{4 \times r_{ic} \times R_{in}}{4 \times r_{ic} - R_{in}}$$

After recalculation, r_{id} becomes:

- for uA741: r_{id} =1MΩ
- for LF411: r_{id} =500GΩ.

The ac analysis allows determination of the A_{VD} and B1 on the amplitude characteristic and the pole frequencies on the phase characteristic. The amplitude and the phase characteristic for an uA741 op amp are presented in Fig. 10 and 11 respectively.

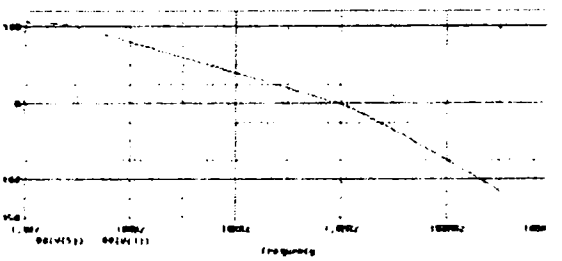

Fig. 10. The amplitude characteristic of the uA741

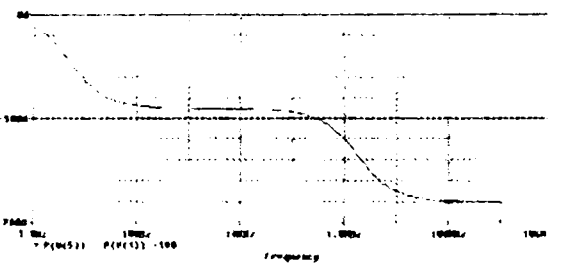

Fig. 11. The phase characteristic of the uA741

The phase characteristic determines the pole frequencies, namely: f_{p1} at the phase angle -45°, f_{p2} at the phase angle -135° respectively.

The frequency characteristics in Fig. 10 and 11 show the following values for the uA741:

- A_{VD} = 106dB,
- B1 = 877kHz,
- f_{p1} = 5Hz, f_{p2} = 1.75MHz.

Similarly, for the LF411, the obtained values are:

- A_{VD} = 112dB,
- B1 = 5.35MHz,
- f_{p1} = 20Hz, f_{p2} = 4.8MHz.

To determine the maximum amplitude of the output signal, which, at limit, corresponds to the saturation

voltage, as well as the maximum slew rate of the output signal, SR, a time-domain analysis is carried out. A rectangular signal, symmetrical with respect to zero, is applied at the input. The output signal is limited to the saturation voltages. The signal variation is a linear ramp, characteristic for the SR-effect. The slope of the output signal is the SR parameter.

For the uA741 op amp the output signal takes the form shown in Fig. 12. The maximum positive and negative values of the output voltage and the SR are respectively:

- $V_{sat}^{+} = +14.613V$,
- $V_{sat}^{-} = -14.613V$, and
- $SR = \frac{28.995V}{63.675\mu s} = 0.455\,V/\mu s$

The SR value is very close to the value specified in the data sheets.

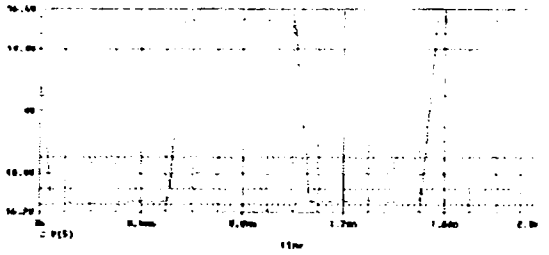

Fig. 12. Time behaviour of the uA741

For the LF411 the following values were obtained:

- $V_{sat}^{+} = +14.176V$,
- $V_{sat}^{-} = -14.176V$, and
- $SR = \frac{28.119V}{13.608\mu s} = 2.066\,V/\mu s$.

IV. CONCLUSIONS

- the proposed test circuits allow fast determination of both static and dynamic parameters for any op amp SPICE model;
- any SPICE version can be used for this purpose;
- the proposed circuits can be described either in text mode, by means of a text editor, or in graphical mode by drawing the circuits;
- the proposed circuits are simple, have small number of nodes allowing fast execution of the SPICE application.

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