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MEMS based broadband phase shifters

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Abstract – A phase shifter based on an array of MEMS is designed and then analyzed by computer simulation. It is shown that for a stable bridge position, the maximum ratio of the equivalent capacitance cannot exceed 1.2. For a microwave signal applied to the bridge, it is also shown that due to the very small time response of the MEMS, the equivalent capacitance depends on the DC voltage only. For this type of phase shifter, if the maximum operating frequency is much lower than the Bragg frequency, the phase shift varies linearly versus the frequency, so broadband applicatons such as pulse processing are possible.
Keywords: MEMS, phase shifter.

I. INTRODUCTION

During the last years, distributed circuits such as switches, phase shifters, BPSK modulators (see for example [1], [2], [3], [4]) have been integrated by using MEMSs (micro-electromechanical systems). Due to the small MEMS series resistance, these circuits have very low insertion loss, being an important advantage for millimeter-wave frequency range. On the other hand, the MEMS device has a high time response to the operating applied voltage, compare to the Schottky-varactor diodes, devices also used for these applications. The circuits based on an array of MEMSs may have a low insertion loss, but also a large frequency bandwidth, due to their distributed structure.

In this paper, a design procedure for the phase shifters based on an array of MEMSs loading a CPW transmission line, is presented in detail. The MEMS analysis is performed for DC voltage as well as for RF signal, showing that the device has a linear behaviour in the microwave frequency range. The MEMS phase shifter is analysed for sinusoidal and square input signals, wherefrom the broadband characteristics of these types of circuits are put into evidence.

II. MEMS ANALYSIS

The MEMS cross section is given in Fig. 1, where l_b and t_b are the length and the thickness of the metal bridge, respectively. In this paper, the width of the metal bridge is w_b. The bridge is suspended at a distance $g+t_d$ from the CPW central line, which, under the bridge, has the width W (g is the air gap under the bridge and t_d is the thickness of the dielectric layer deposited on the CPW central line, having the dielectric constant, $\varepsilon_{r,d}$). When a voltage, V, is applied on the metal bridge, the electrostatic force, F_e, changes the distance between the two metal plates of the MEMS, from $g+t_d$ to $g+t_d-z$. From the mechanical point of view, the following formula may be used for the spring constant, k [5]:

$$k = k_0 \cdot \left[1-\left(1+\frac{W}{l_b}\right)\cdot\left(1-\frac{W}{l_b}\right)^3\right]^{-1}$$

where $k_0 = \dfrac{W}{l_b}\left(\dfrac{32Ewt_b^3}{l_b^3}+\dfrac{8\sigma(1-\nu)w_b t_b}{l_b}\right)$, E is the Young's modulus, ν is the Poisson's ratio and σ is the residual stress. The dynamic equation of motion for the bridge, which may be solved in order to find the position of the bridge along the z-axis, is (see for example [6]):

$$m\cdot\frac{d^2z}{dt^2}+b\cdot\frac{dz}{dt}+k\cdot z=\frac{\varepsilon_0 w_b W V^2}{2\left(g+\dfrac{t_d}{\varepsilon_{r,d}}-z\right)^2},$$

where m is the mass of the bridge and b is the damping coefficient. This dynamic equation has been solved by using a time domain method [7]. Applying this method, for $l_b = 300\,\mu m$, $w_b = 60\,\mu m$, $t_b = 1\,\mu m$, $g = 2.5\,\mu m$, $t_d = 0.3\,\mu m$, $\varepsilon_{r,d} = 7.5$ and for two values of the bridge width ($W = 140\,\mu m$ and $W = 90\,\mu m$), $g-z$ may be computed and graphically represented as in Fig. 2 a. It is important to observe

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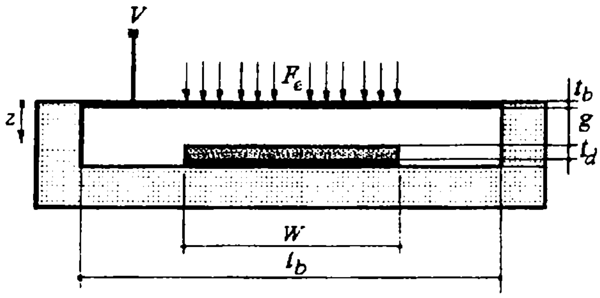


Fig. 1 The MEMS cross section

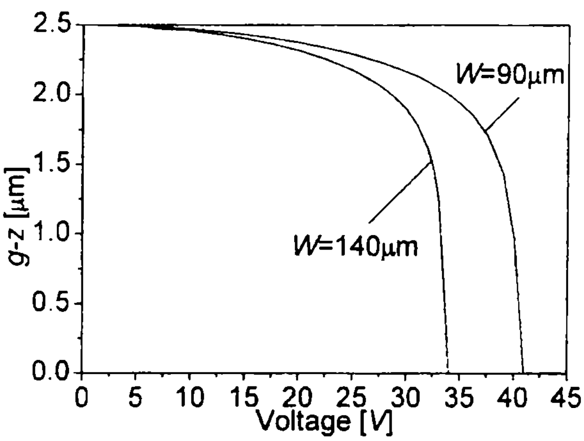
that $g-z$ has a very sharp variation for the applied voltage around the pull-down value. Then, for values of the applied voltage close to the pull-down voltage, the position of the bridge is not stable. In this case, for MEMS applications such as phase shifters, in order to control the phase shift value, the applied voltage must not exceed ~25V, for $W = 140\ \mu m$ and ~30V, for $W = 90\ \mu m$. It is not difficult to show that the normalized equivalent MEMS capacitance, is:

$$\frac{C_s}{C_o} = \frac{1}{1-\dfrac{z}{z_o}},$$

where:

$$z_o = g + \frac{t_d}{\varepsilon_r} \text{ and } C_o = C_s\big|_{V=0} \cdot \frac{\varepsilon_0 w W}{g + \dfrac{t_d}{\varepsilon_r}}$$

is the MEMS capacitance for $V = 0$ (the minimum capacitance value). The normalized capacitance, C_s / C_o, versus z / z_0 is shown in Fig. 2 b, for the same data as for Fig. 2 a. Taking into account the maximum value for the applied voltage given above, from Fig. 2 b, it is drawn the conclusion that the maximum capacitance ratio is ~1.2, a similar estimation as in [8].



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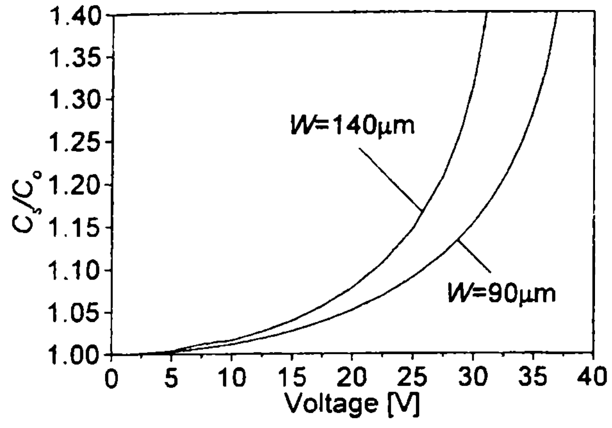


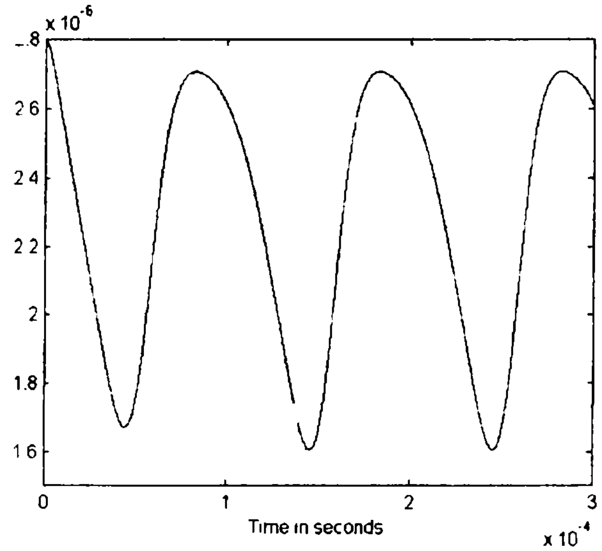
(b)

Fig. 2. The distance between the bridge and the dielectric layer, (a) and the normalized capacitance (b), versus the applied voltage

The MEMS is not a fast device. If a sinusoidal signal is applied on the MEMS bridge, arround a DC voltage, then the bridge position cannot follows the fast variation of the signal. Therefore, if the signal frequency is high enough, the bridge position is possible to be given by the DC voltage only. To prove this, for the MEMS geometrical dimensions given above, the simulation results concerning the MEMS behaviour to the RF signal are shown in Fig. 3, for $W = 140\ \mu m$ and in Fig. 4, for $W = 90\ \mu m$, where the amplitude of the sinusoidal signal, V_{ampl}, is equal to 10V and the DC voltages are equal to 25V and 15V, respectively. The RF frequency is 10KHz, 30KHz and 200KHz. From these figures, it is observed that for a microwave signal applied on the bridge, the MEMS equivalent capacitance depends on the DC voltage only, even if this is a nonlinear capacitance, due to the small time response of this kind of device. As a result, even for high power microwave signal, the MEMS may be seen as a linear device. This observation is important for a phase shifter based on a MEMSs array, because the phase shift will depend only by the apllied DC voltage, without other small signal constrains.

III. PHASE SHIFTERS DESIGN AND ANALYSIS

The phase shifter consists of an array of MEMSs, periodically loading a CPW transmission line. If the length of the CPWs which connect two consecutive MEMSs, l, is small enough, a lumped equivalent circuit may be used [7]. In this paper, Rl, Ll, Cl and Gl are the lumped values of the CPW equivalent circuit, which depend on the CPW distributed parameters (R, L, C and G). Also, R_s, L_s and C_s will be used as notations for the equivalent resistance, inductance and capacitance of the MEMS, respectively. The formulas used for the procedure design of the switch may be derived from this equivalent circuit. If the maximum operating frequency, f_{max}, is lower enough compare to the resonance frequency of the MEMS, then the influence of the MEMS series inductance may be neglected ($\omega L_s << \frac{1}{\omega C_s}$). Also, because the losses due to the CPW transmission lines and due to the MEMSs are small, so $Rl \cong 0$, $Gl \cong 0$ and $R_s \cong 0$. Therefore, taking into account that the circuit consists of n identical cells, the Bragg frequency and the input impedance of the circuit are given by: $f_b = \frac{1}{\pi\sqrt{Ll(C_s + Cl)}}$ and $Z_{in} \cong \sqrt{\frac{Ll}{C_s + Cl}}$, where, the expression for Z_{in} is true only if $f_{\max}^2 / f_b^2 << 1$. For the CPW characteristic impedance, Z_c, the formula $Z_c = \sqrt{\frac{Ll}{Cl}}$, may be used. For the circuit design, a few constraints of the input data must be respected: $Z_{in} = 50\Omega$ and the value for the characteristic impedance of the CPW transmission line, Z_c, must be higher in order to



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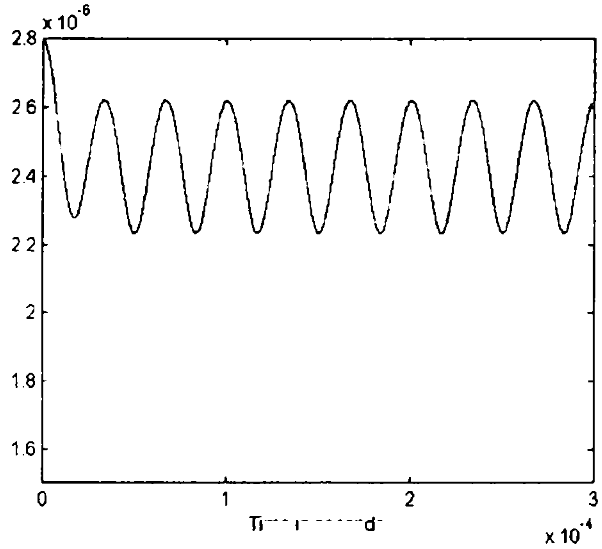

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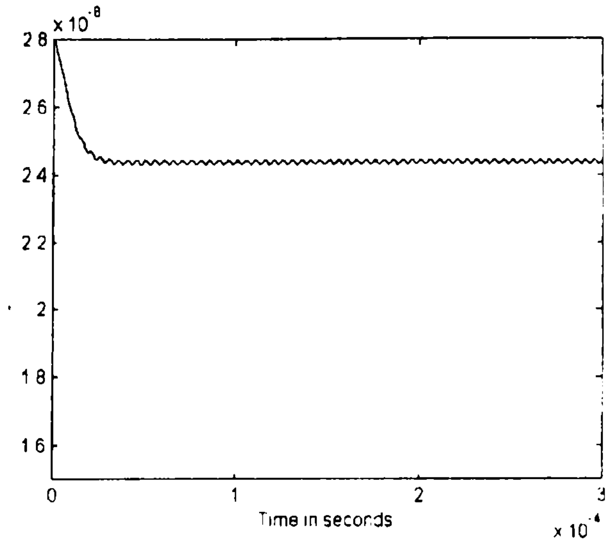
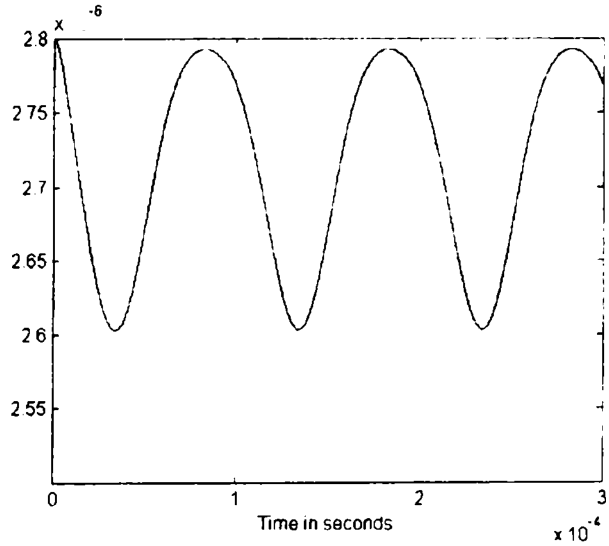


(c)

Fig. 3. The distance between the bridge and the dielectric layer, for the MEMS operating at V_{DC} = 25 V, V_{ampl} = 10 V, W=140μm and f = 10 KHz (a), 30 KHz (b) and 200 KHz (c).



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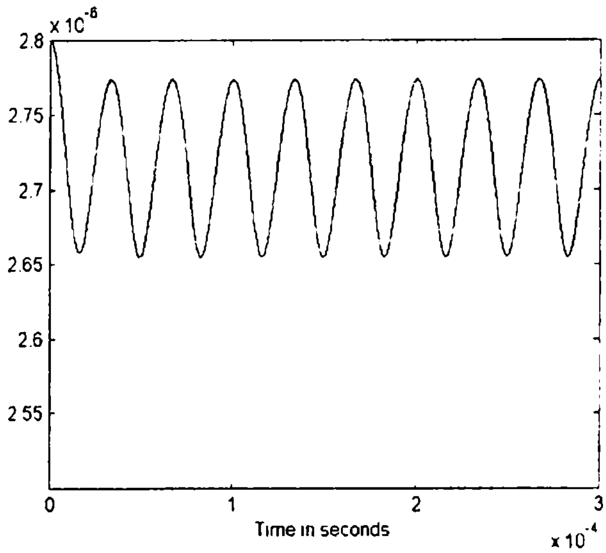

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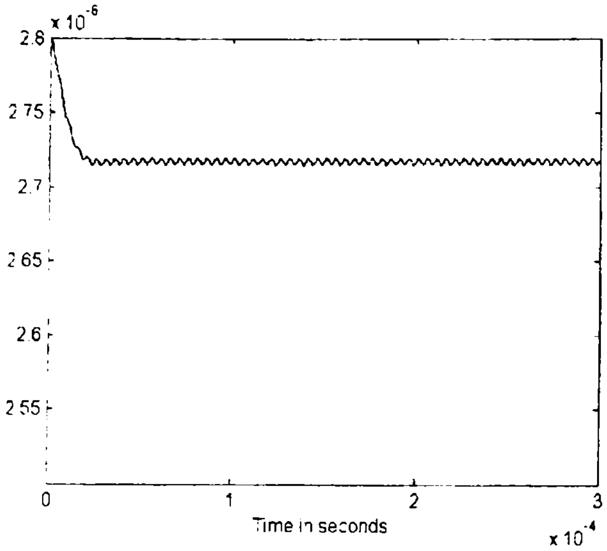


(c)

Fig. 4. The distance between the bridge and the dielectric layer, for the MEMS operating at V_{DC} = 15 V, V_{ampl} = 10 V, W=90μm and f = 10 KHz (a), 30 KHz (b) and 200 KHz (c).

decrease the CPW electrical length, θ (so to decrease the length of the circuit), but, on the other hand, it must be lower in order to reduce the CPW losses, α (Z_c must be chosen to minimize αθ). For $Z_{in} = 50\,\Omega$, $f_{max}/f_b = 0.15$, $\varepsilon_r = 11.9$ (the substrate dielectric constant for silicon), $t = 1$ μm (the thickness of the CPW gold metallization), $w + 2s = 300$ μm (w and s are the width and the slot of the CPW between MEMSs), αθ is minimized if Z_c is 60Ω - 80Ω [7]. In this paper, Z_c=75Ω. Combining the expression for f_b, Z_{in} and Z_c, they are obtained, $Ll = Z_{in}/(\pi f_b)$, $Cl = Z_{in}/(\pi f_b Z_c^2)$ and $C_s = \left|(Z_c/Z_{in})^2 - 1\right| \cdot C_l$. The electrical length of the CPW transmission line which connects two consecutive MEMSs may be obtained with $\theta = 2\pi f_{max}\sqrt{Cl \cdot Ll}$ and then, by using a commercial software, the CPW length, l, it is easily computed. The distances g and t_d are usually imposed by the technological constraints. Assuming that the values for g, t_d and $\varepsilon_{r,d}$ are known, the formula for $w \cdot W$ is: $wW = C_o \cdot \dfrac{g\varepsilon_{r,d} + t_d}{\varepsilon_o \varepsilon_{r,d}}$. For n cells, the maximum phase shift introduced by the circuit, at the maximum operating frequency, may be computed as $\Phi \cong 2\pi f_{max} n\sqrt{Ll(C_s + Cl)}$. This formula for Φ may be used to compute the number of cells, n, if the value for Φ is imposed.

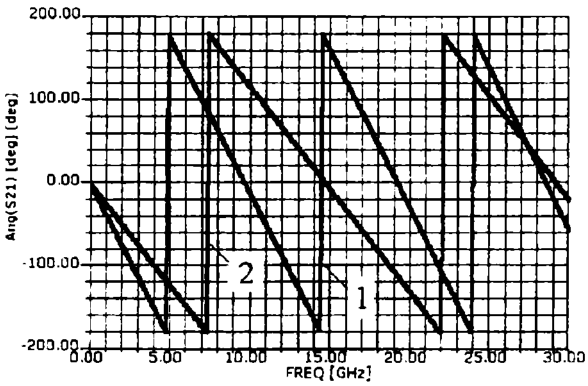
Two phase shifters have been designed, the first one for W = 140μm and the second one for W = 90μm. The design formulas introduced above have been applied for a maximum operating frequencies, f_{max}, of 17GHz for the first circuit and 25GHz for the second one, in the both cases f_b/f_{max} =0.15. For the two circuits, they were obtained θ=11.46deg, $w = 50$ μm, $s = 125$μm, while the CPW lengths and the CPW equivalent inductance and capacitance, between two consecutive MEMSs, are l=223μm, $Ll = 0.141$nH, $Cl = 25$fF, for the first circuit and $l = 150$ μm, $Ll = 0.094$nH, $Cl = 16.7$fF, for the second one. Imposing $W = 140$ μm and $W = 90$ μm (geometrical dimensions for the MEMSs analyzed in section II), for the both circuit, $w_b = 60$ μm. Also, C_s=31.3fF and C_s=20.9fF, corresponding to V_{DC}=25V and 15V, respectively. Taking into account the others geometrical and electrical MEMS parameters (given in section II), it is obtained $L_s = 50.75$ pH. The MEMS series resistance depends on the frequency. For these values and $n = 38$, the maximum phase shift is $\Phi \cong 385$deg, for the both phase shifters, computed at f_{max} = 10GHz for the first circuit and f_{max} = 15GHz, for the second one. The two phase shifters have been numerically analyzed, in order to obtain de magnitude and the phase for S_{21} and also the magnitude for S_{11} (the CPW losses effect are included). The results are shown in Fig. 5, wherefrom, for the phase shift, it is observed a good agreement between the analytical and simulated values (see Fig.5 a). Also, a return loss better than 30dB (see Fig. 5b), has been obtained for the both circuits, while the insertion loss is smaller than 0.5dB for the first circuit and 0.4dB for the second one, up to the maximum operating frequencies. The second phase shifter is lossless compare to the first one because is shorter (the two circuits have the same number of cells).

The phase shift introduced by the circuit may be also analyzed in the time domain. Fig. 6 shows the results for the second phase shifters and two values of the DC voltage, V_{DC}, 10V and 30V. The frequency of the input signal is 15GHz. The delay time is different in the two cases because the MEMS equivalent capacitance depends on the DC voltage. From this figure, the time delay introduced by the circuit is ~74ps for V_{DC}=10V and ~79ps for V_{DC}=30V, these results being in good agreement (5% error) with those obtained by using formula $n\sqrt{Ll(C_s + Cl)}$. The 5ps difference between the two time delay values at 15GHz means a phase shift difference of 27deg. In some applications which ask for a larger value of the phase shift difference, the number of cells must be increased or/and to minimize the influence of the CPW equivalent capacitance.

In order to evaluate the broadband characteristic of this phase shifter, the next simulation has been performed for a square pulse applied to the input of the second circuit. For V_{DC}=10V and pulse width of 10ps, 30ps, 50ps, the output waveforms presented in Fig. 7 show that if the pulse width decreases, for a given Bragg frequency, the dispersive characteristic of the circuit contributes to the pulse shape distorsion. This is because for short pulses, the condition f_b / f_{max}=0.15, which assures the less dispersive character of the circuit, is not true for the spectral components having important amplitudes above $f_{max} \cong 25$GHz. From Fig. 7, it is observed that for pulse width greater than 30ps, the dispersive character of the circuit may be neglected. For an input pulse width of 50ps, the delay time introduced by the circuit is the same as for a sinusoidal wave (see Fig. 6), for V_{DC}=10V as well as for V_{DC}=30V (see Fig. 8), showing the broadband characteristic of the circuit.

IV. CONCLUSIONS

In this paper, a pahase shifter based on an array of MEMSs has been designed and analyzed. It has been shown that in order to use MEMSs in these applications, the maximum ratio of the equivalent capacitance cannot exceed 1.2, for a stable bridge position. Also, due to the very small time response of the MEMS, if a microwave signal is applied to the bridge, the bridge position as well as the equivalent capacitance depend on the DC voltage value only. The analysis results obtained for the MEMSs array phase shifter show that if the maximum operating frequency is much lower than the Bragg frequency, then the phase shift varies linearly versus the frequency. Therefore, the delay time is practically constant up to this maximum operating frequency, so the circuit may be also used as delay circuit for pulses.



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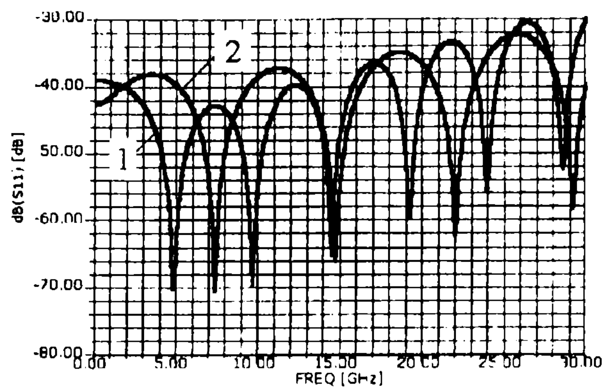

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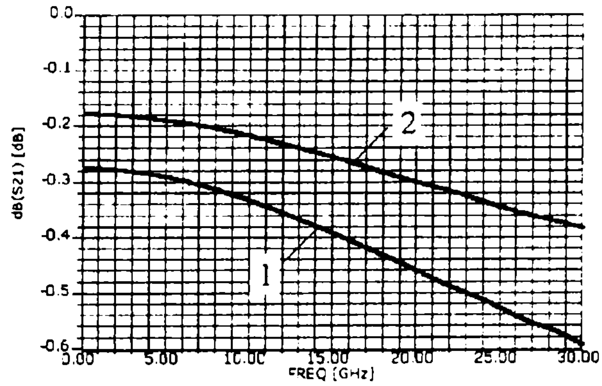
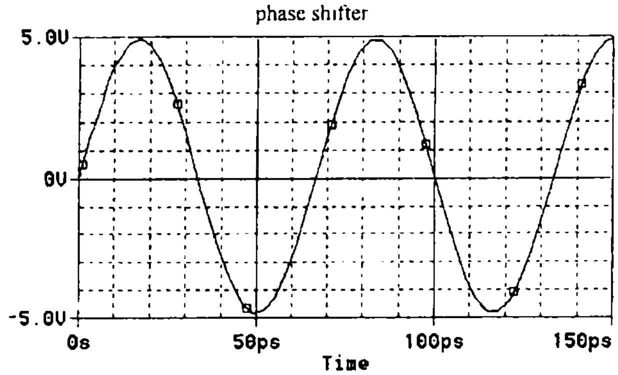


(c)

Fig 5 The numerical results obtained for the phase shift, return loss and insertion loss, for the first (1) and the second (2) phase shifter



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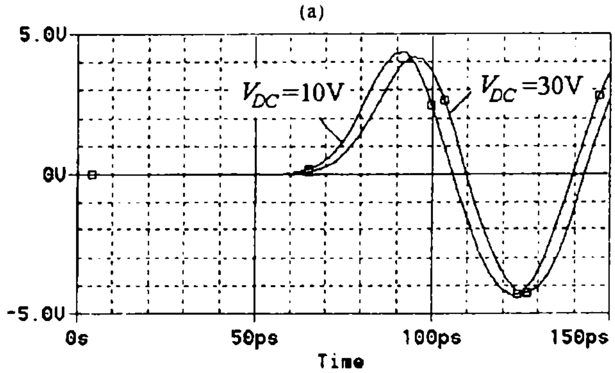

(b)

Fig 6. The input (a) and the output (b) waveforms for the second phase shifter, for V_{DC}=10V and V_{DC}=30V (the input signal has the frequency equal to 15GHz).

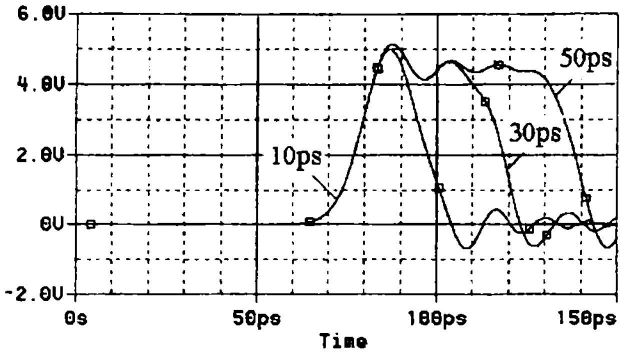

Fig. 7 The output waveforms for pulses of different widths, applied to the input of the second phase shifter (V_{DC} =10V).

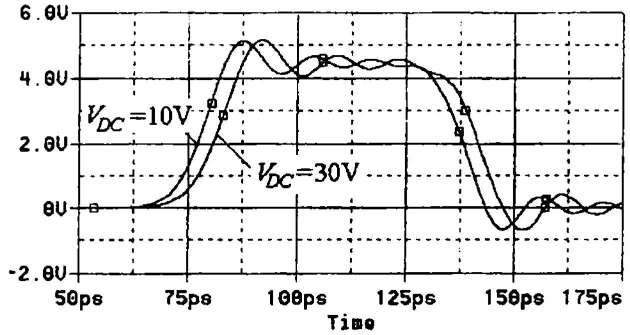

Fig. 8 The output waveforms for a pulse of 50ps width, applied to the input of the second phase shifter operating to V_{DC} =10V and V_{DC} =30V.

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