WIDE RATIO BIDIRECTIONAL DC-DC CONVERTERS FOR SUPERCAPACITOR STORAGE APPLICATIONS

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Abstract:
This thesis presents new wide-ratio bidirectional hybrid DC-DC converters used in supercapacitor storage, frequently employed for enhancing the storage performances in microgrids or electric vehicles. The presented topologies are developed from unidirectional hybrid structures which are characterized by the use of switched cells consisting of identical capacitors or inductors switched between series and parallel connection with the help of diodes. By operating in this manner, the switching cells help achieve a wider (higher in step-up converters or lower in step-down converters) voltage conversion ratio, lower active switch stress, and smaller passive components. The bidirectional structures achieve the same benefits as the unidirectional topologies, with the added benefit of two quadrant operation.
This work if focused on four converter topologies, from which three are proposed by the author. The studied topologies are described analytically, in order to obtain design equations and comparison metrics. Dynamic analysis is performed to achieve a better hardware design of converters, to assess their stability and to design current controllers. Digital simulations are used to aid the design and analysis of the studied converters. Experimental results are acquired for two hybrid topologies in applications with a power scale up to 5kW. In order to measure efficiency and test the influence of different switches, one topology was built using MOSFETs and GaN-FETs. To eliminate some disadvantages, an improved version is proposed for each of the studied topologies.
Power sharing strategies for supercapacitor storage in microgrid applications are proposed and implemented with the help of a hybrid converter. Their operation is tested trough experimental and digital simulations.

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NOMENCLATURE

Abbreviations

DC – direct current
AC – alternative current
PV – photovoltaic
SC – supercapacitor
EDLC – electric double layer capacitor
CBBB – conventional bidirectional buck/boost converter
MOSFET – metal oxide semiconductor field effect transistor
Si-MOSFET – Silicon MOSFET
PWM – pulse width modulation
ESR – equivalent series resistor
RMS – root mean square
BSQZ – bidirectional switched-quasi-z-source converter
CBQ – conventional bidirectional quadratic converter
BQ1, BQ2, BQ3 – new bidirectional quadratic converters
BTMM – bidirectional triangular modular multilevel converter
BSC1, BSC2 – bidirectional switched capacitor converters
BHSC1, BHSC2 – bidirectional hybrid switched capacitor converters
UHSC1, UHSC2 – unidirectional hybrid switched capacitor converters
VCM – valley current mode control
SSA – state space average
LPF – low pass filter
ZOH – zero order hold
ADC – analog to digital converter
I-BHSC1 – improved bidirectional hybrid switched capacitor converter
BHSC2 – bidirectional hybrid switched capacitor converter
RHPZ – right half-plane zero
3L-BB – three level buck boost converter
3L-BHSC2 three level BHSC2 converter
BHSI – bidirectional hybrid switched inductor converter
GaN-FET – gallium nitride field effect transistor
DUSHI – step-down unidirectional hybrid switched inductor converter
UUSHI – step-up unidirectional hybrid switched inductor converter
I-BHSI – improved BHSI converter
EMI – electromagnetic interference
BHSISC – bidirectional hybrid switched inductor switched capacitor converter
I-BHSISC – improved BHSISC
DG_1, DG_2, DG_n – distributed generators
EMS – energy management system
SoC – state of charge
ND-LRZD – nonlinear droop linear resistor and Zener diodes method
ND-NR – nonlinear droop nonlinear resistor method
CV – constant voltage
CC – constant current
Sat. 1, Sat. 2 – saturation blocks
VID – virtual impedance droop method
NVID – nonlinear virtual impedance droop method

Symbols

V_L – lower voltage input of converter
V_H – higher voltage input of converter
I_L – current on the lower voltage side input of converter
I_H – current on the higher voltage side input of converter
R_{load} – load resistor
C, C_1, C_2, C_i, C_{ij} – capacitors
C_{SC} – supercapacitor
C_{bus} – DC bus capacitor
C_H – capacitor from the higher voltage side input of converter
C_L – capacitor from the lower voltage side input of converter
C_{sw} – switched capacitor from a hybrid converter topology
W_C, W_{C1}, W_{C2} – capacitor energy
W_{CH} – energy of C_H capacitor
W_{CL} – energy of C_L capacitor
W_{Csw} – energy of C_L capacitor
W_{CTot} – total capacitor energy
$W_{CTot(x)}$ – total capacitor energy in converter number x
V_C, V_{C1}, V_{C2}, V_{Cij} – average capacitor voltage
V_{Cmax} – maximum capacitor voltage
v_{Csw} – switched capacitor instantaneous voltage
V_{Csw} – switched capacitor average voltage
Δv_{CH} – C_H capacitor voltage ripple
Δv_{CL} – C_L capacitor voltage ripple
Δv_{Csw} – C_{sw} capacitor voltage ripple
r_v – capacitor ripple voltage percentage
i_{CL} –instantaneous current on C_L capacitor
i_{CH} –instantaneous current on C_H capacitor
i_{Csw} –instantaneous current on C_{sw} capacitor
i_{C1}, i_{C2} –instantaneous current on C_1 and C_2 capacitors
L_1, L_2, L_3, L_4, L_i, L_{ij} – inductors
i_{L1}, i_{L2}, i_{L3}, i_{L4} – instantaneous inductor currents, as time functions
i_{L1}^* – i_{L1} reference current
I_{L1}, I_{L2}, I_{L3}, I_{L4}, I_{Lij} – average inductor currents
Δi_{L1}, Δi_{L2}, Δi_{L3}, Δi_{L4} – inductor ripple currents
r_i – inductor ripple current percentage
v_{L1}, v_{L2}, v_{L3}, v_{L4} – instantaneous inductor voltage, as time functions
$\langle v_{L1} \rangle$, $\langle v_{L2} \rangle$, $\langle v_{L3} \rangle$, $\langle v_{L4} \rangle$ – averaged inductor voltage
W_{L1}, W_{L2}, W_{L3}, W_{L4}, W_{Li} – inductor energy
W_{LTot} – total inductor energy
$W_{LTot(X)}$ – total inductor energy in converter with number x
t – *time*
t_{on} – time interval where the main switch(es) are ON in step-down operation
t_{off} – time interval where the main switch(es) are OFF in step-down operation
t_{on}'– time interval where the main switch(es) are ON in step-up operation
t_{off}' – time interval where the main switch(es) are OFF in step-up operation
T – switching period
f – switching frequency
Δt – time interval variation
D – duty cycle, for step-down operation

D' – duty cycle, for step-up operation
S_1, S_2, S_3, S_4, S_5, S_{Aij}, S_{Bij}, S_{Li}, S_{Hi} – active switches
D_1, D_2 - diodes
v_{S1}, v_{S2}, v_{S3}, v_{S4}, v_{S5} – switch voltages
i_{S1}, i_{S2}, i_{S3}, i_{S4}, i_{S5} – switch currents
S – total active switch stress
$S_{(x)}$ – total active switch stress in the converter with number x
V_{S1}, V_{S2}, V_{S3}, V_{S4}, V_{S5}, V_{Sj}, V_{SAij}, V_{SBij} – average switch voltage stresses
I_{S1}, I_{S2}, I_{S3}, I_{S4}, I_{S5}, I_{Sj}, I_{SAij}, I_{SBij} – average switch currents stresses
V_{D1}, V_{D2} – average diode voltage stresses
I_{D1}, I_{D2} – average diode currents stresses
V_{PWMS1}, V_{PWMS2} – switch driving signal
x – state vector
u – input vector
y – output vector
r_{L1}, r_{L2}, r_{L3}, r_{L4} – inductor ESRs
r_{CH}, r_{CL}, r_{C1}, r_{C2}, r_{Csw} – capacitor ESRs
r_H, r_L – high and low voltage inputs resistances
r_{S1}, r_{S2}, r_{S3}, r_{S4} – switch on-state resitances ($R_{DS(on)}$)
A_i – equivalent state matrix for i^{th} state (i=1 for t_{on}, i=2 for t_{off})
A_e – averaged equivalent state matrix
a_{xy_i} – state matrix element of line x, column y, i^{th} state
B_i – equivalent input matrix for i^{th} state (i=1 for t_{on}, i=2 for t_{off})
B_e – averaged equivalent input matrix
b_{xy_i} – state matrix element of line x, column y, i^{th} state
C_{e1}, C_{e2}, C_e – output matrix
d – dynamic duty cycle
$\tilde{x}$ – small signal state vector
$\tilde{d}$ – small signal duty cycle
$\tilde{y}$ – small signal output vector
$G_{P1}(s)$, $G_{P2}(s)$ – system transfer functions in s domain
I – identity matrix
PM – phase margin
GM – gain margin
f_c – crossover frequency
$G_C(s)$ – controller transfer function in s domain
$G_{P10}(z)$, $G_{P1}(z)$, $G_{P0}(z)$, $G_P(z)$ – system transfer functions in z domain
$G_{Cd}(z)$, $G_{C0}(z)$, $G_C(z)$ – controller transfer functions in z domain
$G_{CV}(z)$ – discrete voltage controller in z domain
P_{in} – input power
P_{L1}, P_{L2} – L_1 and L_2 inductor ESR power losses, respectively
P_{Ch} – C_H capacitor ESR power loss
P_{Cl} – C_L capacitor ESR power loss
P_{Snub} – RC snubber power loss
η – converter efficiency
Θ – junction temperature
P_{Condi} – conduction loss in i^{th} switch
P_{Swi} – conduction loss in i^{th} switch
ΔV – DC bus voltage variation

V_d, V_{d1}, V_{d2}, V_{dn},V_{dSC} – DC bus prescribed voltages
R_1, R_2, R_n – droop resistors emulated by converter control
V_{min}, V_{max} – DC bus voltage limits
$\pm I_{max}$ – converter current range
$\pm I_{lim}$ – maximum current range for linear operation
V_{RA} –voltage on R_A resistor
R_A – linear resistor implemented in ND-LRZD method
D_{Z1}, D_{Z2} -Zenner diodes implemented in ND-LRZD method
R_B – nonlinear resistor implemented in ND-NR method
V_{dA}, V_{dB} – current limited voltage sources
ΔV_{RA} – voltage droop for ND-LRZD method
I_{RB} – current through R_B resistor
V_{RB} –voltage on R_B resistor
k_v – gain coefficient for power implementation of ND-NR
α_V – power coefficient for power implementation of ND-NR method
k_1 – output gain coefficient for arctangent implementation of ND-NR
k_2 – input gain coefficient for arctangent implementation of ND-NR
R_{droop} – standard droop resistor
C_{bus} – DC bus capacitance
R_F – virtual filter resistor
C_F – virtual filter capacitor
ΔV_{RC} – virtual impedance voltage

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INTRODUCTION

Motivation

With the increase in pollution corelated to an increase in health risks, renewable resources are more often considered in place of the conventional energy sources. In order to achieve a sustainable, resilient and efficient energy production and utilization in the context of renewable energy, microgrids are more frequently used.

An important aspect in using renewable resources in microgrid applications is the storage of energy. Chemical battery storage is still widely used, but new technology advances in materials drive the development of supercapacitor storage further, allowing them to achieve better characteristics. In terms of energy storage, supercapacitors are approaching the conventional batteries, with additional benefits such as higher power density, longer life cycles and lower maintenance requirements.

Because, in terms of electrical characteristics, supercapacitors operate in a similar way as conventional capacitors, the stored energy is proportional to the squared voltage of the device, resulting in a large voltage variation.

Since DC distribution is most likely to be widely used in the future, as most sources and consumers are actually DC, the power converters for interfacing the supercapacitor to the voltage bus will also be a DC-DC converter. Because of the large variation of the supercapacitor voltage (corelated to the energy), and because of the relatively larger voltage on the DC bus, wide conversion ratio converters are desired.

A class of converters that can achieve wide voltage conversion ratios are the hybrid converters, which use switched inductor or capacitive cells in order to attain their performances.

The main purpose of this thesis is to develop and analyze new bidirectional hybrid topologies and to test them in supercapacitor storage for microgrid applications with different power sharing control strategies.

Thesis outline

This thesis is divided into 8 chapters, which are described in the following paragraphs.

Chapter 1 presents a brief introduction into the field of microgrids with DC distribution and energy storage elements with highlight on supercapacitor storage. An introduction to the unidirectional hybrid converters is also presented in this chapter.

An overview of nine, conventional or state-of-the-art, bidirectional DC-DC topologies is presented, with their respective analytical description. The topologies are chosen for having a wide voltage conversion ratio without the need of coupled inductors, a reduced number of components, and for requiring simple driving strategies for operation.

Parameters such as voltage conversion ratios, total inductor energy, total capacitor energy and total active switch stress are determined for these converters, to be further compared to the proposed topologies in chapter 6.

Chapter 2 presents a bidirectional hybrid switched capacitor converter, which was previously proposed in the scientific literature. This topology achieves a high conversion ratio at lower switch stress and requires small passive components. An

analytical description of the topology is presented for steady state, and a dynamic analysis is performed in order to design the continuous and discontinuous controllers for this topology. A Valley Current Mode Controller is tested for a fast implementation. Frequency response of the linearized converter model, and experimental results are used to test the stability of the design. Topology improvements are proposed for this converter in order to eliminate high frequency common voltage between the inputs.

Chapter 3 presents a different hybrid switched capacitor converter, which is able to achieve the same wide conversion ratio with reduced passive components, but it also features a common ground between the inputs. Analytical descriptions, and a dynamic analysis are performed to compare and to analyze the stability of this topology. Additionally, the dynamic analysis is used to evaluate the influence of different passive components in the stability of the converter. Simulation results and frequency responses of the linearized model are used to test the operation and the stability of the converter.

A multilevel structure is proposed as an improvement for this topology, which is achievable because the topology has common ground between inputs.

Chapter 4 presents a bidirectional hybrid switched inductor converter which, apart from the wide voltage conversion ratio, has the advantage of a lower system order of the linearized model. Steady state analysis is performed in order to present the main characteristics of this topology, and dynamic analysis is used for designing the digital controller and for analyzing the stability of the topology. The operation of the converter is analyzed with two prototypes built with conventional MOSFETs and GaN-FETs, and efficiency results are used for comparisons between the two.

An improved topology is presented which eliminates high frequency switching voltage between the two inputs, while introducing other advantages as well.

Chapter 5 presents a bidirectional hybrid switched inductor switched capacitor converter, a combination between the topology from chapter 2 and chapter 4, which achieves a much wider conversion ratio, and better overall performances. Analytical and dynamical analysis are performed in order to describe the main characteristics of the converter and to improve the hardware design and control architecture of the topology, respectively. Simulation results are used to demonstrate the functionality and performances of the converter.

An improved topology is proposed in the end, which eliminates high frequency switching voltage between inputs and reduces inductor voltage oscillations.

Chapter 6 presents a comparison between all presented topologies from the previous chapters, including the state-of-the-art topologies from chapter 1. The converters are compared in terms of step-up and step-down voltage conversion ratios, total inductor energy, total capacitor energy and total active switch stress, all presented in graphical plots with values normalized to the conventional bidirectional buck-boost converter.

Chapter 7 presents an application of bidirectional wide ratio converters: as an interface between a DC voltage bus in a microgrid and a supercapacitor used for storage. Three nonlinear power sharing strategies are presented, two of which are based on the nonlinear droop strategy, and one based on a nonlinear virtual impedance. The methods are analyzed based on the simulation and experimental results.

Chapter 8 presents the conclusions of this thesis, original contribution of the author and future work for the presented subjects.

Thesis objectives

The main objectives of the thesis are summarized as follows:

- To realize an overview of microgrid structures with emphasis on electrical storage elements
- To realize a review of conventional and state of the art bidirectional DC-DC converters presented in the scientific literature
- To propose new wide voltage conversion ratio bidirectional hybrid DC-DC topologies
- To analyze the operation of the proposed topologies
- To perform an analytical study for all the presented topologies in order to compare them
- To perform the dynamic analysis for the proposed topologies in order to optimize their design and to analyze their stability
- To validate the topologies in steady state and transient operation trough digital simulations
- To build and test experimental prototypes in order to validate the theoretical considerations
- To improve the structure of the proposed topologies in order to avoid eventual vulnerabilities
- To develop power sharing strategies, applied in microgrid structures, for supercapacitor storage application

1. A REVIEW OF BIDIRECTIONAL DC-DC CONVERTERS

1.1. Abstract

This chapter presents an introduction to microgrid structures, with highlight on the advantages of DC distribution, and common voltage levels suitable for these applications. A classification of storage elements is made with emphasis on chemical and electrostatic storage, in batteries and supercapacitors (SC) respectively, and their characteristics in terms of power and energy densities are presented.

As voltages in a DC microgrid have relatively large values compared to usual SC voltages, and because good SC energy utilization is advantageous, a wide voltage ratio bidirectional DC-DC converter is required as an interface to the DC bus.

State-of-the art converter topologies are presented together with their main operation modes and their corresponding steady state equations. These topologies will be used in the following chapters as comparison references for the hybrid structures presented in this work.

1.2. Introduction

Considered an important part in building the future of energy, microgrids are defined as a group of distributed, renewable or conventional resources and loads, interconnected such that they appear as a single unit [1]. The use of distributed resources, in combination to having the possibility to disconnect from the conventional grid, the microgrid is ideal to address concerns such as sustainability, resilience and energy efficiency. Because it can operate completely separated from the grid, the microgrid represents a good option for providing energy where the conventional AC grid is either not available or undependable [2].

Since most modern household consumers use DC voltage, as they include a front-end rectifier, and most renewable energies generate DC or variable frequency AC converted to DC with a power electronics converter, the DC microgrid presents a promising future. If operated at a variable-frequency, the resources that use AC machines can operate more efficiently by using power converters. In industrial applications, the rectifier/inverter motor drives can benefit in terms of efficiency and costs from a DC grid, by eliminating the rectifier. Conventional storage components are largely DC elements and can be used more conveniently in a DC grid, by using DC interface converters. The common power quality problems from AC grids are clearly reduced by using a DC bus, and stability issues are also easier to solve in DC. Because of the innovations in converter technology, the solid state transformer has gained popularity, showing that the initial factor for choosing AC systems (easy power distribution because of the conventional transformer) is no longer valid as power converters achieve good performances [3], [4]. Considering the advances in electric vehicles, their battery chargers can be simplified by using a DC bus, and they can be integrated effortlessly in a vehicle to grid (V2G) operation [5]–[7].

A block diagram of a typical DC microgrid using photovoltaic (PV), wind and hydro renewable resources, battery and supercapacitor as storage elements, with a single connection to the utility grid is presented in Fig. 1.1.

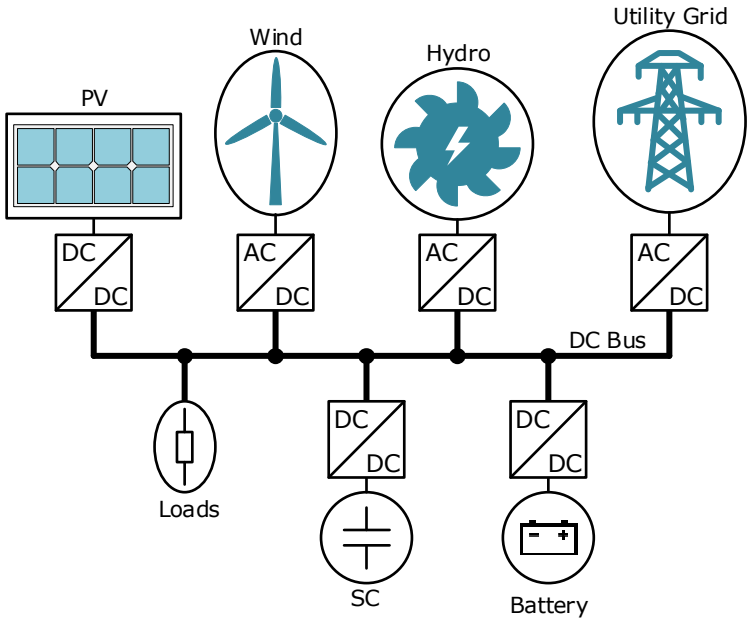

Fig. 1.1. DC Microgrid diagram with renewable resources (Photovoltaic-PV, Wind and Hydro energy), Supercapacitor (SC) and Battery storage, DC loads, and multiple power electronics converters (DC/DC and AC/DC)

Apart from the V2G operation in microgrids, a more important reason for utilizing electric vehicles is to reduce pollution in cities, mostly produced by internal combustion engines. By combusting fuel, the engine is producing power but is also eliminating pollutants in the air. Apart from the carbon dioxide and nitrogen oxides, other pollutants, more relevant from the health perspective, are produced: ultrafine particle matters (PM) which include solid particles and liquid droplets [8]. With sizes smaller than 2.5μm, the PM2.5 is considered to have the biggest influence on health as these carcinogenic particles are easily assimilated through the lungs affecting the nervous, respiratory, and cardiovascular system.

The different types of storage elements present in microgrids can be classified in different types [9]:

- Chemical
  - Chemical – Batteries
  - Electrochemical – Fuel cells
- Electrical
  - Magnetic – Superconducting magnetic energy storage (SMES)
  - Electrostatic – Supercapacitor (SC)
- Mechanical
  - Kinetic – Flywheel
  - Potential – Pumped hydro & compressed air

An ideal storage element has a low cost, large energy density, large power density, infinite life-cycle, small installation cost, and unity efficiency. As the ideal storage element does not exist, combinations between these storage elements are used in hybrid storage systems in order to profit from the larger range of benefits,

and a wider frequency spectrum of the generated energy [10]. The most common storage elements used for microgrid storage are chemical batteries, which have a limited life cycle, a reduced energy and power density, and a large impact on the environment. In order to increase the power density of the storage system, a supercapacitor (SC) can be used in addition to the conventional batteries, as it has a greater power density, a very large life cycle and reduced maintenance costs [11]. Similar to the microgrid, the electric vehicle can also benefit from SC storage for the same advantages.

The SC is popular because of its large power density and an increased energy density and it now has a great impact for microgrid storage, [12], [13], or electric vehicle storage [14], [15].

Supercapacitors can be characterized in three main types, as presented in [16], based on the charge storage techniques (Electrostatically – Helmholtz layer, Electrochemically – Faradaic charge transfer, and a hybrid combination of both [17]), with subtypes depending on the electrode materials:

- Electric double layer capacitors (EDLC) – Electrostatically
  - Activated carbon
  - Carbon nanotubes
  - Graphene
- Pseudocapacitors – Electrochemically
  - Conducting polymers
  - Metal oxides
- Hybrid – Electrochemically + Electrostatically

The most common supercapacitors, the electric double layer capacitors (EDLC), were initially commercialized in 1978 as energy storage solutions for backup power for computer memories [18]. The EDLC uses a higher surface area for the electrodes compared to the conventional capacitors (such as with activated carbon or carbon nanotubes), in order to achieve higher capacitances. In the same time period as the EDLCs, the pseudo capacitors were developed which are characterized by their use of oxidation-reduction reactions and intercalation mechanism for the energy storage [19]. Even if their storage is based on redox reactions, they present the same linear electric characteristics as the EDLC, a linear voltage-charge characteristic, and not a battery (faradaic) characteristic [16], [20]. In comparison to the EDLC, they achieve higher energy densities, but a lower power density. Hybrid capacitors are a combination between EDLC and pseudocapacitors, having two different electrodes, one specific for each of the two technologies.

An overview on the electrochemical and electrostatic energy storage technologies is summarized in Table 1.1, from the perspective of the energy density (specific energy, or massic energy) and the power density (specific power, or gravimetric power density). In the electrochemical category, the common Pb-Acid and Li-Ion batteries are found alongside modern types, such as Zn-Ion, Zn-Air, Na-Ion or the common RuO_2 pseudocapacitors. The improved batteries show larger energy or power densities, such as the Li-Ion with improved cathodes, or the Na-Ion which surpasses even the RuO_2 pseudocapacitors in terms of power density. The hybrid storage supercapacitors (which store energy both, electrostatically and electrochemically) show an improved power density over the electrochemical storage, with a detriment in energy storage compared to the electrochemical storage. Lastly, the electrostatic storage elements, the EDLCs, already achieve the highest power densities, even in commercially available products. Forecasts from 2016 regarding the energy density of the nitrogen doped electrodes of the EDLCs were exceeded by

graphene EDLCs which are approaching the common Li-Ion batteries in terms of energy densities, but with a much greater power density.

Table 1.1. Power and energy density characteristics of different storage elements

Storage technique	Energy Density (Wh/kg)	Power Density (kW/kg)
Electrochemically		
Pb-Acid battery	30	0.13
Li-Ion battery [21]	30-200	0.5
Zn-ion battery [22]	175.1 90	0.43 12
Zn-air battery [23]	68	0.045
Li-ion with amorphous mixed poly-cathode materials [24]	210	1.3
Na-ion battery [25]	364.2	6.75
RuO_2 pseudocapacitors [26]	0.6 - 8.5	0.5 – 5.8
Hybrid (Electrostatically + Electrochemically)		
Commercial activated carbon cathode & mesocarbon microbeads as anode [27]	92.3	5.5
Mesoporous/core–shell Nb_2O_5/carbon anodes [28]	15	18.51
Li-ion based on $LiNi_{0.5}Mn_{1.5}O_4$ & activated carbon [29]	50	1.1
Na-Ion [30]	201 76 50	0.285 8.5 16.5
$NiMoO_4$ alkaline carbon activated [31]	60.9 41.1	0.85 17
MnO_2/Bi_2O_3 pseudocapacitive electrodes [32]	11.3	0.35
Electrostatically (EDLC)		
Commercial available SCs [16], [20], [21]	2-20	3-40
2016 Forecast for nitrogen doped electrodes [33]	41	26
Partially exfoliated graphite foil electrode [34]	65.1	13
Graphene supercapacitor [35]	148.75	41
Polyethylenimine Low-cost nitrogen-doped activated carbon [36]	60.31	0.38
Cellulose-derived carbon nanofibers [37]	51	117
Patronite-reduced graphene oxide hybrids [38]	117	20.65

Even with so many different types of storage elements, a combination of high energy density storage element (battery) and a high power density storage element (supercapacitor) is used in order to benefit from both of their performances [39]. Because most SC technologies try to achieve a linear voltage-charge dependency, the energy stored in the element, W_C, varies proportionally to the squared voltage applied to the capacitance (C):

$$W_C = \frac{C \cdot V_C^2}{2}. \tag{1.1}$$

The SC energy dependency is presented in Fig. 1.2 with respect to the voltage, as percentage from their respective maximum values. From this graph, it is understandable that a wide voltage variation is required to achieve a good energy utilization of the SC. If the SC is charged up to 90% of its nominal voltage 20% of the energy capacity remains unused, and if the SC is discharged down to 30% of its nominal voltage approximately 10% of the energy is still available in the SC.

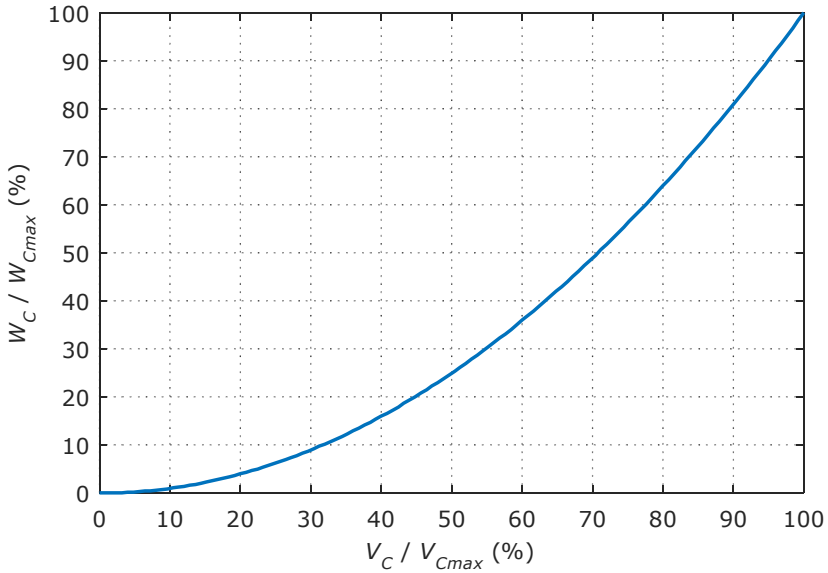

Fig. 1.2. SC energy as a function of capacitor voltage, both represented as percentage of maximum values

A better understanding of the capacitor energy utilization is achieved if the DC bus voltages of the microgrid are considered. Table 1.2 presents an overview of different DC voltage levels with their corresponding standards and applications [40]. The largest voltage considered, 1500V, is the highest limit for low voltage DC distribution according to IEC60038, which can be divided for 750V bipolar distribution, a conventional voltage for tramway power systems. With voltages above 565V a direct interconnection to a three phase 400V AC grid can be achieved by using an inverter.

Table 1.2. Voltage levels, standards, and applications of low voltage DC distribution [40]

Voltage level (V)	**Standards & Codes**	**Applications**
1500	LVdc limit, IEC60038	PV systems, Traction
750		Trams power systems
≥565V		Direct interconnection to 3ph 400V AC grid
400	Telecom DC limit ETSI EN 300 132-3-1	EV, Data centers
380	Emerge Alliance (Data/Telecom std.)	Data centers
325		Direct connection of AC loads with rectifier
230		Compatibility to AC resistive load
120	Limit of SELV and PELV, IEC61140	
75	Lower limit of EU LVD 2014/35/EU	
50	IEEE 802.3bt IEEE 802.3bu	Power over Ethernet
48		Telecom, Trucks, Rural PV systems
24	Emerge Alliance (Occupied Space std.)	Lighting systems
12		Automotive, Lighting
5		Electronics

The ETSI EN 300 132-3-1 standard for telecommunications and datacom equipment sets their maximum voltage at 400V, which is close to the 380V standard for data centers set by Emerge Alliance. These two voltages are close to 375V, half of 750V, which can be used for bipolar distribution yet again.

To achieve compatibility for AC loads, the 325V is taken into account for direct connection of an AC load with internal rectifier (most electronic products), and the 230V voltage is considered for compatibility to AC resistive loads. On the lower voltage side, the international standard for protection against electric shock, IEC61140, sets the limit at 120V, and the European Low Voltage directive, EU LVD 2014/35/EU, sets the lower DC limit at 75V. The 50V limit is considered for power over ethernet, by IEEE 802.3bt and IEEE 802.3bu standards, which is close to the 48V used in the automotive and telecom industry, and even small rural PV systems. For lighting systems, the Emerge Alliance sets the voltage to 24V, while the 12V and 5V are commonly used in automotive, lighting, and low power electronics.

Because the voltage range between 375V and 400V is covered by standards and are commonly used in various applications, this range is also considered for the applications presented in this work. A commercially available SC is used as an example for the required voltage range variation versus its stored energy, the BMOD0063-P125-B04 produced by Maxwell with a capacitance of 63F, maximum voltage of 125V, peak currents of 1.9kA, power density of 1.7kw/kg and energy density of 2.3Wh/kg. Considering the voltage conversion ratio of the converter, V_L / V_H, as a ratio between the low voltage output connected at the SC, V_L, and the high voltage output connected at the DC bus, V_H, the energy of the SC is represented as a function of the voltage conversion ratio in Fig. 1.3.

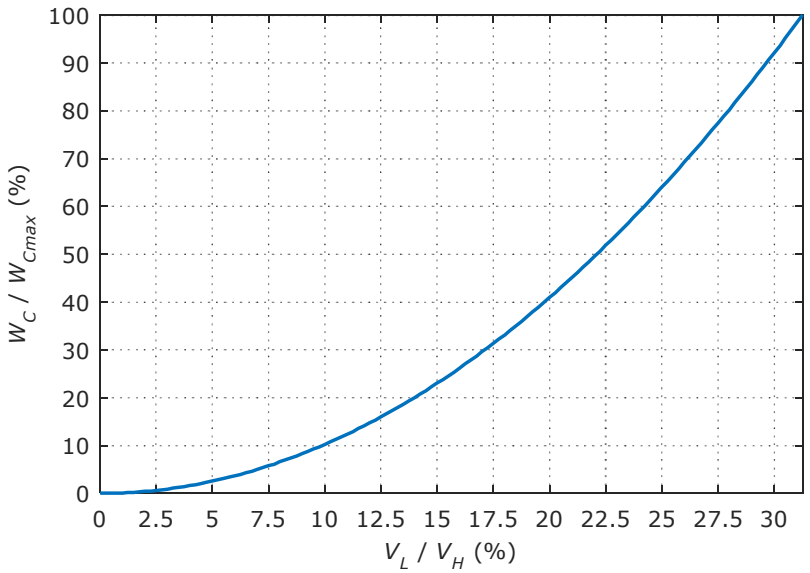

Fig. 1.3. Energy stored in the BMOD0063-P125-B04 SC (63F, 125V, 1900A, 1.7kW/kg, 2.3Wh/kg) as a function of the voltage conversion ratio (V_L / V_H), for V_H = 400V and V_L = 0-125V

In order to achieve at least 90% energy utilization of the SC, a wide conversion ratio, between 10% and at least 31.25%, is required. A greater energy utilization can be achieved by having a wider conversion ratio, therefore wide conversion ratio converters are usually desired for SC storage applications.

As wide ratio converters are desired, the unidirectional hybrid converters developed in [41], [42], are considered as an inspiration for bidirectional topologies, because of their advantages in terms of conversion ratio, number of switches, active and passive component size, and efficiency. The hybrid nature of these converters comes from using switched capacitor or switched inductor cells in their structure, which help achieve the wide voltage conversion ratio. The switching cells are either capacitive, in Fig. 1.4, or inductive, in Fig. 1.5, and by connecting the two identical capacitors or inductors in series, a voltage doubling/halving and a current doubling/halving is achieved, respectively.

In the case of switched capacitive cells, the two capacitors are charged in series and are discharged in parallel, for step-down operation in Fig. 1.4.a, or vice-versa for step-up operation in Fig. 1.4.b,c.

For the switched inductor cells, the two inductors are charged in series, and discharged in parallel for step-down operation, in Fig. 1.5.a,b, and vice-versa for step-up operation in Fig. 1.5.c.

This work focuses on hybrid bidirectional wide ratio converters, with a non-isolated structure, which do not use coupled inductors for achieving their wide conversion ratio. By using bidirectional hybrid switched capacitor or inductive cells, the benefits of hybrid unidirectional converters can be extended for bidirectional operation, with the new developed topologies presented in chapters 2 to 5.

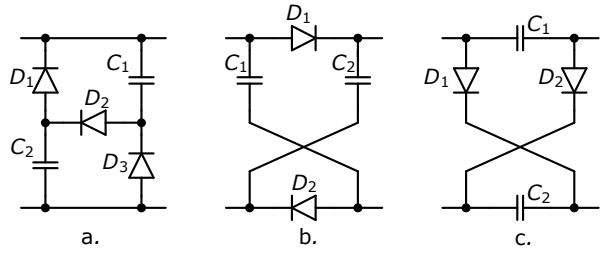

Fig. 1.4. Unidirectional switched capacitive cells,
for step-down (a.) and step-up operation (b, c.) [41], [42]

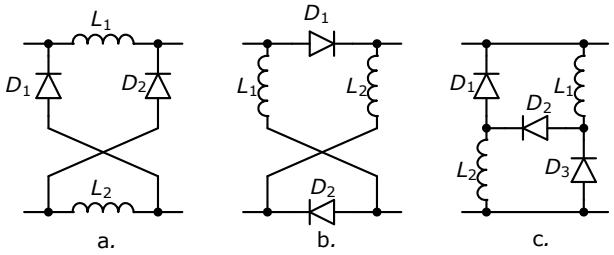

Fig. 1.5. Unidirectional switched inductive cells,
for step-down (a, b.) and step-up operation (c.) [41], [42]

The hybrid topologies presented in this work are compared to other conventional or state-of-the art topologies, with similar characteristics, such as (a.) wide conversion ratio achieved without the use of coupled inductors, (b.) reduced number of active components (≤6), (c.) non-isolated topologies, (d.) with simple driving schemes (only two equivalent switching states, and without multiphase operation) as most two-switching-states converters can be upgraded into multiphase or multilevel topologies.

1.3. State-of-the-art Bidirectional DC-DC Converters

1.3.1. The conventional bidirectional buck/boost converter (CBBB)

One of the most utilized bidirectional DC-DC converter is the Conventional Bidirectional Buck/Boost (CBBB) converter, shown in Fig. 1.6. Most applications in which this topology is employed are either for storage in microgrid applications, [43]–[47], or transportation [48], [49].

This chapter is used as a template, in terms of steady state analysis in continuous conduction mode for each converter from the following chapters. The schematic has two voltage sources at the two inputs, a lower voltage source, V_L, represented in the left side of the converter, and a higher voltage source, V_H, represented in the right of the converter. The two sources are used to show that the converter has a bidirectional operation and it can direct the current flow to or from each one of the two.

The current flow in the schematic illustrates a step-down operation for positive currents, i_{L1}, I_L, I_H >0, and a step-up operation for negative currents, i_{L1}, I_L, I_H <0. The two operation modes are considered identical, the only difference being the sign of the currents.

The analysis of the converters is done under a few assumptions:

- all components are ideal,
- the capacitors are large enough to consider a constant voltage,
- the converter operates in steady state,
- the converter operates in continuous conduction mode (CCM).

In order to analyze the CBBB converter in steady state operation, the equivalent schematics for the two switching intervals, t_{on} and t_{off}, are presented in Fig. 1.7. During the t_{on} switching interval, the inductor is connected between the two voltage sources, therefore the inductor current is increasing. During the t_{off} interval, the inductor is connected in parallel to the low voltage source (V_L), and the inductor current is decreasing.

Based on the two equivalent schematics, the main theoretical waveforms of the CBBB are presented in Fig. 1.8: inductor voltage, v_{L1}, and current, i_{L1}; switch voltages, v_{S1}, v_{S2}, and currents, i_{S1}, i_{S2}; and the ripple voltages on the input capacitors Δv_{CH} and Δv_{CL}. All waveforms are scaled relatively to each other, except for the ripple voltage on capacitors. The ripple voltage is approximated by considering an ideal capacitor and by integrating the capacitor current.

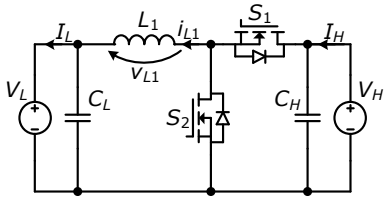

Fig. 1.6. Conventional bi-directional buck/boost converter (CBBB)

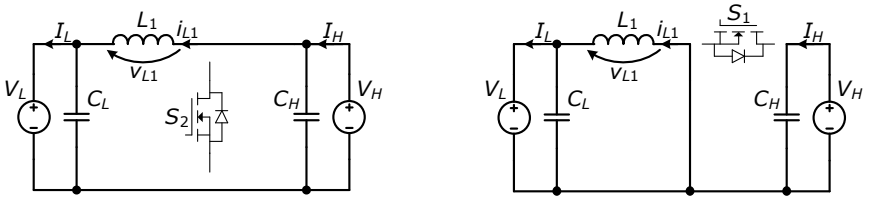

Fig. 1.7. CBBB equivalent schematics during
t_{on} (S_1 is ON, S_2 is OFF - left); and t_{off} (S_1 is OFF, S_2 is ON - right)

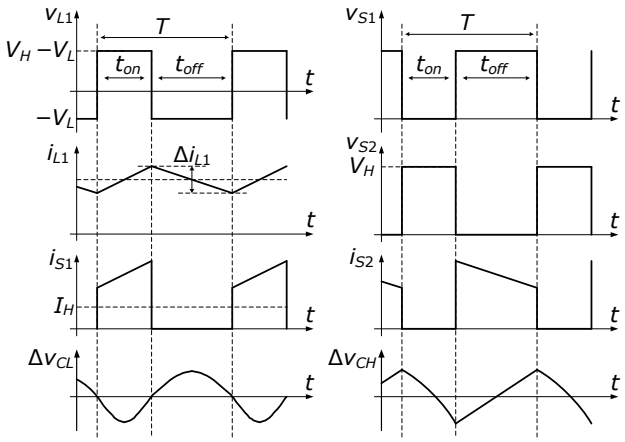

Fig. 1.8. Main theoretical waveforms of the CBBB: L_1 inductor voltages and currents (v_{L1}, i_{L1});
S_1 and S_2 switch voltages and currents (v_{S1}, v_{S2}, i_{S1}, i_{S2});
ripple voltages on the input capacitors (Δv_{CH} and Δv_{CL})

Because bidirectional converters operate in either step-up and step-down mode, a duty cycle proportional to the step-down conversion ratio (V_L / V_H), D, and a duty cycle proportional to the step-up conversion ratio (V_H / V_L), D', are defined:

$$D = \frac{t_{on}}{T},\ D' = \frac{t_{off}}{T}, \tag{1.2}$$

where T is the switching period, and $T = t_{on} + t_{off}$.

From Fig. 1.7, the inductor voltages are expressed for the two switched intervals:

$$\begin{aligned} t_{on} &: v_{L1} = V_H - V_L, \\ t_{off} &: v_{L1} = -V_L. \end{aligned} \tag{1.3}$$

Because the converter is operating in steady state, the averaged inductor voltage on one switching period is 0. Therefore, by applying the volt-second balance, the following is written:

$$\langle v_{L1} \rangle = D \cdot (V_H - V_L) + (1 - D) \cdot (-V_L) = 0. \tag{1.4}$$

From (1.4), the steady state relation between the two voltages is represented in step-down form:

$$V_L = V_H \cdot D, \tag{1.5}$$

or in step-up form:

$$V_H = V_L \cdot \frac{1}{1 - D}. \tag{1.6}$$

As all components are considered ideal, unity efficiency is considered, therefore only one current, I_L, on the low voltage side, is chosen for characterizing the operation point of the converter. The I_L current is equal to the average value of the inductor current, I_{L1}:

$$I_L = I_{L1}. \tag{1.7}$$

Usually, in the design of a converter, a maximum inductor ripple current, Δi_{L1}, is chosen as a percentage, r_i, of the nominal inductor current:

$$r_i = \frac{\Delta i_{L1}}{I_{L1}}. \tag{1.8}$$

Recommended values for the ripple percentage are between 20% to 50%, as suggested by application notes for low power converters [50], but this value can be optimized, as shown in [51]. The ripple percentage for this work is considered constant for all studied converters, so that an objective comparison can be made.

In order to design the inductor based on r_i, the voltage-current dependency for an ideal inductor is used:

$$v_{L1} = L_1 \cdot \frac{di_{L1}}{dt}. \tag{1.9}$$

In a discretized form, the following inductor relationship is true:

$$L_1 = \frac{v_{L1} \cdot \Delta t}{\Delta i_{L1}}, \tag{1.10}$$

where Δt is the time interval on which the current ripple is calculated. By considering $\Delta t = t_{on}$, and using (1.2), (1.5), (1.7) and (1.8), into (1.10), the inductor value is calculated:

$$L_1 = \frac{V_L \cdot (V_H - V_L)}{r_i \cdot f \cdot I_L \cdot V_H}, \tag{1.11}$$

where f is the switching frequency.

In order to compare the performances of any converter in terms of inductor requirements, the total inductor energy is used. This measure is calculated as the sum of the energy for each inductor from the circuit:

$$W_{LTot} = \sum W_{Li} = W_{L1}. \tag{1.12}$$

As the CBBB has only one inductor, the inductor energy is calculated with:

$$W_{L1} = \frac{L_1 \cdot I_{L1}^{\ 2}}{2}, \tag{1.13}$$

and it is equal to the total inductor energy:

$$W_{LTot} = \frac{I_L \cdot V_L \cdot (V_H - V_L)}{2 \cdot r_i \cdot f \cdot V_H}. \tag{1.14}$$

In this expression, the total inductor energy is only dependent on the input voltages, the current on the low voltage side, inductor ripple current percentage, and the switching frequency. These values are corelated to the input power, conversion ratio, inductor ripple percentage and switching frequency.

In order to calculate the required capacitances, the inductor current is described by a time function for the two switching intervals, as follows:

$$i_{L1}(t) = \begin{cases} I_{L1} + \Delta i_{L1} \cdot (t / t_{on} - 1/2), & t \in [0, t_{on}) \\ I_{L1} + \Delta i_{L1} \cdot ((T - t) / t_{off} - 1/2), & t \in [t_{on}, T] \end{cases} \tag{1.15}$$

Similar to the inductor ripple current percentage, r_i, a capacitor ripple voltage percentage is defined:

$$r_v = \frac{\Delta v_{CH}}{V_{CH}} = \frac{\Delta v_{CL}}{V_{CL}}. \tag{1.16}$$

The initial theoretical assumptions consider constant capacitor voltages therefore, a small voltage ripple percentage of approximately 2% is used in designs. Because the calculations are performed considering ideal capacitors, without an Equivalent Series Resistor (ESR), the actual ripple voltage will have larger values. If the ESR is more significant, i.e. for electrolytic capacitors, the design should be performed by using the RMS current of each capacitor. Nevertheless, the following method for calculating the capacitance is still useful for comparing different topologies in terms of capacitor requirements.

In order to calculate the capacitances, currents from each capacitor are required as time functions. Therefore, the currents from the two capacitors are expressed:

$$i_{CL} = i_{L1} - I_L, \tag{1.17}$$

$$i_{CH} = I_H - i_{S1}. \tag{1.18}$$

Starting from the voltage-current dependency of an ideal capacitor,

$$i_C = C \cdot \frac{dv_C}{dt}, \tag{1.19}$$

the integral form of the relationship can be expressed for each of the two capacitors, during a complete charge or discharge cycle. The charge or discharge cycle of each capacitor is observed in Fig. 1.8: C_L charges during $t_{on}/2$ to $t_{on}+t_{off}/2$, and discharges during $t_{off}/2$ to $T+t_{on}/2$; C_H charges during t_{off} and discharges during t_{on}. Based on the inductor current time function from (1.15), and the capacitor currents from (1.17) and (1.18) the integral form of relation (1.19) is expressed in order to calculate the two capacitors:

$$C_L = \frac{1}{\Delta v_{CL}} \int_{t_{on}/2}^{t_{on}+t_{off}/2} (i_{L1} - I_L)dt = \frac{1}{-\Delta v_{CL}} \int_{t_{on}+t_{off}/2}^{T+t_{on}/2} (i_{L1} - I_L)dt, \tag{1.20}$$

$$C_H = \frac{1}{\Delta v_{CH}} \int_{t_{on}}^{T} I_H\, dt = \frac{1}{-\Delta v_{CH}} \int_{0}^{t_{on}} (I_H - i_{L1})dt. \tag{1.21}$$

The two capacitances are calculated as:

$$C_L = \frac{r_i \cdot I_L}{8 \cdot r_v \cdot f \cdot V_L}, \tag{1.22}$$

$$C_H = \frac{I_L \cdot V_L \cdot (V_H - V_L)}{r_v \cdot f \cdot V_H^{\,3}}. \tag{1.23}$$

These values may not be the actual ones for the capacitors used for the converter, as they do not include the ESR. However, these values can be successfully used for comparing different converters designed with the same procedure.

In order to make the comparison, the capacitor energies are calculated:

$$W_C = \frac{C \cdot V_C^{\,2}}{2}, \tag{1.24}$$

and added for all capacitors in a converter in order to calculate the total capacitor energy:

$$W_{CTot} = \sum W_{Ci} = W_{CL} + W_{CH}. \tag{1.25}$$

The energy for each of the two capacitors is:

$$W_{CH} = \frac{I_L \cdot V_L \cdot (V_H - V_L)}{2 \cdot r_v \cdot f \cdot V_H}, \tag{1.26}$$

$$W_{CL} = \frac{r_i \cdot I_L \cdot V_L}{16 \cdot r_v \cdot f}, \tag{1.27}$$

The total capacitor energy results as:

$$W_{CTot} = \frac{I_L \cdot V_L \cdot (8 \cdot V_H - 8 \cdot V_L + r_i \cdot V_H)}{16 \cdot r_v \cdot f \cdot V_H}. \tag{1.28}$$

The total capacitor energy for a converter is another metric used in this work for comparison to other converters, apart from the total inductor energy and the conversion ratio.

In order to characterize a converter in terms of active switch stress, the total active switch stress is used [52], which is calculated as:

$$S = \sum_j V_{Sj} \cdot I_{Sj}, \tag{1.29}$$

where V_{Sj} is the voltage stress on the j^{th} switch, and I_{Sj} is usually the peak or RMS current on the switch. Since r_i has low values, the averaged switch current during its conduction time is used in place of the peak current, in order to simplify the analysis. Therefore, the voltages and current switch stresses on the two transistors are:

$$V_{S1} = V_{S2} = V_H, \tag{1.30}$$

$$I_{S1} = I_{S2} = I_{L1} = I_L. \tag{1.31}$$

The total active switch stress for the CBBB is:

$$S = V_{S1} \cdot I_{S1} + V_{S2} \cdot I_{S2} = 2 \cdot I_L \cdot V_H. \tag{1.32}$$

1.3.2. The bidirectional Switched-Quasi-Z-Source converter (BSQZ)

The bidirectional Switched-Quasi-Z-Source (BSQZ) converter [53], presented in Fig. 1.9, uses a switched capacitive and inductive network (C_1, C_2 and L_2) that, similar to hybrid converters, helps achieve a wider conversion ratio.

The main and the most important difference when compared to the hybrid converters, is that the two capacitors from the network are charged/discharged directly from the input capacitor. The operation of the converter is explained by the two equivalent states, for t_{on} switching period in Fig. 1.10 (S_1 - OFF, S_2, S_3 - ON) and t_{off} switching period in Fig. 1.11 (S_1 - ON, S_2, S_3 - OFF). As observed in Fig. 1.10, during t_{on} the two capacitors are connected in series and, together, in parallel to the input capacitor, period in which one capacitor chargers the other, and large current spikes might appear which depend on the parasitic resistances of the circuit and are difficult to control. During t_{off}, the capacitors are connected in series through L_2 inductor, therefore one capacitor charges the other with a constant current. The main equations of the BSQZ are summarized in Table 1.3.

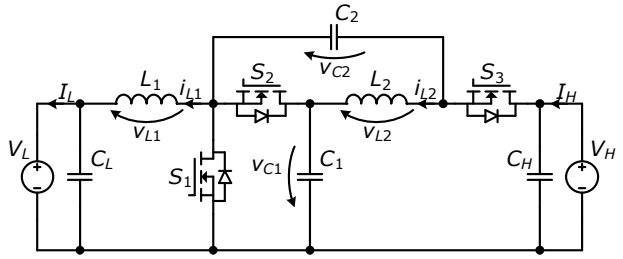

Fig. 1.9. Switched-Quasi-Z-Source bi-directional (BSQZ) converter proposed in [53]

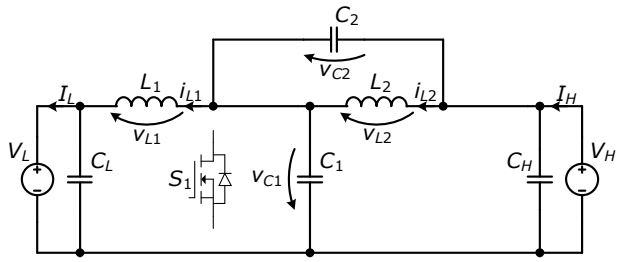

Fig. 1.10. Equivalent schematic during t_{on} of the BSQZ (S_1 is turned OFF, S_2 and S_3 are turned ON)

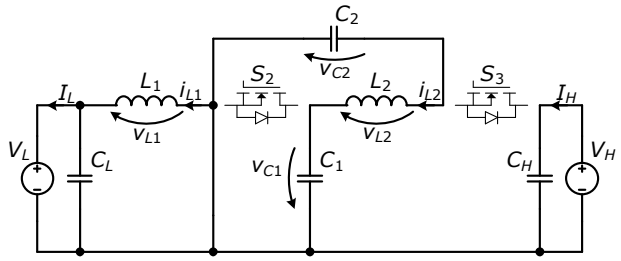

Fig. 1.11. Equivalent schematic during t_{off} of the BSQZ (S_1 is turned ON, S_2 and S_3 are turned OFF)

Table 1.3. Main equations of the BSQZ

Conversion ratio	**Active devices**
$v_{L1}(t_{on}) = V_{C1} - V_L$, $v_{L1}(t_{off}) = -V_L$, $v_{L2}(t_{on}) = V_{C2}$, $v_{L2}(t_{off}) = V_{C2} - V_{C1}$, $V_{C1} = \frac{V_H + V_L}{2}, V_{C2} = \frac{V_H - V_L}{2}$, $V_L = V_H \cdot \frac{D}{2-D}, V_H = V_L \cdot \frac{1+D'}{1-D'}$,	$V_{S1} = V_{S2} = V_{C1}$, $V_{S3} = V_H - V_{C2}$, $I_{S1} = I_{L1} + I_{L2}$, $I_{S2} = I_{S3} = \frac{I_{L1} + I_{L2}}{2}$, $S = \sum_{j=1}^{4} V_{Sj} \cdot I_{Sj} = \frac{I_L \cdot (V_H + V_L)^2}{V_H}$
Inductors	**Capacitors**
$I_{L1} = I_L$, $I_{L2} = I_H$, $L_1 = \frac{V_L \cdot (V_H - V_L)}{r_i \cdot f \cdot I_L \cdot (V_H + V_L)}$, $L_2 = \frac{V_H \cdot (V_H - V_L)}{2 \cdot r_i \cdot f \cdot I_L \cdot V_L}$, $W_{L1} = \frac{I_L \cdot V_L \cdot (V_H - V_L)}{2 \cdot r_i \cdot f \cdot (V_H + V_L)}$, $W_{L2} = \frac{I_L \cdot V_L \cdot (V_H - V_L)}{4 \cdot r_i \cdot f \cdot V_H}$, $W_{LTot} = \frac{I_L \cdot V_L \cdot (3 \cdot V_H^2 - 2 \cdot V_H \cdot V_L - V_L^2)}{4 \cdot r_i \cdot f \cdot V_H \cdot (V_H + V_L)}$.	$i_{CL} = i_{L1} - I_L$, $i_{CH} = I_H - i_{S3}$, $i_{C1}(t_{off}) = -i_{C2}(t_{off}) = i_{L2}$ $C_L = \frac{1}{\Delta v_{CL}} \int_{t_{on}/2}^{t_{on}+t_{off}/2} i_{CL} dt = \frac{r_i \cdot I_L}{8 \cdot r_v \cdot f \cdot V_L}$, $C_H = \frac{-1}{\Delta v_{CH}} \int_0^{t_{on}} i_{CH} dt = \frac{I_L \cdot V_L \cdot (V_H - V_L)}{r_v \cdot f \cdot V_H^2 \cdot (V_H + V_L)}$, $C_1 = \frac{1}{\Delta v_{C1}} \int_{t_{on}}^{T} i_{C1} dt = \frac{2 \cdot I_L \cdot V_L \cdot (V_H - V_L)}{r_v \cdot f \cdot V_H \cdot (V_H + V_L)^2}$, $C_2 = \frac{-1}{\Delta v_{C2}} \int_{t_{on}}^{T} i_{C2} dt = \frac{2 \cdot I_L \cdot V_L}{r_v \cdot f \cdot V_H \cdot (V_H + V_L)}$, $W_{CL} = \frac{r_i \cdot I_L \cdot V_L}{16 \cdot r_v \cdot f}, W_{CH} = \frac{I_L \cdot V_L \cdot (V_H - V_L)}{2 \cdot r_v \cdot f \cdot (V_H + V_L)}$, $W_{C1} = \frac{I_L V_L (V_H - V_L)}{4 r_v \cdot f \cdot V_H}, W_{C2} = \frac{I_L V_L (V_H - V_L)^2}{4 r_v \cdot f \cdot V_H \cdot (V_H + V_L)}$, $W_{CTot} = \frac{I_L \cdot V_L \cdot (V_H \cdot (1 + r_i/16) - V_L (1 - r_i/16))}{r_v \cdot f \cdot (V_H + V_L)}$.

1.3.3. The conventional bidirectional quadratic converter (CBQ)

The conventional bidirectional quadratic converter (CBQ), is a very popular wide ratio converter, as it uses two cascaded CBBB converters in order to achieve the combined conversion ratios of the two [54]. The operation of the CBQ is explained by the two equivalent switching states, for t_{on} switching period in Fig. 1.13 (S_1, S_3 - OFF, S_2, S_4 - ON) and t_{off} switching period in Fig. 1.14 (S_1, S_3 - ON, S_2, S_4 - OFF), and it is identical to the CBBB when viewed from the perspective of the two converters within the CBQ. The main equations of the CBQ are summarized in Table 1.4.

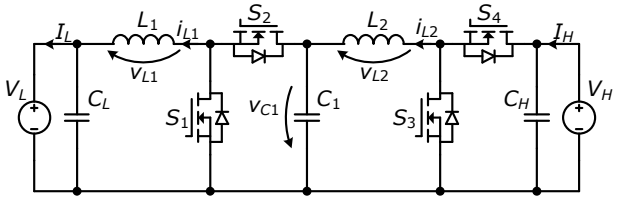

Fig. 1.12. Conventional bi-directional quadratic converter (CBQ) [54]

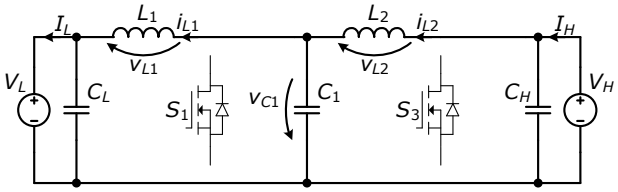

Fig. 1.13. Equivalent schematic during t_{on} of the CBQ (S_1 and S_3 are turned OFF, S_2 and S_4 are turned ON)

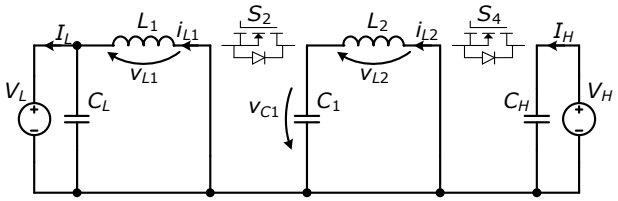

Fig. 1.14. Equivalent schematic during t_{off} of the CBQ (S_1 and S_3 are turned ON, S_2 and S_4 are turned OFF)

Table 1.4. Main equations of the CBQ

Conversion ratio	**Active devices**
$v_{L1}(t_{on}) = V_{C1} - V_L$, $v_{L1}(t_{off}) = -V_L$, $v_{L2}(t_{on}) = V_H - V_{C1}$, $v_{L2}(t_{off}) = -V_{C1}$, $V_{C1} = \sqrt{V_H \cdot V_L}$, $V_L = V_H \cdot D^2$, $V_H = V_L \cdot \frac{1}{(1-D')^2}$.	$V_{S1} = V_{S2} = V_{C1}$, $V_{S3} = V_{S4} = V_H$, $I_{S1} = I_{S2} = I_{L1}$, $I_{S3} = I_{S4} = I_{L2}$, $S = \sum_{j=1}^{4} V_{Sj} \cdot I_{Sj} = 4 \cdot I_L \cdot \sqrt{V_H \cdot V_L}$
Inductors	**Capacitors**
$I_{L1} = I_L$, $I_{L2} = D \cdot I_{L1}$, $L_1 = \frac{V_L \cdot (\sqrt{V_H} - \sqrt{V_L})}{r_i \cdot f \cdot I_L \cdot \sqrt{V_H}}$, $L_2 = \frac{V_H - \sqrt{V_H \cdot V_L}}{r_i \cdot f \cdot I_L}$,	$i_{CL} = i_{L1} - I_L$, $i_{CH} = I_H - i_{S3}$, $i_{C1} = i_{L2} - i_{S2}$ $C_L = \frac{1}{\Delta v_{CL}} \int_{t_{on}/2}^{t_{on}+t_{off}/2} i_{CL} dt = \frac{r_i \cdot I_L}{8 \cdot r_v \cdot f \cdot V_L}$,

$W_{L1} = W_{L2} = \frac{I_L \cdot V_L \cdot (\sqrt{V_H} - \sqrt{V_L})}{2 \cdot r_i \cdot f \cdot \sqrt{V_H}}$, $W_{LTot} = \frac{I_L \cdot V_L \cdot (\sqrt{V_H} - \sqrt{V_L})}{r_i \cdot f \cdot \sqrt{V_H}}$.	$C_H = \frac{-1}{\Delta v_{CH}} \int_0^{t_{on}} i_{CH} dt = \frac{I_L \cdot V_L \cdot (\sqrt{V_H} - \sqrt{V_L})}{r_v \cdot f \cdot V_H^{5/2}}$, $C_1 = \frac{-1}{\Delta v_{C1}} \int_0^{t_{on}} i_{C1} dt = \frac{I_L \cdot (\sqrt{V_H} - \sqrt{V_L})}{r_v \cdot f \cdot V_H^{3/2}}$, $W_{CL} = \frac{r_i \cdot I_L \cdot V_L}{16 \cdot r_v \cdot f}$, $W_{CH} = \frac{I_L \cdot V_L \cdot (\sqrt{V_H} - \sqrt{V_L})}{2 \cdot r_v \cdot f \cdot \sqrt{V_H}}$, $W_{C1} = \frac{I_L \cdot V_L \cdot (\sqrt{V_H} - \sqrt{V_L})}{2 \cdot r_v \cdot f \cdot \sqrt{V_H}}$, $W_{CTot} = \frac{I_L \cdot V_L \cdot (\sqrt{V_H} \cdot (1 + r_i / 16) - \sqrt{V_L})}{r_v \cdot f \cdot \sqrt{V_H}}$.

1.3.4. The bidirectional quadratic converter (BQ1)

Having a different structure, as shown in Fig. 1.15, the bidirectional quadratic (BQ1) converter, proposed in [55], can achieve the same quadratic conversion ratio as the CBQ. The BQ1 uses a different layout for the same components as the CBQ, but it achieves the same values for the components, as presented in Table 1.5.

The operation of the BQ1 is explained by the two equivalent switching states, for t_{on} switching period in Fig. 1.16 (S_1, S_3 - OFF, S_2, S_4 - ON) and t_{off} switching period in Fig. 1.17 (S_1, S_3 - ON, S_2, S_4 - OFF), and by comparing the equivalent schematics to the CBQ, the same operation is observed from the perspective of the passive components.

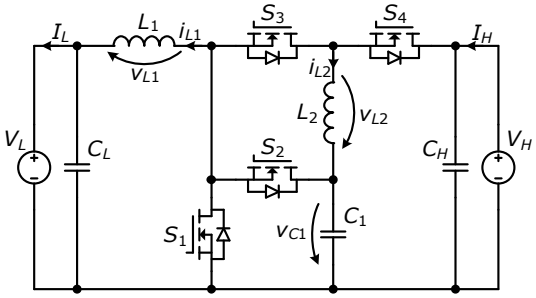

Fig. 1.15. The bi-directional quadratic converter (BQ1) proposed in [55]

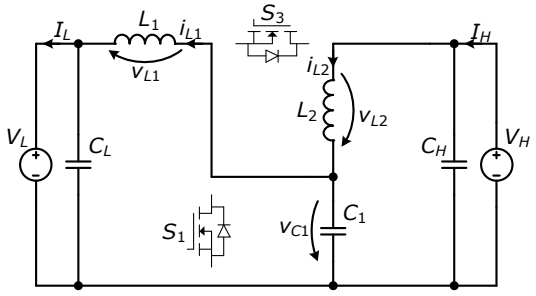

Fig. 1.16. Equivalent schematic during t_{on} of the BQ1 (S_1 and S_3 are turned OFF, S_2 and S_4 are turned ON)

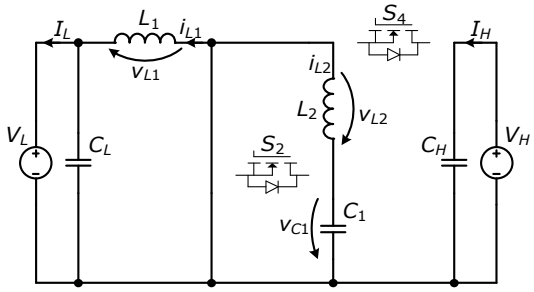

Fig. 1.17. Equivalent schematic during t_{off} of the BQ1 (S_1 and S_3 are turned ON, S_2 and S_4 are turned OFF)

Table 1.5. Main equations of the BQ1

Conversion ratio	**Active devices**
$v_{L1}(t_{on}) = V_{C1} - V_L$, $v_{L1}(t_{off}) = -V_L$, $v_{L2}(t_{on}) = V_H - V_{C1}$, $v_{L2}(t_{off}) = -V_{C1}$, $V_{C1} = \sqrt{V_H \cdot V_L}$, $V_L = V_H \cdot D^2$, $V_H = V_L \cdot \frac{1}{(1-D')^2}$.	$V_{S1} = V_{S2} = V_{C1}$, $V_{S3} = V_H - V_{C1}$, $V_{S4} = V_H$, $I_{S1} = I_{L1} + I_{L2}$, $I_{S2} = I_{L1}$, $I_{S3} = I_{S4} = I_{L2}$, $S = \sum_{j=1}^{4} V_{Sj} \cdot I_{Sj} = 4 \cdot I_L \cdot \sqrt{V_H \cdot V_L}$
Inductors	**Capacitors**
$I_{L1} = I_L$, $I_{L2} = D \cdot I_{L1}$, $L_1 = \frac{V_L \cdot (\sqrt{V_H} - \sqrt{V_L})}{r_i \cdot f \cdot I_L \cdot \sqrt{V_H}}$, $L_2 = \frac{V_H - \sqrt{V_H \cdot V_L}}{r_i \cdot f \cdot I_L}$, $W_{L1} = W_{L2} = \frac{I_L \cdot V_L \cdot (\sqrt{V_H} - \sqrt{V_L})}{2 \cdot r_i \cdot f \cdot \sqrt{V_H}}$, $W_{LTot} = \frac{I_L \cdot V_L \cdot (\sqrt{V_H} - \sqrt{V_L})}{r_i \cdot f \cdot \sqrt{V_H}}$.	$i_{CL} = i_{L1} - I_L$, $i_{CH} = I_H - i_{S4}$, $i_{C1} = i_{L2} - i_{S2}$ $C_L = \frac{1}{\Delta v_{CL}} \int_{t_{on}/2}^{t_{on}+t_{off}/2} i_{CL} dt = \frac{r_i \cdot I_L}{8 \cdot r_v \cdot f \cdot V_L}$, $C_H = \frac{-1}{\Delta v_{CH}} \int_0^{t_{on}} i_{CH} dt = \frac{I_L \cdot V_L \cdot (\sqrt{V_H} - \sqrt{V_L})}{r_v \cdot f \cdot V_H^{5/2}}$, $C_1 = \frac{-1}{\Delta v_{C1}} \int_0^{t_{on}} i_{C1} dt = \frac{I_L \cdot (\sqrt{V_H} - \sqrt{V_L})}{r_v \cdot f \cdot V_H^{3/2}}$, $W_{CL} = \frac{r_i \cdot I_L \cdot V_L}{16 \cdot r_v \cdot f}$, $W_{CH} = \frac{I_L \cdot V_L \cdot (\sqrt{V_H} - \sqrt{V_L})}{2 \cdot r_v \cdot f \cdot \sqrt{V_H}}$, $W_{C1} = \frac{I_L \cdot V_L \cdot (\sqrt{V_H} - \sqrt{V_L})}{2 \cdot r_v \cdot f \cdot \sqrt{V_H}}$, $W_{CTot} = \frac{I_L \cdot V_L \cdot (\sqrt{V_H} \cdot (1 + r_i / 16) - \sqrt{V_L})}{r_v \cdot f \cdot \sqrt{V_H}}$.

1.3.5. The bidirectional quadratic converter (BQ2)

Another bidirectional quadratic converter (BQ2) proposed in [56], shows that a different topology can be used to achieve the quadratic conversion ratio, with the topology presented in Fig. 1.18.

The operation of the BQ2 is explained by the two equivalent switching states, for t_{on} switching period in Fig. 1.19 (S_1, S_2 - OFF, S_3, S_4 - ON) and t_{off} switching period in Fig. 1.20 (S_1, S_2 - ON, S_3, S_4 - OFF). In the case of the BQ2, the equivalent schematics are different compared to the CBQ, but the main equations are identical, as shown in Table 1.6.

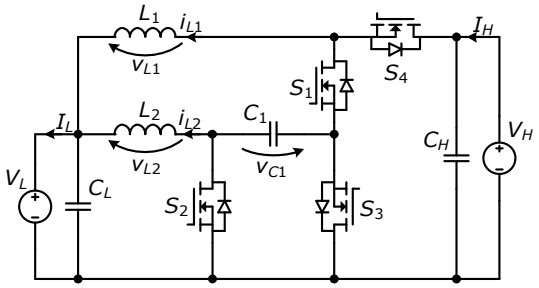

Fig. 1.18. The bi-directional quadratic converter (BQ2) proposed in [56]

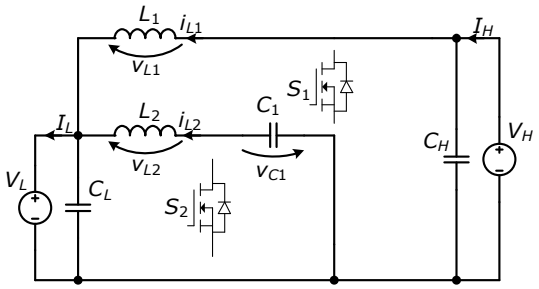

Fig. 1.19. Equivalent schematic during t_{on} of the BQ2 (S_1 and S_2 are turned OFF, S_3 and S_4 are turned ON)

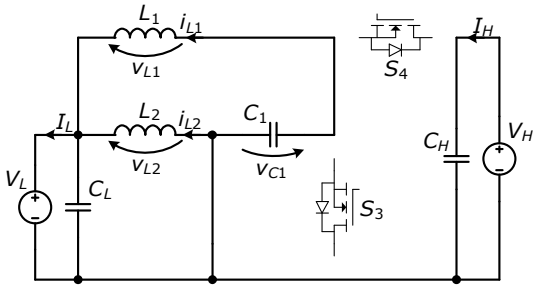

Fig. 1.20. Equivalent schematic during t_{off} of the BQ2 (S_1 and S_2 are turned ON, S_3 and S_4 are turned OFF)

Table 1.6. Main equations of the BQ2

Conversion ratio	**Active devices**
$v_{L1}(t_{on}) = V_H - V_L$, $v_{L1}(t_{off}) = -V_{C1} - V_L$, $v_{L2}(t_{on}) = V_{C1} - V_L$, $v_{L2}(t_{off}) = -V_L$, $V_{C1} = \sqrt{V_H \cdot V_L}$, $V_L = V_H \cdot D^2$, $V_H = V_L \cdot \frac{1}{(1-D')^2}$.	$V_{S1} = V_H$, $V_{S2} = V_{S3} = V_{C1}$, $V_{S4} = V_H + V_{C1}$, $I_{S1} = I_{S4} = I_{L1}$, $I_{S2} = I_{L1} + I_{L2}$, $I_{S3} = I_{L2}$, $S = \sum_{j=1}^{4} V_{Sj} \cdot I_{Sj} = 4 \cdot I_L \cdot \sqrt{V_H \cdot V_L}$
Inductors	**Capacitors**
$I_{L1} = D \cdot I_L$, $I_{L2} = (1-D) \cdot I_{L1}$, $L_1 = \frac{V_H - V_L}{r_i \cdot f \cdot I_L}$, $L_2 = \frac{V_L}{r_i \cdot f \cdot I_L}$,	$i_{CL} = i_{L1} + i_{L2} - I_L$, $i_{CH} = I_H - i_{S4}$, $i_{C1} = i_{S2} - i_{L2}$ $C_L = \frac{1}{\Delta v_{CL}} \int_{t_{on}/2}^{t_{on}+t_{off}/2} i_{CL} dt = \frac{r_i \cdot I_L}{8 \cdot r_v \cdot f \cdot V_L}$,

$W_{L1} = \frac{I_L \cdot V_L \cdot (V_H - V_L)}{2 \cdot r_i \cdot f \cdot V_H}$, $W_{L2} = \frac{I_L \cdot V_L \cdot (\sqrt{V_L / V_H} - 1)^2}{2 \cdot r_i \cdot f}$, $W_{LTot} = \frac{I_L \cdot V_L \cdot (\sqrt{V_H} - \sqrt{V_L})}{r_i \cdot f \cdot \sqrt{V_H}}$.	$C_H = \frac{-1}{\Delta v_{CH}} \int_0^{t_{on}} i_{CH} dt = \frac{I_L \cdot V_L \cdot (\sqrt{V_H} - \sqrt{V_L})}{r_v \cdot f \cdot V_H^{5/2}}$, $C_1 = \frac{-1}{\Delta v_{C1}} \int_0^{t_{on}} i_{C1} dt = \frac{I_L \cdot (\sqrt{V_H} - \sqrt{V_L})}{r_v \cdot f \cdot V_H^{3/2}}$, $W_{CL} = \frac{r_i \cdot I_L \cdot V_L}{16 \cdot r_v \cdot f}$, $W_{CH} = \frac{I_L \cdot V_L \cdot (\sqrt{V_H} - \sqrt{V_L})}{2 \cdot r_v \cdot f \cdot \sqrt{V_H}}$, $W_{C1} = \frac{I_L \cdot V_L \cdot (\sqrt{V_H} - \sqrt{V_L})}{2 \cdot r_v \cdot f \cdot \sqrt{V_H}}$, $W_{CTot} = \frac{I_L \cdot V_L \cdot (\sqrt{V_H} \cdot (1 + r_i / 16) - \sqrt{V_L})}{r_v \cdot f \cdot \sqrt{V_H}}$.

1.3.6. The bidirectional quadratic converter (BQ3)

A bidirectional quadratic converter (BQ3) can be realized by using diodes in addition to the transistors, as the topology proposed in [57] is employing. The resulting topology, with its schematic presented in Fig. 1.21, has three and not four transistors, contrary to other topologies. Because of the use of diodes, the equivalent switching states are actually three, one for t_{on} switching period for buck operation (or t_{off}' in boost operation) in Fig. 1.22 (S_2, D_1, D_2 - OFF, S_1, S_3 - ON), one for the t_{off} switching period during buck operation in Fig. 1.23 (S_1, D_2, S_3 - OFF, D_1, S_2 - ON), and one for the t_{on}' of boost mode in Fig. 1.24 (S_1, D_1, S_3 - OFF, D_2, S_2 - ON).

Even if the topology is very different compared to the CBQ, BQ1, or BQ2, the mathematical expressions that characterize the BQ3 are identical, as presented in Table 1.7, with an exception for the total active switch stress, as additional components are employed. The equivalent schematics during the switching are identical to the schematics of the CBQ, which justifies the identical equations for the passive components.

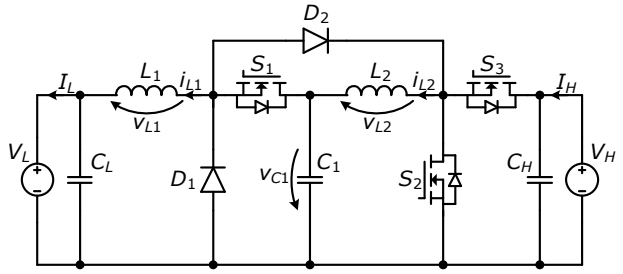

Fig. 1.21. The bi-directional quadratic converter (BQ3) proposed in [57]

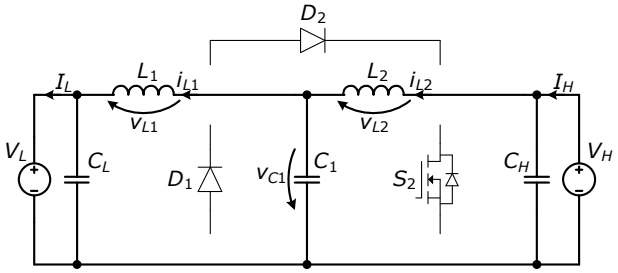

Fig. 1.22. Equivalent schematic of the BQ3 during t_{on} (buck mode) or t_{off}' (boost mode) (S_2, D_1, D_2 are turned OFF, S_1 and S_3 are turned ON)

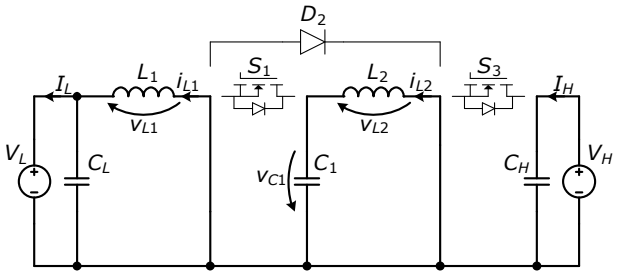

Fig. 1.23. Equivalent schematic of the BQ3 during t_{off} (buck mode) (S_1, D_2, S_3 are turned OFF, D_1 and S_2 and are turned ON)

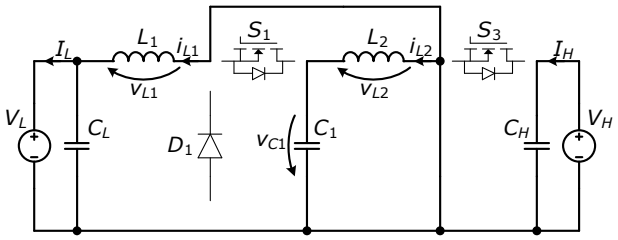

Fig. 1.24. Equivalent schematic of the BQ3 during t_{on}' (boost mode) (S_1, D_1, S_3 are turned OFF, D_2 and S_2 and are turned ON)

Table 1.7. Main equations of the BQ3

Conversion ratio	**Active devices**
$v_{L1}(t_{on}) = V_{C1} - V_L$, $v_{L1}(t_{off}) = -V_L$, $v_{L2}(t_{on}) = V_H - V_{C1}$, $v_{L2}(t_{off}) = -V_{C1}$, $V_{C1} = \sqrt{V_H \cdot V_L}$, $V_L = V_H \cdot D^2$, $V_H = V_L \cdot \frac{1}{(1-D')^2}$.	$V_{S1} = V_{C1}$, $V_{S2} = V_{S3} = V_{D1} = V_{C1}$, $V_{D2} = V_H - V_{C1}$, $I_{S1} = I_{D1} = I_{D2} = I_{L1}$, $I_{S2} = I_{L1} + I_{L2}$, $S = \sum_{j=1}^{2} V_{Sj} \cdot I_{Sj} + \sum_{j=1}^{2} V_{Dj} \cdot I_{Dj}$, $S = I_L \cdot (2 \cdot V_H + 3 \cdot \sqrt{V_H \cdot V_L})$
Inductors	**Capacitors**
$I_{L1} = I_L$, $I_{L2} = D \cdot I_{L1}$,	$i_{CL} = i_{L1} - I_L$, $i_{CH} = I_H - i_{S3}$, $i_{C1} = i_{L2} - i_{S1}$

$L_1 = \frac{V_L \cdot (\sqrt{V_H} - \sqrt{V_L})}{r_i \cdot f \cdot I_L \cdot \sqrt{V_H}}$, $L_2 = \frac{V_H - \sqrt{V_H \cdot V_L}}{r_i \cdot f \cdot I_L}$, $W_{L1} = W_{L2} = \frac{I_L \cdot V_L \cdot (\sqrt{V_H} - \sqrt{V_L})}{2 \cdot r_i \cdot f \cdot \sqrt{V_H}}$, $W_{LTot} = \frac{I_L \cdot V_L \cdot (\sqrt{V_H} - \sqrt{V_L})}{r_i \cdot f \cdot \sqrt{V_H}}$.	$C_L = \frac{1}{\Delta v_{CL}} \int_{t_{on}/2}^{t_{on}+t_{off}/2} i_{CL} dt = \frac{r_i \cdot I_L}{8 \cdot r_v \cdot f \cdot V_L}$, $C_H = \frac{-1}{\Delta v_{CH}} \int_0^{t_{on}} i_{CH} dt = \frac{I_L \cdot V_L \cdot (\sqrt{V_H} - \sqrt{V_L})}{r_v \cdot f \cdot V_H^{5/2}}$, $C_1 = \frac{-1}{\Delta v_{C1}} \int_0^{t_{on}} i_{C1} dt = \frac{I_L \cdot (\sqrt{V_H} - \sqrt{V_L})}{r_v \cdot f \cdot V_H^{3/2}}$, $W_{CL} = \frac{r_i \cdot I_L \cdot V_L}{16 \cdot r_v \cdot f}$, $W_{CH} = \frac{I_L \cdot V_L \cdot (\sqrt{V_H} - \sqrt{V_L})}{2 \cdot r_v \cdot f \cdot \sqrt{V_H}}$, $W_{C1} = \frac{I_L \cdot V_L \cdot (\sqrt{V_H} - \sqrt{V_L})}{2 \cdot r_v \cdot f \cdot \sqrt{V_H}}$, $W_{CTot} = \frac{I_L \cdot V_L \cdot (\sqrt{V_H} \cdot (1 + r_i / 16) - \sqrt{V_L})}{r_v \cdot f \cdot \sqrt{V_H}}$.

1.3.7. The bidirectional triangular modular multilevel converter (BTMM)

The bidirectional modular multilevel converter with triangular structure (BTMM), is proposing a converter structure which is designed in a modular system, with the number of modules depending on the voltage ratio between the inputs [58]. The schematic shown in Fig. 1.25, is a two-level structure, using three identical modules designed to operate at the same duty cycle, D = 50% , under the same voltage and current parameters. The authors of the paper consider a constant duty cycle, and the voltage ratio should be adjusted by adjusting the number of the modules used. This work considers the two-level schematic, and an actual variable duty cycle, in order to achieve a better comparison to other topologies, and to limit the number of the switches used (≤6).

The operation of the BTMM is shown with the equivalent schematics for the two switching states, t_{on} switching period in Fig. 1.26 (S_{A21}, S_{A11}, S_{A12} - OFF, S_{B21}, S_{B11}, S_{B12} - ON) and t_{off} switching period in Fig. 1.27 (S_{A21}, S_{A11}, S_{A12} - ON, S_{B21}, S_{B11}, S_{B12} - OFF). Because of the complex structure, the equations of the BTMM are also more complex, as presented in Table 1.8.

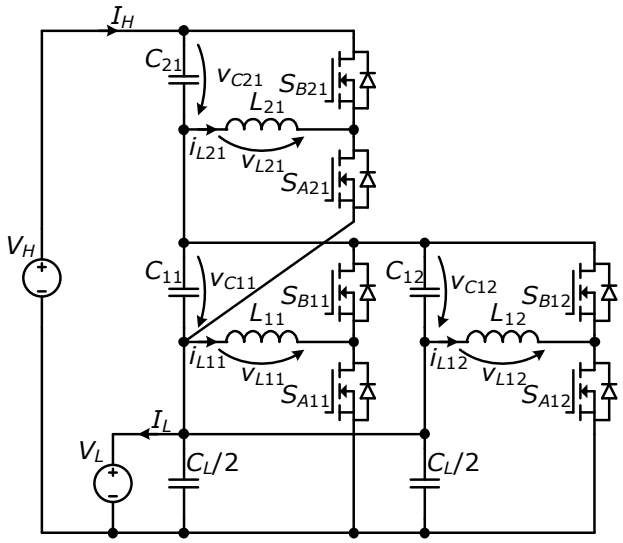

Fig. 1.25. The bidirectional modular multilevel converter with triangular structure (BTMM) proposed in [58]

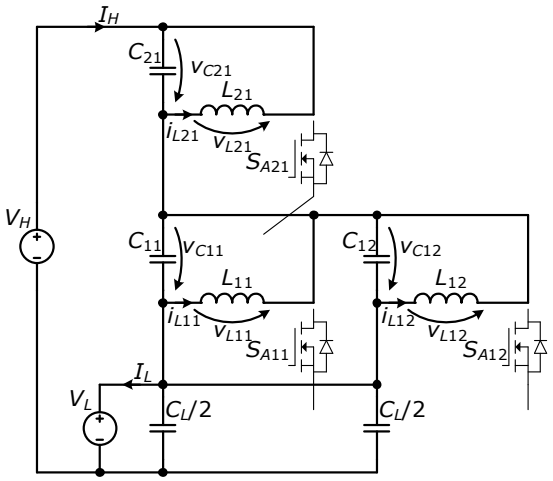

Fig. 1.26. Equivalent schematic during t_{on} of the BTMM
(S_{A21}, S_{A11}, S_{A12} are turned OFF, S_{B21}, S_{B11}, S_{B12} are turned ON)

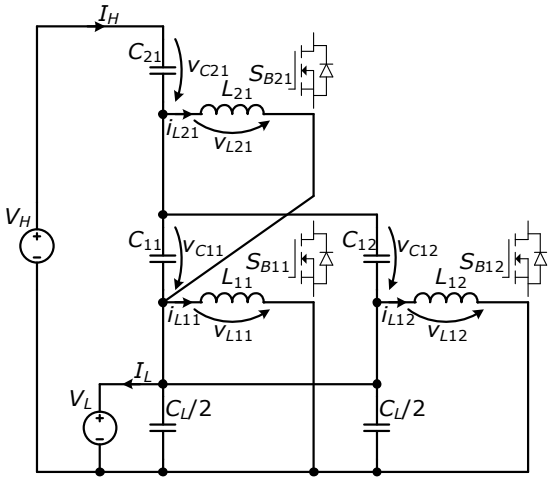

Fig. 1.27. Equivalent schematic during t_{off} of the BTMM
(S_{A21}, S_{A11}, S_{A12} are turned ON, S_{B21}, S_{B11}, S_{B12} are turned OFF)

Table 1.8. Main equations of the BTMM

Conversion ratio	**Active devices**
$v_{L11}(t_{on}) = V_{C11}$, $v_{L21}(t_{on}) = V_{C21}$, $v_{L11}(t_{off}) = V_L$, $v_{L21}(t_{off}) = V_{C11}$, $v_{L11} = v_{L12}$, $V_{C11} = \frac{V_L \cdot (1-D)}{D}$, $V_{C21} = \frac{V_{C11} \cdot (1-D)}{D}$, $V_L = V_H \cdot \frac{D^2}{D^2 - D + 1}$, $V_H = V_L \cdot \frac{D'^2 - D' + 1}{(1-D')^2}$.	$V_{SA11} = V_{SA12} = V_{SB11} = V_{SB12} = V_{C11} + V_L$, $V_{SA21} = V_{SB21} = V_H - V_L$, $I_{SA11} = I_{SB11} = I_{SA12} = I_{SB12} = I_{L11}$, $I_{SA21} = I_{SB21} = I_{L21}$, $S = \sum_{i,j} V_{SAij} \cdot I_{SAij} + \sum_{i,j} V_{SBij} \cdot I_{SBij}$ $S = \frac{2 I_L V_L (V_H - V_L)^2 (k - V_L^{1/2} k^{1/2})}{V_H (2V_L^2 - 3V_H V_L + V_H V_L^{1/2} k^{1/2})}$
Inductors	**Capacitors**
$I_{L11} = I_{L12} = \frac{I_H}{2 \cdot D^2}$, $I_{L21} = \frac{I_H}{D}$, $L_{11} = L_{12} = \frac{V_H \cdot V_L \cdot (V_L - 2 \cdot V_H + \sqrt{V_L \cdot k})^2}{2 \cdot r_i \cdot f \cdot I_L \cdot (V_H - V_L)^3}$, $L_{21} = \frac{-V_H \cdot V_L \cdot (V_L - 2 \cdot V_H + \sqrt{V_L \cdot k})^3}{2 \cdot r_i \cdot f \cdot I_L \cdot (V_H - V_L)^2 \cdot (V_L - \sqrt{V_L \cdot k})^2}$, $W_{L11} = \frac{I_L \cdot V_L \cdot (V_H - V_L)}{4 \cdot r_i \cdot f \cdot V_H}$, $W_{L21} = \frac{I_L V_L (\sqrt{k V_L^3} + 2V_H^2 - V_L^2 - 2V_H \sqrt{k V_L})}{2 \cdot r_i \cdot f \cdot V_H \cdot (2 \cdot V_H - V_L - \sqrt{V_L \cdot k})}$,	$i_{CL}(t_{on}) = I_H - I_L$, $i_{C11}(t_{on}) = I_H / 2 - i_{L11}$, $i_{C21}(t_{on}) = I_H$ $C_L = \frac{-1}{\Delta v_{CL}} \int_0^{t_{on}} i_{CL} dt$, $C_{11} = \frac{-1}{\Delta v_{CH}} \int_0^{t_{on}} i_{C11} dt$, $C_{21} = \frac{-1}{\Delta v_{C21}} \int_0^{t_{on}} i_{C21} dt$,

$$W_{LTot} = \frac{I_L V_L}{256 \cdot r_L \cdot f \cdot V_H^2 \cdot (V_H - V_L)^2} \cdot (640 V_H^2 V_L^2 + 5 V_L^{3/2} k^{5/2} + 14 V_L^{5/2} k^{3/2} - 3 V_L^{7/2} k^{1/2}$$
$$-192 V_H V_L^3 - 704 V_H^3 V_L + 256 V_H^4 - 16 V_H^2 V_L^{1/2} k^{3/2})$$

$$W_{CTot} = \frac{I_L V_L (2V_H^2 k^{1/2} - 8V_H^2 V_L^{1/2} - V_L^2 k^{1/2} + 10 V_H V_L^{3/2} - 3V_L^{5/2})}{2 \cdot r_C \cdot f \cdot V_H \cdot (V_H k^{1/2} - 3V_H V_L^{1/2} + 2V_L^{3/2})}.$$

$$k = 4 \cdot V_H - 3 \cdot V_L$$

1.3.8. The bidirectional switched capacitor converter (BSC1)

The bidirectional switched capacitor (BSC1) converter, presented in Fig. 1.28, uses two capacitors that are connected in series to the high voltage input, in order to achieve a voltage halving effect [59]. Even if this topology resembles a hybrid converter, the main difference is that the two capacitors are charged/discharged from another capacitor, which might result in large current spikes.

The equivalent schematics for the two switching states are presented in Fig. 1.29 for t_{on} switching period (S_1, S_3 - OFF, S_2, S_4 - ON), and in Fig. 1.30 for t_{off} switching period (S_1, S_3 - ON, S_2, S_4 - OFF). During t_{on} the two switched capacitors (C_1 and C_2) are connected in series to the high voltage input, and during t_{off} they are connected in parallel in order to equalize their voltage. This operation results in uncontrolled currents.

In order to calculate the main equations of the BSC1 from Table 1.9, the assumption is made that the two capacitor voltages are equal to half of V_H. The BSC1 presents a conversion ratio that is limited to maximum 0.5 in the step-down operation mode, which is an important difference when comparing to the rest of the studied topologies.

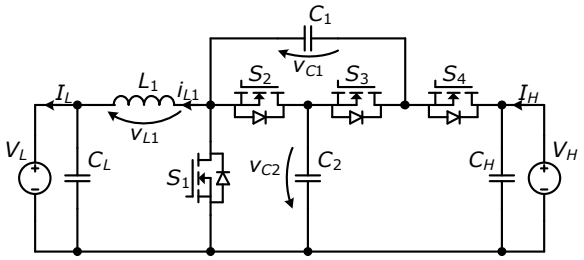

Fig. 1.28. The bi-directional switched capacitor converter (BSC1) proposed in [59]

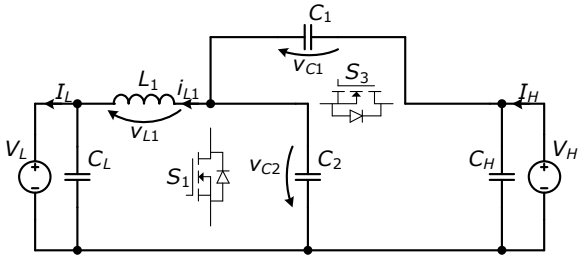

Fig. 1.29. Equivalent schematic during t_{on} of the BSC1
(S_1 and S_3 are turned OFF, S_2 and S_4 are turned ON)

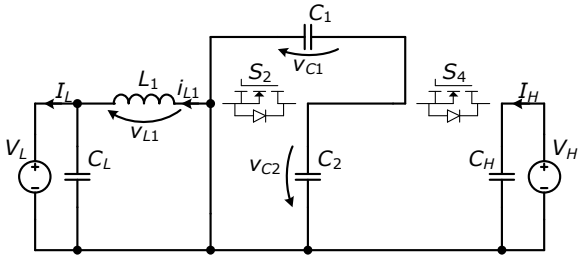

Fig. 1.30. Equivalent schematic during t_{off} of the BSC1
(S_1 and S_3 are turned ON, S_2 and S_4 are turned OFF)

Table 1.9. Main equation of BSC1

Conversion ratio	**Active devices**
$v_{L1}(t_{on}) = V_{C2} - V_L$, $v_{L1}(t_{off}) = -V_L$, $V_{C1} = V_{C2} = \frac{V_H}{2}$, $V_L = V_H \cdot \frac{D}{2}, V_H = V_L \cdot \frac{2}{1-D}$.	$V_{S1} = V_{C2}$, $V_{S2} = V_{S3} = V_{C1}$, $V_{S4} = V_H - V_{C2}$, $I_{S1} = \frac{I_{L1} \cdot (2-D)}{2 \cdot (1-D)}$, $I_{S2} = I_{S4} = I_{L1}/2$, $I_{S3} = \frac{I_{L1} \cdot D}{2 \cdot (1-D)}$ $S = \sum_{j=1}^{4} V_{Sj} \cdot I_{Sj} = \frac{I_L \cdot V_H \cdot (V_H - V_L)}{(V_H - 2 \cdot V_L)}$
Inductors	**Capacitors**
$I_{L1} = I_L$, $L_1 = \frac{V_L \cdot (V_H - 2 \cdot V_L)}{r_i \cdot f \cdot I_L \cdot V_H}$, $W_{LTot} = W_{L1} = \frac{I_L \cdot V_L \cdot (V_H/2 - V_L)}{r_i \cdot f \cdot V_H}$.	$i_{CL} = i_{L1} - I_L$, $i_{CH} = I_H - i_{S4}$, $i_{C1}(t_{on}) = i_{C2}(t_{on}) = i_{L1}/2$, $C_L = \frac{1}{\Delta v_{CL}} \int_{t_{on}/2}^{t_{on}+t_{off}/2} i_{CL} dt = \frac{r_i \cdot I_L}{8 \cdot r_v \cdot f \cdot V_L}$, $C_H = \frac{-1}{\Delta v_{CH}} \int_0^{t_{on}} i_{CH} dt = \frac{I_L \cdot V_L \cdot (V_H - 2 \cdot V_L)}{r_v \cdot f \cdot V_H^3}$, $C_1 = \frac{1}{\Delta v_{C1}} \int_0^{t_{on}} i_{C1} dt = \frac{2 \cdot I_L \cdot V_L}{r_v \cdot f \cdot V_H^2}$, $W_{CL} = \frac{r_i \cdot I_L \cdot V_L}{16 \cdot r_v \cdot f}$, $W_{CH} = \frac{I_L \cdot V_L \cdot (V_H - 2 \cdot V_L)}{2 \cdot r_v \cdot f \cdot V_H}$, $W_{CTot} = \frac{I_L \cdot V_L \cdot (V_H \cdot (1 + r_i/16) - V_L)}{r_v \cdot f \cdot V_H}$.

1.3.9. The bidirectional switched capacitor converter (BSC2)

A different bidirectional switched capacitor (BSC2) topology is proposed in [60] with the schematic shown in Fig. 1.31. The BSC2 also presents a conversion ratio limited to 0.5 which is achieved by connecting different voltage capacitors in parallel, with the same disadvantage of BSC1 and BSQZ converters: a large current spike when the capacitors are switched.

The equivalent schematics for the two switching states are presented in Fig. 1.32 for t_{on} switching period (S_3 - OFF, S_1, S_2 - ON), and in Fig. 1.33 for t_{off} switching period (S_3 - ON, S_1, S_2 - OFF). The two intermediary capacitors (C_1 and C_2) are always connected in series to the high voltage input, but during t_{on} the C_1 is connected in parallel to the V_L input, resulting in larger current spike between the two capacitors. To calculate the main equations of the BSC2 from Table 1.10, the assumption is made that C_L and C_1 have equal voltages.

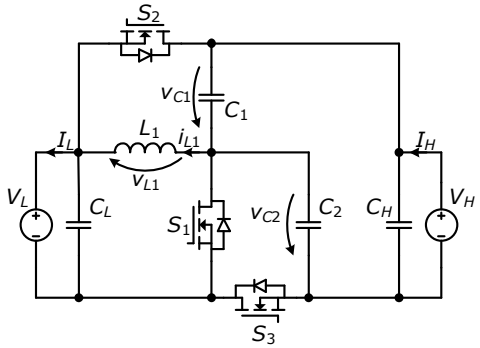

Fig. 1.31. The bi-directional switched capacitor converter (BSC2) proposed in [60]

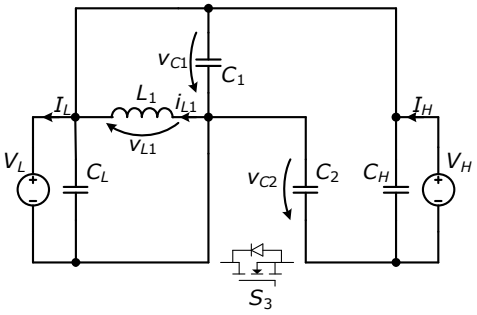

Fig. 1.32. Equivalent schematic during t_{on} of the BSC2
(S_3 is turned OFF, S_1 and S_2 are turned ON)

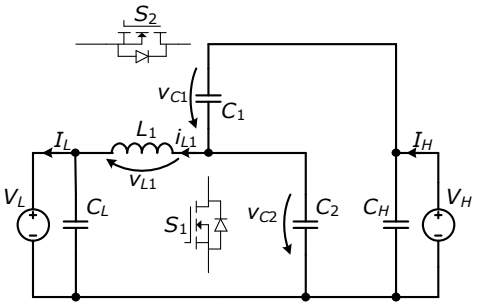

Fig. 1.33. Equivalent schematic during t_{off} of the BSC2
(S_3 is turned ON, S_1 and S_2 are turned ON)

Table 1.10. Main equations of the BSC2

Conversion ratio	**Active devices**
$v_{L1}(t_{on}) = -V_{C1} = -V_L$, $v_{L1}(t_{off}) = V_{C2} - V_L$, $V_{C1} = V_L$, $V_{C2} = V_H - V_L$, $V_L = V_H \cdot \frac{D}{1+D}$, $V_H = V_L \cdot \frac{2-D}{1-D}$.	$V_{S1} = V_{C2}$, $V_{S2} = V_H - V_L$, $V_{S3} = V_{C2}$, $I_{S1} = I_{L1} \cdot \frac{1}{1-D}$, $I_{S2} = I_{L1} \cdot \frac{D}{1-D}$, $I_{S3} = I_{L1}$, $S = \sum_{j=1}^{3} V_{Sj} \cdot I_{Sj} = \frac{2 \cdot I_L \cdot (V_H - V_L)^3}{V_H \cdot (V_H - 2 \cdot V_L)}$
Inductors	**Capacitors**
$I_{L1} = \frac{I_L}{1+D}$, $L_1 = \frac{V_H \cdot V_L \cdot (V_H - 2 \cdot V_L)}{r_i \cdot f \cdot I_L \cdot (V_H - V_L)^2}$, $W_{LTot} = W_{L1} = \frac{I_L \cdot V_L \cdot (V_H - 2 \cdot V_L)}{2 \cdot r_i \cdot f \cdot V_H}$,	$i_{CL} = i_{S2} + i_{L1} - I_L$, $i_{CH}(t_{on}) = I_H - i_{L1}/2$, $i_{C1}(t_{on}) = i_{L1}/2$, $i_{C2}(t_{on}) = -i_{L1}/2$, $C_L = \frac{1}{\Delta v_{CL}} \int_{t_{on}/2}^{t_{on}+t_{off}/2} i_{CL} dt$, $C_L = \frac{I_L \cdot (r_i \cdot V_H \cdot (V_H - V_L) + 4 \cdot V_L^2)}{8 \cdot r_v \cdot f \cdot V_L \cdot V_H \cdot (V_H - V_L)}$, $C_H = \frac{-1}{\Delta v_{CH}} \int_{t_{on}/2}^{t_{on}+t_{off}/2} i_{CH} dt = \frac{r_i \cdot I_L \cdot V_L}{8 \cdot r_v \cdot f \cdot V_H^2}$, $C_1 = \frac{1}{\Delta v_{C1}} \int_0^{t_{on}} i_{C1} dt = \frac{I_L}{2 \cdot r_v \cdot f \cdot V_H}$, $C_2 = \frac{1}{\Delta v_{C2}} \int_0^{t_{on}} i_{C2} dt = \frac{I_L \cdot V_L}{2 \cdot r_v \cdot f \cdot V_H \cdot (V_H - V_L)}$, $W_{CTot} = \frac{I_L V_L (2V_H^2 - 2V_L V_H + 2V_L^2 + r_i (V_H^2 - V_L V_H))}{8 \cdot r_v \cdot f \cdot V_H \cdot (V_H - V_L)}$.

1.4. Conclusions

This chapter presented an overview of the microgrid structure, with emphasis on the advantages of DC solutions, such as cheaper construction of household or industrial consumers, easier integration of renewable resources or storage elements, V2G integration, and simpler solutions to common issues in conventional AC grids, all advantages encouraged by the advances in power electronics technologies.

A summary of the storage solutions for microgrids is presented, with an emphasis on chemical versus electrostatic storage performances. While batteries have the benefit of larger energy density, the SCs have the advantage of larger power densities, and together they can operate in a hybrid storage system to achieve best performances.

A selection of possible voltage levels for DC microgrids is presented, and, in order to have a good energy utilization of the SC, a wide conversion ratio converter is desired as an interface to the DC bus. This work focuses on hybrid converters to achieve wide conversion ratios, which make use of switched capacitor or inductive cells to achieve their advantages. A large range of state-of-the-art converter topologies are also presented in this chapter and are going to be compared to the hybrid topologies.

2. THE BIDIRECTIONAL HYBRID SWITCHED CAPACITOR CONVERTER (BHSC1)

2.1. Abstract

This chapter presents a Bidirectional Hybrid Switched Capacitor converter (BHSC1) which uses a switched capacitive cell in its structure in order to achieve a wider voltage conversion ratio. The analysis of this converter includes a steady state analysis, performed in a similar manner to the CBBB converter, and a dynamic analysis which is used for the design of an analog and a digital controller. The stability of this converter is addressed by analyzing the frequency response of the linearized system, and the experimental and simulation results for transient operation of the BHSC1. In addition to the two controllers, an additional valley current mode controller is employed as well. An improved version of the BHSC1 is proposed in order to address some shortcomings of the topology.

2.2. Overview

The schematic of the BHSC1 is developed from the Unidirectional Hybrid Switched Capacitor converter (UHSC1), which operates in step-up mode (Fig. 2.1), and it was initially proposed in several papers [42], [61], [62]. The UHSC1 was experimentally tested in [63], [64]. The UHSC1 converter resembles a boost converter with a switched capacitive cell (D_1, C_1, D_2, C_2,) connected at the output. The capacitors are charged in parallel and discharged in series to the output, achieving a voltage doubling effect.

The BHSC1 was initially proposed in [62], and it was tested in steady state operation in [65], with a Valley Current-Mode control (VCM) in [66], or in terms of stability operation in [67].

As presented in Fig. 2.2 the BHSC1 converter uses transistors in place of the initial diodes, with antiparallel diodes, for bidirectional power flow. As it is the case for the CBBB presented in 1.3.1, positive currents in circuit indicate step-up operation, while negative currents indicate step-down operation. One driving signal is used, which is applied directly to S_2 and S_3, and inverted for S_1.

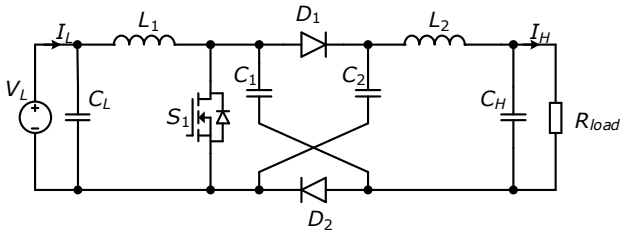

Fig. 2.1. The Unidirectional Step-Up Hybrid Switched Capacitor converter (UHSC1) [41], [42], [61], [62]

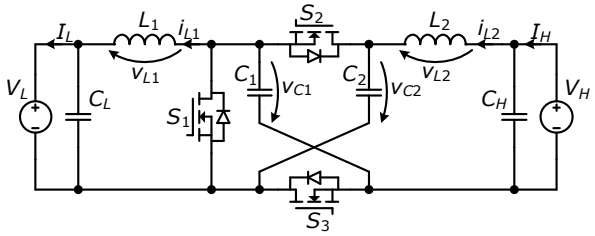

Fig. 2.2. The Bidirectional Hybrid Switched Capacitor converter (BHSC1) [62], [65]–[67] (i_{L1}, i_{L2} >0 ↔ step-down operation; i_{L1}, i_{L2} < 0 ↔ step-up operation)

2.3. Steady state analysis

The steady state analysis of the BHSC1 converter is made starting from the equivalent switching schematics for the two switching intervals, t_{on} and t_{off}, presented in Fig. 2.3 and Fig. 2.4, respectively. Similar to the UHSC1 converter, the BHSC1 uses identical capacitors in the switching cell, and the voltage across them is considered equal ($v_{C1} = v_{C2} = V_{Csw}$).

During the t_{on} interval, the two capacitors are connected in parallel through the inductors between the two inputs (V_H and V_L). The i_{L1} current indicates the charge or discharge of the switched capacitors (C_1, C_2), as it is larger than i_{L2}.

During the t_{off} interval, the capacitors are connected in series to the high voltage side trough the L_2 inductor, and L_1 inductor is connected in parallel to the low voltage side.

In step-down operation the two capacitors are charged in series from the high voltage input, V_H, and are discharged in parallel to the low voltage side V_L, achieving a voltage halving. The step-up operation is similar to that of the UHSC1, where the capacitors are charged in parallel and discharged in series.

From the two equivalent schematics, the main theoretical waveforms are extracted in Fig. 2.5

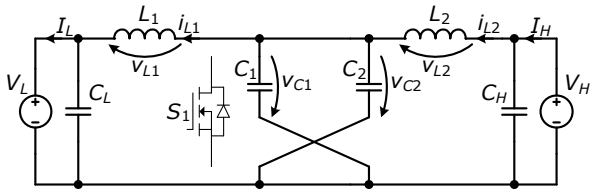

Fig. 2.3. Equivalent schematic of BHSC1 during t_{on} interval (S_1 is turned OFF, S_2 and S_3 are turned ON)

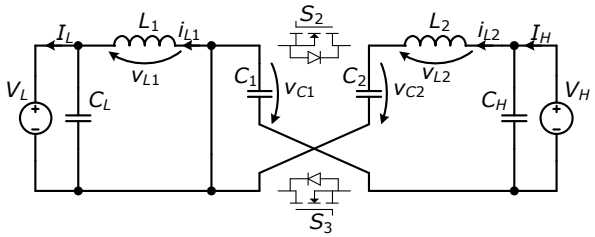

Fig. 2.4. Equivalent schematic of BHSC1 during t_{off} interval (S_1 is turned ON, S_2 and S_3 are turned OFF)

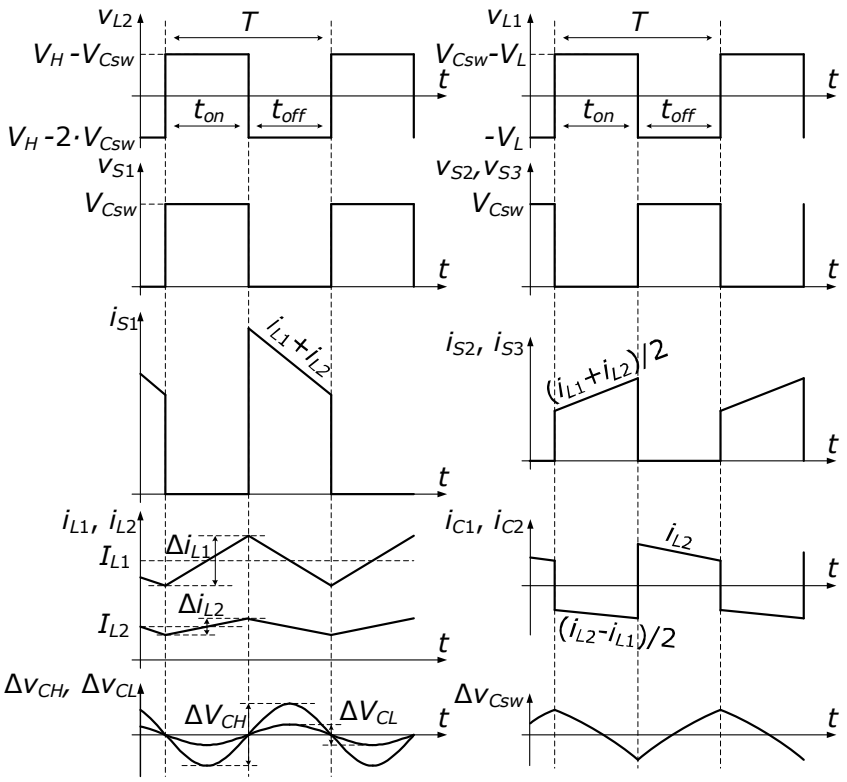

Fig. 2.5. Main theoretical waveforms of the BHSC1 : L_1, L_2 inductor voltages and currents (v_{L1}, v_{L2}, i_{L1}, i_{L2}); S_1, S_2 and S_3 switches voltages and currents (v_{S1}, v_{S2}, v_{S3}, i_{S1}, i_{S2}, i_{S3}); C_1, C_2 switched capacitors currents (i_{C1}, i_{C2}); ripple voltages on the capacitors (Δv_{CH}, Δv_{CL}, Δv_{Csw})

As presented in section 1.3.1, the analysis of the BHSC1 starts with considering the duty cycle, D, for the step-down operation mode, and the duty cycle, D', for step-up mode:

$$D = \frac{t_{on}}{T},\ D' = \frac{t_{off}}{T}. \tag{2.1}$$

The voltages on the two inductors corresponding to the two equivalent schematics during the switching intervals, Fig. 2.3 and Fig. 2.4, are:

$$\begin{aligned} t_{on} &: v_{L1} = V_{Csw} - V_L,\ v_{L2} = V_H - V_{Csw}, \\ t_{off} &: v_{L1} = -V_L,\ v_{L2} = V_H - 2 \cdot V_{Csw}. \end{aligned} \tag{2.2}$$

The same simplifying assumptions are used as in 1.3.1 (ideal components, constant voltage on capacitors, steady state operation), and in addition, identical voltages and currents on the two switched capacitors are considered. By applying the volt-second balance, the following are used:

$$\begin{aligned}\langle v_{L1}\rangle &= D\cdot(V_{Csw}-V_L)+(1-D)\cdot(-V_L)=0,\\ \langle v_{L2}\rangle &= D\cdot(V_H-V_{Csw})+(1-D)\cdot(V_H-2\cdot V_{Csw})=0,\end{aligned} \tag{2.3}$$

to determine the steady state voltage on one switching capacitor:

$$V_{Csw}=\frac{V_L}{D}=\frac{V_H}{2-D}=\frac{V_L+V_H}{2}, \tag{2.4}$$

The conversion ratios for step-down, or step-up mod are calculated:

$$V_L=V_H\cdot\frac{D}{2-D}. \tag{2.5}$$

$$V_H=V_L\cdot\frac{1+D'}{1-D'}. \tag{2.6}$$

The BHSC1 has the same conversion ratio as the converter presented in 1.3.2. Similarly, the duty ratio can be calculated from (2.4) as:

$$D=\frac{2\cdot V_L}{V_H+V_L}. \tag{2.7}$$

The average value of the low voltage side current is equal to the L_1 inductor current:

$$I_L=I_{L1} \tag{2.8}$$

As defined for the CBBB converter in 1.3.1, a ripple current percentage is defined for the two inductors:

$$r_i=\frac{\Delta i_{L1}}{I_{L1}}=\frac{\Delta i_{L2}}{I_{L2}}, \tag{2.9}$$

and by using the voltage-current dependency of an inductor, the values of the two inductors are determined:

$$L_1=\frac{v_{L1}\cdot\Delta t}{\Delta i_{L1}}=\frac{V_L\cdot(V_H-V_L)}{r_i\cdot f\cdot I_L\cdot(V_H+V_L)}, \tag{2.10}$$

$$L_2=\frac{v_{L2}\cdot\Delta t}{\Delta i_{L2}}=\frac{V_H\cdot(V_H-V_L)}{r_i\cdot f\cdot I_L\cdot(V_H+V_L)}. \tag{2.11}$$

The energy stored in each inductor is calculated as:

$$W_{L1}=\frac{L_1\cdot I_{L1}^{\,2}}{2}=\frac{I_L\cdot V_L\cdot(V_H-V_L)}{2\cdot r_i\cdot f\cdot(V_H+V_L)}, \tag{2.12}$$

$$W_{L2}=\frac{L_2\cdot I_{L2}^{\,2}}{2}=\frac{I_L\cdot V_L^{\,2}\cdot(V_H-V_L)}{2\cdot r_i\cdot f\cdot V_H\cdot(V_H+V_L)}. \tag{2.13}$$

The total inductor energy is equal to the sum of the energy of each inductor:

$$W_{LTot}=\sum W_{Li}=\sum\frac{L_i\cdot I_{Li}^{\,2}}{2}=W_{L1}+W_{L2}, \tag{2.14}$$

resulting to total inductor energy:

$$W_{LTot} = \frac{I_L \cdot V_L \cdot (V_H - V_L)}{2 \cdot r_i \cdot f \cdot V_H}. \tag{2.15}$$

The BHSC1 and the CBBB have the same total inductor energy as presented in 1.3.1, but the BHSC1 achieves a higher conversion ratio.

In order to calculate the capacitor requirements, the mathematical functions of the inductor currents are defined as the following time functions:

$$i_{L1}(t) = \begin{cases} I_{L1} + \Delta i_{L1} \cdot (t / t_{on} - 1/2), & t \in [0, t_{on}) \\ I_{L1} + \Delta i_{L1} \cdot ((T-t) / t_{off} - 1/2), & t \in [t_{on}, T] \end{cases} \tag{2.16}$$

$$i_{L2}(t) = \begin{cases} I_{L2} + \Delta i_{L2} \cdot (t / t_{on} - 1/2), & t \in [0, t_{on}) \\ I_{L2} + \Delta i_{L2} \cdot ((T-t) / t_{off} - 1/2), & t \in [t_{on}, T] \end{cases} \tag{2.17}$$

A ripple percentage is defined similarly as in 1.3.1, equal for all capacitors:

$$r_v = \frac{\Delta v_{CH}}{V_{CH}} = \frac{\Delta v_{CL}}{V_{CL}} = \frac{\Delta v_{Csw}}{V_{Csw}}, \tag{2.18}$$

The current for each capacitor is described with the following relations:

$$i_{CL} = i_{L1} - I_L, \tag{2.19}$$

$$i_{CH} = I_H - i_{L2}, \tag{2.20}$$

$$i_{Csw} = \begin{cases} (i_{L2} - i_{L1}) / 2, & t \in [0, t_{on}) \\ i_{L2}, & t \in [t_{on}, T] \end{cases} \tag{2.21}$$

Starting from the voltage-current dependency of an ideal capacitor, the following are used for calculating the capacitances:

$$C_L = \frac{1}{\Delta v_{CL}} \int_{t_{on}/2}^{t_{on}+t_{off}/2} (i_{L1} - I_L) dt, \tag{2.22}$$

$$C_H = \frac{-1}{\Delta v_{CH}} \int_{t_{on}/2}^{t_{on}+t_{off}/2} (I_H - i_{L2}) dt, \tag{2.23}$$

$$C_1 = C_2 = C_{sw} = \frac{1}{\Delta v_{Csw}} \int_{t_{on}}^{T} i_{L2}\, dt. \tag{2.24}$$

Both C_H and C_L capacitors have current functions with a similar shape, with the difference that one is discharging while the other is charging. If i_{L2} current is positive, the C_{sw} capacitors are charging during t_{off} time interval and vice versa. The final values of the capacitors are calculated as:

$$C_L = \frac{r_i \cdot I_L}{8 \cdot r_v \cdot f \cdot V_L}, \tag{2.25}$$

$$C_H = \frac{r_i \cdot I_L \cdot V_L}{8 \cdot r_v \cdot f \cdot V_H^2}, \tag{2.26}$$

$$C_{sw} = \frac{2 \cdot I_L \cdot V_L \cdot (V_H - V_L)}{r_v \cdot f \cdot V_H \cdot (V_H + V_L)^2}. \tag{2.27}$$

The total capacitor energy is calculated as the sum of each capacitor energy:

$$W_{CTot} = \sum W_{Ci} = \sum \frac{C_i \cdot V_{Ci}^2}{2} = W_{CL} + W_{CH} + 2 \cdot W_{Csw}, \tag{2.28}$$

and each individual capacitor energy is calculated as:

$$W_{CH} = \frac{r_i \cdot I_L \cdot V_L}{16 \cdot r_v \cdot f}, \tag{2.29}$$

$$W_{CL} = \frac{r_i \cdot I_L \cdot V_L}{16 \cdot r_v \cdot f}, \tag{2.30}$$

$$W_{Csw} = \frac{I_L \cdot V_L \cdot (V_H - V_L)}{4 \cdot r_v \cdot f \cdot V_H}, \tag{2.31}$$

The total capacitor energy results as:

$$W_{CTot} = \frac{I_L \cdot V_L \cdot (4 \cdot V_H - 4 \cdot V_L + r_i \cdot V_H)}{8 \cdot r_v \cdot f \cdot V_H}. \tag{2.32}$$

Comparing the W_{CTot} for the CBBB and for the BHSC1, it results that the second has a slightly higher capacitor requirement compared to the first, and it can be neglected because r_i is considered to be small enough.

The total active switch stress, for the three transistors, is calculated as:

$$S = \sum_{j=1}^{3} V_{Sj} \cdot I_{Sj}, \tag{2.33}$$

by taking into account the average voltage and current stresses from:

$$V_{S1} = V_{S2} = V_{S3} = V_{Csw}, \tag{2.34}$$

$$I_{S1} = I_{L1} + I_{L2}, \quad I_{S2} = I_{S3} = I_{S1} / 2. \tag{2.35}$$

The total active switch stress is calculated as:

$$S = V_{S1} \cdot I_{S1} + V_{S2} \cdot I_{S2} + V_{S3} \cdot I_{S3} = \frac{I_L \cdot (V_H + V_L)^2}{V_H}, \tag{2.36}$$

The total active switch stress for the BHSC1 has a value which is much lower than that of the CBBB converter.

2.4. Dynamic analysis

In order to perform the dynamic modeling, the State Space Averaging (SSA) method is used, a method which is widely used for this purpose [52], [68]. The first step in applying the method is writing the equations for the two equivalent schematics in the general form for state-space representation:

$$\dot{x} = A_i \cdot x + B_i \cdot u, \tag{2.37}$$

where i=1 and i=2 for the equations corresponding to t_{on} and t_{off} intervals, respectively.

For this system, x represents the state vector containing the state variables, which are the two inductor currents and the capacitor voltages, and u contains the input vector with the system inputs, which are the voltages on the two sides. The two vectors are described as follows:

$$x = \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{Csw} \\ v_{CL} \\ v_{CH} \end{bmatrix}, \quad u = \begin{bmatrix} V_L \\ V_H \end{bmatrix}. \tag{2.38}$$

In order to have a good model for the converter, the parasitic resistances from the circuits are taken into account when writing the equations, therefore the schematic of the BHSC1 with the parasitic components is shown in Fig. 2.6.

The equivalent schematics of the BHSC1 during the two switching intervals are presented in Fig. 2.7 and Fig. 2.8, respectively. The state (A_i) and input (B_i) matrices are expressed according to their elements, as follows:

$$A_i = \begin{bmatrix} a_{11_i} & a_{12_i} & a_{13_i} & a_{14_i} & 0 \\ a_{21_i} & a_{22_i} & a_{23_i} & 0 & a_{25_i} \\ a_{31_i} & a_{32_i} & 0 & 0 & 0 \\ a_{41_i} & 0 & 0 & a_{44_i} & 0 \\ 0 & a_{52_i} & 0 & 0 & a_{55_i} \end{bmatrix}, \quad B_i = \begin{bmatrix} b_{11_i} & 0 \\ 0 & b_{22_i} \\ 0 & 0 \\ b_{41_i} & 0 \\ 0 & b_{52_i} \end{bmatrix}. \tag{2.39}$$

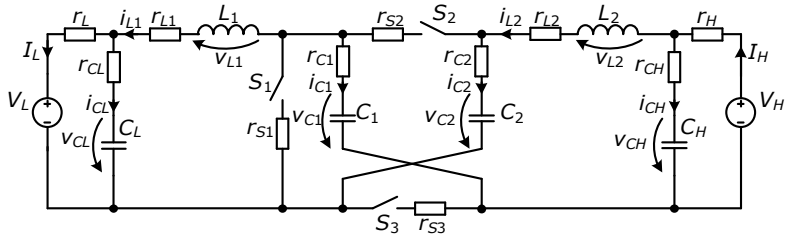

Fig. 2.6. BHSC1 schematic used for the SSA analysis . The schematic includes the following parasitic components: r_{L1}, r_{L2} – inductor ESRs; r_{CH}, r_{CL}, r_{C1}, r_{C2} – capacitor ESRs; r_{S1}, r_{S2}, r_{S3} – switch on-state resitances; r_H, r_L – high and low voltage bus resistances. Component values are provided in Table 2.1

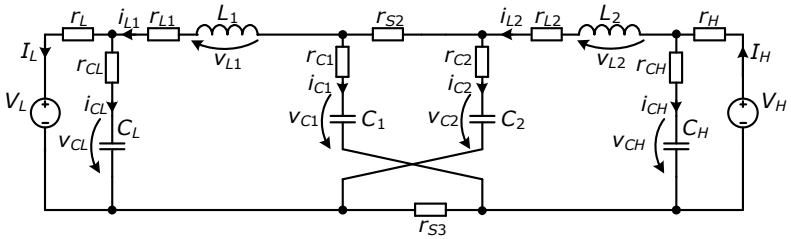

Fig. 2.7. BHSC1 equivalent schematic during t_{on} interval used for SSA

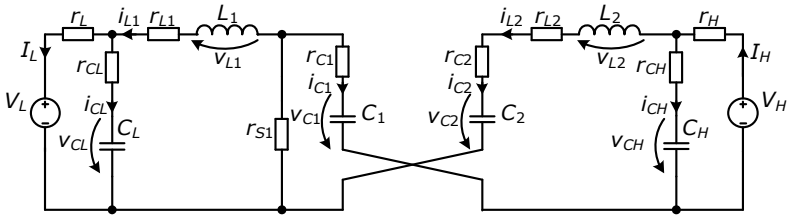

Fig. 2.8. BHSC1 equivalent schematic during t_{off} interval used for SSA

Based on schematic from Fig. 2.7, the relations (2.37), (2.38), (2.39) are used to express the elements of the state matrix (A_1) for t_{on} switching interval:

$$a_{11_1} = -\frac{\frac{r_{Csw}}{2} + r_{L1} + \frac{r_{S2}}{2} + \frac{r_{CL} \cdot r_L}{r_{CL} + r_L}}{L_1}, \tag{2.40}$$

$$a_{12_1} = \frac{r_{Csw} + r_{S2}}{2 \cdot L_1},\ a_{13_1} = \frac{1}{L_1},\ a_{14_1} = \frac{-r_L}{L_1 \cdot (r_{CL} + r_L)}, \tag{2.41}$$

$$a_{22_1} = -\frac{\frac{r_{Csw}}{2} + r_{L2} + \frac{r_{S2}}{2} + \frac{r_{CH} \cdot r_H}{r_{CH} + r_H}}{L_2} \tag{2.42}$$

$$a_{21_1} = \frac{r_{Csw} - r_{S3}}{2 \cdot L_2},\ a_{23_1} = -\frac{1}{L_2},\ a_{25_1} = \frac{r_H}{L_2 \cdot (r_{CH} + r_H)}, \tag{2.43}$$

$$a_{31_1} = -\frac{1}{2 \cdot C_{sw}},\ a_{32_1} = -a_{31_1}, \tag{2.44}$$

$$a_{41_1} = \frac{r_L}{C_L \cdot (r_{CL} + r_L)},\ a_{44_1} = \frac{-1}{C_L \cdot (r_{CL} + r_L)}, \tag{2.45}$$

$$a_{52_1} = \frac{-r_H}{C_H \cdot (r_{CH} + r_H)},\ a_{55_1} = \frac{-1}{C_H \cdot (r_{CH} + r_H)}, \tag{2.46}$$

and the elements of the input matrix (B_1):

$$b_{11_1} = \frac{-r_{CL}}{L_1 \cdot (r_{CL} + r_L)},\ b_{22_1} = \frac{r_{CH}}{L_2 \cdot (r_{CH} + r_H)}, \tag{2.47}$$

$$b_{41_1} = \frac{1}{C_L \cdot (r_{CL} + r_L)},\ b_{52_1} = \frac{1}{C_H \cdot (r_{CH} + r_H)}. \tag{2.48}$$

Based on the schematic from Fig. 2.8, relations (2.37), (2.38) and (2.39), are used to express the elements of the state matrix (A_2), for t_{off} switching interval:

$$a_{11_2} = -\frac{r_{L1} + r_{S1} + \frac{r_{CL} \cdot r_L}{r_{CL} + r_L}}{L_1},\ a_{12_2} = \frac{r_{S1}}{L_1},\ a_{13_2} = 0,\ a_{14_2} = \frac{-r_L}{L_1 \cdot (r_{CL} + r_L)}, \tag{2.49}$$

$$a_{22_2} = -\frac{2 \cdot r_{Csw} + r_{L2} + r_{S1} + \frac{r_{CH} \cdot r_H}{r_{CH} + r_H}}{L_2}, \tag{2.50}$$

$$a_{21_2} = -\frac{r_{S1}}{L_2},\ a_{23_2} = -\frac{2}{L_2},\ a_{25_2} = \frac{r_H}{L_2 \cdot (r_{CH} + r_H)} \tag{2.51}$$

$$a_{31_2} = 0,\ a_{32_2} = \frac{1}{C_{sw}},\ a_{41_2} = \frac{r_L}{C_L \cdot (r_{CL} + r_L)},\ a_{44_2} = \frac{-1}{C_L \cdot (r_{CL} + r_L)}, \tag{2.52}$$

$$a_{52_2} = \frac{-r_H}{C_H \cdot (r_{CH} + r_H)},\ a_{55_2} = \frac{-1}{C_H \cdot (r_{CH} + r_H)}, \tag{2.53}$$

and the elements of the input matrix (B_2):

$$b_{11_2} = \frac{-r_{CL}}{L_1 \cdot (r_{CL} + r_L)},\ b_{22_2} = \frac{r_{CH}}{L_2 \cdot (r_{CH} + r_H)}, \tag{2.54}$$

$$b_{41_2} = \frac{1}{C_L \cdot (r_{CL} + r_L)},\ b_{52_2} = \frac{1}{C_H \cdot (r_{C_H} + r_H)}. \tag{2.55}$$

In order to express the two discontinuous systems as one continuous system, the state equations can be averaged according to the dynamic duty cycle, d, as:

$$\dot{x} = (d \cdot A_1 + (1-d) \cdot A_2) \cdot x + (d \cdot B_1 + (1-d) \cdot B_2) \cdot u, \tag{2.56}$$

which results in a continuous but nonlinear system, also called a large-signal model.

In order to apply the theory of linear systems, the model from (2.56) can be linearized by considering small variations around a steady state point, for the state variables, x, duty cycle, d, and outputs, y:

$$x = X + \tilde{x}, \quad d = D + \tilde{d}, \quad y = Y + \tilde{y}. \tag{2.57}$$

The newly formed system, has the small signal variation of the duty cycle considered as input:

$$\begin{cases} \dot{\tilde{x}} = A_e \cdot \tilde{x} + B_e \cdot \tilde{d} \\ \tilde{y} = C_e \cdot \tilde{x} \end{cases}, \tag{2.58}$$

with the equivalent state (A_e) and input (B_e) matrices calculated as:

$$A_e = (A_1 \cdot D + A_2 \cdot (1-D)), \tag{2.59}$$

$$B_e = ((A_1 - A_2) \cdot X + (B_1 - B_2) \cdot u). \tag{2.60}$$

The output matrices, C_{e1} and C_{e2}, are defined for the system to output the i_{L1} and the i_{L2} current, respectively:

$$C_{e1} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \end{bmatrix},\ C_{e2} = \begin{bmatrix} 0 & 1 & 0 & 0 & 0 \end{bmatrix}. \tag{2.61}$$

A control to output transfer function can be calculated with:

$$\tilde{y} = C_e \cdot (s \cdot I - A_e)^{-1} \cdot B_e \cdot \tilde{d}. \tag{2.62}$$

Using the two output matrices, the transfer functions of the system are:

$$G_{P1}(s) = \frac{\tilde{y}}{\tilde{d}} = \frac{\tilde{i}_{L1}}{\tilde{d}}, \tag{2.63}$$

$$G_{P2}(s) = \frac{\tilde{y}}{\tilde{d}} = \frac{\tilde{i}_{L2}}{\tilde{d}}. \tag{2.64}$$

Using the parameters of the BHSC1 from Table 2.1, the two transfer functions are calculated as:

$$G_{P1}(s) = \frac{8.28 \cdot 10^5 \cdot s^4 + 1.58 \cdot 10^{10} \cdot s^3 + 6.04 \cdot 10^{13} \cdot s^2 + 4.63 \cdot 10^{16} \cdot s + 9.34 \cdot 10^{19}}{s^5 + 1.93 \cdot 10^4 \cdot s^4 + 7.84 \cdot 10^7 \cdot s^3 + 7.72 \cdot 10^{10} \cdot s^2 + 1.25 \cdot 10^{14} \cdot s + 3.01 \cdot 10^{16}}, \tag{2.65}$$

$$G_{P2}(s) = \frac{1.54 \cdot 10^5 \cdot s^4 + 3.01 \cdot 10^9 \cdot s^3 + 1.22 \cdot 10^{13} \cdot s^2 + 1.01 \cdot 10^{16} \cdot s + 1.38 \cdot 10^{19}}{s^5 + 1.93 \cdot 10^4 \cdot s^4 + 7.84 \cdot 10^7 \cdot s^3 + 7.72 \cdot 10^{10} \cdot s^2 + 1.25 \cdot 10^{14} \cdot s + 3.01 \cdot 10^{16}}, \tag{2.66}$$

The BHSC1 is a bidirectional converter, therefore a method for controlling the power flow is desired. One of the two inductor currents is chosen as output of the system because the current through inductors is a state variable and by controlling one inductor current, the power flow is indirectly controlled. Because the i_{L1} current is larger than i_{L2}, it will be further used as the control variable of the system.

The Bode plots of the two transfer functions from (2.65) and (2.66), are presented in Fig. 2.9. In addition, Bode plots were also obtained from the simulations of the switching model of the BHSC1, realized in the PSIM software. The simulation is performed by introducing small oscillations around a constant duty cycle and by measuring its influence at the output. As the simulation uses a switching model of the converter, its accuracy is very precise, but a long simulation time is required (approximately 1h on i7-4800MQ CPU @ 2.7GHz with PSIM v12). As shown in the figure, the SSA method is very close to the simulation results, therefore it can be used for a faster analysis. Other methods for obtaining the Bode plot for the BHSC1 are also possible, such as the PWM switch model presented in [67].

Table 2.1. BHSC1 parameters for the dynamic analysis

Element	**Value**	**Unit**	**Description**
V_H	400	V	Nominal voltage at the high voltage side
V_L	50	V	Nominal voltage at the low voltage side
C_H	470	μF	Capacitance of the high voltage side capacitor
C_L	470	μF	Capacitance of the low voltage side capacitor
C_1, C_2	705	μF	Capacitance of the switched capacitors
L_1	270	μH	Inductance of the low voltage side inductor
L_2	1.47	mH	Inductance of the high voltage side inductor
r_{S1}, r_{S2}, r_{S3}	10	mΩ	On-state resistance of the switches
r_H	350	mΩ	Parasitic resistance of the supply line at V_H
r_L	50	mΩ	Parasitic resistance of the supply line at V_L
r_{CH}	100	mΩ	Equivalent series resistance of C_H
r_{CL}	100	mΩ	Equivalent series resistance of C_L
r_{C1}	50	mΩ	Equivalent series resistance of C_1
r_{L1}	4.5	mΩ	Low voltage side inductor resistance
r_{L2}	158	mΩ	High voltage side inductor resistance
T	50	μs	Switching period
f	20	kHz	Switching frequency
D	0.24	-	Duty cycle of the steady state operation point
I_{L1}	55	A	Steady state value of the L_1 inductor current

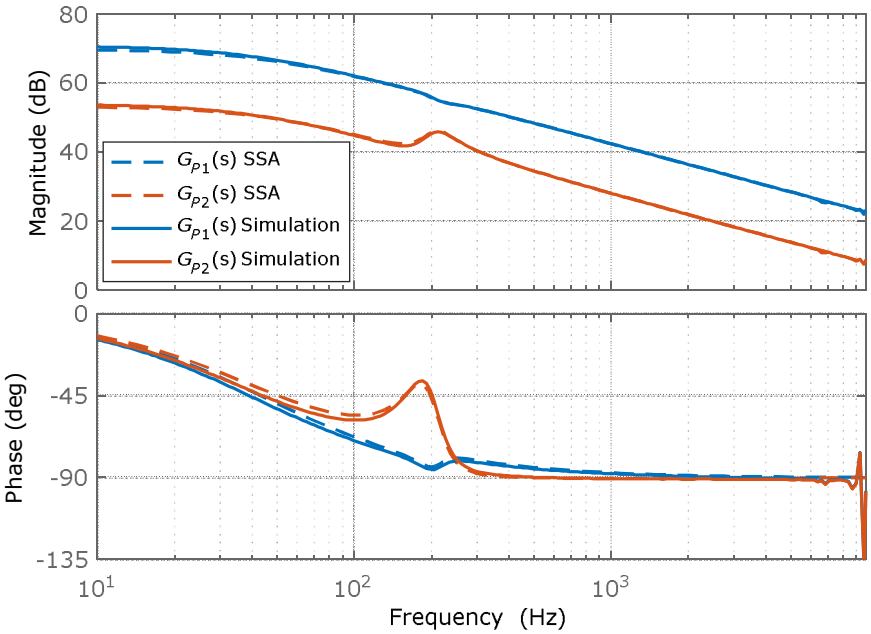

Fig. 2.9. Open loop Bode plots of the BHSC1 dynamic model : continuous time model of G_{P1}(s) and G_{P2}(s), obtained by SSA method or through the simulation of the converter switching model realized in PSIM software

2.5. Valley Current Mode Control

A controller was required for an initial test of the BHSC1 in a bidirectional setup, a controller that is easy to implement, operates at a constant switching frequency, has an analog implementation, does not require any tuning and it has a stable and robust operation. To meet these requirements, a Valley Current Mode (VCM) control was used with the BHSC1 [66]. The VCM control was chosen in favor of the Peak Current Mode control, as i_{L1} current was measured for boost operation ($-i_{L1}>0$ ↔ step-up operation), where high step-up duty cycles (D') are required therefore no compensating ramp is needed [69].

Even if the BHSC1 is represented with MOSFET transistors, IGBT transistors with antiparallel diodes can be used as well. A prototype using the SKM75GB123 IGBT modules was built in order to benefit from the higher voltage and power capabilities of the IGBT modules for a lower cost.

The setup used to test the prototype is presented in Fig. 2.11. The parameters for the BHSC1 are presented in Table 2.1. In order to make possible a bidirectional operation, the setup uses a battery bank for the V_L side, and a DC voltage source connected in parallel to a resistor load, R_{load}, on the V_H side.

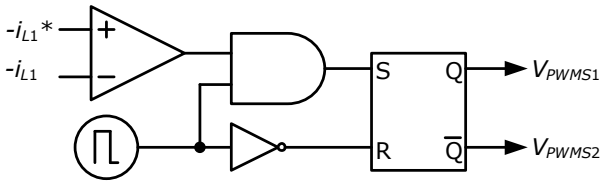

Fig. 2.10. Valley Current Mode control (VCM) schematic for the BHSC1 control. The control is realized from the step-up perspective, therefore -i_{L1} is used in the loop

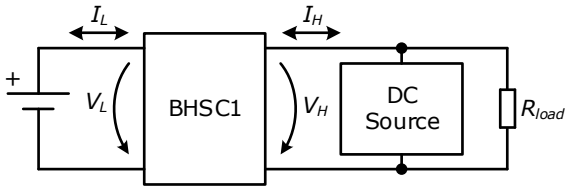

Fig. 2.11. Experimental test setup consisting of the BHSC1 converter , a battery on V_L side, and a DC source in parallel to a load Resistance, R_{load}, on the V_H side for bidirectional operation

Table 2.2. Experimental setup equipment for the BHSC1

Element	**Device**	**Manufacturer**	**Characteristics**
Battery	6 OPzV.block.solar 420	Moll Solar	6x8V, 421Ah
DC Source	TC.P.10.400.400.S	Regatron	0-10kW, 0-400V, 0-50A
R_{load}	-	-	39 Ohm/ 8kW

Experimental and simulation results are presented from Fig. 2.12 to Fig. 2.16, in steady state and transient operation, for both step-up and step-down modes in order to show the basic operation of the BHSC1 and to show the performance of the controller.

The first set of results present the steady state operation, in Fig. 2.12 and Fig. 2.13 for step-down and step-up operation, respectively. The controlled current, i_{L1}, and the two inductor voltages, v_{L1}, v_{L2}, are presented, and they show a good resemblance to the theoretical waveforms from Fig. 2.5. A good correspondence is observed between the simulation results and the experimental results.

The transient responses from Fig. 2.14 to Fig. 2.16, presents the operation of the BHSC1 while transitioning from step-up to step-down (Fig. 2.14) or vice versa (Fig. 2.15, Fig. 2.16), offering a fast and stable operation with no overshoot for the control variable. The PWM signals for the switches, V_{PWMS1} for S_1 and V_{PWMS2} for S_2/S_3, are shown in Fig. 2.14 and Fig. 2.15. If MOSFET transistors are used, active freewheeling can be achieved in order to improve the efficiency, and the driving signal can be applied during both operating modes for all transistors. A main difference between the two transitions, is between the rise or fall times, as the VCM control limits the maximum duty cycle, depending on the clock signal from Fig. 2.10.

Apart from the i_{L1}, the low and high voltage inputs waveforms, V_L, V_H, are also shown in Fig. 2.16 to show their variation during a transient response.

A Bode plot was obtained through simulation of the BHSC1 controlled by the VCM, in Fig. 2.17, which already confirms the previously obtained transient results. The phase margin, *PM*, of 100°, at the crossover frequency, f_c, of 3.12kHz, confirms a damped and stable response of the system.

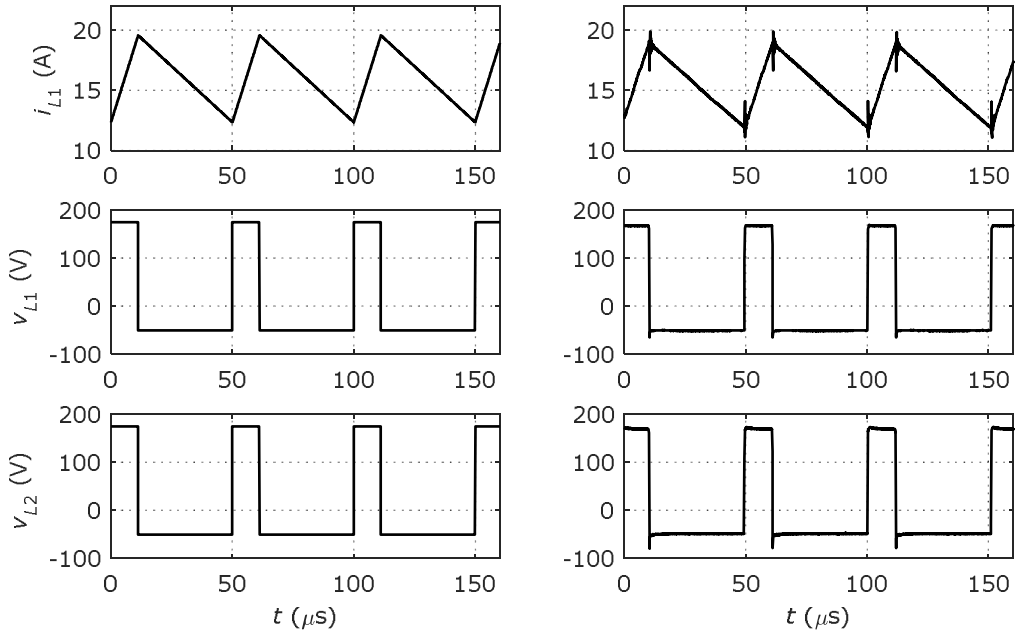

Fig. 2.12. BHSC1 simulation (left) and experimental (right) waveforms for steady state operation, operating at I_{L1}=16A, V_L=50V, V_H=400V, P_{in}=0.8kW, (i_{L1}, and v_{L1}, v_{L2} are the current and voltages for L_1 and L_2 inductors, respectively)

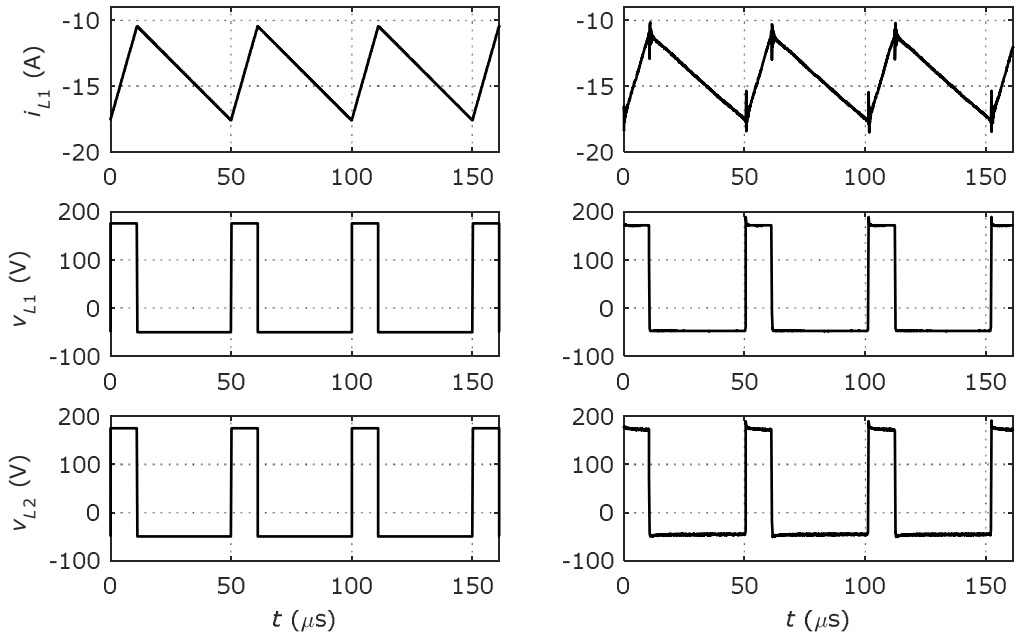

Fig. 2.13. BHSC1 simulation (left) and experimental (right) waveforms for steady state operation, operating at I_{L1}=-14A, V_L=50V, V_H=400V, P_{in}=0.7kW, (i_{L1}, and v_{L1}, v_{L2} are the current and voltages for L_1 and L_2 inductors, respectively)

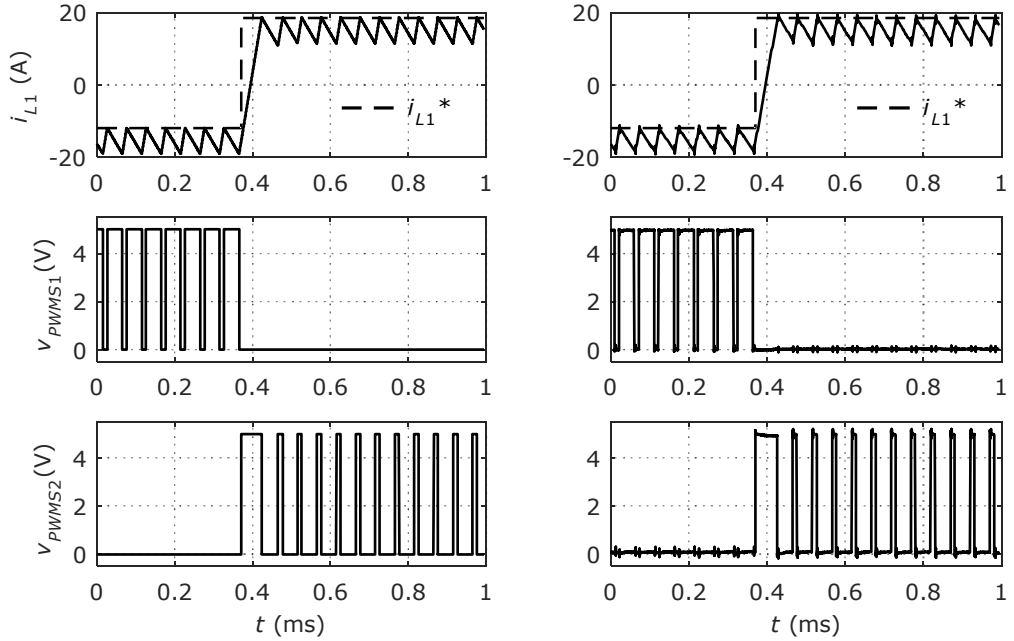

Fig. 2.14. BHSC1 simulation (left) and experimental (right) waveforms for transient operation, controlled by the VCM controller applied to -i_{L1}: transition from -i_{L1}*=12A (step-up) to -i_{L1}*=-18.6A (step-down), i_{L1} =±15A, V_L=50V, V_H=400V, P_{in}=±0.75kW, (i_{L1} is the current from L_1 inductor, V_{PWMS1}, V_{PWMS2} are the control signals for S_1 and S_2/S_3 switches, respectively)

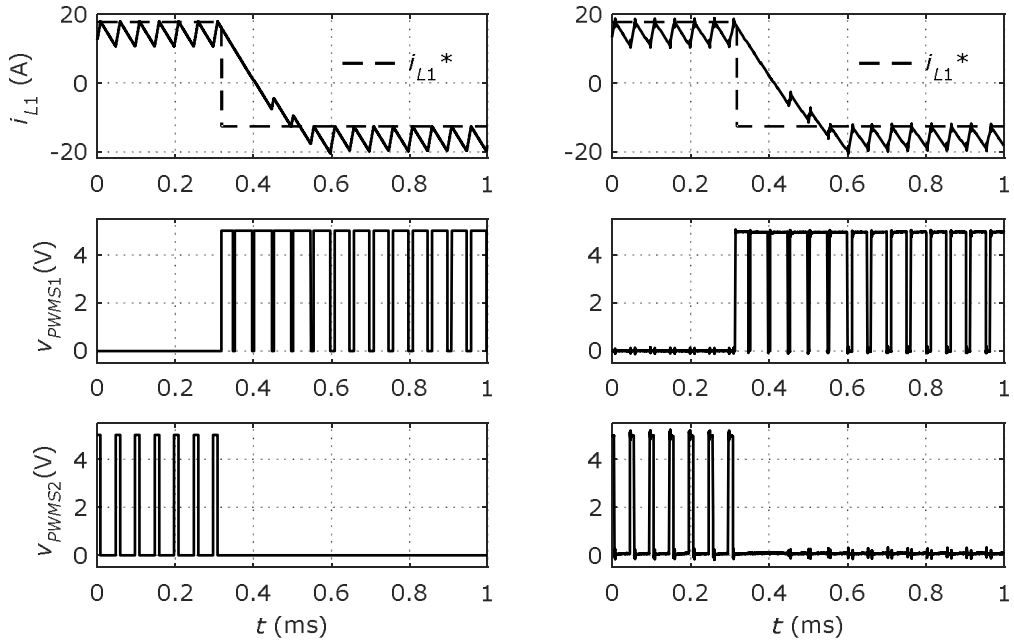

Fig. 2.15. BHSC1 simulation (left) and experimental (right) waveforms for transient operation, controlled by the VCM controller applied to -i_{L1}: transition from -i_{L1}*=-17.8A (step-down) to -i_{L1}*=12.7A (step-up), i_{L1} =±15A, V_L=50V, V_H=400V, P_{in}=±0.75kW, (i_{L1} is the current from L_1 inductor, V_{PWMS1}, V_{PWMS2} are the control signals for S_1 and S_2/S_3 switches, respectively)

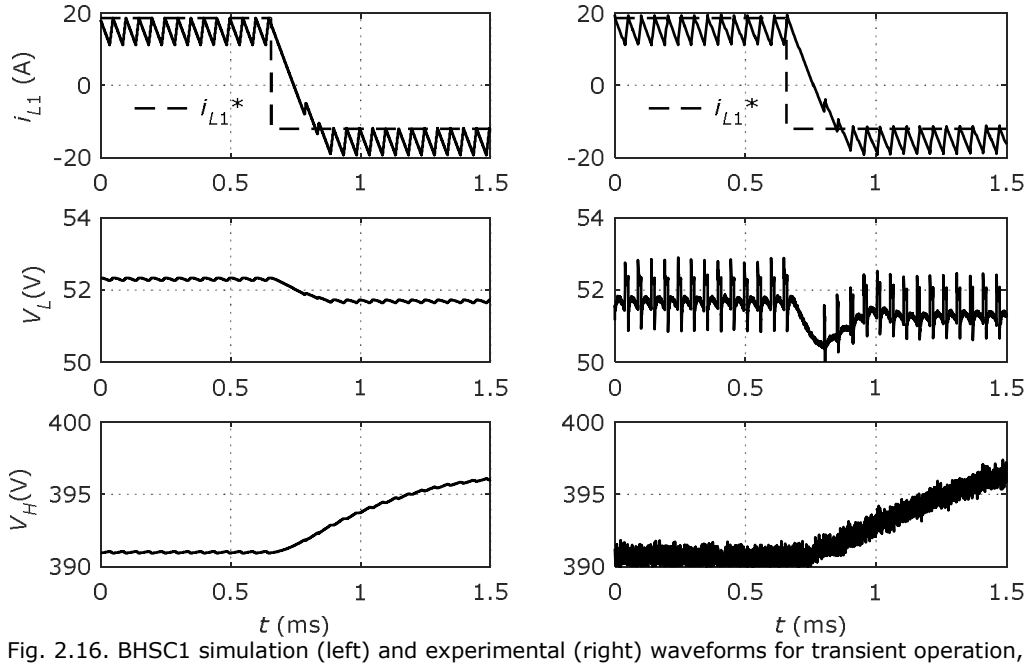

Fig. 2.16. BHSC1 simulation (left) and experimental (right) waveforms for transient operation, controlled by the VCM controller applied to -i_{L1}: transition from -i_{L1}*=-17.8A (step-down) to -i_{L1}*=12.7A (step-up), i_{L1} =±15A, V_L=52V, V_H=400V, P_{in}=±0.78kW, (i_{L1} is the current from L_1 inductor, V_L, V_H are the low and high voltage inputs, respectively)

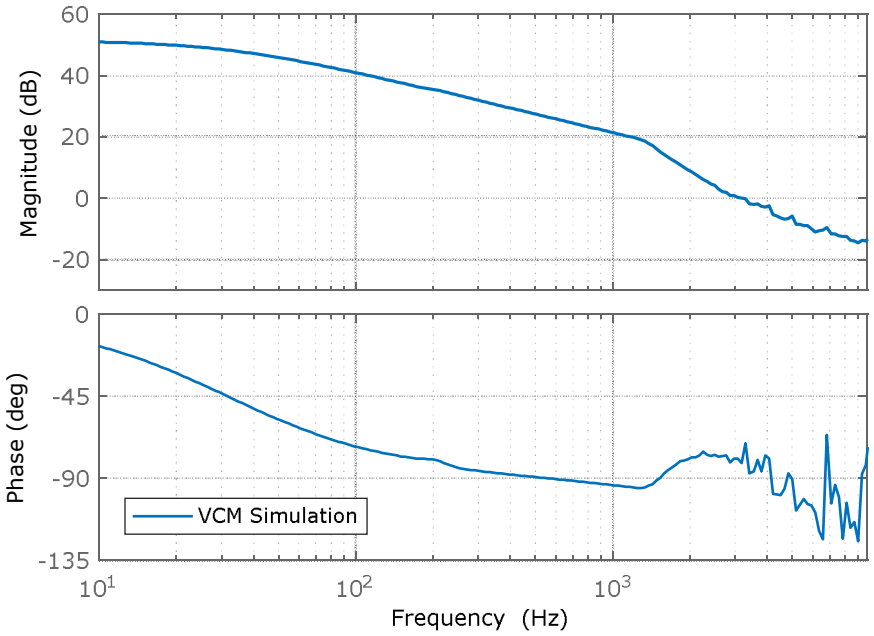

Fig. 2.17. Open loop Bode plots of the BHSC1 model controlled by the VCM control - results obtained through simulation of the converter switching model realized in PSIM software: PM=100°, f_c=3.12kHz

Even if the BHSC1 is capable of operating with a fast transition between the two operating modes, as already presented in Fig. 2.12 to Fig. 2.16, because the i_{L2} current is not controlled, large oscillations appear on this current when i_{L1} has fast transitions. For this reason, a first-order low pass filter (LPF) with the cutting frequency of 100Hz is used for filtering the reference current, i_{L1}*, in order to dampen the oscillations on the i_{L2} current. The simulation waveforms from Fig. 2.18 show the operation of the BHSC1 converter controlled by the VCM controller with or without an 100Hz LPF on the reference current i_{L1}*. It is shown that by slowing the overall dynamics of the system, the oscillations from i_{L2} are drastically reduced without introducing any other detriments in performances.

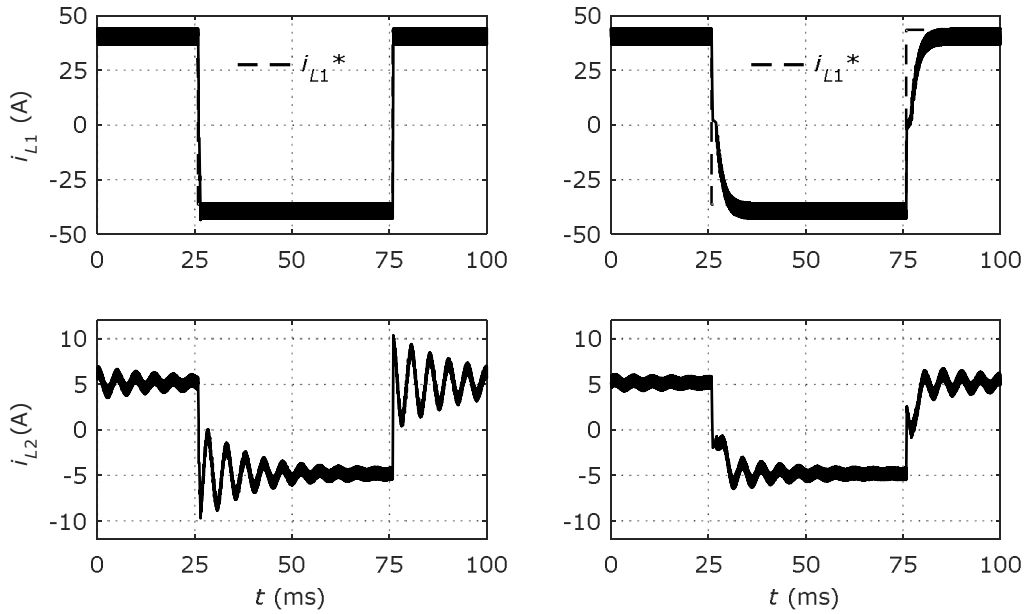

Fig. 2.18. Simulation waveforms for transient operation of the BHSC1 , controlled by the VCM controller with (right) or without (left) an 100Hz LPF applied to the reference, -i_{L1}*: i_{L1} =±40A, V_L=50V, V_H=400V, P_{in}=±2kW, (i_{L1}, i_{L2} are the currents from L_1 and L_2 inductors, respectively)

2.6. Analog Controller design

An additional analog controller was designed based on the SSA modelling provided in 2.4, specifically the Bode plot of the G_{P1}(s), which considers the i_{L1} as control variable for the BHSC1 converter [67].

The K factor method was used in order to design the controller, following the method described in [68]. The first step for the design was choosing the crossover frequency at f_c = 1.5kHz, which was chosen based on the switching frequency, f = 20kHz. According to Fig. 2.9, the gain of the transfer function at 1.5 kHz is 38dB, and the gain of the PWM modulator and sensor gain are 1. Based on the shape of the Bode plot, [68] suggest using a "Type II" controller, a transfer function with an integrator and a zero-pole pair, in order to obtain characteristics such as a stable system, fast dynamic, and zero error for steady-state operation.

To obtain the *PM*=70° at f_c=1.5kHz, with the 38dB gain of the system, the K factor method provides the following transfer function for the G_C(s) controller:

$$G_C(s) = \frac{1.75 \cdot 10^6 \cdot s + 3.851 \cdot 10^9}{2200 \cdot s^2 + 1.562 \cdot 10^8 \cdot s}. \tag{2.67}$$

The Bode plot of the G_C(s) controller is presented in Fig. 2.19. The open loop Bode plot of the controller and the BHSC1 model obtained by the SSA method, G_C(s)· G_{P1}(s), together with the PSIM simulation of the switching model of the converter controlled by the analog controller are presented in Fig. 2.20. A good concordance can be observed between both methods for obtaining the Bode plots, therefore the SSA method results are confirmed. The *PM* and the f_c confirm the initial design parameters.

The simulation and the experimental results from Fig. 2.21 and from Fig. 2.22 confirm the stable operation of the G_C(s) controller with the LPF. A good transition between the two operating modes, from step-up to step-down mode, in Fig. 2.21, or vice versa in Fig. 2.22, is observed. The experiment and the simulation results have a good resemblance except for the ripple currents from the inductors, which have been filtered by the oscilloscope during measurement. If the LPF is used in order to limit the oscillations of i_{L2}, the rise time of the current is slowed down to 5ms, approximately 10 times slower.

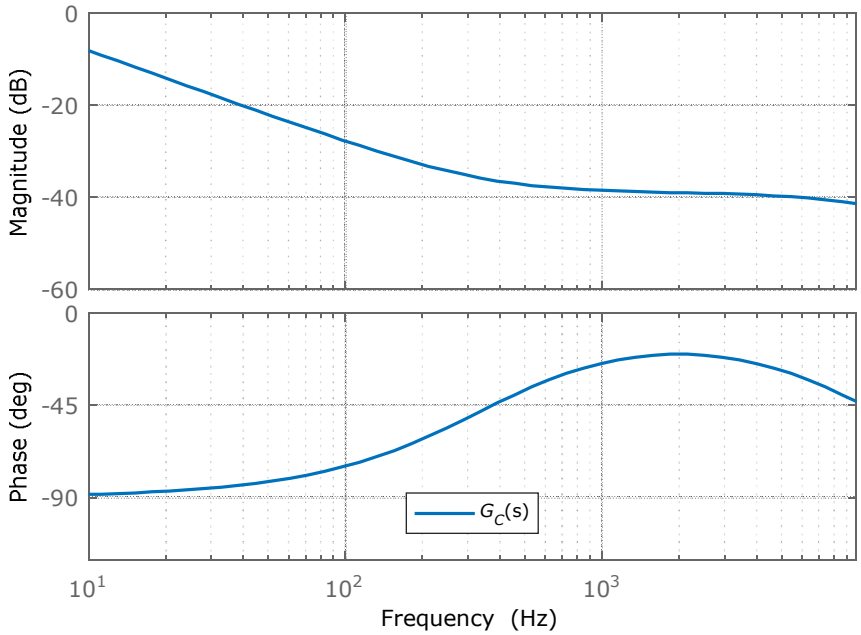

Fig. 2.19. Bode plot of the "Type II" G_C(s) controller designed for the BHSC1 using the K factor method [68]

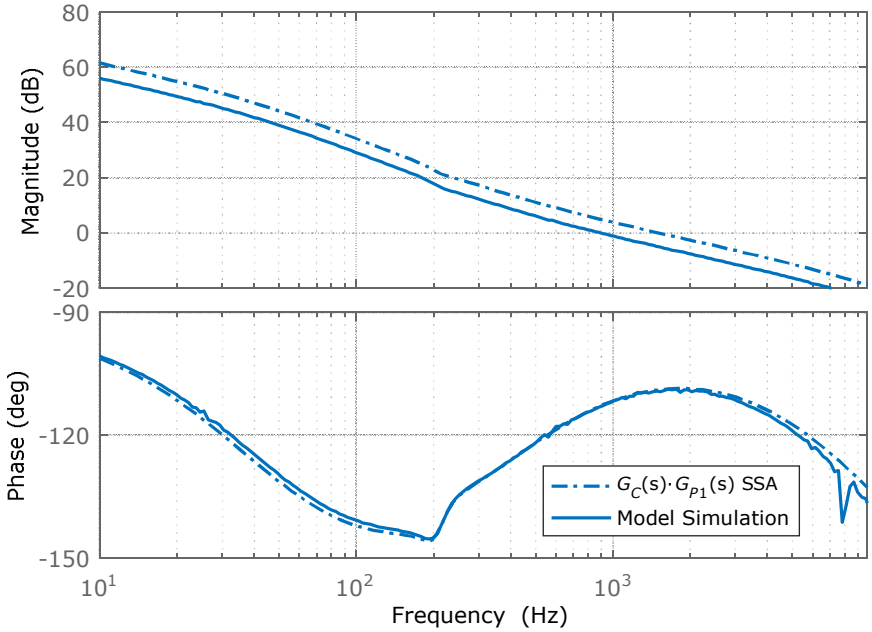

Fig. 2.20. Open loop Bode plots of the BHSC1 model controlled by $G_C(s)$: response of the SSA model, $G_C(s) \cdot G_{P1}(s)$; the Model Simulation with analog controller and switching model of the BHSC1⇒ PM=71°, f_c=1.5kHz

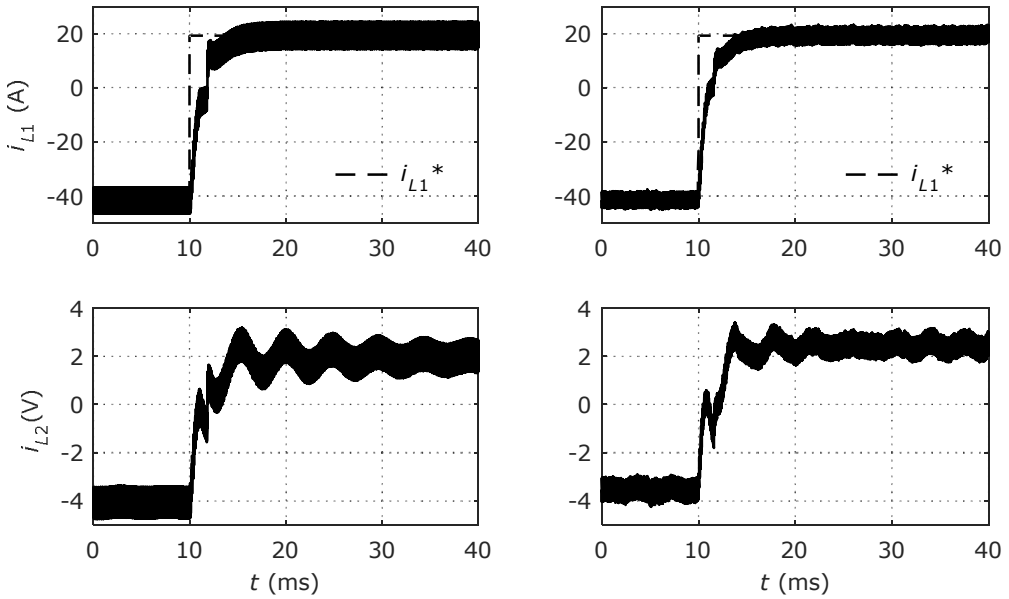

Fig. 2.21. BHSC1 simulation (left) and experimental (right) waveforms for transient operation, controlled by the $G_C(s)$ controller with LPF at 100Hz on i_{L1}*: transition from i_{L1}*=-40A (step-up) to i_{L1}*=20A (step-down), V_L=50V, V_H=400V, P_{in}=-2/1kW, (i_{L1} and i_{L2} are the currents from L_1 and L_2 inductors, respectively)

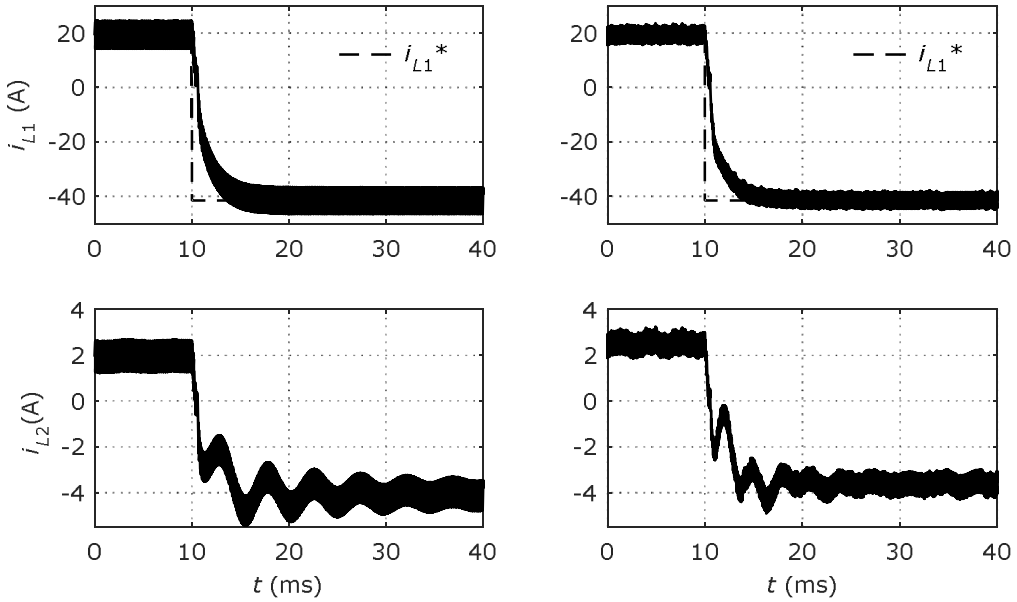

Fig. 2.22. BHSC1 simulation (left) and experimental (right) waveforms for transient operation, controlled by the G_C(s) controller with LPF at 100Hz on i_{L1}*: transition from i_{L1}*=20A (step-down) to i_{L1}*=-40A (step-up), V_L=50V, V_H=400V, P_{in}=1/-2kW, (i_{L1} and i_{L2} are the currents from L_1 and L_2 inductors, respectively)

2.7. Digital Controller design

The digital current controller was designed starting from the Bode plots presented in Fig. 2.9 and the continuous dynamic model of BHSC1 from (2.65). In order to design the digital controller, a discrete transfer function is required for the BHSC1 model. Therefore, the system from (2.65) is discretized using the Zero Order Hold (ZOH) method as:

$$G_{P10}(z) = (1 - z^{-1})\,\mathcal{Z}\left[\frac{G_{P1}(s)}{s}\right]. \tag{2.68}$$

As the digital controller is implemented in a microcontroller (TMS320F28335), it is important to consider its influence on the system. The chosen microcontroller, as many other, uses a trigger for acquiring the ADC signal at half of the t_{on} switching period in order to avoid any switching noise and to obtain an average value for the measured current. Because of this operating method, an additional delay equal to one sampling period, T, must be introduced to the discrete model in order to have a more accurate model. The delay can be introduced with a z^{-1} in the discrete model, or by using a Padé approximation of a time delay in the s domain. Therefore, the more accurate discrete model is:

$$G_{P1}(z) = z^{-1} \cdot G_{P1}(z) \tag{2.69}$$

The Bode plots of the two discretized models are compared with the Bode plots obtained from the PSIM simulation of the BHSC1 converter with the added

microcontroller, in Fig. 2.23. The Bode plots show that the final discretized model is in good concordance with the simulation model, therefore it can be used for the controller design.

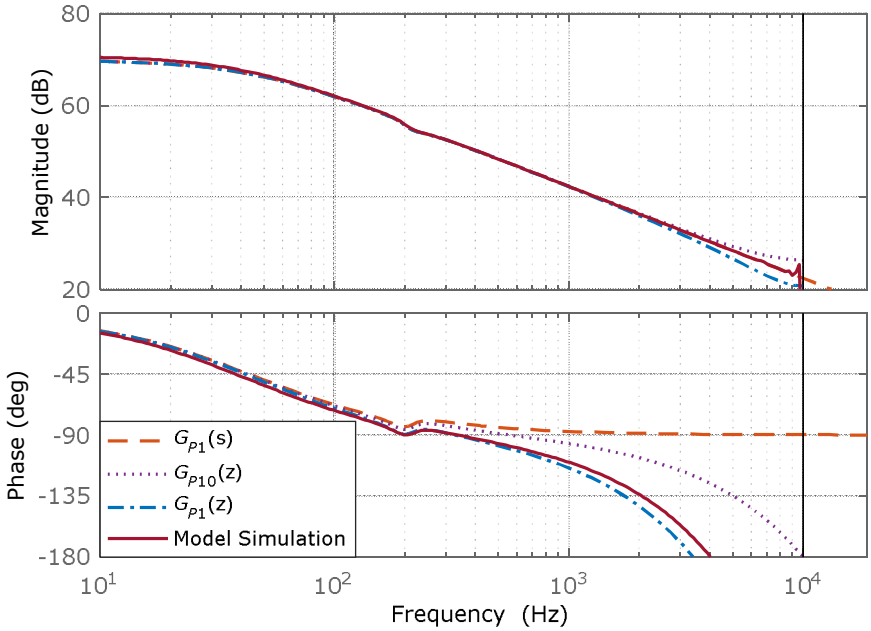

Fig. 2.23. Open loop Bode plots of the BHSC1 dynamic model : continuous time model - G_{P1}(s); ZOH discretized model accounting for the PWM hold - G_{P10}(z); discretized transfer function including an additional ADC delay G_{P1}(z); the Model Simulation which also includes the microcontroller (TMS320F28335) and the switching model of the converter

The i_{L1} current controller was designed based on the Bode plot of G_{P1}(z), from Fig. 2.23. The controller was designed by directly shaping the open loop Bode plot of the system through changes made in the controller, such that the following requirements are met: fast response, zero steady state error, a small overshoot (≤10%) which is achievable with a phase margin (*PM*) of approximately 60°, a gain margin (*GM*) greater or close to 10dB, and a cutoff frequency (f_c) lesser than 25% of the switching frequency of the converter.

In order to satisfy the requirements, a pole was added in the origin to eliminate the steady state error, and a zero was added while adjusting the gain of the controller for achieving the rest of the requirements. The procedure was performed in the MATLAB software with the help of the controlSystemDesigner application, which also plots the step signal response and the Root Locus of the system.

The Bode plot of the open loop system, consisting of G_{Cd}(z) · G_{P1}(z), is presented in Fig. 2.24, together with the simulated response. The required performances are achieved, having phase margin of 60.7° at the cutoff frequency of 1.11kHz and the gain margin of 10.5dB.

The final transfer function of the controller is:

$$G_{Cd} = 8.5763 \cdot 10^{-3} \cdot \frac{z - 0.989}{z - 1}, \tag{2.70}$$

and its Bode plot is presented in Fig. 2.25.

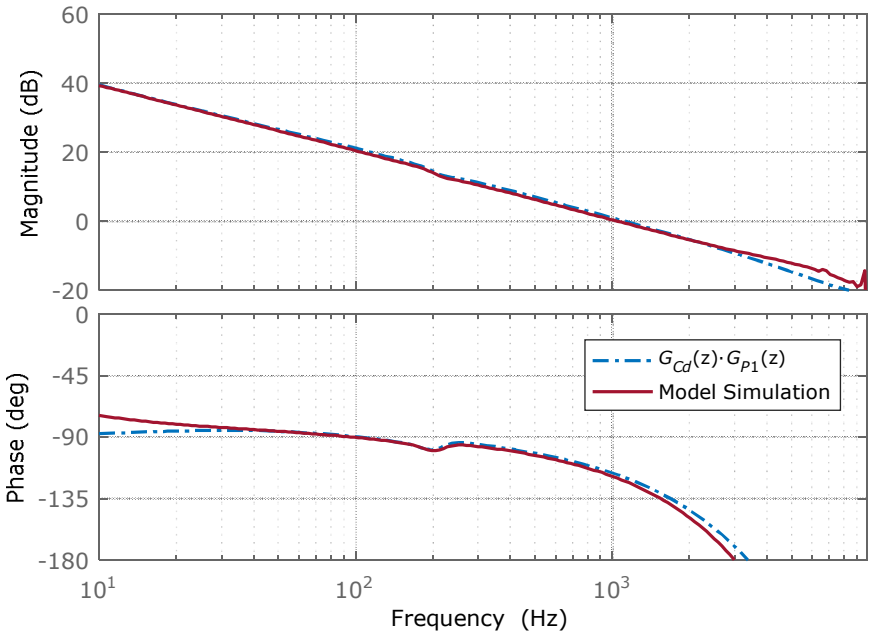

Fig. 2.24. Open loop Bode plots of the BHSC1 model controlled by $G_{Cd}(z)$: discrete model, $G_{Cd}(z) \cdot G_{P1}(z) \Rightarrow PM$=60.7°, f_c=1.11kHz, GM=10.5dB; the Model Simulation including the microcontroller (TMS320F28335) and switching model of BHSC1

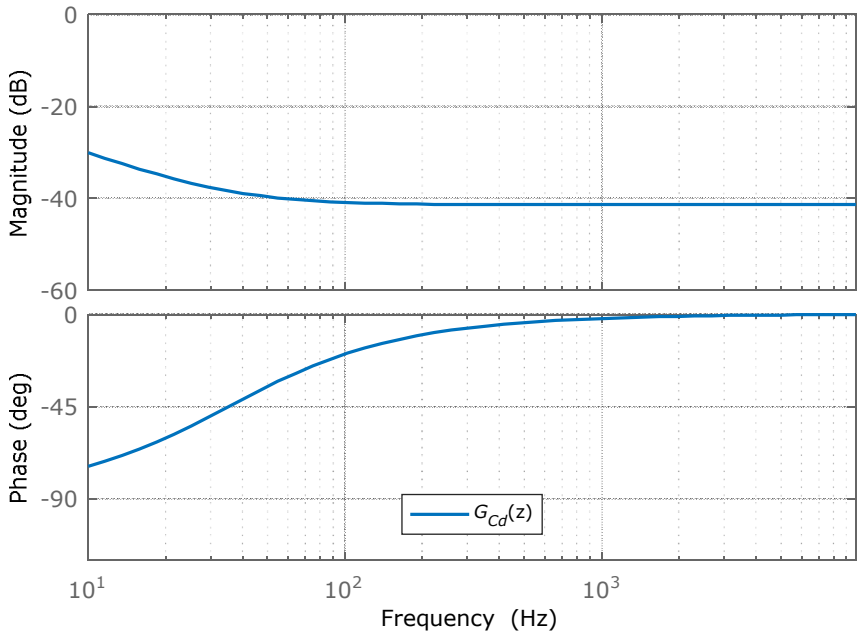

Fig. 2.25. Bode plots of the $G_{Cd}(z)$ controller designed for the model of the BHSC1 which includes the additional delay

Comparing the digital to the analog implementation, it appears that better performance could be achieved in the analog structure, as the system is not limited by the Nyquist frequency limit. The discrete controller could not benefit from the structure of the Type II controller used for the analog controller, but a simple PI structure achieves acceptable results for the discrete domain.

Simulations for the BHSC1 converter with the discrete controller, $G_{Cd}(z)$, are presented in Fig. 2.26, with the LPF applied for the reference in order to limit the i_{L2} current oscillations. The operation of the converter with the discrete controller is similar to its operation with the analog controller, presented in Fig. 2.21 and Fig. 2.22.

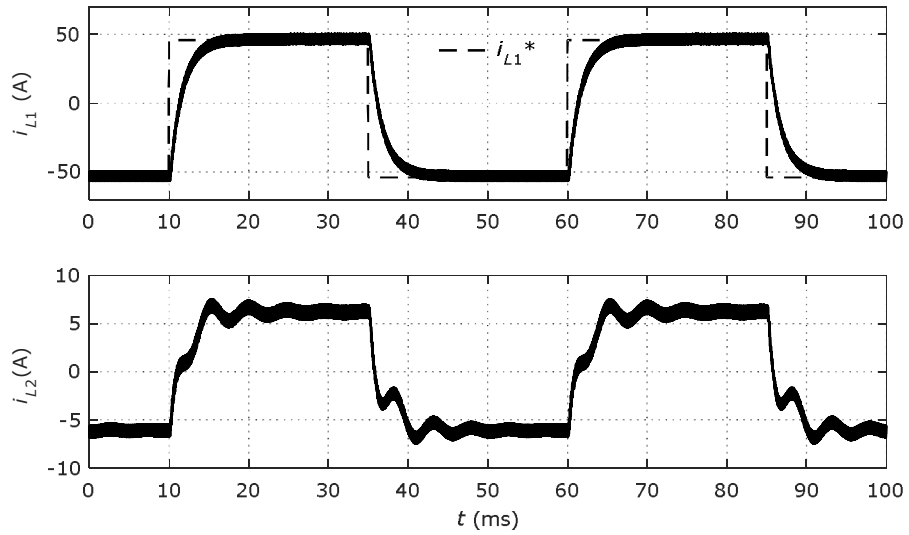

Fig. 2.26. Simulation waveforms for transient operation of the BHSC1, controlled by the $G_{Cd}(z)$ controller with an 100Hz LPF applied to the reference (i_{L1}*), implemented in the microcontroller (TMS320F28335): i_{L1} =±50A, V_L=50V, V_H=400V, P_{in}=±2.5kW, (i_{L1}, i_{L2} are the currents from L_1 and L_2 inductors, respectively)

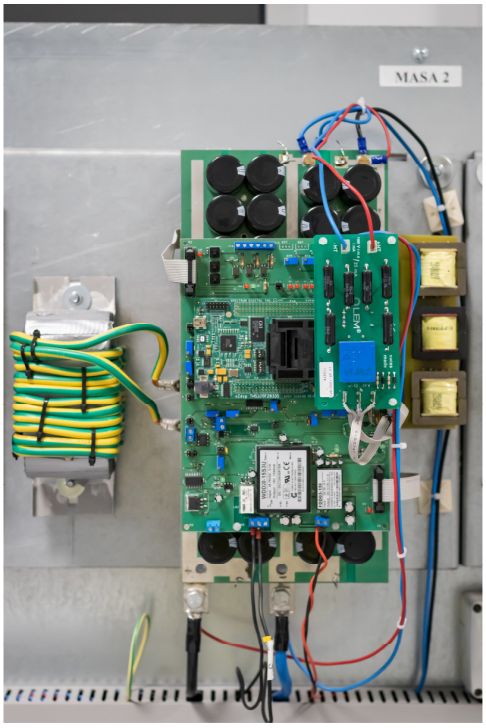

Fig. 2.27. BHSC1 prototype

2.8. Topology improvements

The BHSC1 topology, presented in Fig. 2.2, has benefits in terms of conversion ratio when compared to the CBBB, but it does not have the advantage of the a common ground between the two inputs. This disadvantage is more significant considering that the voltage between the two inputs, V_H and V_L, has a frequency equal to the switching frequency.

In order to eliminate this disadvantage, few changes can be made with the BHSC1 schematic, without losing its advantages. The main change is splitting L_1, L_2 or both inductors, into two, one on the high side and the other on the low side, so that the voltage between the two inputs, will be constant. The two inductors from one side can be magnetically coupled in order to reduce the size of the inductor housings. The new improved schematic is presented in Fig. 2.28, with the two coupled inductors on each input.

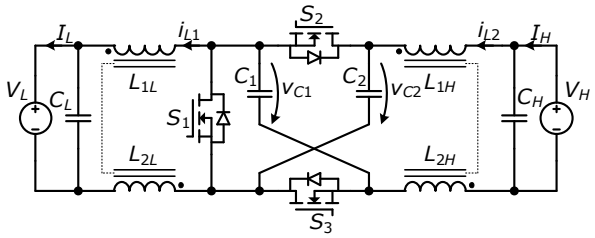

Fig. 2.28. The Improved Bidirectional Hybrid Switched Capacitor converter (I-BHSC1)

2.9. Conclusions

A theoretical analysis was performed for the BHSC1 converter for the steady state and dynamic operation. The analytical description of the BHSC1 is desired in order to obtain the metrics used for comparing this topology to other converters. The dynamic modeling was performed in order to obtain the linear model of the BHSC1, which was used for designing an analog and a digital controller. Simulations for both controllers were realized, using models for the analog components and for the microcontroller respectively. A valley current mode controller was also tested with similar results.

As a single inductor current controller was used, and because of the increased number of state variables, damped oscillations were observed in the second inductor current. The oscillations were attenuated by slowing down the controller with the help of a low pass filter placed at the reference.

The simulation results have a good similitude to the dynamic results obtained by mathematical analysis, and with the experimental results, for the transient operation.

Finally, an improved topology is proposed for the BHSC1, which eliminates the high frequency voltage between the two inputs, without decreasing its performances.

3. THE BIDIRECTIONAL HYBRID SWITCHED CAPACITOR CONVERTER (BHSC2)

3.1. Abstract

This chapter presents another Bidirectional Hybrid Switched Capacitor converter (BHSC2) which uses a different switched capacitive cell in its structure, achieving the same benefit of high voltage conversion ratio as the BHSC1 but with the added benefit of common ground between the two inputs. This advantage helps to achieve simple multiphase operation, or it allows the upgrade of the topology in a multi-level structure. Similar to the BHSC1, this chapter includes the steady state and the dynamic analysis of the BHSC2. The stability of the converter is investigated from the frequency response, and from the poles and zeros of the system. The influence of the passive components is analyzed in order to achieve the best design in terms of stability. A controller is designed for the BHSC2, and simulation results are used to demonstrate the transient operation of the converter between step-up and step-down operation modes. Since the BHSC2 has a common ground between inputs, an extended multilevel structure is proposed.

3.2. Overview

The BHSC2 schematic is developed from the Unidirectional Hybrid Switched Capacitor converter (UHSC2), presented in Fig. 3.1, which was initially proposed in [42] for step-down operation. The UHSC2 was experimentally tested in [70], with good results. The unidirectional topology uses a switched capacitor cell (D_2, D_3, D_4, C_2, C_1) at the input of a conventional buck converter, which helps divide the input voltage during the t_{on} switching interval.

The BHSC2, shown in Fig. 3.2, was proposed in [71], and analyzed for steady state and dynamic operation, addressing the sizing and stability of the converter. The main difference between the BHSC2 and the UHSC2, is the use of transistors, in place of diodes, achieving bidirectional current flow through switches. Similar to the CBBB presented in 1.3.1, positive currents indicate step-up operation, while negative currents indicate step-down operation. Even if the converter uses 5 switches, only one driving signal is used, applied directly to S_1, S_3 and S_5, and inverted for S_2 and S_4.

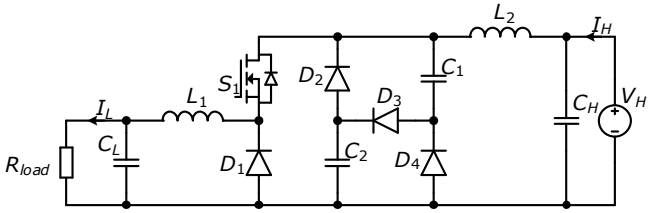

Fig. 3.1. The Unidirectional Hybrid Switched Capacitor converter (UHSC2) [42], [70]

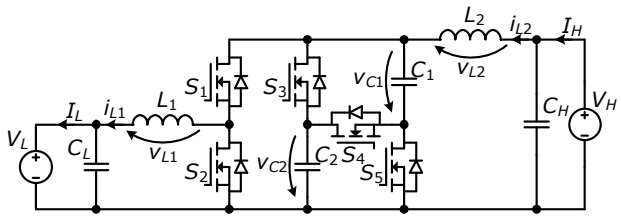

Fig. 3.2. The Bidirectional Hybrid Switched Capacitor converter (BHSC2) [71]
(i_{L1}, i_{L2} >0 ↔ step-down operation; i_{L1}, i_{L2} < 0 ↔ step-up operation)

3.3. Steady state analysis

The steady state analysis of the BHSC2 is performed starting from the equivalent switching schematics for the two switching intervals, t_{on} and t_{off}, presented in Fig. 3.3 and Fig. 3.4, respectively. The BHSC2 converter operates like the UHSC2 converter, therefore the two capacitors from the switching cells are considered identical, and the voltage across them equal ($v_{C1} = v_{C2} = V_{Csw}$).

During the t_{on} interval, the two capacitors are connected in parallel through the inductors, between the two inputs (V_H and V_L).

During the t_{off} interval, the capacitors are connected in series to the high voltage side, V_H, with the L_2 inductor, and L_1 inductor is connected in parallel to the low voltage side, V_L.

The i_{L1} current indicates the charge or discharge of the switched capacitors (C_1, C_2) during t_{on}, as their current is $i_{C1} = i_{C2} = (i_{L2} - i_{L1})/2$, and i_{L1} is always larger than i_{L2}. During t_{off} the charging or discharging of the capacitors is dictated solely by the i_{L2} current.

Based on the two equivalent schematics, the main theoretical waveforms are shown in Fig. 3.5.

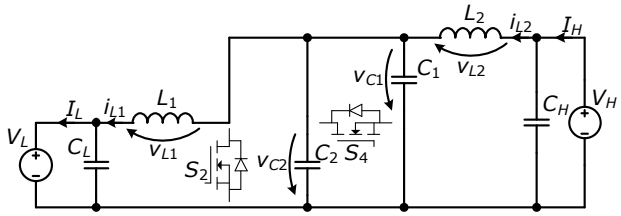

Fig. 3.3. Equivalent schematic of BHSC2 during t_{on} interval
(S_1, S_3 and S_5 is turned ON, S_2 and S_4 are turned OFF)

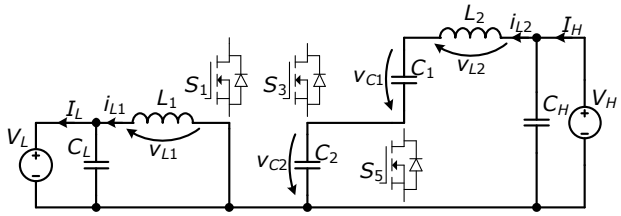

Fig. 3.4. Equivalent schematic of BHSC2 during t_{off} interval
(S_1, S_3 and S_5 is turned OFF, S_2 and S_4 are turned ON)

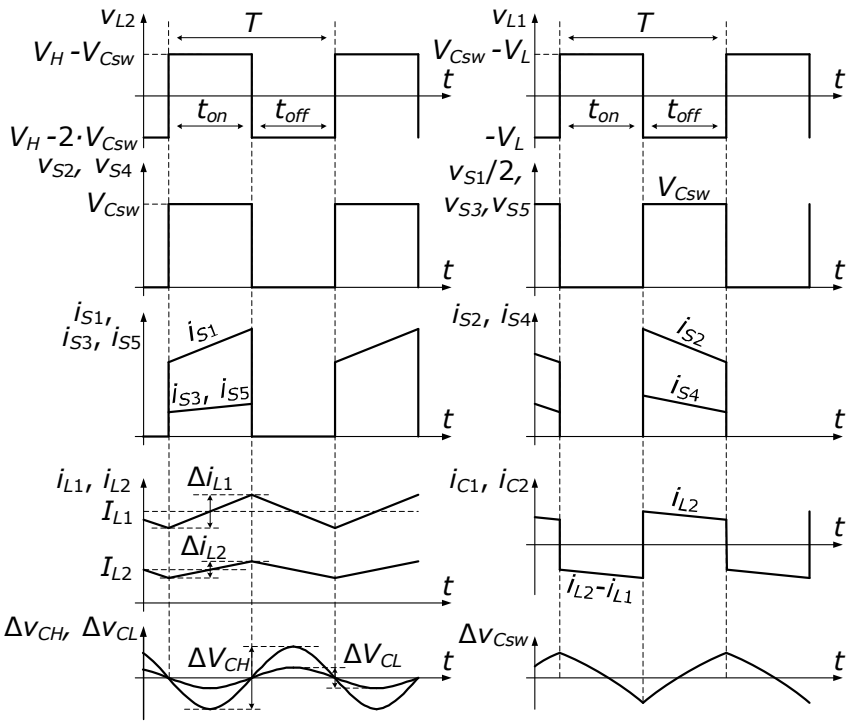

Fig. 3.5. Main theoretical waveforms of the BHSC2: L_1, L_2 inductor voltages and currents (v_{L1}, v_{L2}, i_{L1}, i_{L2}); S_1, S_2 and S_3 switches voltages and currents (v_{S1} - v_{S5}, i_{S1} - i_{S5}); C_1, C_2 switched capacitors currents (i_{C1}, i_{C2}); ripple voltages on the capacitors (Δv_{CH}, Δv_{CL}, Δv_{Csw})

Similar to the analysis of the CBBB converter, in 1.3.1, the steady state analysis of the BHSC2 begins by considering D the duty cycle for the step-down mode of operation, and D' the duty cycle for step-up mode:

$$D = \frac{t_{on}}{T},\ D' = \frac{t_{off}}{T}. \tag{3.1}$$

The inductor voltages corresponding to the two switching intervals are calculated from Fig. 3.3 and Fig. 3.4:

$$\begin{aligned} t_{on}&: v_{L1} = V_{Csw} - V_L,\ \ v_{L2} = V_H - V_{Csw}, \\ t_{off}&: v_{L1} = -V_L,\qquad\ \ v_{L2} = V_H - 2 \cdot V_{Csw}. \end{aligned} \tag{3.2}$$

The simplifying assumptions from 1.3.1 are used (ideal components, constant voltage on capacitors, steady state operation) and, in addition, identical capacitances, voltages and current for the switched capacitors are also considered. Therefore, the volt-second balance can be applied:

$$\begin{aligned} \langle v_{L1} \rangle &= D \cdot (V_{Csw} - V_L) + (1 - D) \cdot (-V_L) = 0, \\ \langle v_{L2} \rangle &= D \cdot (V_H - V_{Csw}) + (1 - D) \cdot (V_H - 2 \cdot V_{Csw}) = 0, \end{aligned} \tag{3.3}$$

The steady state voltage on one of the two switched capacitors is determined:

$$V_{Csw} = \frac{V_L}{D} = \frac{V_H}{2-D} = \frac{V_L + V_H}{2}. \tag{3.4}$$

The conversion ratios for the two input voltages, in step-down or step-up form are determined:

$$V_L = V_H \cdot \frac{D}{2-D}, \tag{3.5}$$

$$V_H = V_L \cdot \frac{1+D'}{1-D'}. \tag{3.6}$$

The BHSC2 converter achieves the same conversion ratios as the BHSC1 converter and the BSQZ converter from 1.3.2. The steady state duty cycle can be calculated from the two input voltages as:

$$D = \frac{2 \cdot V_L}{V_H + V_L} \tag{3.7}$$

In order to calculate the passive components, the average inductor currents are considered:

$$I_L = I_{L1},\ I_H = I_{L2}. \tag{3.8}$$

Similar to the analysis of the CBBB converter in 1.3.1, a ripple current percentage is defined for the two inductors:

$$r_i = \frac{\Delta i_{L1}}{I_{L1}} = \frac{\Delta i_{L2}}{I_{L2}}. \tag{3.9}$$

By using the voltage-current dependency of an ideal inductor the values for the two inductors are determined as:

$$L_1 = \frac{v_{L1} \cdot \Delta t}{\Delta i_{L1}} = \frac{V_L \cdot (V_H - V_L)}{r_i \cdot f \cdot I_L \cdot (V_H + V_L)}, \tag{3.10}$$

$$L_2 = \frac{v_{L2} \cdot \Delta t}{\Delta i_{L2}} = \frac{V_H \cdot (V_H - V_L)}{r_i \cdot f \cdot I_L \cdot (V_H + V_L)}. \tag{3.11}$$

Because the BHSC2 requires the same inductors as the BHSC1, the same inductor energy is required:

$$W_{L1} = \frac{L_1 \cdot {I_{L1}}^2}{2} = \frac{I_L \cdot V_L \cdot (V_H - V_L)}{2 \cdot r_i \cdot f \cdot (V_H + V_L)}, \tag{3.12}$$

$$W_{L2} = \frac{L_2 \cdot {I_{L2}}^2}{2} = \frac{I_L \cdot V_L^2 \cdot (V_H - V_L)}{2 \cdot r_i \cdot f \cdot V_H \cdot (V_H + V_L)}, \tag{3.13}$$

and the same total inductor energy is calculated similarly with:

$$W_{LTot} = \sum W_{Li} = \sum \frac{L_i \cdot {I_{Li}}^2}{2} = W_{L1} + W_{L2}, \tag{3.14}$$

$$W_{LTot} = \frac{I_L \cdot V_L \cdot (V_H - V_L)}{2 \cdot r_i \cdot f \cdot V_H}. \tag{3.15}$$

From (3.15) it can be concluded that the BHSC2, BHSC1 and CBBB have the same inductor energy requirements, the first two having the advantage of a higher conversion ratios, and the BHSC2 also benefiting from the common voltage ground between inputs.

In order to calculate the required capacitances and to calculate the total capacitor energy, the inductor currents are defined as time functions:

$$i_{L1}(t) = \begin{cases} I_{L1} + \Delta i_{L1} \cdot (t / t_{on} - 1/2), & t \in [0, t_{on}) \\ I_{L1} + \Delta i_{L1} \cdot ((T-t) / t_{off} - 1/2), & t \in [t_{on}, T] \end{cases} \tag{3.16}$$

$$i_{L2}(t) = \begin{cases} I_{L2} + \Delta i_{L2} \cdot (t / t_{on} - 1/2), & t \in [0, t_{on}) \\ I_{L2} + \Delta i_{L2} \cdot ((T-t) / t_{off} - 1/2), & t \in [t_{on}, T] \end{cases} \tag{3.17}$$

A voltage ripple percentage is defined for the three capacitors, similar to the CBBB converter from 1.3.1:

$$r_v = \frac{\Delta v_{CH}}{V_{CH}} = \frac{\Delta v_{CL}}{V_{CL}} = \frac{\Delta v_{Csw}}{V_{Csw}}. \tag{3.18}$$

The currents from each capacitor, as time functions, are:

$$i_{CL} = i_{L1} - I_L, \tag{3.19}$$

$$i_{CH} = I_H - i_{L2}, \tag{3.20}$$

$$i_{Csw} = \begin{cases} (i_{L2} - i_{L1}) / 2, & t \in [0, t_{on}) \\ i_{L2}, & t \in [t_{on}, T] \end{cases}. \tag{3.21}$$

Applying the voltage-current dependency of an ideal capacitor for the three capacitors, the following can be used to calculate the capacitances:

$$C_L = \frac{1}{\Delta v_{CL}} \int_{t_{on}/2}^{t_{on}+t_{off}/2} (i_{L1} - I_L) dt, \tag{3.22}$$

$$C_H = \frac{-1}{\Delta v_{CH}} \int_{t_{on}/2}^{t_{on}+t_{off}/2} (I_H - i_{L2}) dt, \tag{3.23}$$

$$C_{sw} = C_1 = C_2 = \frac{1}{\Delta v_{Csw}} \int_{t_{on}}^{T} i_{L2}\, dt. \tag{3.24}$$

Because the operation is similar, the capacitors of the BHSC2 are identical to the BHSC1 converter, even if the topologies are very different. The capacitors are calculated with:

$$C_L = \frac{r_i \cdot I_L}{8 \cdot r_v \cdot f \cdot V_L}, \tag{3.25}$$

$$C_H = \frac{r_i \cdot I_L \cdot V_L}{8 \cdot r_v \cdot f \cdot V_H^{\,2}}, \tag{3.26}$$

$$C_{sw} = \frac{2 \cdot I_L \cdot V_L \cdot (V_H - V_L)}{r_v \cdot f \cdot V_H \cdot (V_H + V_L)^2}. \tag{3.27}$$

The total capacitor energy is calculated with:

$$W_{CTot} = \sum W_{Ci} = \sum \frac{C_i \cdot V_{Ci}^2}{2} = W_{CL} + W_{CH} + 2 \cdot W_{Csw}, \tag{3.28}$$

With the individual capacitance energies calculated:

$$W_{CH} = \frac{r_i \cdot I_L \cdot V_L}{16 \cdot r_v \cdot f}, \tag{3.29}$$

$$W_{CL} = \frac{r_i \cdot I_L \cdot V_L}{16 \cdot r_v \cdot f}, \tag{3.30}$$

$$W_{Csw} = \frac{I_L \cdot V_L \cdot (V_H - V_L)}{4 \cdot r_v \cdot f \cdot V_H}, \tag{3.31}$$

the total capacitor energy is calculated as:

$$W_{CTot} = \frac{I_L \cdot V_L \cdot (4 \cdot V_H - 4 \cdot V_L + r_i \cdot V_H)}{8 \cdot r_v \cdot f \cdot V_H}. \tag{3.32}$$

Both BHSC2 and BHSC1 have the same total capacitor energy, as both have the same capacitances and same voltages, and are slightly higher than the values of the CBBB converter.

The total active switch stress for the BHSC2 converter is calculated with:

$$S = \sum_{j=1}^{5} V_{Sj} \cdot I_{Sj}, \tag{3.33}$$

By taking into account the voltage and current stresses on the switches:

$$V_{S1} / 2 = V_{S2} = V_{S3} = V_{S4} = V_{S5} = V_{Csw}, \tag{3.34}$$

$$I_{S1} = I_{S2} = I_{L1}, \quad I_{S3} = I_{S4} = (I_{L1} - I_{L2})/2, \quad I_{S4} = I_{L2}. \tag{3.35}$$

The total active switch stress is:

$$S = V_{S1} \cdot I_{S1} + V_{S2} \cdot I_{S2} + V_{S3} \cdot I_{S3} + V_{S4} \cdot I_{S4} + V_{S5} \cdot I_{S5} = 2 \cdot I_L \cdot (V_H + V_L). \tag{3.36}$$

The BHSC2 converter has an advantage over the CBBB converter in terms of conversion ratio while keeping a common ground connection between the negative terminals of the input voltages, unlike the BHSC1. This is achieved at the cost of a larger total active switch stress, as observed in (3.36). In other words, the BHSC2 achieves the advantages of the BHSC1 converter with the additional common ground between inputs, with the cost of added total stress on the active switches, and an increased number of switches.

3.4. Dynamic analysis

The dynamic modeling of the BHSC2 converter is performed similarly to the BHSC1 converter in chapter 2.4, by applying the SSA method. The first step in applying the method is considering the general form for the state equations:

$$\dot{x} = A_i \cdot x + B_i \cdot u, \tag{3.37}$$

where i=1 and i=2 for the equations corresponding to t_{on} and t_{off} intervals, respectively.

Similar to the BHSC1, x represents the state vector containing the state variables (the two inductor currents and the capacitor voltages), and u contains the input vector with the system inputs (the voltages on the two sides). The two vectors are:

$$x = \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{Csw} \\ v_{CL} \\ v_{CH} \end{bmatrix}, \quad u = \begin{bmatrix} V_L \\ V_H \end{bmatrix}. \tag{3.38}$$

The state (A_i) and input (B_i) matrices are expressed with their elements, as follows:

$$A_i = \begin{bmatrix} a_{11_i} & a_{12_i} & a_{13_i} & a_{14_i} & 0 \\ a_{21_i} & a_{22_i} & a_{23_i} & 0 & a_{25_i} \\ a_{31_i} & a_{32_i} & 0 & 0 & 0 \\ a_{41_i} & 0 & 0 & a_{44_i} & 0 \\ 0 & a_{52_i} & 0 & 0 & a_{55_i} \end{bmatrix}, \quad B_i = \begin{bmatrix} b_{11_i} & 0 \\ 0 & b_{22_i} \\ 0 & 0 \\ b_{41_i} & 0 \\ 0 & b_{52_i} \end{bmatrix}. \tag{3.39}$$

The schematic of the BHSC2 converter with the added parasitic resistances, that are required for an improved model, is presented in Fig. 3.6. The two equivalent schematics, according to the t_{on} and t_{off} switching states, are presented in Fig. 3.7 and Fig. 3.8, respectively.

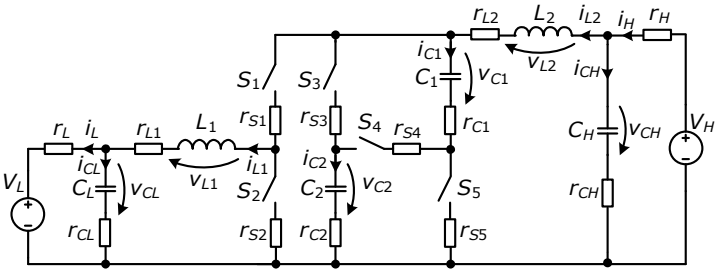

Fig. 3.6. BHSC2 schematic used for the SSA analysis. The schematic includes the following parasitic components: r_{L1}, r_{L2} – inductor ESRs; r_{CH}, r_{CL}, r_{C1}, r_{C2} – capacitor ESRs; r_{S1}-r_{S5} – switch on-state resitances; r_H, r_L – high and low voltage bus resistances. Component values are provided in Table 3.1

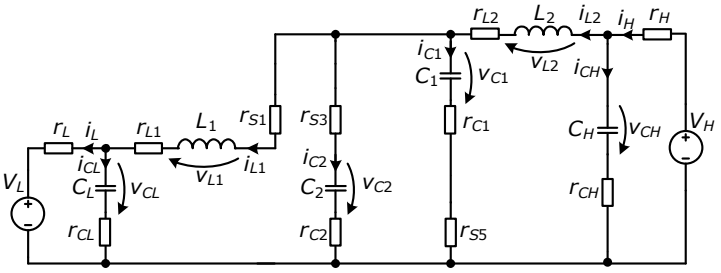

Fig. 3.7. BHSC2 equivalent schematic during t_{on} interval used for SSA

From the schematic presented in Fig. 3.7 and the equations (3.37), (3.38), (3.39), the elements of the state matrix (A_1), for t_{on} switching interval, are expressed:

$$a_{11_1} = -\frac{\frac{r_{Csw}}{2} + r_{L1} + r_{S1} + \frac{r_{S3}}{2} + \frac{r_{CL} \cdot r_L}{r_{CL} + r_L}}{L_1}, \tag{3.40}$$

$$a_{12_1} = \frac{r_{Csw} + r_{S3}}{2 \cdot L_1},\ a_{13_1} = \frac{1}{L_1},\ a_{14_1} = \frac{-r_L}{L_1 \cdot (r_{CL} + r_L)}, \tag{3.41}$$

$$a_{22_1} = -\frac{\frac{r_{Csw}}{2} + r_{L2} + \frac{r_{S3}}{2} + \frac{r_{CH} \cdot r_H}{r_{CH} + r_H}}{L_2} \tag{3.42}$$

$$a_{21_1} = \frac{r_{Csw} + r_{S3}}{2 \cdot L_2},\ a_{23_1} = -\frac{1}{L_2},\ a_{25_1} = \frac{r_H}{L_2 \cdot (r_{CH} + r_H)}, \tag{3.43}$$

$$a_{31_1} = -\frac{1}{2 \cdot C_{sw}},\ a_{32_1} = -a_{31_1}, \tag{3.44}$$

$$a_{41_1} = \frac{r_L}{C_L \cdot (r_{CL} + r_L)},\ a_{44_1} = \frac{-1}{C_L \cdot (r_{CL} + r_L)}, \tag{3.45}$$

$$a_{52_1} = \frac{-r_H}{C_H \cdot (r_{CH} + r_H)},\ a_{55_1} = \frac{-1}{C_H \cdot (r_{CH} + r_H)}, \tag{3.46}$$

Under the same considerations, the elements of the input matrix (B_1), are:

$$b_{11_1} = \frac{-r_{CL}}{L_1 \cdot (r_{CL} + r_L)},\ b_{22_1} = \frac{r_{CH}}{L_2 \cdot (r_{CH} + r_H)}, \tag{3.47}$$

$$b_{41_1} = \frac{1}{C_L \cdot (r_{CL} + r_L)},\ b_{52_1} = \frac{1}{C_H \cdot (r_{CH} + r_H)}, \tag{3.48}$$

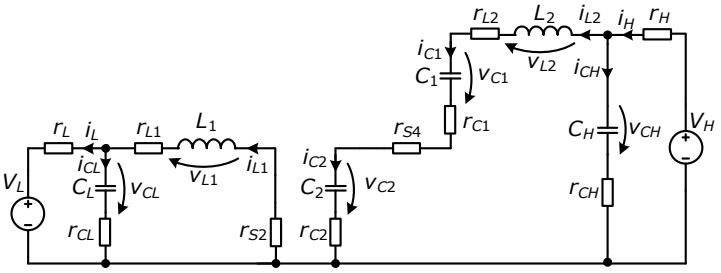

Fig. 3.8. BHSC2 equivalent schematic during t_{off} interval used for SSA

From the equations (3.37), (3.38), (3.39) and the schematic from Fig. 3.8, the elements of the state matrix (A_2), for t_{on} switching interval, are expressed as:

$$a_{11_2} = -\frac{r_{L1} + r_{S2} + \frac{r_{CL} \cdot r_L}{r_{CL} + r_L}}{L_1},\ a_{12_2} = 0,\ a_{13_2} = 0,\ a_{14_2} = \frac{-r_L}{L_1 \cdot (r_{CL} + r_L)}, \tag{3.49}$$

$$a_{22_2} = -\frac{2 \cdot r_{Csw} + r_{L2} + r_{S4} + \frac{r_{CH} \cdot r_H}{r_{CH} + r_H}}{L_2}, \tag{3.50}$$

$$a_{21_2} = 0,\ a_{23_2} = -\frac{2}{L_2},\ a_{25_2} = \frac{r_H}{L_2 \cdot (r_{CH} + r_H)} \tag{3.51}$$

$$a_{31_2} = 0,\ a_{32_2} = \frac{1}{C_{sw}},\ a_{41_2} = \frac{r_L}{C_L \cdot (r_{CL} + r_L)},\ a_{44_2} = \frac{-1}{C_L \cdot (r_{CL} + r_L)}, \tag{3.52}$$

$$a_{52_2} = \frac{-r_H}{C_H \cdot (r_{CH} + r_H)},\ a_{55_2} = \frac{-1}{C_H \cdot (r_{CH} + r_H)}, \tag{3.53}$$

With the same considerations, the elements of the input matrix (B_2), are:

$$b_{11_2} = \frac{-r_{CL}}{L_1 \cdot (r_{CL} + r_L)},\ b_{22_2} = \frac{r_{CH}}{L_2 \cdot (r_{CH} + r_H)}, \tag{3.54}$$

$$b_{41_2} = \frac{1}{C_L \cdot (r_{CL} + r_L)},\ b_{52_2} = \frac{1}{C_H \cdot (r_{C_H} + r_H)}. \tag{3.55}$$

Averaging the equations according to the dynamic duty cycle, d, for the equivalent states, the following continuous and nonlinear system is written:

$$\dot{x} = (d \cdot A_1 + (1-d) \cdot A_2) \cdot x + (d \cdot B_1 + (1-d) \cdot B_2) \cdot u. \tag{3.56}$$

The system is linearized by considering small signal variations around a steady state point, for the state variables, x, duty cycle, d, and outputs, y:

$$x = X + \tilde{x}, \quad d = D + \tilde{d}, \quad y = Y + \tilde{y}. \tag{3.57}$$

The newly formed system is expressed as:

$$\begin{cases} \dot{\tilde{x}} = A_e \cdot \tilde{x} + B_e \cdot \tilde{d} \\ \tilde{y} = C_e \cdot \tilde{x} \end{cases}, \tag{3.58}$$

with the equivalent state (A_e) and input (B_e) matrices:

$$A_e = (A_1 \cdot D + A_2 \cdot (1 - D)), \tag{3.59}$$

$$B_e = ((A_1 - A_2) \cdot X + (B_1 - B_2) \cdot u), \tag{3.60}$$

and the output matrices, C_{e1} and C_{e2}, defined for the system to output the i_{L1} or the i_{L2} current, respectively:

$$C_{e1} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \end{bmatrix}, \quad C_{e2} = \begin{bmatrix} 0 & 1 & 0 & 0 & 0 \end{bmatrix}. \tag{3.61}$$

Considering the two output matrices, the following control to output transfer functions are calculated:

$$G_{P1}(s) = \frac{\tilde{y}}{\tilde{d}} = \frac{\tilde{i}_{L1}}{\tilde{d}}, \tag{3.62}$$

$$G_{P2}(s) = \frac{\tilde{y}}{\tilde{d}} = \frac{\tilde{i}_{L2}}{\tilde{d}}, \tag{3.63}$$

by using:

$$\tilde{y} = C_e \cdot (s \cdot I - A_e)^{-1} \cdot B_e \cdot \tilde{d} \tag{3.64}$$

Values for the passive components for the BHSC2 were developed based on the equations from chapter 3.3, and the results are summarized in Table 3.1. The stability of converters can be affected because of the low ESR of capacitors (1-3 mΩ), as presented in [64], therefore the poles and zeros of the systems were calculated for the initial values of the passive components (shown in parentheses), and for the actual values of the capacitors, designed according to the maximum RMS ripple current.

Table 3.1. BHSC2 parameters for the dynamic analysis (initial values in parentheses)

Element	**Value**	**Unit**	**Description**
V_H	400	V	Nominal voltage at the high voltage side
V_L	100	V	Nominal voltage at the low voltage side
C_H	220 (7.8)	μF	Capacitance of the high voltage side capacitor
C_L	10000 (0.5)	μF	Capacitance of the low voltage side capacitor
C_1, C_2	10000 (18)	μF	Capacitance of the switched capacitors
r_v	2	%	Capacitance voltage ripple percentage
L_1	94	μH	Inductance of the low voltage side inductor
L_2	470	μH	Inductance of the high voltage side inductor
r_i	20	%	Inductor current ripple percentage
r_{S1} - r_{S5}	30	mΩ	On-state resistance of the switches
r_H	350	mΩ	Parasitic resistance of the supply line at V_H
r_L	50	mΩ	Parasitic resistance of the supply line at V_L
r_{CH}	328.3 (3)	mΩ	Equivalent series resistance of C_H
r_{CL}	28.67 (1)	mΩ	Equivalent series resistance of C_L
r_{C1}	8.6 (2)	mΩ	Equivalent series resistance of C_1
r_{L1}	20	mΩ	Low voltage side inductor resistance
r_{L2}	53	mΩ	High voltage side inductor resistance
T	12.5	μs	Switching period
D	0.4213	-	Duty cycle of the steady state operation point
I_{L1}	50	A	Steady state value of the L_1 inductor current

The poles and zeros of the system with the initial design values (shown in parentheses in Table 3.1) show that if these capacitors are used, a right half-plane zero (RHPZ) appears for the G_{P1}(s) transfer function. In order to avoid the RHPZ, electrolytic capacitors are used for the design, as suggested in [64], because of their higher capacitance and ESR values. The new poles and zeros of the system are shown in Table 3.3.

Table 3.2. Poles and zeros of the process with initial values

Transfer function	**Poles**	**Zeros**
$\boldsymbol{G_{P1}}$**(s)**	-40849151.7; -362447.944; -500.2799 ± 14134.6715i; -1049.685;	-40849673.2; -362448.131; **1036.851 ± 13549.279i**
$\boldsymbol{G_{P2}}$**(s)**	-40849151.7; -362447.944; -500.2799 ± 14134.6715i; -1049.685;	-40849151.7; -363187.332; -6192 ± 14895i

Table 3.3. Poles and zeros of the process with final values

Transfer function	**Poles**	**Zeros**
$\boldsymbol{G_{P1}}$**(s)**	-6253.186; -989.618 + 611.839i; -550.415 ± 283.316i	-6252.68; -1271.132; -504.63 ± 317.763i
$\boldsymbol{G_{P2}}$**(s)**	-6253.186; -989.618 + 611.839i; -550.415 ± 283.316i	-6701.245; -481.099; -854 ± 711.752i

The transfer functions of the final transfer functions are also expressed as:

$$G_{P1}(s) = \frac{2.65 \cdot 10^{6} \cdot s^{4} + 2.62 \cdot 10^{10} \cdot s^{3} + 4.21 \cdot 10^{13} \cdot s^{2} + 2.84 \cdot 10^{16} \cdot s + 7.49 \cdot 10^{18}}{s^{5} + 9.33 \cdot 10^{3} \cdot s^{4} + 2.32 \cdot 10^{7} \cdot s^{3} + 2.67 \cdot 10^{10} \cdot s^{2} + 1.46 \cdot 10^{13} \cdot s + 3.24 \cdot 10^{15}}, \quad (3.65)$$

$$G_{P2}(s) = \frac{5.346 \cdot 10^{5} \cdot s^{4} + 4.75 \cdot 10^{9} \cdot s^{3} + 8.94 \cdot 10^{12} \cdot s^{2} + 7.69 \cdot 10^{15} \cdot s + 2.13 \cdot 10^{18}}{s^{5} + 9.33 \cdot 10^{3} \cdot s^{4} + 2.32 \cdot 10^{7} \cdot s^{3} + 2.67 \cdot 10^{10} \cdot s^{2} + 1.46 \cdot 10^{13} \cdot s + 3.24 \cdot 10^{15}}, \quad (3.66)$$

Similar to the BHSC1, a current control method is desired for the BHSC2. The i_{L1} current is chosen as control variable, as it is much larger than i_{L2}, and is a state variable.

The bode plots of the two transfer functions from (3.65), (3.66) are presented in Fig. 3.9 together with the bode plots obtained from the simulation of the switching model of the BHSC2. The two sets of results have a good resemblance.

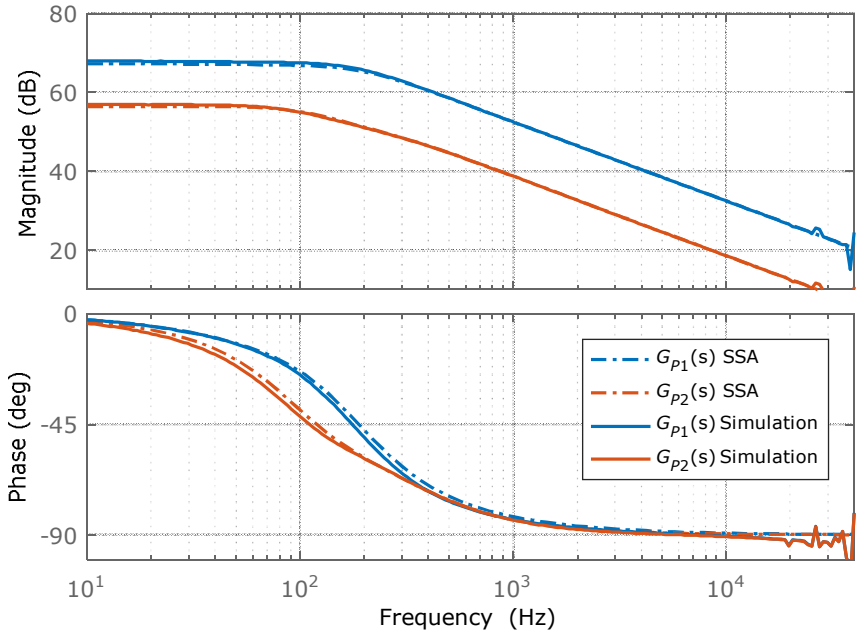

Fig. 3.9. Open loop Bode plots of the BHSC2 dynamic model : continuous time model of $G_{P1}(s)$ and $G_{P2}(s)$, obtained by SSA method or from the simulation of the converter switching model realized in PSIM software

3.5. Controller design

A controller was designed for the BHSC2 converter starting from the SSA model and from the Bode plots presented in Fig. 3.9. The controller was designed to satisfy a few requirements: a fast response, zero steady state error, a small overshoot (≤1%) which is achievable with a phase margin (*PM*) of approximately 90°, a gain margin (*GM*) greater or close to 10dB, and a cutoff frequency (f_c) lesser than 25% of the switching frequency of the converter.

The procedure for designing the controller was to directly shape the Bode plot of the open loop system in order to satisfy the requirements. The tool used for this purpose was the controlSystemDesigner application from the MATLAB software. A pole was added in origin to eliminate the steady state error, and an additional zero was added to increase the phase, while adjusting the gain of the controller. The final transfer function of the controller is:

$$G_C(s) = \frac{0.02754 \cdot (s + 4075)}{s} \tag{3.67}$$

The Bode plot of the open loop system, consisting of $G_C(s) \cdot G_{P1}(s)$, is presented in Fig. 3.10, together with the simulated response. The required performances are achieved, having phase margin of 87.2° at the cutoff frequency of 11kHz. The Bode plot of the controller is presented in Fig. 3.11.

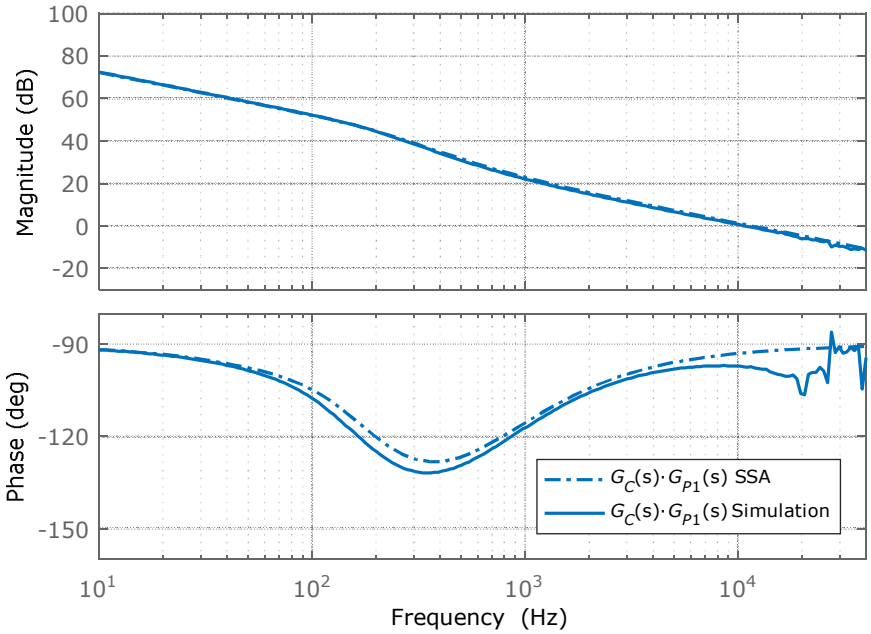

Fig. 3.10. Open loop Bode plots of the BHSC2 model controlled by $G_C(s)$: response of the SSA model, $G_C(s) \cdot G_{P1}(s)$; the Model Simulation with analog controller and switching model of the BHSC2⇒ PM=87.2°, f_c=11kHz

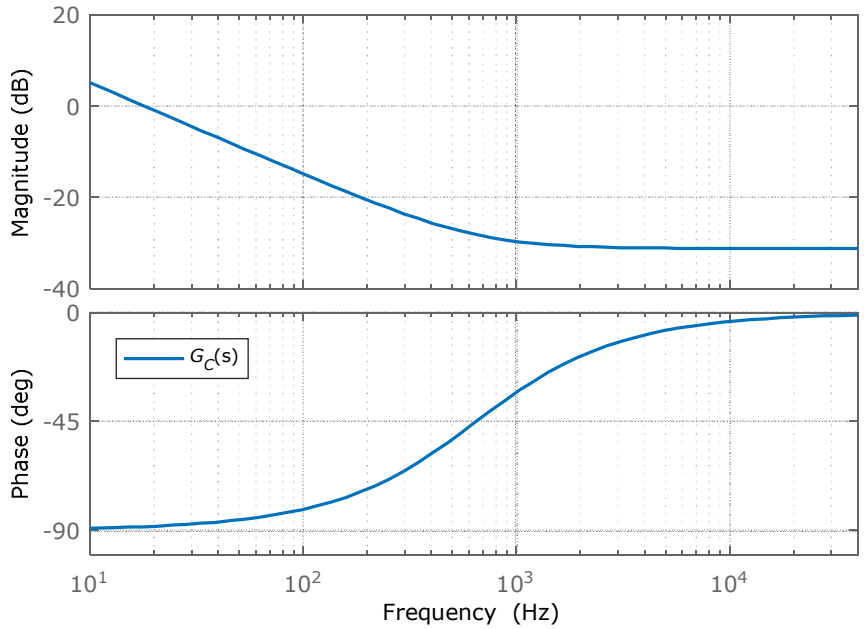

Fig. 3.11. Bode plots of the $G_C(s)$ controller designed for the BHSC2 converter

3.6. Simulation results

Simulation results are obtained for the BHSC2 converter with the parameters from in Table 3.1, and controlled by the $G_C(s)$ from (3.67).

Simulation for steady state operation are presented in Fig. 3.12, which are in good concordance with the theoretical waveforms from Fig. 3.5, with the exception of the switched capacitor voltages, that have a ripple more influenced by the capacitor ESR.

Results for transient response are presented in Fig. 3.13, where the BHSC2 operates in both step-up and step-down. In comparison to the BHSC1, the oscillations, of the i_{L2} current are greatly reduced because the dynamics of the converter were observed and corrected from the design phase. A much faster dynamic is possible with this converter, and no filter is required for the reference current.

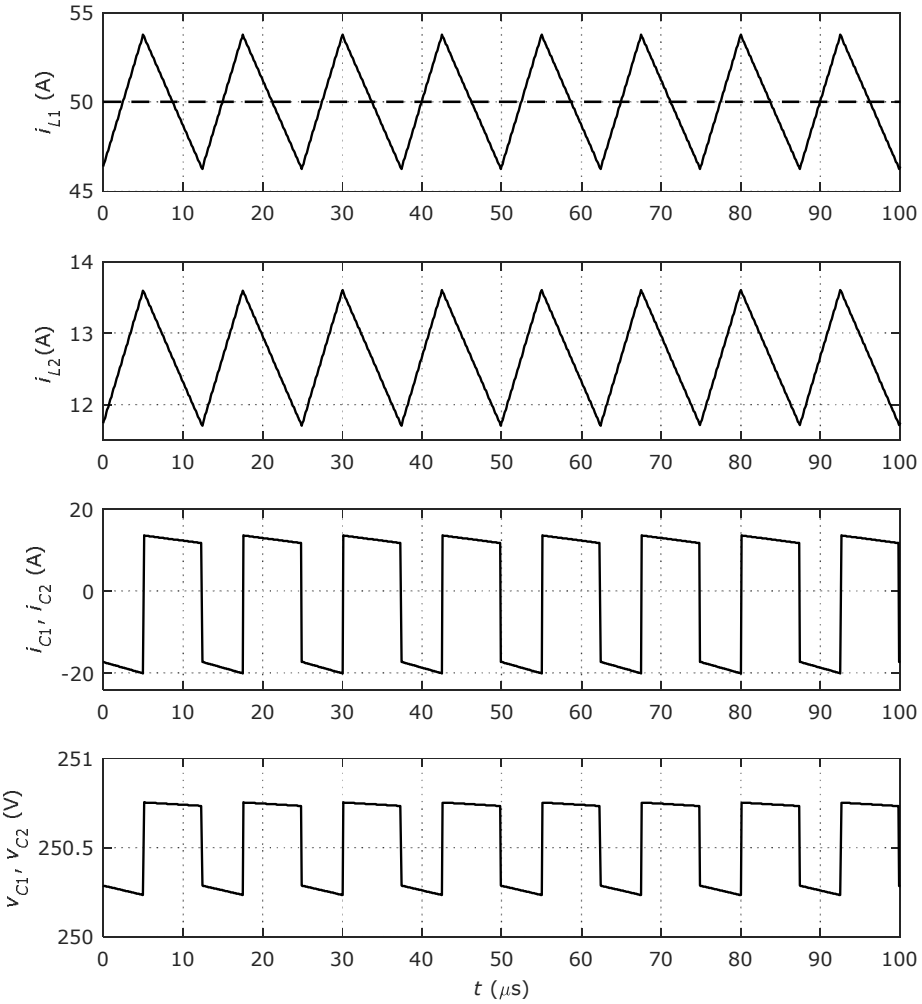

Fig. 3.12. Simulation waveforms for steady state operation of the BHSC2: i_{L1}=50A, V_L=100V, V_H=400V, P_{in}=5kW, (i_{L1}, i_{L2} are the currents from L_1 and L_2 inductors, respectively, i_{C1}, i_{C2} v_{C1}, v_{C2} are the currents and voltages on the switched capacitors, respectively)

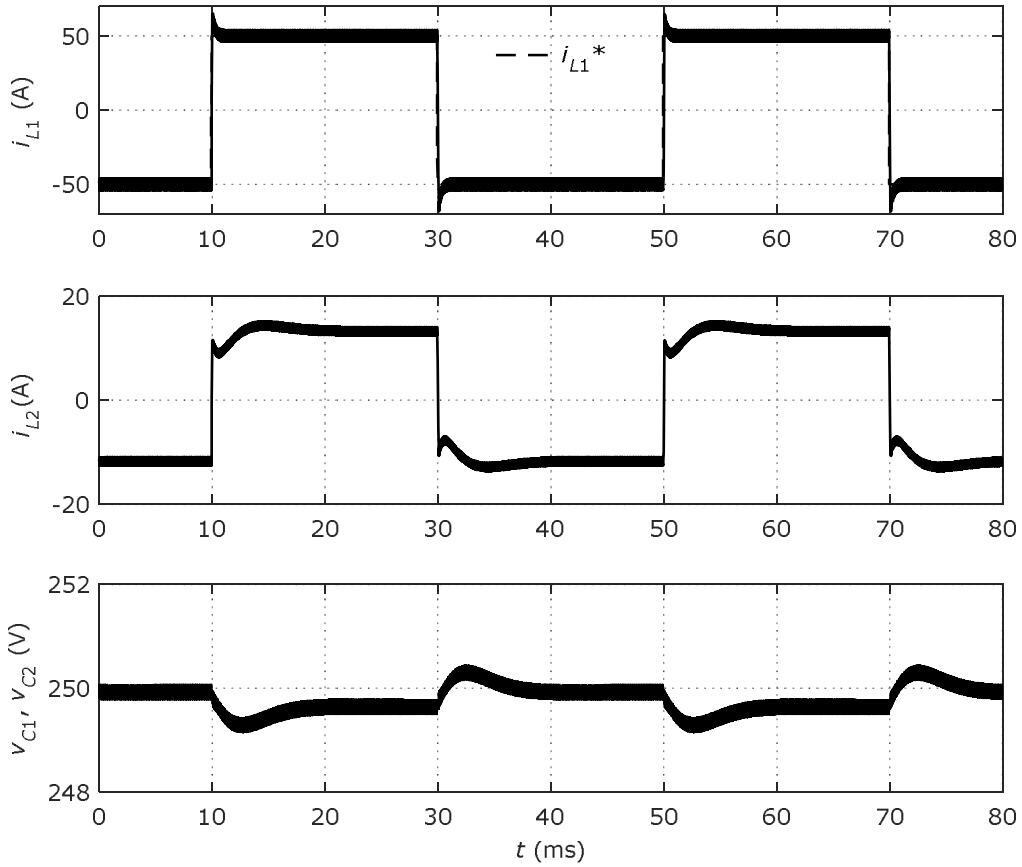

Fig. 3.13. Simulation waveforms for transient operation of the BHSC2, controlled by the G_C(s) controller: i_{L1} =±50A, V_L=100V, V_H=400V, P_{in}=±5kW, (i_{L1}, i_{L2} are the currents from L_1 and L_2 inductors, respectively, v_{C1}, v_{C2} are the voltages on the switched capacitors)

3.7. Topology improvements

Some benefits can be achieved by connecting multiple converters in multiphase configuration, or in a multilevel structure, as shown in [72]. Therefore, the BHSC2 topology is improved into a multilevel structure.

Similar to the three level buck boost (3L-BB) converter presented in [73], the BHSC2 converter can be modified into a three level topology (3L-BHSC2), as shown in Fig. 3.14. The main reason this topology can be modified effortlessly, is the existence of the common ground between the inputs, similar to the CBBB. Possible benefits of the new 3L-BHSC2 include smaller passive components, an increased conversion ratio, lower stress on the active switches, lower ripple at the inputs and faster dynamics.

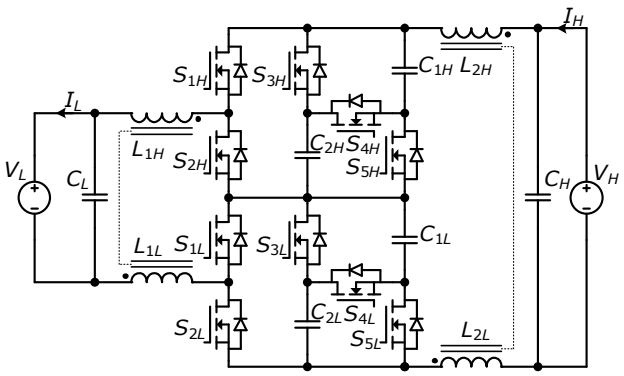

Fig. 3.14. Three level improved topology for the BHSC2 converter (3L-BHSC2)

3.8. Conclusions

The theoretical analysis was performed for the BHSC2 converter, in steady state and dynamic operation. The analytical results for steady state operation of the BHSC2 was performed in order to achieve the metrics required for comparisons with other topologies. The dynamic modeling was performed in order to obtain a linear model of the BHSC2 which was initially used to achieve a more stable design, and afterwards it was used to design a current controller which controls the power flow. In comparison to the BHSC1, this converter does not require slowing the reference current with a low pass filter, and a faster response is achieved. A disadvantage of the topology is an increase in the total active switch stress, as the BHSC2 has two more additional switches in comparison to the BHSC1.

Simulation results are used to confirm de dynamic analysis and to show the operation of the BHSC2 in transient and steady state mode.

Additionally, an improved BHSC2 topology is proposed, which translates the initial schematic into a multilevel topology, having the additional benefits of the multi-level structures.

4. THE BIDIRECTIONAL HYBRID SWITCHED INDUCTOR CONVERTER (BHSI)

4.1. Abstract

This chapter presents a Bidirectional Hybrid Switched Inductor converter (BHSI), which, as the name suggests, uses a switched inductor cell in order to achieve the higher voltage conversion ratio. A steady state analysis is performed for the BHSI, similar to the CBBB converter, which is further used for passive components sizing and comparisons to other topologies. The dynamic modeling of the BHSI is performed in order to obtain the model used for the controller design. In terms of stability analysis, the effects of incorrect modeling of the microcontroller are presented and confirmed by experimental results. Two prototypes are built for the BHSI converter using conventional Silicon MOSFETs and new Gallium-Nitride FETs, and their influence on the topology is presented. The efficiency of the prototypes is measured and compared to the theoretical results. An improved topology is proposed which eliminates some disadvantages of the topology.

4.2. Overview

The structure of the BHSI is developed starting from the two Unidirectional Hybrid Switched Inductor converters, which operate in step-down (Fig. 4.1 - DUSHI) and in step-up (Fig. 4.2 - UUHSI) mode, respectively.

The step-down structure was initially proposed in [42], together with the UHSC1 (Fig. 2.1) and UHSC2 (Fig. 3.1), and it was experimentally tested in [74], [75]. The step-up structure was proposed in [76] and it was tested and improved in multiple papers [77]–[80]. The DUHSI topology resembles a conventional buck converter with the switched inductor connected at the output, replacing the conventional inductor and freewheeling diode. The UUHSI topology is a boost converter which uses two inductors and two transistors in order to connect the inductors in parallel to the source, which are then discharged in series to the output.

The schematic of the BHSI, shown in Fig. 4.3, contains three transistors, with their respective antiparallel diodes. The operation of the BHSI is identical to the operation of DUHSI and UUHSI, in the step-down and step-up modes respectively, with the added possibility of using active rectification if MOSFET transistors are used. As a result, only one driving signal is used, applied directly to S_1 switch, and inverted for S_2 and S_3.

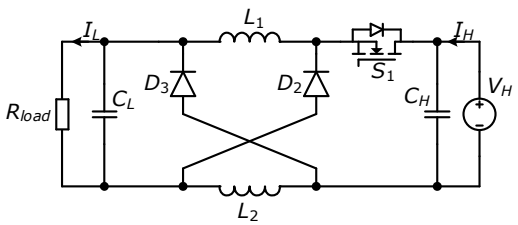

Fig. 4.1. The Step-Down Unidirectional Hybrid Switched Inductor converter (DUHSI) [42]

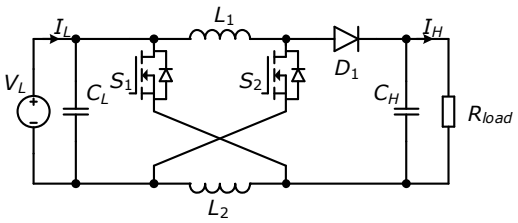

Fig. 4.2. The Step-Up Unidirectional Hybrid Switched Inductor converter (UUHSI) [76]

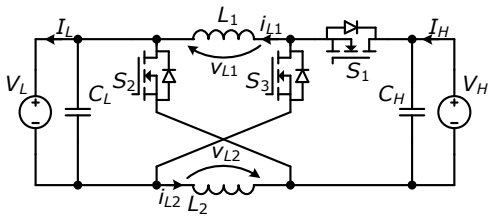

Fig. 4.3. The Bidirectional Hybrid Switched Inductor converter (BHSI) [81]

Like the DUHSI and UUHSI, the BHSI uses two identical inductors, for which the currents are considered identical. As for the previous converters, positive currents indicate step-down operation mode, while negative currents indicate step-up operation mode.

4.3. Steady state analysis

The analysis of the BHSI starts with the two equivalent schematics during the t_{on} and t_{off} switching interval, presented in Fig. 4.4 and Fig. 4.5 respectively. During the t_{on} interval the S_1 switch is turned ON, and the S_2 and S_3 switches are turned OFF. Similar to the unidirectional schematics, the two inductors and their currents are considered identical for both intervals ($L_1 = L_2$, $i_{L1} = i_{L2}$).

During the t_{on} interval, the two inductors are connected in series between the two inputs (V_H and V_L), and the current on the low voltage side is equal to the current through the inductors. The voltage difference between V_H and V_L is divided between the two inductors.

During the t_{off} interval, the two inductors are connected in parallel to V_L, and the current on the low voltage side is equal to double the current through the inductors.

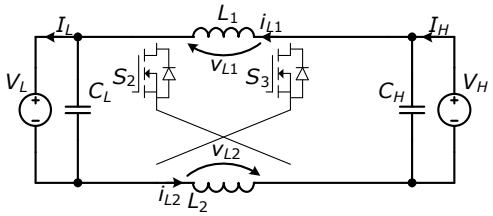

Fig. 4.4. Equivalent schematic of BHSI during t_{on} interval
(S_1 is turned ON, S_2 and S_3 are turned OFF)

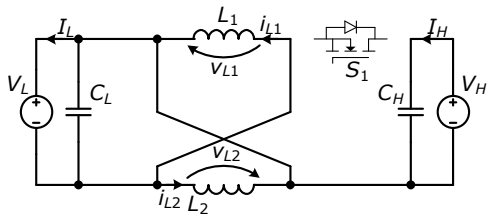

Fig. 4.5. Equivalent schematic of BHSI during t_{off} interval
(S_1 is turned OFF, S_2 and S_3 are turned ON)

Using the two equivalent schematics, the main theoretical waveforms are drawn in Fig. 4.6: inductor voltages (v_{L1}, v_{L2}) and currents (i_{L1}, i_{L2}), switch voltages (v_{S1}, v_{S2}, v_{S3}) and currents (i_{S1}, i_{S2}, i_{S3}) input and output currents with the capacitor ripple current (i_H-i_{CH} and i_L+i_{CL}), and the ripple voltages on the input capacitors (Δv_{CH} and Δv_{CL}). The main difference when comparing this topology with the conventional buck converter, is the current ripple on the low voltage side, which has larger variations, but as it is shown in chapter 6, this does not require larger capacitors, but the contrary. An additional difference is for the switch voltage stresses, which is larger for S_1, but smaller for S_2 and S_3. The shape of the voltage ripple on the input capacitors, is noticeably different, as it is dependent on the capacitor ripple currents.

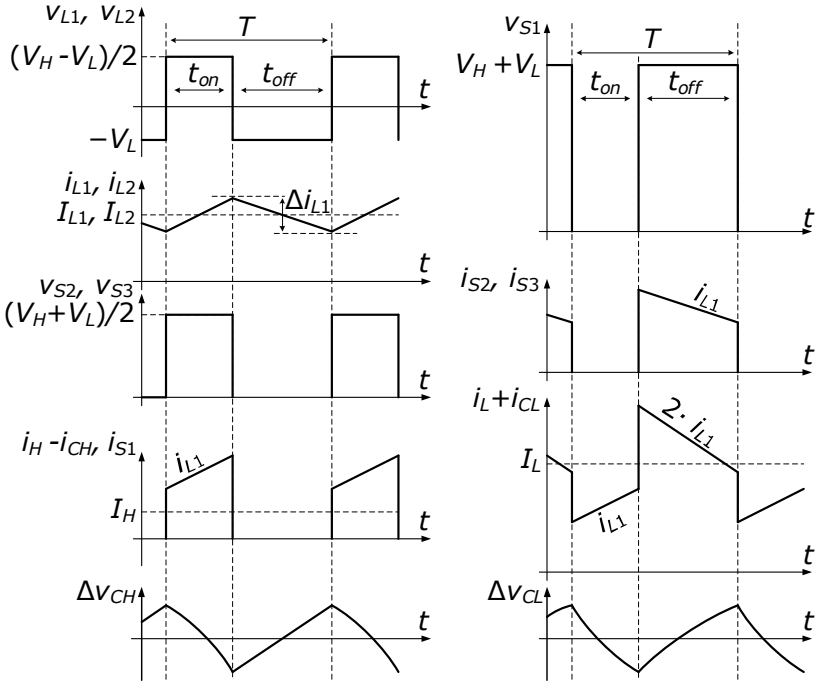

Fig. 4.6. Main theoretical waveforms of the BHSI : L_1, L_2 inductor voltages and currents (v_{L1}, v_{L2}, i_{L1}, i_{L2}); S_1, S_2 and S_3 switches voltages and currents (v_{S1}, v_{S2}, v_{S3}, i_{S1}, i_{S2}, i_{S3}); input currents with the added capacitor ripple currents (i_H-i_{CH} and i_L+i_{CL}); ripple voltages on the input capacitors (Δv_{CH} and Δv_{CL})

Similar to the analysis of the conventional buck/boost converter, presented in 1.3.1, the steady state analysis of the BHSI begins by considering *D* the duty cycle for the step-down mode of operation, and *D'* the duty cycle for step-up mode:

$$D = \frac{t_{on}}{T},\ D' = \frac{t_{off}}{T}. \tag{4.1}$$

The inductor voltages on the two switching intervals, represented in Fig. 4.4 and Fig. 4.5, are calculated considering an even distribution between them for t_{on} interval:

$$\begin{aligned} &t_{on} : v_{L1} + v_{L2} = V_H - V_L,\ \ v_{L1} = v_{L2} = \frac{V_H - V_L}{2}, \\ &t_{off} : v_{L1} = v_{L2} = -V_L. \end{aligned} \tag{4.2}$$

Using the same simplifying assumptions (ideal components, constant voltage on capacitors, steady state operation) as in 1.3.1, and identical voltages and currents on the two inductors, the volt-second balance can be written:

$$\langle v_{L1} \rangle = D \cdot \frac{V_H - V_L}{2} + (1 - D) \cdot (-V_L) = 0, \tag{4.3}$$

To determine the voltage conversion ratio, defined in step-down and step-up modes respectively:

$$V_L = V_H \cdot \frac{D}{2 - D}, \tag{4.4}$$

$$V_H = V_L \cdot \frac{1 + D'}{1 - D'}. \tag{4.5}$$

As shown in the analysis of the BHSC1 and BHSC2 converters in 2.3 and 3.3 respectively, their conversion ratio for and the BHSI conversion ratio is identical, even if the topologies are very distinct. Similarly, the duty ratio can be calculated with:

$$D = \frac{2 \cdot V_L}{V_H + V_L}. \tag{4.6}$$

Considering that the I_L current is equal to I_{L1} current during t_{on} and $2 \cdot I_{L1}$ during t_{off}, by averaging on a switching period, the inductor current is calculated from the low voltage current, with the following:

$$I_{L1} = I_L \cdot \frac{1}{2 - D}. \tag{4.7}$$

Similar to the analysis from 1.3.1, an inductor ripple current percentage is defined for the two inductors:

$$r_i = \frac{\Delta i_{L1}}{I_{L1}} = \frac{\Delta i_{L2}}{I_{L2}}, \tag{4.8}$$

and by using the voltage-current dependency of an inductor, the value of the inductors is determined:

$$L_1 = L_2 = \frac{v_{L1} \cdot \Delta t}{\Delta i_{L1}} = \frac{2 \cdot V_H \cdot V_L \cdot (V_H - V_L)}{r_i \cdot f \cdot I_L \cdot (V_L + V_H)^2}. \tag{4.9}$$

With the inductance value, the energy is calculated:

$$W_{L1} = W_{L2} = \frac{L_1 \cdot I_{L1}^2}{2} = \frac{I_L \cdot V_L \cdot (V_H - V_L)}{4 \cdot r_i \cdot f \cdot V_H}, \tag{4.10}$$

and is used to calculate the total inductor energy:

$$W_{LTot} = \sum W_{Li} = \sum \frac{L_i \cdot I_{Li}^2}{2} = 2 \cdot W_{L1}, \tag{4.11}$$

The total inductor energy is finally calculated as:

$$W_{LTot} = \frac{I_L \cdot V_L \cdot (V_H - V_L)}{2 \cdot r_i \cdot f \cdot V_H}. \tag{4.12}$$

Similar to BHSC1 and BHSC2, the BHSI converter has the same total inductor energy as the conventional bidirectional buck/boost converter, but it achieves better conversion ratios for the same duty cycle.

The two inductor currents are described as the following time function:

$$i_{L1}(t) = i_{L2}(t) = \begin{cases} I_{L1} + \Delta i_{L1} \cdot (t / t_{on} - 1/2), & t \in [0, t_{on}) \\ I_{L1} + \Delta i_{L1} \cdot ((T - t) / t_{off} - 1/2), & t \in [t_{on}, T] \end{cases} \tag{4.13}$$

which is used for calculating the capacitances.

In order to calculate the capacitances, a voltage ripple percentage is defined, as in 1.3.1:

$$r_v = \frac{\Delta v_{CH}}{V_{CH}} = \frac{\Delta v_{CL}}{V_{CL}}. \tag{4.14}$$

The two capacitor currents are described based on the inductor current function, (4.13):

$$i_{CL} = \begin{cases} i_{L1} - I_L, & t \in [0, t_{on}) \\ 2 \cdot i_{L1} - I_L, & t \in [t_{on}, T] \end{cases}, \tag{4.15}$$

$$i_{CH} = \begin{cases} I_H - i_{L1}, & t \in [0, t_{on}) \\ I_H, & t \in [t_{on}, T] \end{cases}. \tag{4.16}$$

Using the voltage-current dependency of the ideal capacitor, the relations for calculating the capacitors are described:

$$C_L = \frac{1}{-\Delta v_{CL}} \int_0^{t_{on}} (i_{L1} - I_L) dt, \tag{4.17}$$

$$C_H = \frac{1}{-\Delta v_{CH}} \int_0^{t_{on}} (I_H - i_{L1}) dt. \tag{4.18}$$

Both relations are written for the t_{on} interval, where both capacitors are discharging, but the same result will be obtained by calculated for the t_{off} interval. The values for the capacitors are calculated as:

$$C_L = \frac{I_L \cdot (V_H - V_L)}{r_v \cdot f \cdot V_H \cdot (V_H + V_L)}, \tag{4.19}$$

$$C_H = \frac{I_L \cdot V_L \cdot (V_H - V_L)}{r_v \cdot f \cdot V_H^{\,2} \cdot (V_H + V_L)}. \tag{4.20}$$

The total capacitor energy is calculated as:

$$W_{CTot} = \sum W_{Ci} = \sum \frac{C_i \cdot V_{Ci}^{\,2}}{2} = W_{CL} + W_{CH}, \tag{4.21}$$

Having the C_H and C_L capacitor energy calculated with:

$$W_{CH} = \frac{I_L \cdot V_L \cdot (V_H - V_L)}{2 \cdot r_v \cdot f \cdot (V_H + V_L)}, \tag{4.22}$$

$$W_{CL} = \frac{I_L \cdot V_L^{\,2} \cdot (V_H - V_L)}{2 \cdot r_v \cdot f \cdot V_H \cdot (V_H + V_L)}, \tag{4.23}$$

the total capacitor energy is calculated:

$$W_{CTot} = \frac{I_L \cdot V_L \cdot (V_H - V_L)}{2 \cdot r_v \cdot f \cdot V_H}. \tag{4.24}$$

Because of the large input and output ripple currents, the BHSI may seem to require a larger filter capacitor, but relation (4.24) shows the contrary. In comparison to the CBBB, BHSC1 and BHSC2, the BHSI has the lowest capacitor requirements.

Having three transistors, the total switch stress is calculated with:

$$S = \sum_{j=1}^{3} V_{Sj} \cdot I_{Sj}, \tag{4.25}$$

The average voltage and current stresses are given in:

$$V_{S1} / 2 = V_{S2} = V_{S3} = (V_H + V_L) / 2, \tag{4.26}$$

$$I_{S1} = I_{S2} = I_{S3} = I_{L1}, \tag{4.27}$$

and the total switch stress is calculated as:

$$S = V_{S1} \cdot I_{S1} + V_{S2} \cdot I_{S2} + V_{S3} \cdot I_{S3} = \frac{I_L \cdot (V_H + V_L)^2}{V_H}. \tag{4.28}$$

Comparing the BHSI to BHSC1, they show the same stress on the switches, which is much lower than the CBBB.

4.4. Dynamic analysis

The dynamic modeling is performed similar to the BHSC1 and BHSC2, by using the SSA method, in which the following state space representation is used:

$$\dot{x} = A_i \cdot x + B_i \cdot u, \tag{4.29}$$

where i=1 and i=2 for the equations corresponding to t_{on} and t_{off} respectively.

The main advantage of the BHSI compared to the BHSC1 and BHSC2 is the reduced order of the system, which is made possible by considering the inductor currents identical. With this simplification, the states and the input vectors are described in the following:

$$x = \begin{bmatrix} i_{L1} \\ v_{CH} \\ v_{CL} \end{bmatrix}, \quad u = \begin{bmatrix} V_H \\ V_L \end{bmatrix}. \tag{4.30}$$

In order to have a precise model for the converter, the parasitic resistor from Fig. 4.7 are introduced in the schematic. If needed, the model can be further simplified by eliminating the input capacitors from the schematic without greatly sacrificing the accuracy of the model.

The equivalent schematics of the BHSI during the two switching intervals are presented in Fig. 4.8 and Fig. 4.9 respectively.

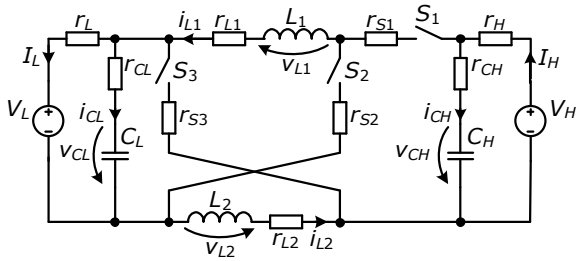

Fig. 4.7. BHSI schematic used for the SSA analysis. The schematic includes the following parasitic components: r_{L1}, r_{L2} – inductor ESRs; r_{CH}, r_{CL} – capacitor ESRs; r_{S1}, r_{S2}, r_{S3} – switch on-state resitances; r_H, r_L – high and low voltage bus resistances. Component values are provided in Table 4.1

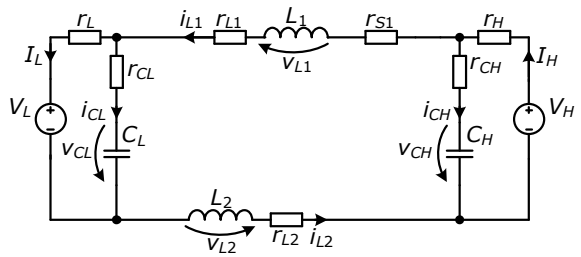

Fig. 4.8. BHSI equivalent schematic during t_{on} interval used for SSA

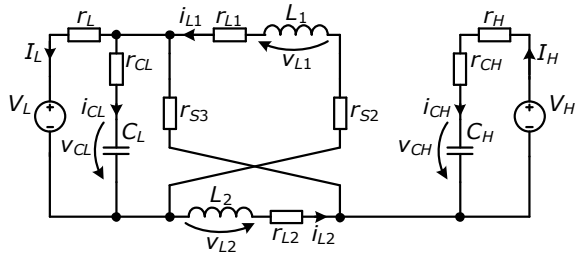

Fig. 4.9. BHSI equivalent schematic during t_{off} interval used for SSA

Based on (4.29), (4.30) and Fig. 4.8, the following state (A_1) and input (B_1) matrices are determined for t_{on} switching interval:

$$A_1 = \begin{bmatrix} -\dfrac{r_{L1} + \dfrac{r_{S1}}{2} + \dfrac{r_{CH} \cdot r_H}{2 \cdot (r_{CH} + r_H)} + \dfrac{r_{CL} \cdot r_L}{2 \cdot (r_{CL} + r_L)}}{L_1} & \dfrac{r_H}{2 \cdot L_1 \cdot (r_{CH} + r_H)} & \dfrac{-r_L}{2 \cdot L_1 \cdot (r_{CL} + r_L)} \\ \dfrac{-r_H}{C_H \cdot (r_{CH} + r_H)} & \dfrac{-1}{C_H \cdot (r_{CH} + r_H)} & 0 \\ \dfrac{r_L}{C_L \cdot (r_{CL} + r_L)} & 0 & \dfrac{-1}{C_L \cdot (r_{CL} + r_L)} \end{bmatrix}, \quad (4.31)$$

$$B_1 = \begin{bmatrix} \dfrac{r_{CH}}{2 \cdot L_1 \cdot (r_{CH} + r_H)} & \dfrac{-r_{CL}}{2 \cdot L_1 \cdot (r_{CL} + r_L)} \\ \dfrac{1}{C_H \cdot (r_{CH} + r_H)} & 0 \\ 0 & \dfrac{1}{C_L \cdot (r_{CL} + r_L)} \end{bmatrix}. \quad (4.32)$$

For t_{off} switching interval, starting from (4.29), (4.30) and Fig. 4.8, the following state (A_2) and input (B_2) matrices are determined:

$$A_2 = \begin{bmatrix} -\dfrac{r_{L1} + r_{S2} + \dfrac{2 \cdot r_{CL} \cdot r_L}{(r_{CL} + r_L)}}{L_1} & 0 & \dfrac{-r_L}{L_1 \cdot (r_{CL} + r_L)} \\ 0 & \dfrac{-1}{C_H \cdot (r_{CH} + r_H)} & 0 \\ \dfrac{2 \cdot r_L}{C_L \cdot (r_{CL} + r_L)} & 0 & \dfrac{-1}{C_L \cdot (r_{CL} + r_L)} \end{bmatrix}, \quad (4.33)$$

$$B_2 = \begin{bmatrix} 0 & \dfrac{-r_{CL}}{L_1 \cdot (r_{CL} + r_L)} \\ \dfrac{1}{C_H \cdot (r_{CH} + r_H)} & 0 \\ 0 & \dfrac{1}{C_L \cdot (r_{CL} + r_L)} \end{bmatrix}. \quad (4.34)$$

Similar to section 2.4, the next step is the linearization of the model by applying a small signal to the sate variables, the duty cycle and the output:

$$x = X + \tilde{x}, \quad d = D + \tilde{d}, \quad y = Y + \tilde{y}. \quad (4.35)$$

The new linearized system is:

$$\begin{cases} \dot{\tilde{x}} = A_e \cdot \tilde{x} + B_e \cdot \tilde{d} \\ \tilde{y} = C_e \cdot \tilde{x} \end{cases}, \tag{4.36}$$

where the equivalent state (A_e), input (B_e), are averaged as:

$$A_e = (A_1 \cdot D + A_2 \cdot (1 - D)), \tag{4.37}$$

$$B_e = ((A_1 - A_2) \cdot X + (B_1 - B_2) \cdot u), \tag{4.38}$$

and the output matrix is defined in order to output the i_{L1} current:

$$C_e = \begin{bmatrix} 1 & 0 & 0 \end{bmatrix}. \tag{4.39}$$

The control to output transfer function is defined as:

$$G_P(s) = \frac{\tilde{y}}{\tilde{d}} = \frac{\tilde{i}_{L1}}{\tilde{d}}, \tag{4.40}$$

The parameters of the converter used for the calculation of the transfer function are detailed in Table 4.1. Using these parameters, the control to output transfer function is calculated:

$$G_P(s) = \frac{1.811 \cdot 10^6 \cdot s^2 + 1.722 \cdot 10^{10} \cdot s + 4.197 \cdot 10^{13}}{s^3 + 1.045 \cdot 10^4 \cdot s^2 + 3.027 \cdot 10^7 \cdot s + 1.87 \cdot 10^{10}}. \tag{4.41}$$

In order to design the controller, the Bode plots of the control to output transfer function are represented in Fig. 4.10. In this figure the following are plotted: the continuous time transfer function, G_P(s), together with the discretized transfer function, G_{P0}(z), the discretized transfer function including an additional delay G_P(z), and the model simulation which also includes the microcontroller (F28379D) apart from the switching model of the BHSI.

The discretization of the transfer function is realized by using the Zero-order-hold method in order to take into account the hold effect of the PWM:

$$G_{P0}(z) = (1 - z^{-1})\, \mathcal{Z}\left[\frac{G_P(s)}{s}\right]. \tag{4.42}$$

Table 4.1. BHSI parameters for the dynamic analysis

Element	**Value**	**Unit**	**Description**
V_H	300	V	Nominal voltage at the high voltage side
V_L	60	V	Nominal voltage at the low voltage side
C_H	1.98	mF	Capacitance of the high voltage side capacitor
C_L	4.23	mF	Capacitance of the low voltage side capacitor
L_1, L_2	100	µH	Inductance of the two switched inductors
r_{S1}, r_{S2}, r_{S3}	40	mΩ	On-state resistance of the switches
r_H	37.5	mΩ	Parasitic resistance of the supply line at V_H
r_L	23.7	mΩ	Parasitic resistance of the supply line at V_L
r_{CH}	50	mΩ	Equivalent series resistance of C_H
r_{CL}	35.2	mΩ	Equivalent series resistance of C_L
r_{L1}, r_{L2}	9	mΩ	Inductor resistances
T	25	µs	Switching period
f	40	kHz	Switching frequency
D	0.347	-	Duty cycle of the steady state operation point
I_{L1}, I_{L2}	30	A	Steady state value of the inductor currents

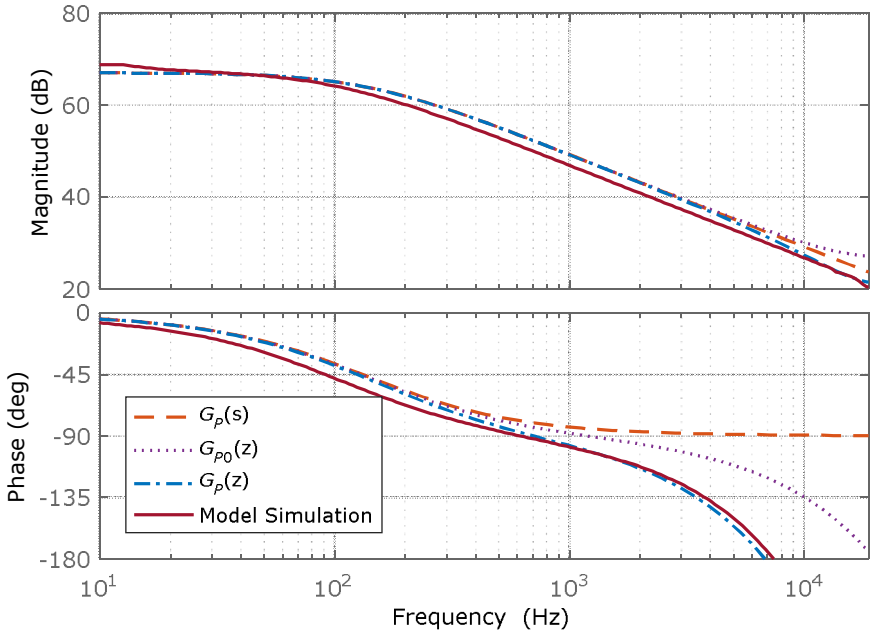

Fig. 4.10. Open loop Bode plots of the BHSI dynamic model: continuous time model - G_P(s); ZOH discretized model accounting for the PWM hold - G_{P0}(z); discretized transfer function including an additional ADC delay G_P(z); the Model Simulation which also includes the microcontroller (TMS320F28377S) and the switching model of the converter

Because the ADC of the microcontroller is triggered by the PWM (in order to eliminate switching noise), an additional delay time is required to be added to G_{P0}(z). The delay can be either a simple z^{-1}, as described in 2.7, or, in this case, a Padé approximation of a delay inserted in the s domain transfer function, and then discretized. The latter is used as the response is slightly closer to the simulation model:

$$G_p(z) = (1 - z^{-1})\,\mathcal{Z}\left[\frac{P(s)\cdot G_p(s)}{s}\right], \tag{4.43}$$

where P(s) is the delay approximation, and is calculated as:

$$P(s) = \frac{-T\cdot s + 2}{T\cdot s + 2}. \tag{4.44}$$

4.5. Controller design

The i_{L1} current controller was designed based on the Bode plots from Fig. 4.10 for two cases, one for the process without the additional delay, G_{P0}(z), and one for the process with the delay, G_P(z), in order to show the different operation.

The method for designing the control was the direct shaping the open loop response of the process with the controller, while having in mind a fast response, zero steady state error, a small overshoot (≤5%) which is achievable with a phase margin (*PM*) of approximately 70°, a gain margin (*GM*) greater or close to 10dB, and a cutoff frequency (f_c) lesser than 25% of the switching frequency of the BHSI.

With these requirements, a pole was added in the origin in order to achieve zero steady state error, and a zero was added while adjusting the gain of the controller in order to achieve the desirable phase margin, gain margin and cutoff frequency. The procedure was performed in MATLAB software with the help of the controlSystemDesigner application, which also helps to visualize the changes in a short time, with a display of a step signal response and Root Locus in addition to the Bode plots.

Initially the $G_{C0}(z)$ controller was designed to achieve the control requirements, for the BHSI modeled by $G_{P0}(z)$, in order to show the large difference that appears when not taking into account the ADC delay. From the results displayed in Fig. 4.11, the expected performance is shown to be close to the requirements, achieving a PM=64.2°, f_c=4.98kHz and GM=9.8dB. For the real process however, $G_C(z)$ this controller achieves different characteristics, having a much lower phase margin, PM=25.9° at f_c=4.59kHz and GM=3.59dB which will lead to unexpected results as presented in the following section, 4.6. The model simulation does show a difference from the model, but it presents the same stability characteristics (PM, f_c, and GM). The transfer function of the controller is described in the following:

$$G_{C0} = 17.329 \cdot 10^{-3} \cdot \frac{z - 0.9369}{z - 1}. \tag{4.45}$$

In order to achieve the expected results, the $G_C(z)$ controller was designed, following the same steps as for $G_{C0}(z)$ but for the $G_P(z)$ process. The results displayed in Fig. 4.12 with the transfer function of the new controller in (4.46), show that the expected performance is achieving the requirements, having a PM=68.5° at f_c=1.55kHz and GM=13.8dB.

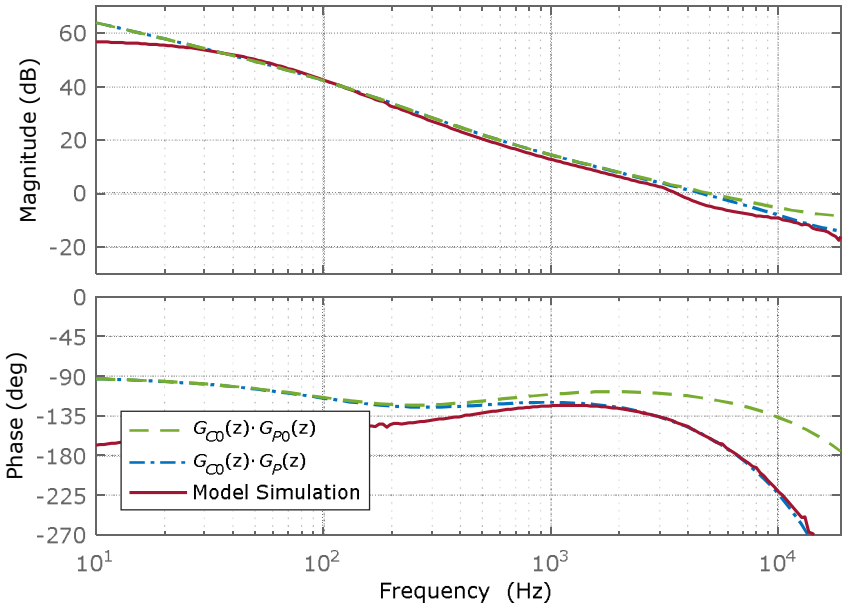

Fig. 4.11. Open loop Bode plots of the BHSI model controlled by $G_{C0}(z)$: expected response of the discretized model without ADC delay, $G_{C0}(z) \cdot G_{P0}(z) \Rightarrow PM$=64.2°, f_c=4.98kHz GM=8.41dB; actual response of the model with delay, $G_{C0}(z) \cdot G_P(z) \Rightarrow PM$=25.9°, f_c=4.59kHz, GM=3.59dB; the Model Simulation with microcontroller (TMS320F28377S) and switching model of BHSI

$$G_C = 5.4236 \cdot 10^{-3} \cdot \frac{z - 0.9802}{z - 1} \tag{4.46}$$

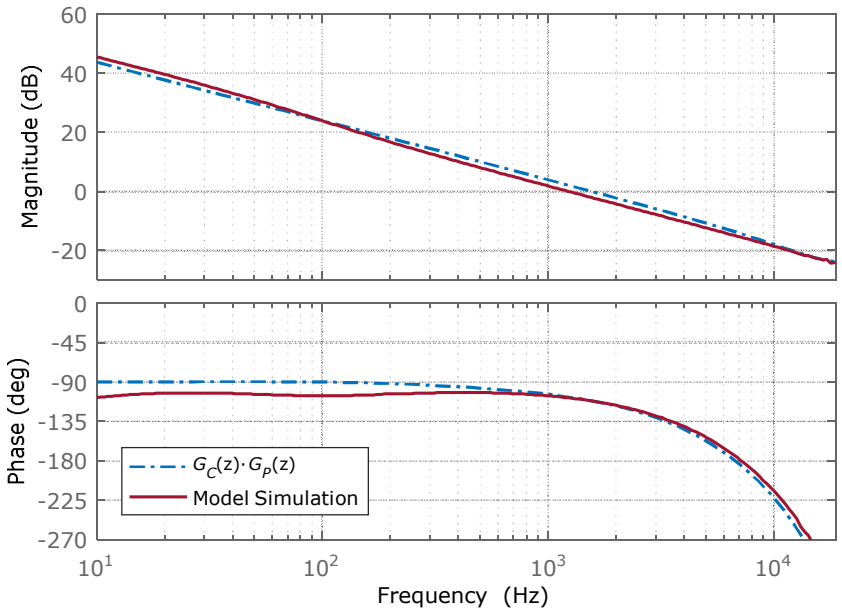

Fig. 4.12. Open loop Bode plots of the BHSI model controlled by $G_C(z)$: response of the actual model, $G_C(z) \cdot G_P(z) \Rightarrow PM$=68.5°, f_c=1.55kHz, GM=13.8dB; the Model Simulation with microcontroller (TMS320F28377S) and switching model of BHSI

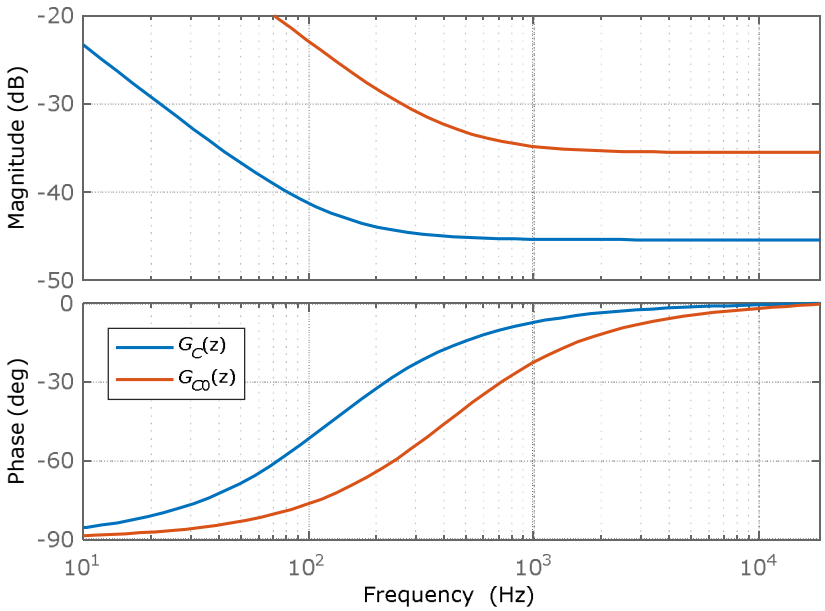

Fig. 4.13. Bode plots of the two controllers: $G_{C0}(z)$ – designed for an incomplete model of the BHSI; $G_C(z)$ – designed for the model of the BHSI which also includes the ADC delay

4.6. Simulation and experimental results

Two prototypes were built for the BHSI converter, using conventional Si-MOSFETs and new GaN-FETs, so that their influence in terms of efficiency and operation can be observed on this topology. The converter was designed with the parameters from Table 4.1, and with the transistors specified in Table 4.2.

Table 4.2. Switching devices characteristics

Symbol	Device		Unit	Description
	IXFK80N60P3 MOSFET	TPH3207WS GaN		
r_S	77	35	mΩ	Drain-source on-state resistance ($R_{DS(on)}$)
V_{SP}	4.33	7	V	Transistor switching point voltage
R_G	1	0	Ω	Internal gate resistance
Q_{GD}	48	6	nC	Gate-Drain charge
Q_{GS}	56	10	nC	Gate-Source charge
C_{OSS}	1240	202	pF	Output Capacitance
Q_{RRm}	1.4	0.175	µC	Reverse recovery charge of internal diode
I_{Tm}	40	32	A	Current at which Q_{RRm} was measured
V_{SD}	1.5	1.9	V	Source-Drain diode voltage drop
R_{th}	0.4	1.11	°C/W	Thermal resistance
$V_{DD(on)}$	15	15	V	Driver turn-on voltage
$V_{DD(off)}$	-3	-3	V	Driver turn-off voltage
R_{Don}	1	1	Ω	Internal driver resistances for t_{on} and t_{off}, respectively
R_{Doff}	0.37	0.4	Ω	
R_{Eon}	5.1	15	Ω	External driver resistances for t_{on} and t_{off}, respectively
R_{Eoff}	2	10	Ω	

Because of the series connection of the two inductors, the parasitic capacitances of the transistors, and the slight differences in inductances, voltage oscillations might appear on the two inductors, which can be undesirable. This phenomenon was studied for the unidirectional topology in [78], having the theoretical oscillations presented in Fig. 4.14. In order to dampen the oscillations, a passive RC snubber was added in parallel to one of the two inductors, having a resistance of 231Ω and a capacitance of 4.7nF.

The experimental setup, with the block diagram presented in Fig. 4.15 was realized in order to test the operation of the experimental prototype, and to measure its efficiency. The setup uses a supercapacitor bank (with the C_{SC} capacitance), a BHSI prototype, a DC bus capacitor (C_{bus}), an electronic load set up for constant voltage and a constant voltage DC source. The parallel connection of the load and the source is realized through a diode, and their purpose is to emulate the bidirectional functionality of a DC voltage bus.

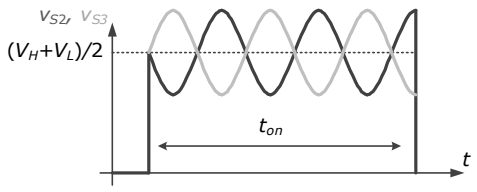

Fig. 4.14. S_2 and S_3 voltage oscillations during t_{on} due to their parasitic capacitance, and the tolerance of the two inductors (without adding an additional snubber)

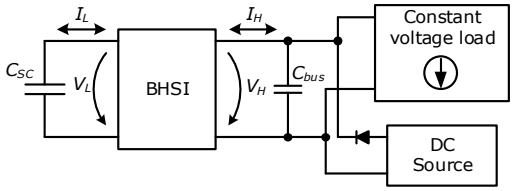

Fig. 4.15. Test setup consisting of a supercapacitor bank (C_{SC}), the BHSI converter, a bus capacitor (C_{bus}), a constant voltage load and a DC source (parameters in Table 4.3)

Table 4.3. Experimental setup equipment of the BSHI

Element	**Device**	**Manufacturer**	**Characteristics**
C_{SC}	BMOD0063 P125 B04	Maxwell	63F, 125V, 1900A, 1.7kW/kg, 2.3Wh/kg
Load	EA-EL 9400-50	Elektro-Automatik	0-2.4kW, 0-400V, 0-50A
DC Source	TC.P.10.400.400.S	Regatron	0-10kW, 0-400V, 0-50A
C_{bus}	-	-	10mF

Experimental and simulation results are presented from Fig. 4.16 to Fig. 4.28, for steady state or transient operation for both the Si-MOSFET and GaN prototypes, in order to analyze the dynamic operation. The simulation results are performed with the switching model of the converter which also includes the microcontroller, with its ADC and PWM specifications, and are used to confirm the operation of the prototypes.

The first set of results present the steady state operation of the two prototypes in Fig. 4.16 and Fig. 4.17 respectively. The inductor currents (i_{L1}, i_{L2}) and voltages (v_{L1}, v_{L2}) are presented, with the added RC snubber. The voltage inductor presents a small damped oscillation as previously discussed. Because of the voltage oscillations, small and insignificant current oscillations are also present. Because of the smaller parasitic capacitances of the GaN-FET devices, the inductor voltage oscillation should be more quickly damped as shown in the simulation results (Fig. 4.17), therefore it can be concluded that other parasitic capacitance are also present in the circuit (such as the voltage probe capacitance). Another small difference is observed between the experimental results: the oscillations from the Si-MOSFET prototype have slightly higher distortions that the GaN-FET prototype.

Transient response results are acquired for the BHSI controlled by either the $G_{C0}(z)$ or $G_C(z)$ controller, in order to show the influence of the control design without taking into account the additional delay of the ADC conversion, as discussed in 4.5. The operation of the BHSI controlled by $G_{C0}(z)$ shows a fast response, with a rapid transition between a step-up to a step-down mode, and vice versa , in Fig. 4.18 and Fig. 4.19, respectively, for the GaN-FET prototype with power levels of 1-2kW. Because of the low *PM* and *GM* (Fig. 4.11), an overshoot of approximately 40% is observed, which may be unacceptable because of the stress on the switches. The close-ups of the transition between the operation modes, from Fig. 4.20, Fig. 4.21 and Fig. 4.22, shows a quick settling time, within a few switching periods, regardless of the transitioning sequence. The Si-MOSFET prototype results, from Fig. 4.21 and Fig. 4.22 shows no difference in transient operation from the GaN-FET prototype.

The operation of the BHSI controlled by $G_C(z)$ controller shows a slower response, but with a good transition between step-up and a step-down mode, for the Si-MOSFET prototype in Fig. 4.23 and Fig. 4.24, or for the GaN prototype, in Fig. 4.25 and Fig. 4.26, for power levels of 1-2kW. Because of a significantly higher *PM* and *GM* (Fig. 4.12) the overshoot is reduced, at the cost of a slower response. The close-ups of the transitions, in Fig. 4.27 and Fig. 4.28 show a settling time of 0.4ms, 33% larger than the settling time of the BHSI with the $G_{C0}(z)$ of 0.3ms, shown in Fig. 4.22.

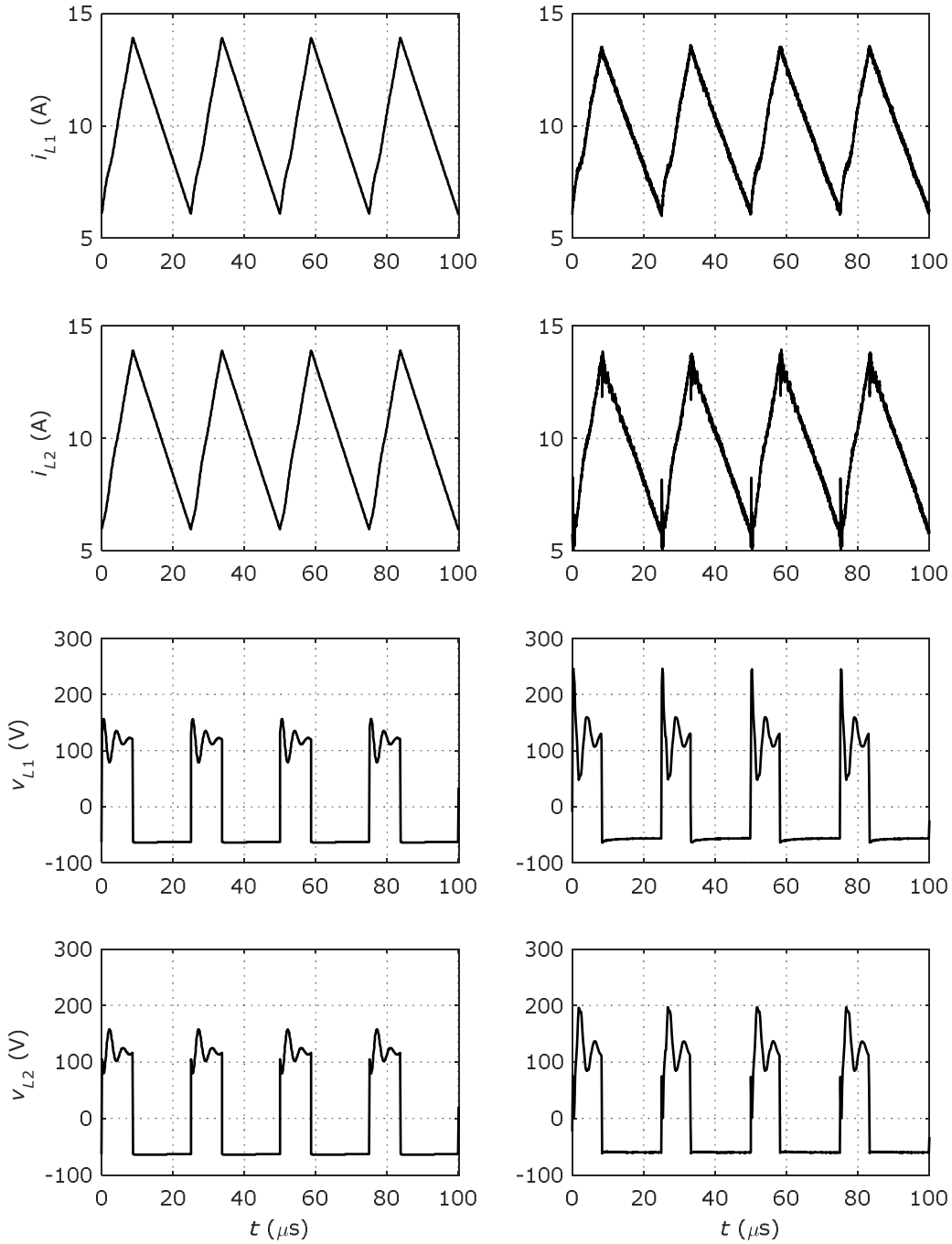

Fig. 4.16. BHSI with Si-MOSFETs simulation (left) and experimental (right) waveforms for steady state operation, operating at I_{L1}=I_{L2}=10A, V_L=60V, V_H=300V, P_{in}=1kW, C_{SC}=2x63F (i_{L1}, i_{L2}, and v_{L1}, v_{L2} are the currents and voltages for L_1 and L_2 inductors, respectively)

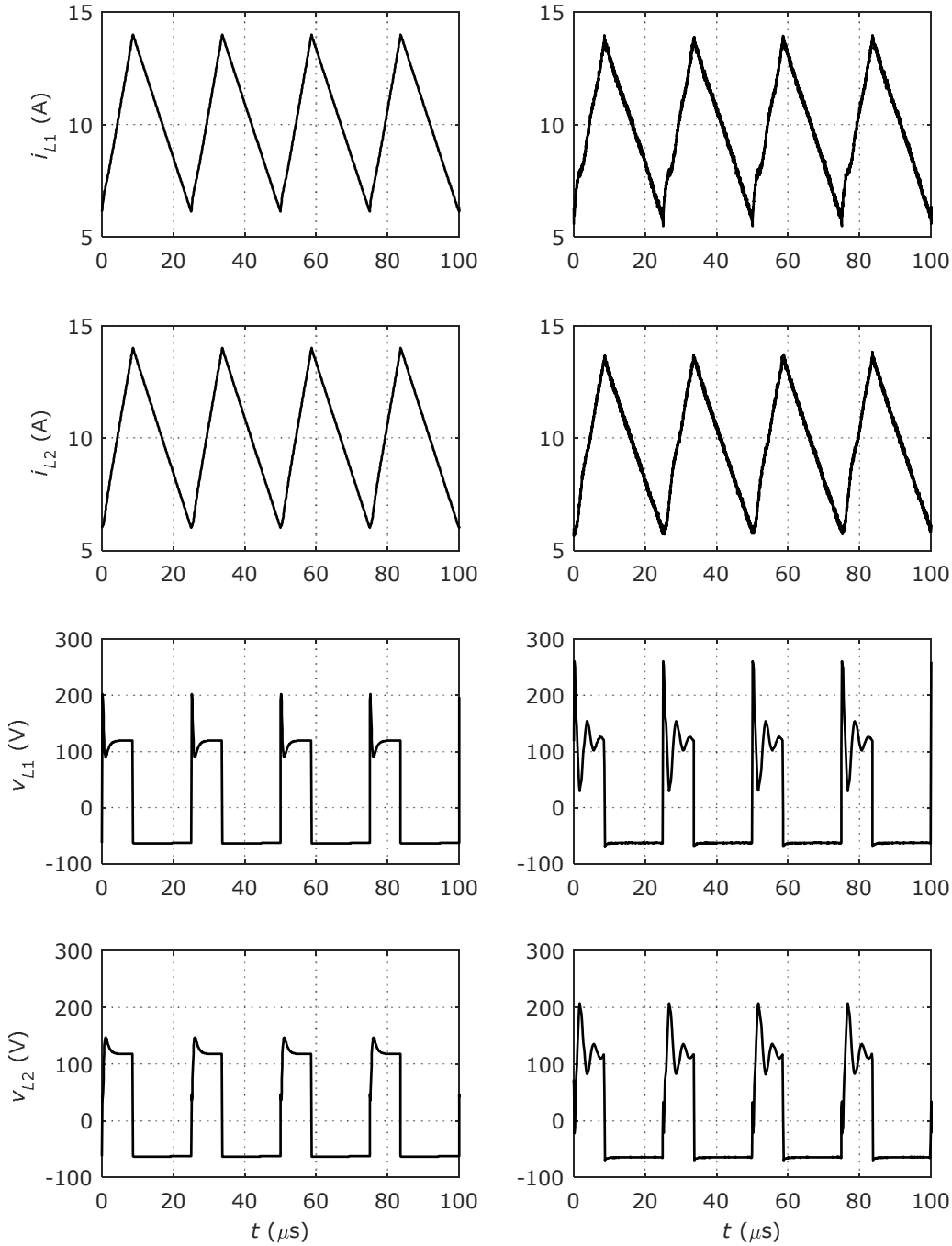

Fig. 4.17. BHSI with GaN-FETs simulation (left) and experimental (right) waveforms for steady state operation, operating at I_{L1}=I_{L2}=10A, V_L=60V, V_H=300V, P_{in}=1kW, C_{SC}=2x63F (i_{L1}, i_{L2}, and v_{L1}, v_{L2} are the currents and voltages for L_1 and L_2 inductors, respectively)

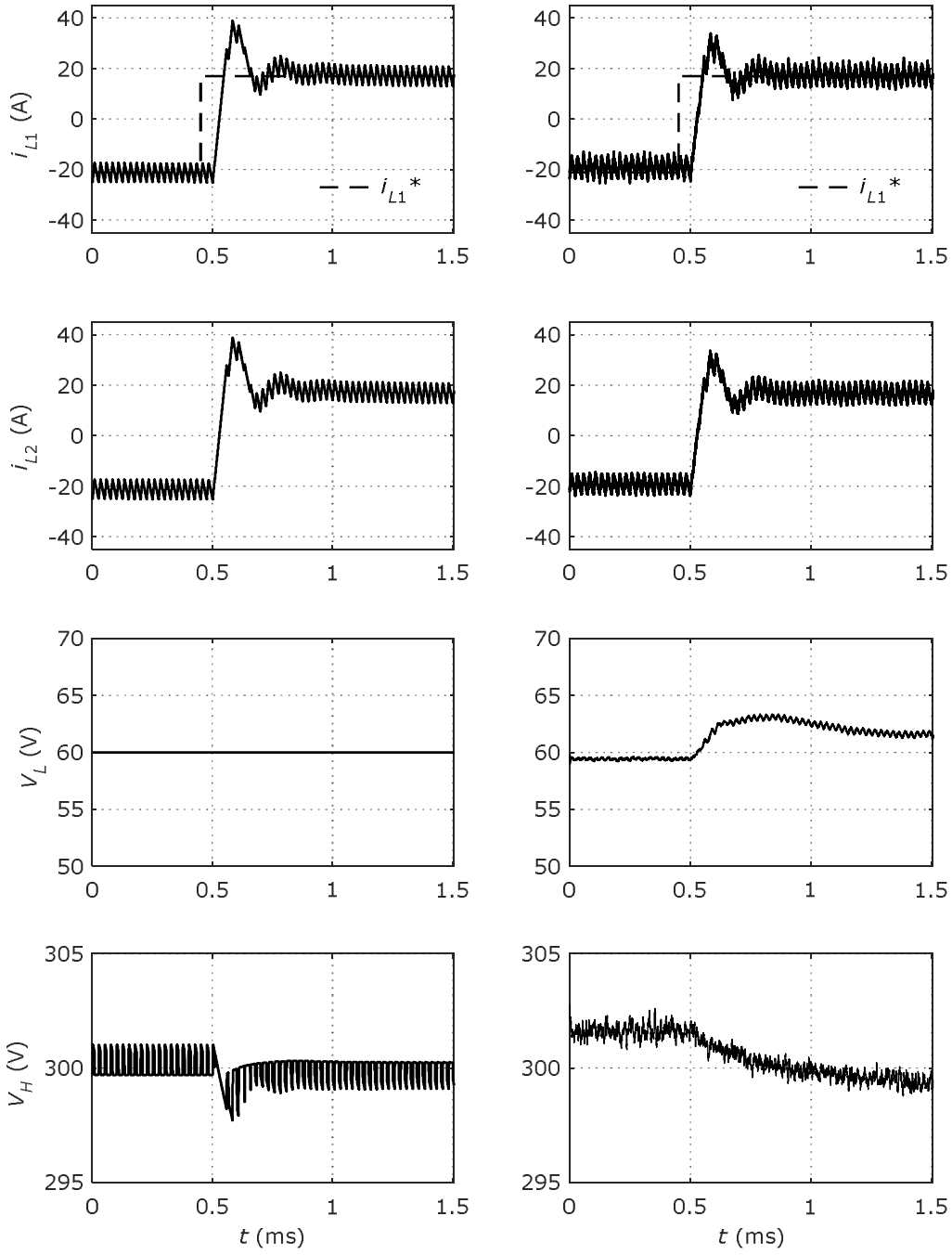

Fig. 4.18. BHSI with GaN-FETs simulation (left) and experimental (right) waveforms for transient operation, controlled by $G_{C0}(z)$ (tuned for $G_{P0}(z)$): transition from i_{L1}*=-20A (step-up) to i_{L1}*=20A (step-down), V_L=60V, V_H=300V, P_{in}=±2kW, C_{SC}=63F (i_{L1}, i_{L2}, are the currents from L_1 and L_2 inductors, respectively, V_L, V_H are the low and high voltage inputs, respectively)

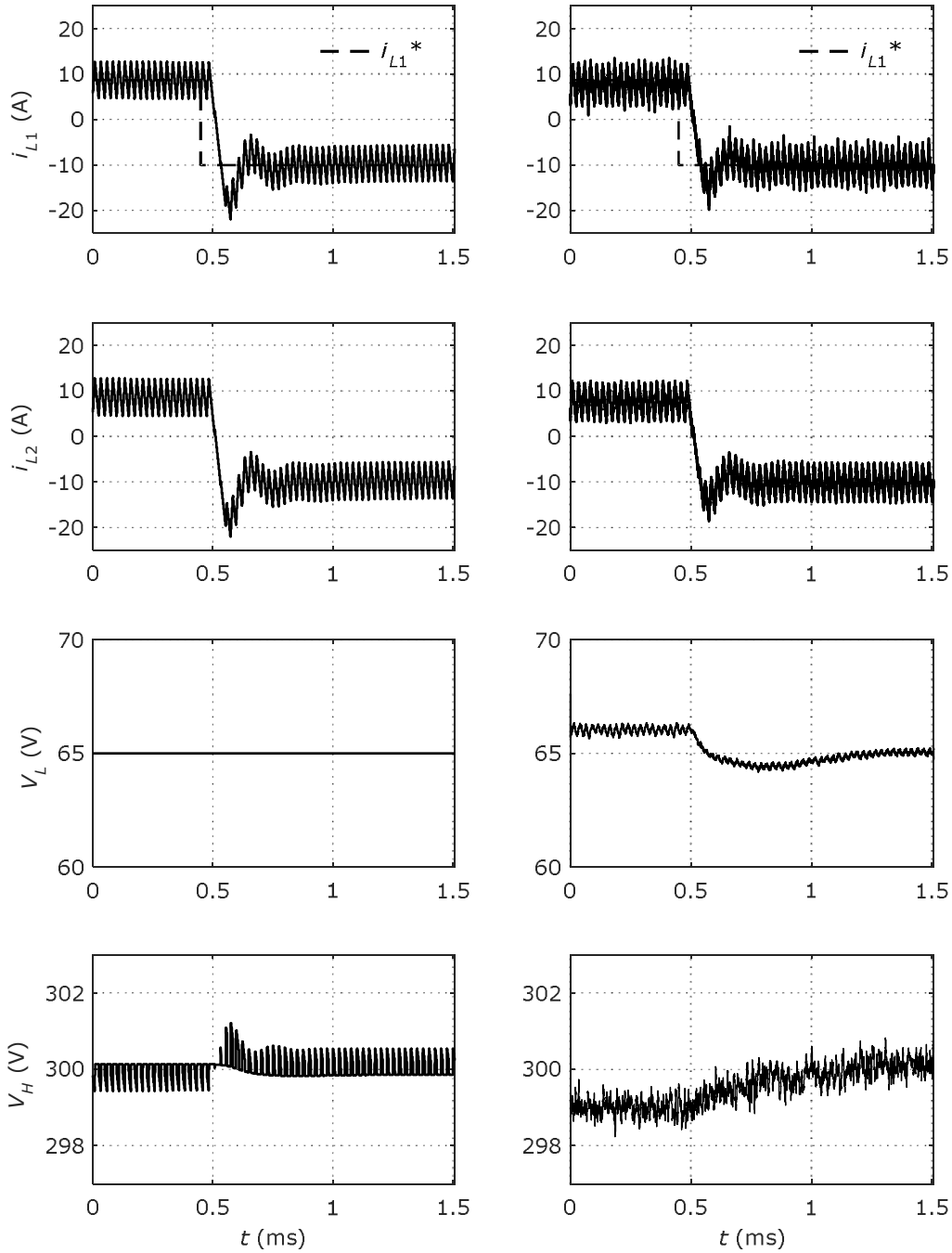

Fig. 4.19. BHSI with GaN-FETs simulation (left) and experimental (right) waveforms for transient operation, controlled by $G_{C0}(z)$ (tuned for $G_{P0}(z)$): transition from i_{L1}*=10A (step-down) to i_{L1}*=-10A (step-up), V_L=65V, V_H=300V, P_{in}=±1.07kW, C_{SC}=63F (i_{L1}, i_{L2}, are the currents from L_1 and L_2 inductors, respectively, V_L, V_H are the low and high voltage inputs, respectively)

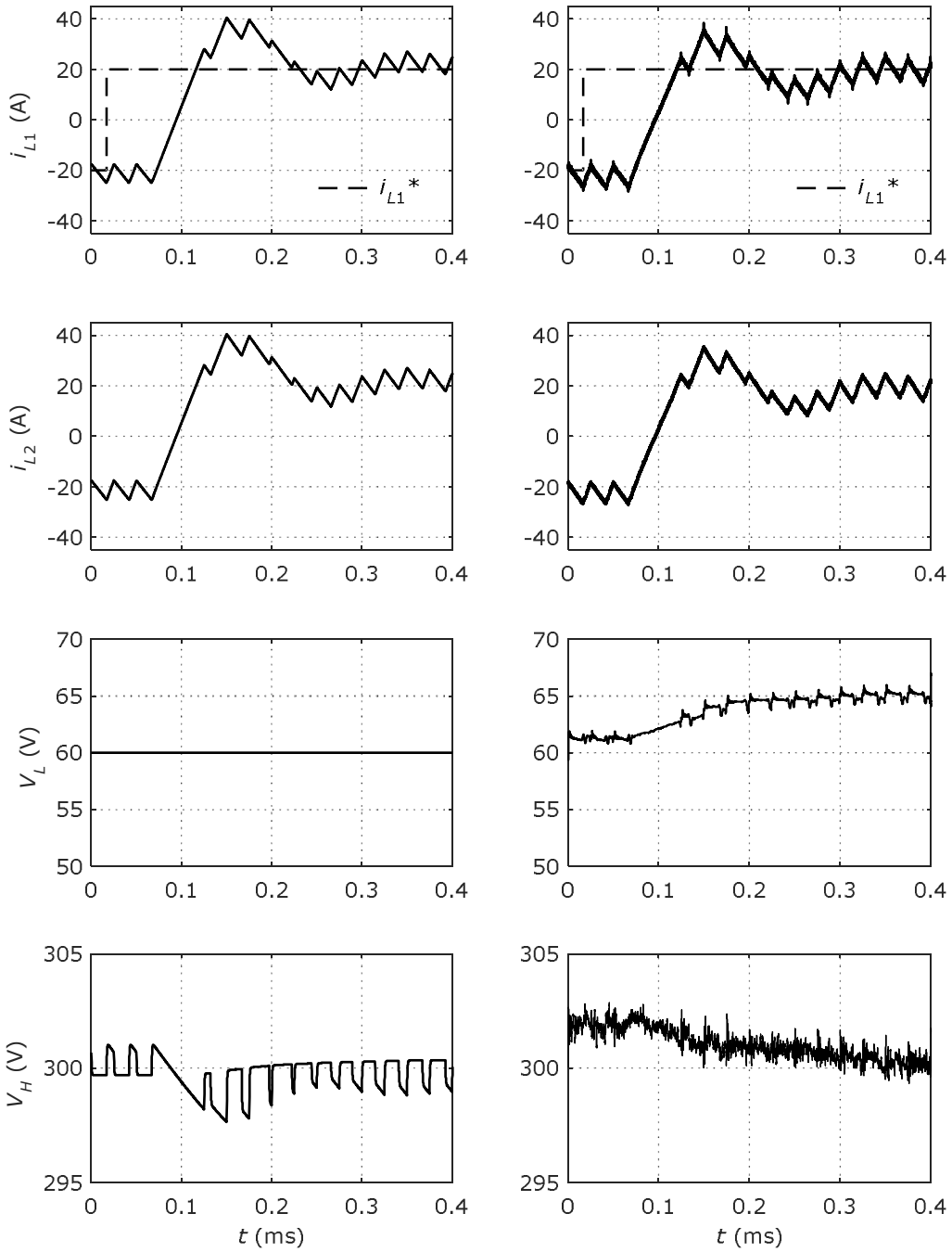

Fig. 4.20. BHSI with GaN-FETs simulation (left) and experimental (right) waveforms for transient operation, controlled by $G_{C0}(z)$ (tuned for $G_{P0}(z)$): transition from i_{L1}*=-20A (step-up) to i_{L1}*=20A (step-down), V_L=60V, V_H=300V, P_{in}=±2kW, C_{SC}=63F (i_{L1}, i_{L2}, are the currents from L_1 and L_2 inductors, respectively, V_L, V_H are the low and high voltage inputs, respectively)

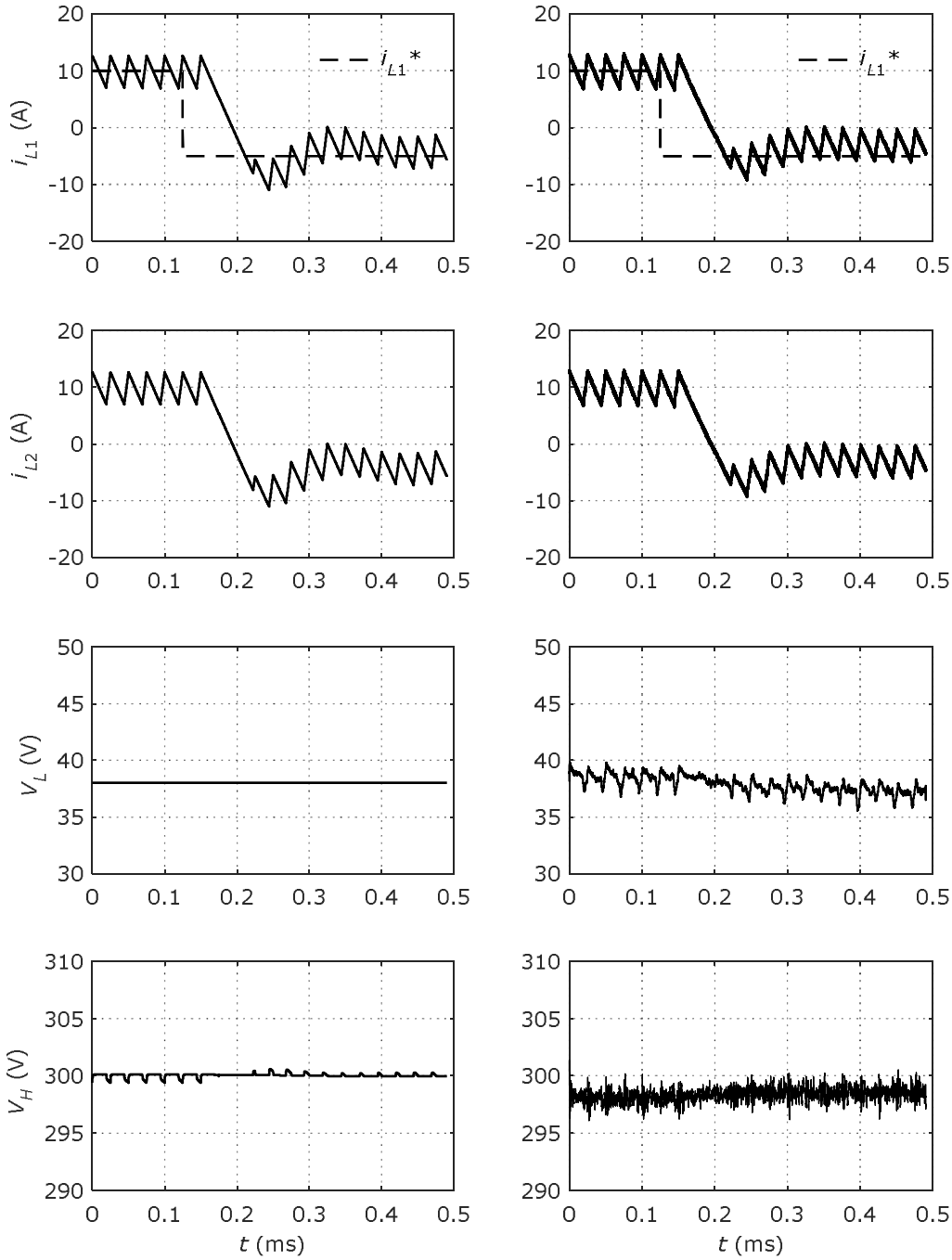

Fig. 4.21. BHSI with Si-MOSFETs simulation (left) and experimental (right) waveforms for transient operation, controlled by $G_{C0}(z)$ (tuned for $G_{P0}(z)$): transition from i_{L1}*=10A (step-down) to i_{L1}*=-5A (step-up), V_L=40V, V_H=300V, P_{in}=705W/-350W, C_{SC}=63F (i_{L1}, i_{L2}, are the currents from L_1 and L_2 inductors, respectively, V_L, V_H are the low and high voltage inputs, respectively)

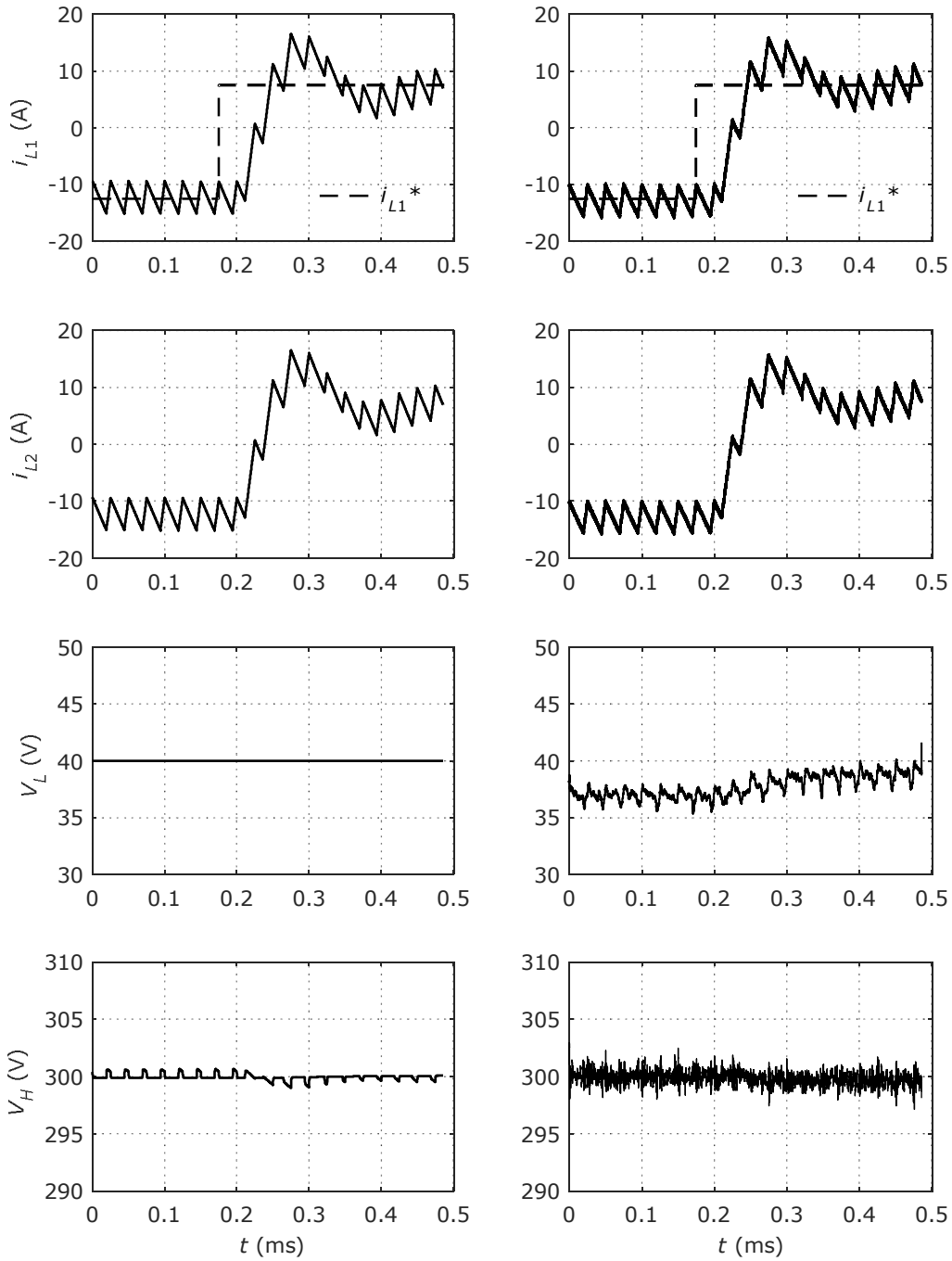

Fig. 4.22. BHSI with Si-MOSFETs simulation (left) and experimental (right) waveforms for transient operation, controlled by $G_{C0}(z)$ (tuned for $G_{P0}(z)$): transition from i_{L1}*=-12.5A (step-up) to i_{L1}*=7.5A (step-down), V_L=40V, V_H=300V, P_{in}=-880W/530W, C_{SC}=63F (i_{L1}, i_{L2}, are the currents from L_1 and L_2 inductors, respectively, V_L, V_H are the low and high voltage inputs, respectively)

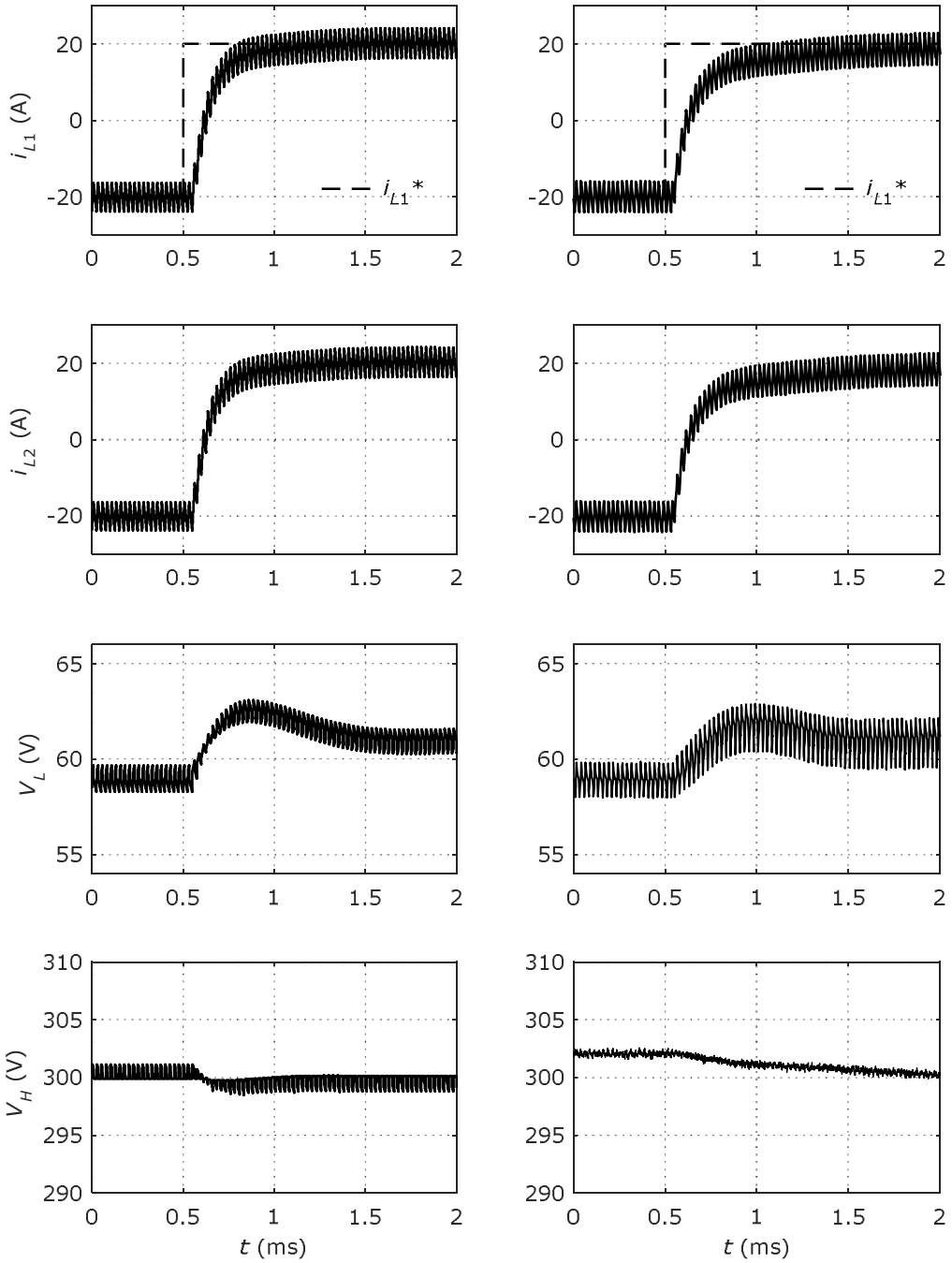

Fig. 4.23. BHSI with Si-MOSFETs simulation (left) and experimental (right) waveforms for transient operation, controlled by G_C(z) (tuned for G_P(z)): transition from i_{L1}*=-20A (step-up) to i_{L1}*=20A (step-down), V_L=60V, V_H=300V, P_{in}=±2kW, C_{SC}=126F (i_{L1}, i_{L2}, are the currents from L_1 and L_2 inductors, respectively, V_L, V_H are the low and high voltage inputs, respectively)

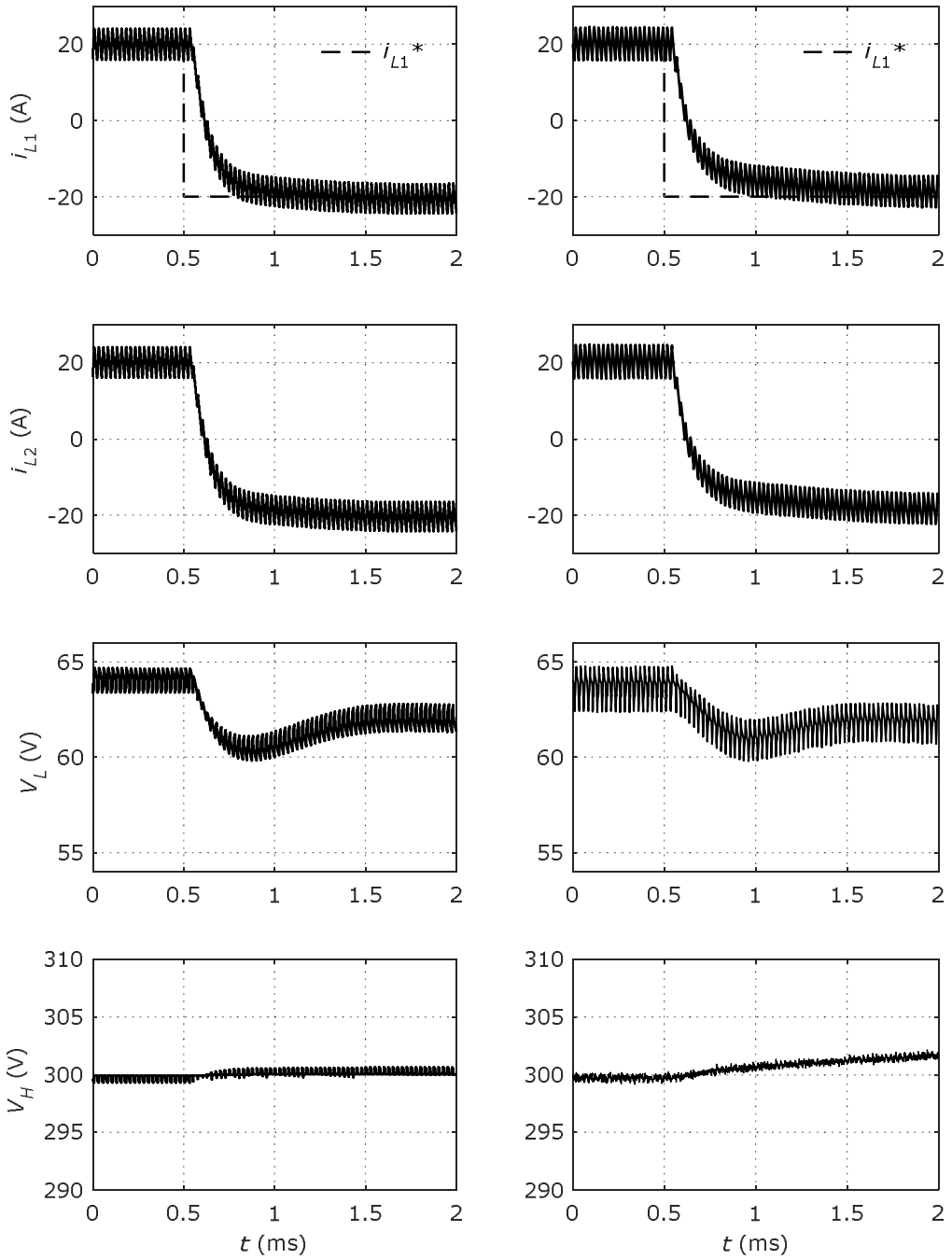

Fig. 4.24. BHSI with Si-MOSFETs simulation (left) and experimental (right) waveforms for transient operation, controlled by $G_C(z)$ (tuned for $G_P(z)$): transition from i_{L1}*=20A (step-down) to i_{L1}*=-20A (step-up), V_L=65V, V_H=300V, P_{in}=±2.14kW, C_{SC}=126F (i_{L1}, i_{L2}, are the currents from L_1 and L_2 inductors, respectively, V_L, V_H are the low and high voltage inputs, respectively)

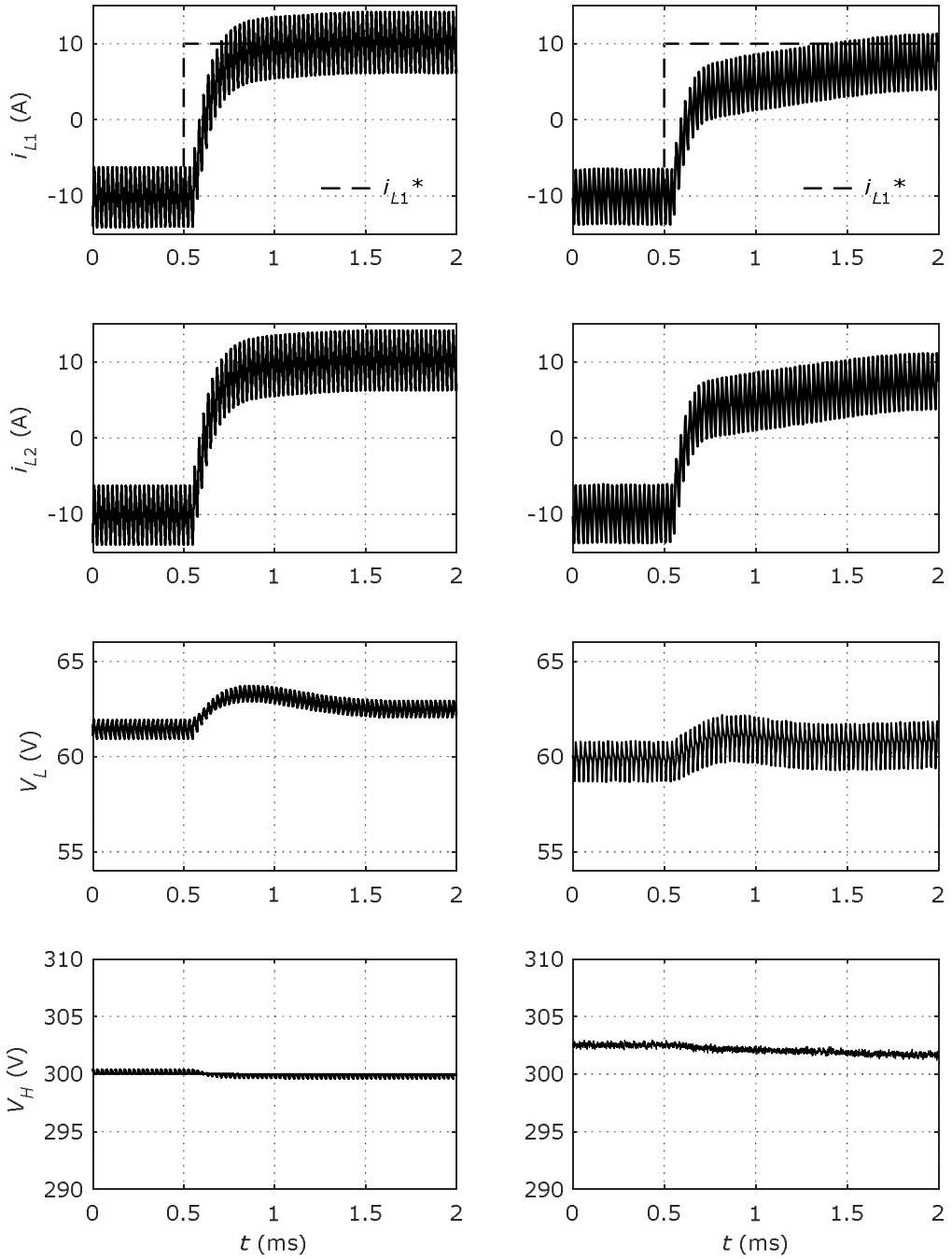

Fig. 4.25. BHSI with GaN-FETs simulation (left) and experimental (right) waveforms for transient operation, controlled by $G_C(z)$ (tuned for $G_P(z)$): transition from i_{L1}*=-10A (step-up) to i_{L1}*=10A (step-down), V_L=61V, V_H=300V, P_{in}=±1kW, C_{SC}=126F (i_{L1}, i_{L2}, are the currents from L_1 and L_2 inductors, respectively, V_L, V_H are the low and high voltage inputs, respectively)

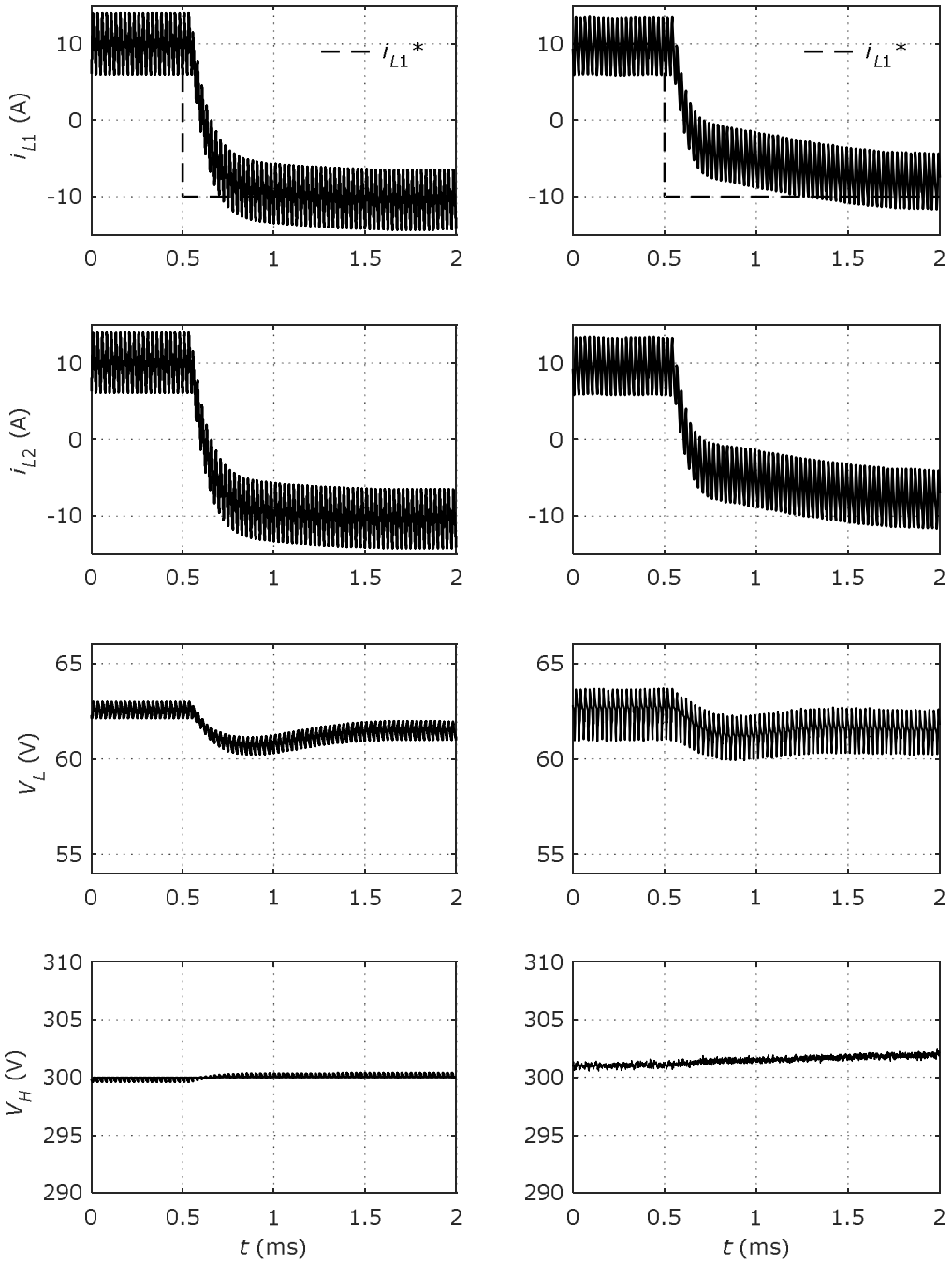

Fig. 4.26. BHSI with GaN-FETs simulation (left) and experimental (right) waveforms for transient operation, controlled by $G_C(z)$ (tuned for $G_P(z)$): transition from i_{L1}*=10A (step-down) to i_{L1}*=-10A (step-up), V_L=62V, V_H=300V, P_{in}=±1.03kW, C_{SC}=126F (i_{L1}, i_{L2}, are the currents from L_1 and L_2 inductors, respectively, V_L, V_H are the low and high voltage inputs, respectively)

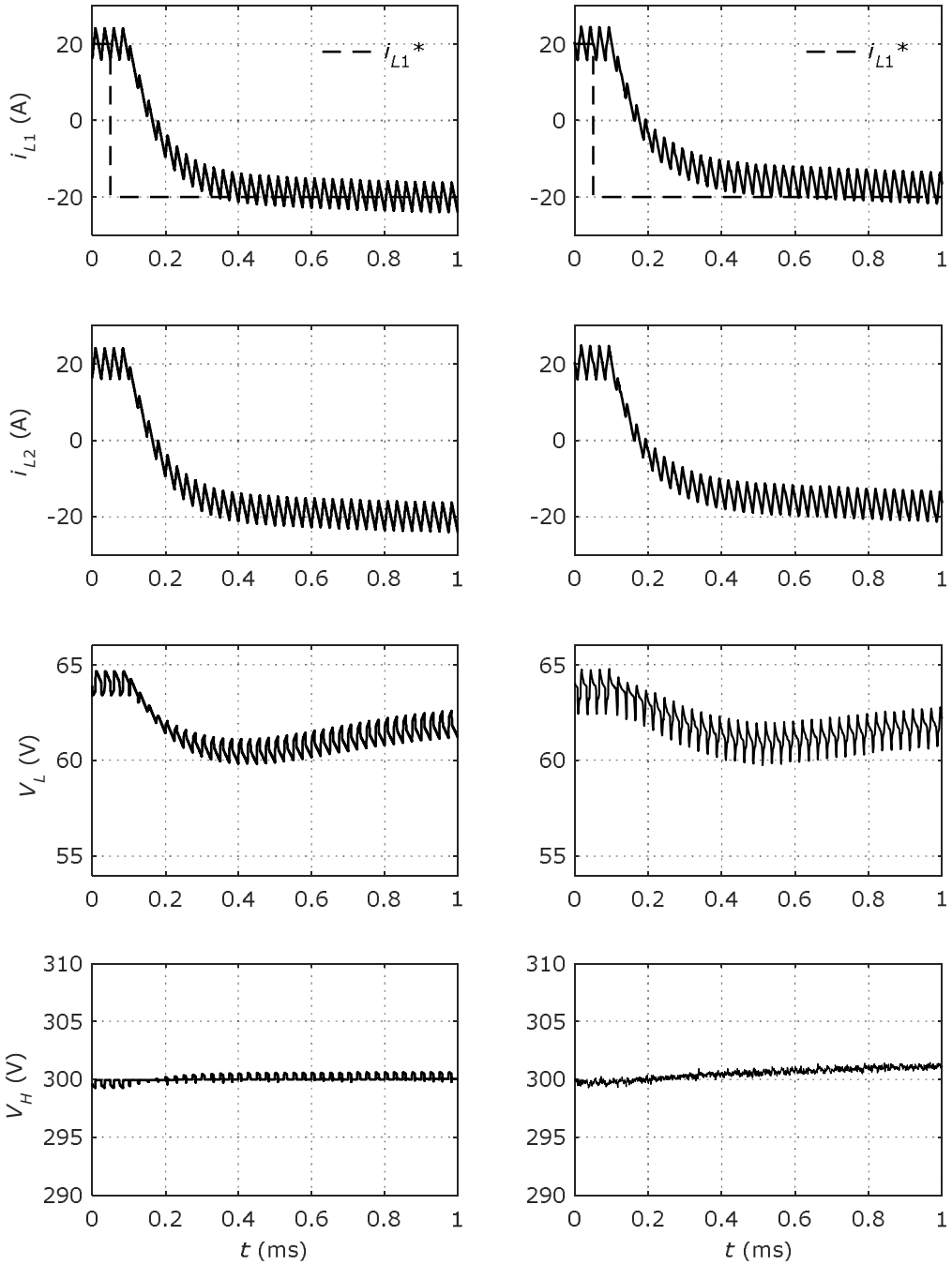

Fig. 4.27. BHSI with Si-MOSFETs simulation (left) and experimental (right) waveforms for transient operation, controlled by $G_C(z)$ (tuned for $G_P(z)$): transition from i_{L1}*=20A (step-down) to i_{L1}*=-20A (step-up), V_L=65V, V_H=300V, P_{in}=±2.14kW, C_{SC}=126F (i_{L1}, i_{L2}, are the currents from L_1 and L_2 inductors, respectively, V_L, V_H are the low and high voltage inputs, respectively)

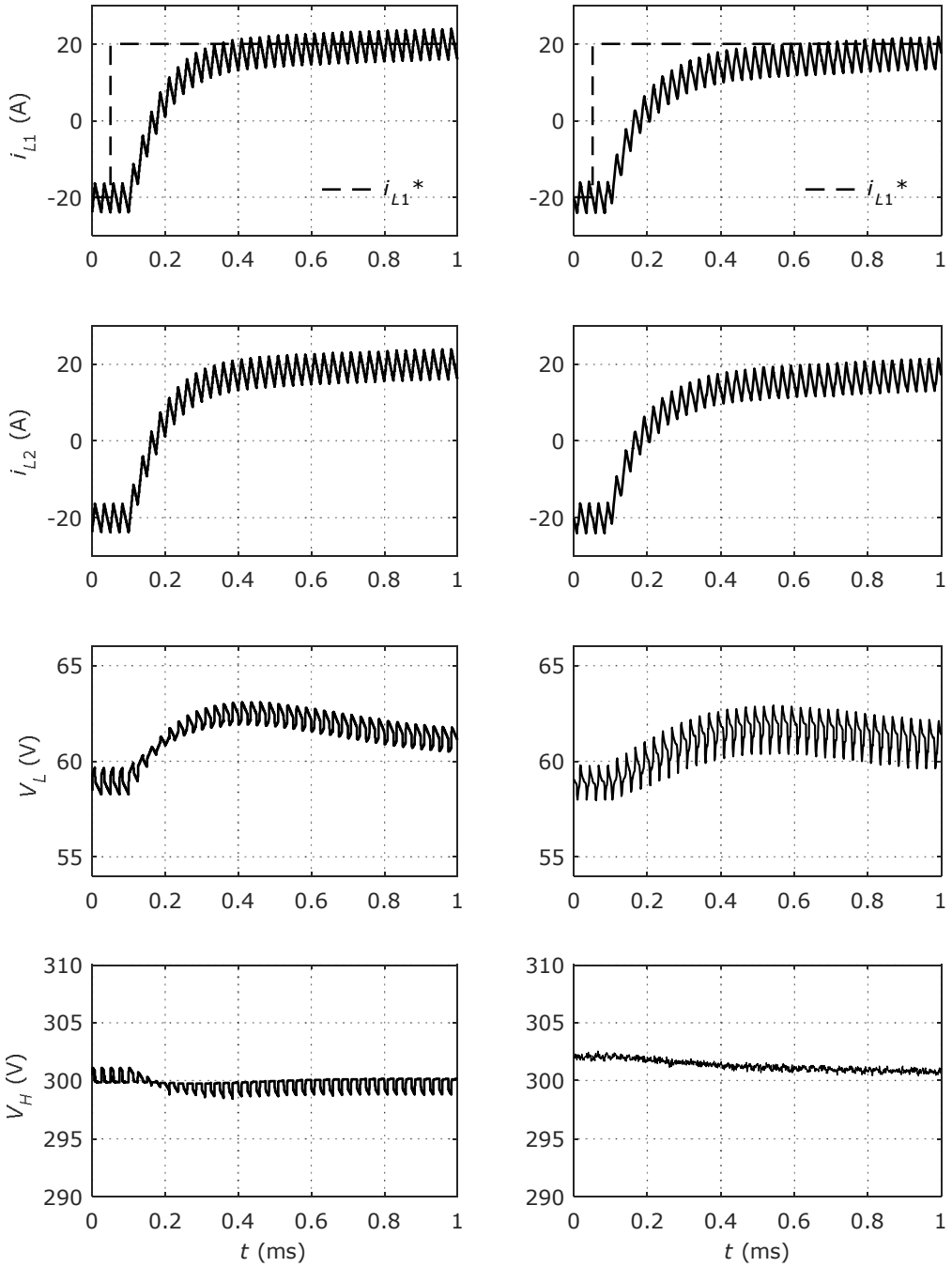

Fig. 4.28. BHSI with Si-MOSFETs simulation (left) and experimental (right) waveforms for transient operation, controlled by $G_C(z)$ (tuned for $G_P(z)$): transition from i_{L1}*=-20A (step-up) to i_{L1}*=20A (step-down), V_L=60V, V_H=300V, P_{in}=±2kW, C_{SC}=126F (i_{L1}, i_{L2}, are the currents from L_1 and L_2 inductors, respectively, V_L, V_H are the low and high voltage inputs, respectively)

Photos of the two prototypes with Si-MOSFETs and GaN-FETs are shown in Fig. 4.29 and Fig. 4.30, respectively.

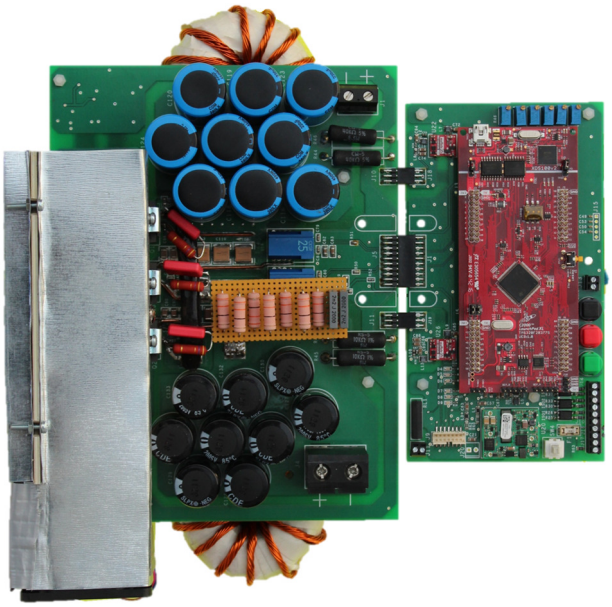

Fig. 4.29. BHSI prototype with Si-MOSFETs (IXFK80N60P3)

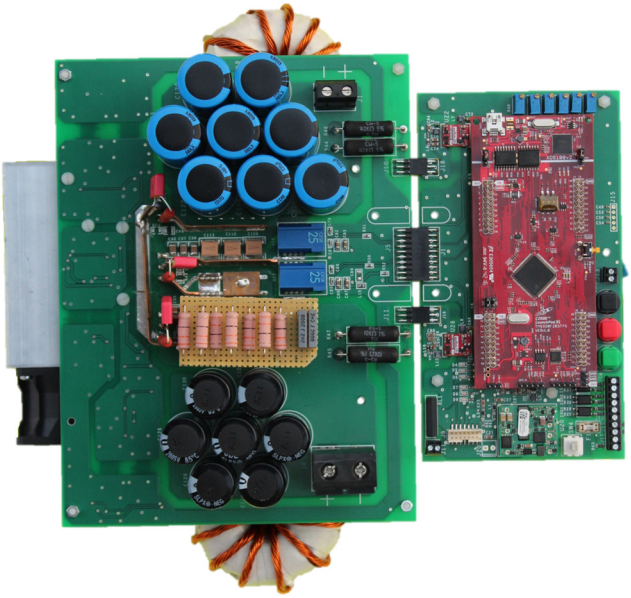

Fig. 4.30. BHSI prototype with GaN-FETs (TPH3207WS)

4.7. Efficiency results

The efficiency of the two prototypes was calculated, by directly measuring the input and output currents and voltages, and it was compared with the theoretical analysis. The theoretical analysis for the efficiency of the BHSI includes the distribution of power losses of the active switches and passive components, and also the temperatures of the switches.

To calculate the active switch losses, the parameters from Table 4.2 were used, together with the device's respective datasheets. The switch losses were calculated by adding the conduction losses, from the drain-source on-state resistance ($R_{DS(on)}$), and the switching losses, calculated with the method presented in [82]. Based on the power losses and the thermal resistances of the case, the active device temperature was calculated.

The calculations and measurements were performed on both prototypes of the BHSI for the Si-MOSFET prototype in Fig. 4.31, and the GaN-FET prototype in Fig. 4.32, in both operation modes, step-down and step-up.

Results show that the efficiency for step-down operation is higher for both the Si-MOSFET and GaN-FET prototypes, with 2% improvement for the latter. A good correspondence is shown between the mathematical calculations, and the experimental measurements.

In step-up operation, a difference is shown between calculations, for both the Si-MOSFET and GaN-FET prototypes, of approximately 4% for the first, and 2% for the latter. The difference may be accounted by a few factors such as different turn-on delay between S_2 and S_3 switches, the voltage oscillations on the inductors, or a higher dv/dt on S_1 during S_2 - S_3 during turn-on.

The temperature of the active switches during each operation mode is below 70°C, which indicates that higher powers are possible with regards to the power dissipation capabilities of the switching devices. The power loss distribution of the switches shows how the switching and conductive losses are distributed for the S_1 and S_2/S_3 switches, for the considered power range. An important difference is for the reverse recovery loss for the GaN-FET which is considered negligible, therefore reducing the overall losses. The conductive losses are also lower for the GaN-FET, because of the lower $R_{DS(on)}$. As expected, the most significative difference, is in the switching loss of S_1 for the GaN-FET, being approximately 30% of that of the Si-MOSFET prototype.

The distribution of the power losses in the switches, for both prototypes and for both operating modes at nominal power, is presented in Fig. 4.33 and Fig. 4.34 for Si-MOSFET devices and GaN-FET devices respectively. From these diagrams it can be concluded that the GaN-FET devices have approximately 30% lower losses than the Si-MOSFETs.

The active switch losses are small for these prototypes compared to the rest of the losses, which are calculated and shown in Fig. 4.35. Apart from the active switch losses, other losses are considered in: the inductor resistance (P_{L1}, P_{L2}), ESR of C_H capacitor (P_{Ch}) and C_L capacitor (P_{Cl}), the RC snubber (P_{Snub}). Both prototypes present almost identical passive components, therefore the two losses are considered identical.

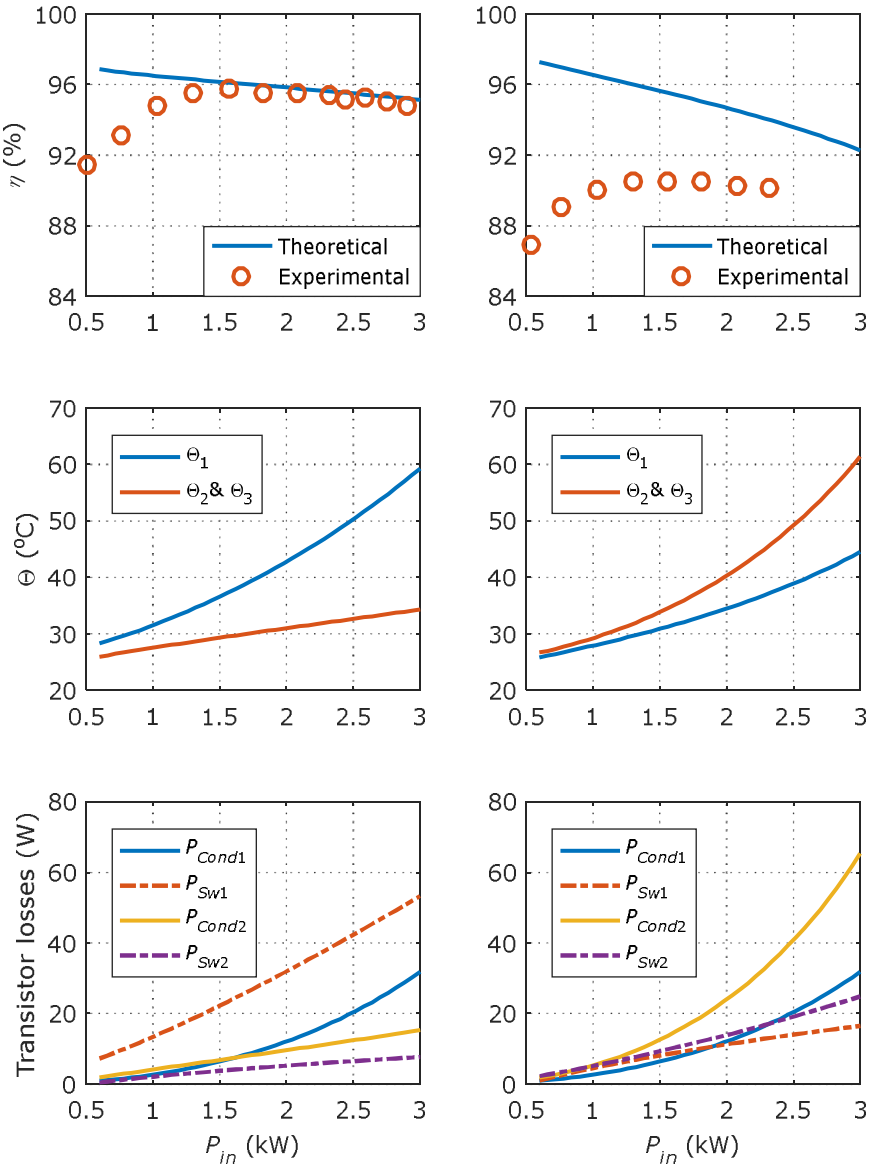

Fig. 4.31. Theoretical and Experimental efficiency results (η), active switch temperatures (Θ), and power loss distributions for the Si-MOSFET (IXFK80N60P3) prototype of the BHSI (with parameters from Table 4.1) for both, step-down (left) and step-up (right) operation modes, V_L=60V, V_H=300V, f=40kHz, P_{in}=0.5-3kW, C_{SC}=126F

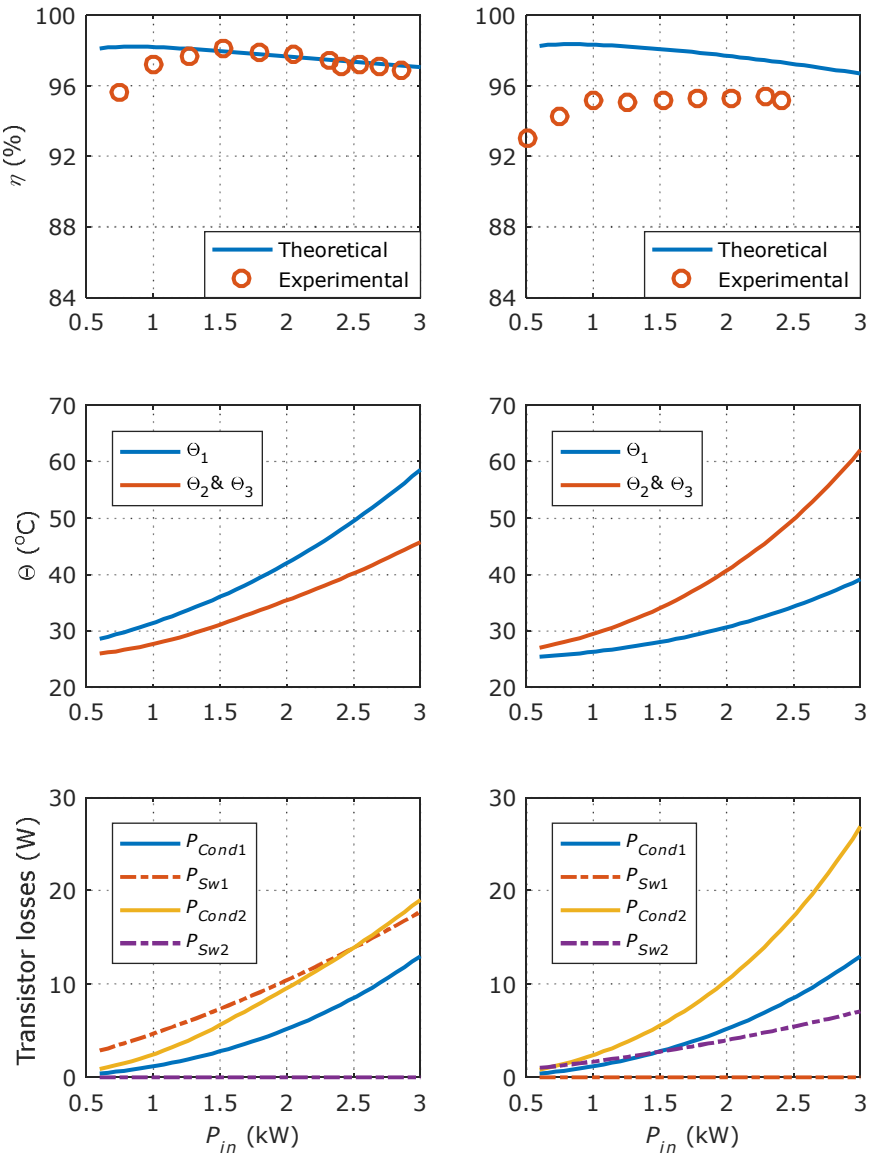

Fig. 4.32. Theoretical and Experimental efficiency results (η), active switch temperatures (Θ), and power loss distributions for the GaN-FET (TPH3207WS) prototype of the BHSI (with parameters from Table 4.1) for both, step-down (left) and step-up (right) operation modes, V_L=60V, V_H=300V, f=40kHz, P_{in}=0.5-3kW, C_{SC}=126F

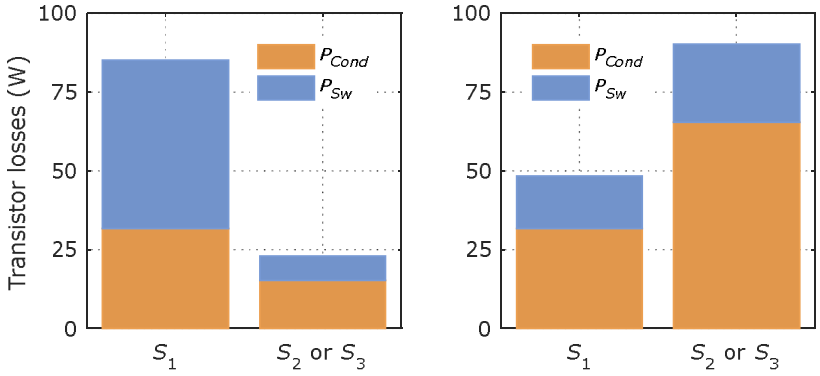

Fig. 4.33. Power loss distribution in the active switches of the BHSI (parameters in Table 4.1), for Si-MOSFETs (IXFK80N60P3), in step-down operation (left) and step-up operation (right) (V_L=60V, V_H=300V, f=40kHz, P_{in}=3kW, C_{SC}=126F)

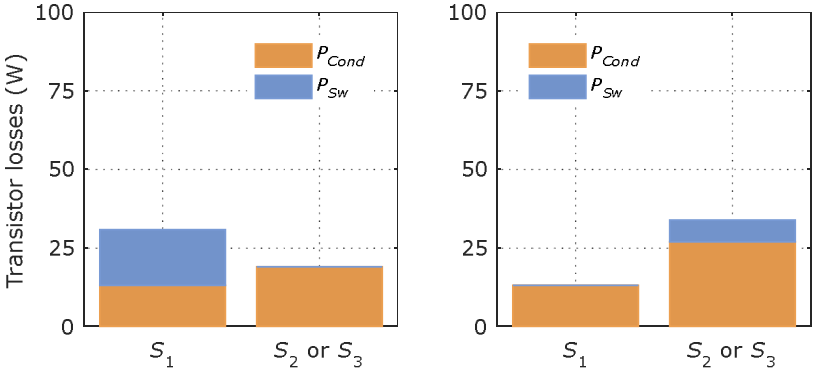

Fig. 4.34. Power loss distribution in the active switches of the BHSI (parameters in Table 4.1), for GaN-FETs (TPH3207WS), in step-down operation (left) and step-up operation (right) (V_L=60V, V_H=300V, f=40kHz, P_{in}=3kW, C_{SC}=126F)

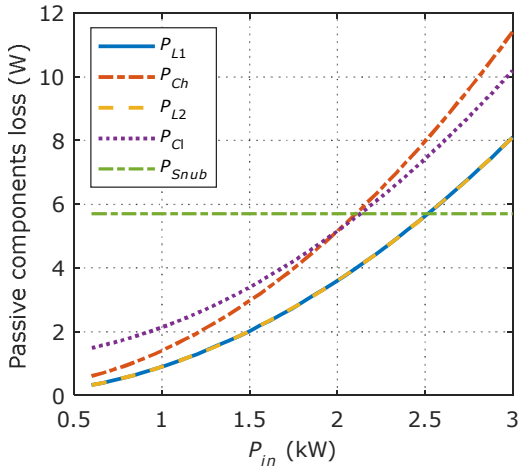

Fig. 4.35. BHSI (with parameters in Table 4.1) passive components power loss distribution, identical for both prototypes: P_{L1}, P_{L2} –power loss in the inductor resistance, P_{Ch} – power loss in C_H capacitor ESR, P_{Cl} – power loss in C_L capacitor ESR, P_{Snub} – power loss in the RC snubber (V_L=60V, V_H=300V, f=40kHz, P_{in}=0.5-3kW, C_{SC}=126F)

4.8. Topology improvements

Because the voltage oscillation that appears on the two inductors during the series connection of the two inductors might be undesirable for several reasons, an Improved schematic of the Bidirectional Hybrid Switched Inductor converter (I-BHSI) which eliminates the oscillations is presented in Fig. 4.36 [83].

A method for eliminating the oscillations in the unidirectional boost topology was proposed in [78], by using an additional capacitor and diode. The method described here however, uses a different schematic that can operate in bidirectional mode. The improvement of the BHSI consist of adding and additional switch, and two capacitors, C_1 and C_2, in parallel to each one of the two newly formed half bridges (S_{L1} – S_{H1} and S_{L2} – S_{H2}).

In addition to the elimination of the oscillations, the two capacitors maintain a constant voltage between the two sources, V_H and V_L, therefore they eliminate the high switching frequency voltage between sources. In comparison to the BHSI, the I-BHSI has an additional advantage: it can use commercially available half-bridges, and the layout of the transistors helps achieve a smaller switching loop for each half bridge. The use of half bridges has a benefit in PCB design, and for the mathematical analysis because of the numerous studies available on this subject [84]–[86].

Even if additional components are added to the schematic, the relations from section 4.3 are still applicable. The operation of the I-BHSI is similar to that of the BHSI, as it can be observed from the two equivalent switching states from Fig. 4.37. The results remain unchanged, even if in this schematic all transistors have the same voltage stress.

Simulation results are provided in Fig. 4.38, where the waveforms of the I-BHSI are presented with or without the additional capacitors, C_1 and C_2.

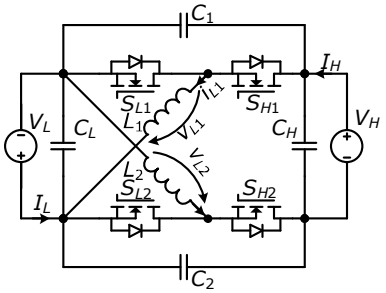

Fig. 4.36. The Improved Bidirectional Hybrid Switched Inductor converter (I-BHSI) [83]

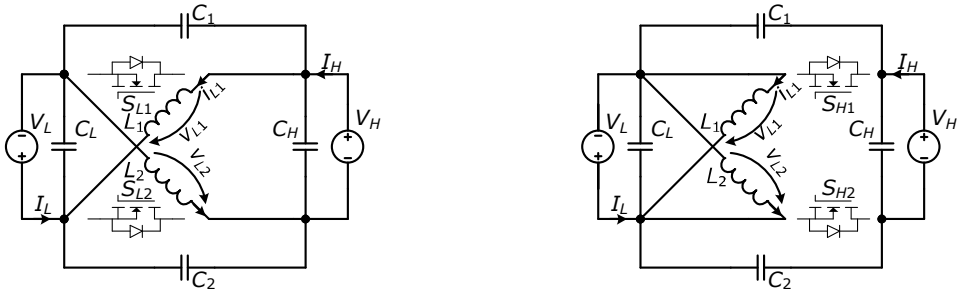

Fig. 4.37. Equivalent schematic of I-BHSI during t_{on} interval (left) and t_{off} interval (right)
(t_{on}: S_{H1} and S_{H2} are turned ON, S_{L1} and S_{L2} are turned OFF;
t_{off}: S_{H1} and S_{H2} are turned OFF, S_{L1} and S_{L2} are turned ON)

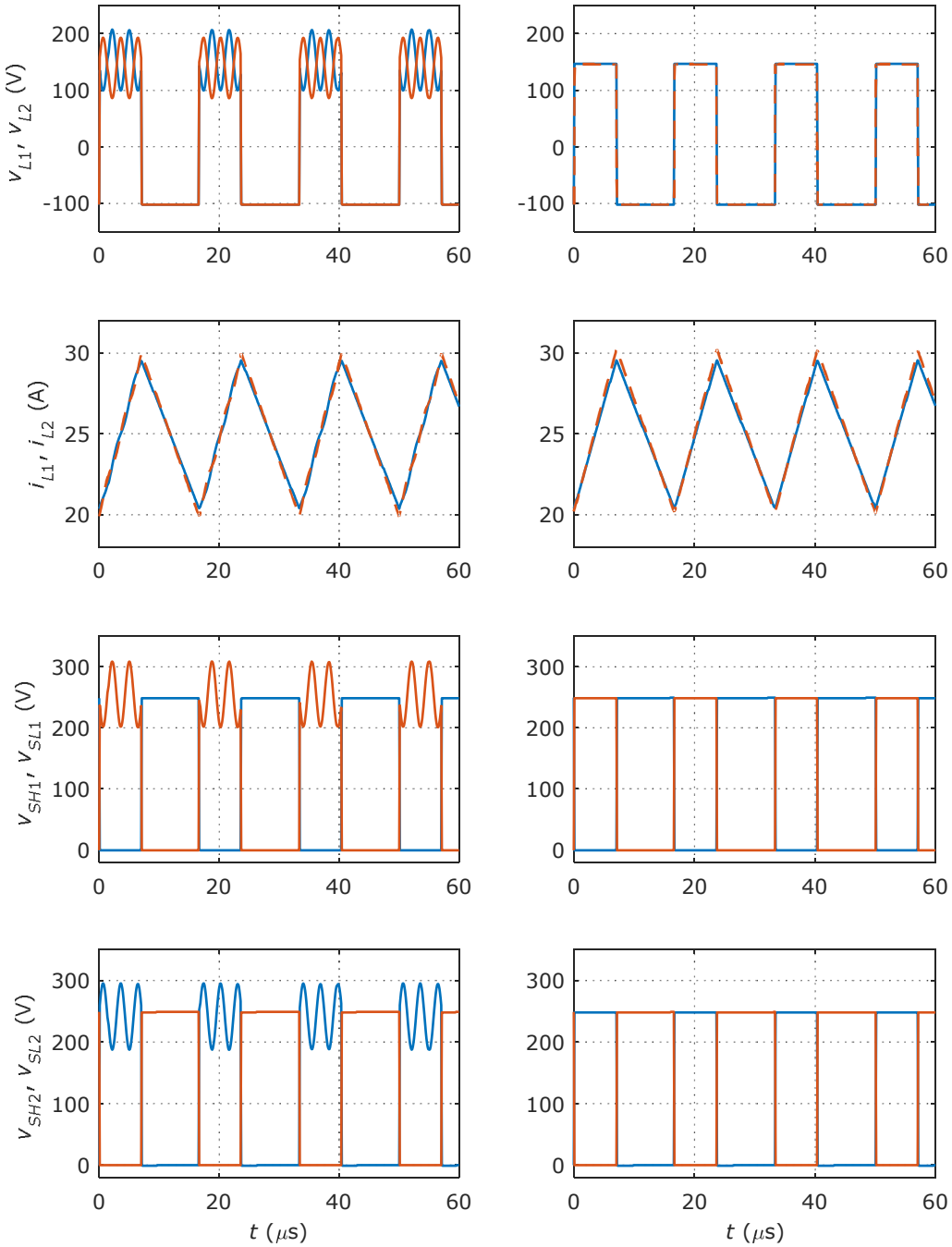

Fig. 4.38. Simulation waveforms for the I-BHSI with C_1 and C_2 (right), and without (left) (i_{L1}, i_{L2}, and v_{L1}, v_{L2} are the currents and voltages for L_1 and L_2 inductors, respectively; v_{SH1}, v_{SL1}, and v_{SH2}, v_{SL2} are the switches voltages from the two half bridges)

The I-BHSI without the capacitors is actually the BHSI converter with an additional switch, which does change the operation of the converter. As shown in the results, the complete schematic of I-BHSI does not present voltage oscillations on the inductors, and therefore on transistors, limiting the maximum voltage on the switches, and reducing EMI.

4.9. Conclusions

A theoretical analysis was performed for the BHSI converter in steady state and dynamic operation. The analytical description is beneficial for obtaining the metrics required for an objective comparison to other topologies. Based on the dynamic model of the BHSI, a digital controller was designed and the influence of an incorrect modelling of the microcontroller was shown in the frequency response of the system and from experimental results. The two prototypes built for the BHSI converter, using Si-MOSFETs and GaN-FETs show an insignificant difference in the operation of the converter, but significant results for its efficiency. Simulation results confirm the dynamic modeling and are in good concordance to the experimental results.

The oscillations which were also found in the unidirectional topologies, are also present in the BHSI, but can be damped by using an simple RC snubber, or they can be eliminated with the improved version of this topology, which is also presented and analyzed in this chapter.

5. THE BIDIRECTIONAL HYBRID SWITCHED INDUCTOR SWITCHED CAPACITOR CONVERTER (BHSISC)

5.1. Abstract

This chapter presents a Bidirectional Hybrid Switched Inductor Switched Capacitor converter (BHSISC) which uses a combination between a switched inductor and a switched capacitor cell, similar to the BHSI converter in chapter 4 and the BHSC1 in chapter 2. The analysis of the BHSISC contains a steady state analysis, similar to the rest of the converters in this work, and then continues with a dynamic analysis. The dynamic analysis is used to achieve a more stable design of the passive components, and for designing the current controller required to control the power flow in the converter. An improved version of the BHSISC is additionally proposed, which might improve the operation of the converter.

5.2. Overview

The schematic of the BHSISC, proposed in [73], is presented in Fig. 5.1, and at the first glance it seems to operate very similar to the two converters from which this topology is created. The switched inductor cell is formed by the S_1-S_2-L_1-L_2 components, and the switched capacitor cell is formed by the S_3-S_4-C_1-C_2 components.

The converter requires one driving signal for S_3 and S_4, and the same signal inverted and applied to S_1 and S_2. Like the rest of the converters analyzed in this work, positive currents indicate step-up operation, while negative currents indicate step-down operation.

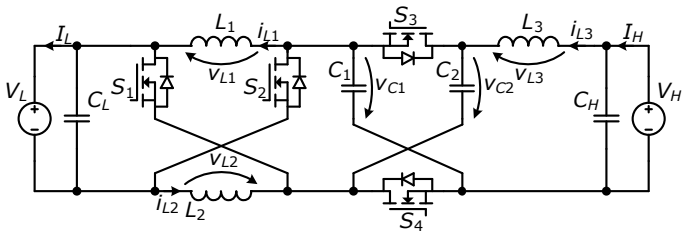

Fig. 5.1. The Bidirectional Hybrid Switched Inductor Switched Capacitor converter (BHSISC) [73] (i_{L1}, i_{L2} >0 ↔ step-down operation; i_{L1}, i_{L2} < 0 ↔ step-up operation)

5.3. Steady state analysis

The two equivalent switching schematics for the t_{on} and t_{off} intervals, presented in Fig. 5.2 and Fig. 5.3, respectively, are used for the steady state analysis of the BHSISC converter. The same initial assumptions made for the BHSI and BHSC1 converters are also considered for the BHSISC converter, therefore the two switched inductors are considered identical (L_1 = L_2) and their currents equal (i_{L1} = i_{L2}), and the two switched capacitors are considered identical (C_1 = C_2) and their voltages equal (v_{C1} = v_{C2}= v_{Csw}). Based on the two equivalent schematics, the main theoretical waveforms are represented in Fig. 5.4.

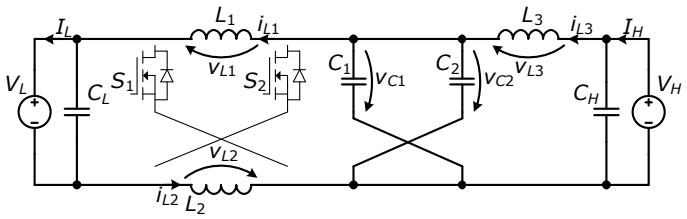

Fig. 5.2. Equivalent schematic of BHSISC during t_{on} interval (S_3 and S_4 are turned ON, S_1 and S_2 are turned OFF)

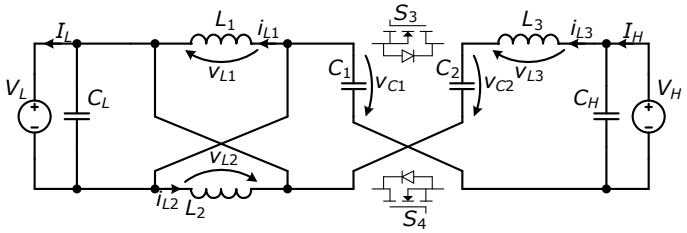

Fig. 5.3. Equivalent schematic of BHSISC during t_{off} interval (S_3 and S_4 are turned OFF, S_1 and S_2 are turned ON)

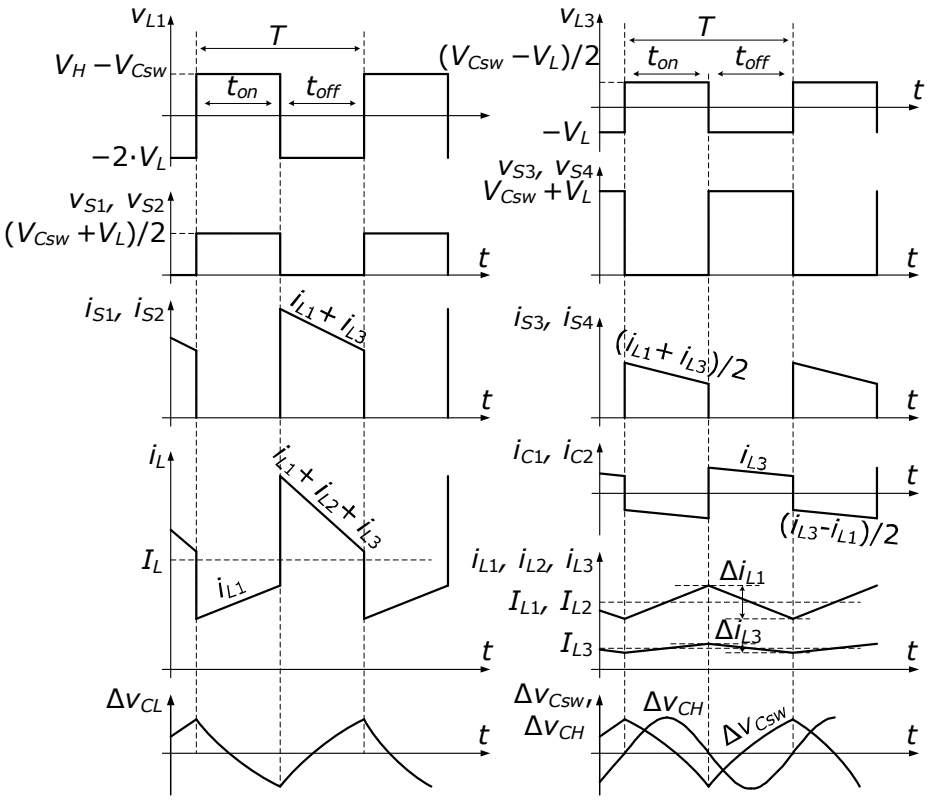

Fig. 5.4. Main theoretical waveforms of the BHSISC: L_1, L_2, L_3 inductor voltages and currents (v_{L1}, v_{L2}, v_{L3}, i_{L1}, i_{L2}, i_{L3}); S_1 - S_4 switches voltages and currents (v_{S1} - v_{S4}, i_{S1} - i_{S4}); C_1, C_2 switched capacitors currents (i_{C1}, i_{C2}); ripple voltages on the capacitors (Δv_{CH}, Δv_{CL}, Δv_{Csw})

During the t_{on} interval, the two switched capacitors are connected in parallel between the two inputs, through the two switched inductors to the low voltage input, V_L, and through L_3 inductor to the high voltage input, V_H.

During the t_{off} interval, the capacitors are connected in series to V_L and through L_3 to the high voltage side, V_H. The two switched inductors are connected in parallel to V_L.

The analysis of the BHSISC converter starts by considering D the duty cycle for the step-down mode of operation, and D' the duty cycle for step-up mode, similar to the analysis of the CBBB converter, from 1.3.1:

$$D = \frac{t_{on}}{T}, D' = \frac{t_{off}}{T}, \tag{5.1}$$

From the two equivalent switching schematics, Fig. 5.2 and Fig. 5.3, the inductor voltages are expressed as:

$$\begin{aligned} &t_{on}: v_{L1} + v_{L2} = V_{Csw} - V_L, \quad v_{L3} = V_H - V_{Csw}, \\ &t_{off}: v_{L1} = v_{L2} = -V_L, \qquad v_{L3} = V_H - 2 \cdot V_{Csw} - V_L. \end{aligned} \tag{5.2}$$

In addition to the simplifying assumptions from 1.3.1 (ideal components, constant voltage on capacitors, steady state operation) identical voltages, and identical currents are considered for the switching capacitors and switching inductors respectively, and by applying the volt-second balance:

$$\begin{aligned} &\langle v_{L1} \rangle = \langle v_{L2} \rangle = D \cdot \frac{V_{Csw} - V_L}{2} + (1 - D) \cdot (-V_L) = 0, \\ &\langle v_{L3} \rangle = D \cdot (V_H - V_{Csw}) + (1 - D) \cdot (V_H - 2 \cdot V_{Csw} - V_L) = 0, \end{aligned} \tag{5.3}$$

the voltage on the switched capacitors is calculated:

$$V_{Csw} = \frac{V_L \cdot (D-1) + V_H}{2 - D} = V_L \cdot \frac{(2 - D)}{D} = \frac{V_L + V_H}{2}. \tag{5.4}$$

From (5.4) and (5.1) the conversion ratio for step-down and step-up operations are:

$$V_L = V_H \cdot \frac{D}{4 - 3 \cdot D}, \tag{5.5}$$

$$V_H = V_L \cdot \frac{1 + 3 \cdot D'}{1 - D'}. \tag{5.6}$$

The BHSISC converter achieves a much better conversion ratio compared to the BHSI or BHSC1 converters, comparable to the quadratic structures, without using more switches compared to the quadratic topologies.

Relation (5.5) can be written in order to calculate the duty cycle as:

$$D = \frac{4 \cdot V_L}{V_H + 3 \cdot V_L}. \tag{5.7}$$

To calculate the passive components, the average inductor currents are calculated as:

$$I_{L1} = \frac{I_L \cdot (V_H + V_L)}{2 \cdot V_H}, \quad I_H = I_{L3}. \tag{5.8}$$

The inductor ripple current percentage, identical for all three inductors, is defined in the same way as in 1.3.1:

$$r_i = \frac{\Delta i_{L1}}{I_{L1}} = \frac{\Delta i_{L2}}{I_{L2}} = \frac{\Delta i_{L3}}{I_{L3}}. \tag{5.9}$$

From the voltage-current dependency of an ideal inductor the inductances for the three inductors are calculated:

$$L_1 = L_2 = \frac{v_{L1} \cdot \Delta t}{\Delta i_{L1}} = \frac{2 \cdot V_L \cdot V_H \cdot (V_H - V_L)}{r_i \cdot f \cdot I_L \cdot (V_H^2 + 4 \cdot V_L \cdot V_H + 3 \cdot V_L^2)}, \tag{5.10}$$

$$L_3 = \frac{v_{L3} \cdot \Delta t}{\Delta i_{L3}} = \frac{2 \cdot V_H \cdot (V_H - V_L)}{r_i \cdot f \cdot I_L \cdot (V_H + 3 \cdot V_L)}. \tag{5.11}$$

The energies for the three inductors are calculated with:

$$W_{L1} = W_{L2} = \frac{L_1 \cdot I_{L1}^2}{2} = \frac{I_L \cdot V_L \cdot (V_H^2 - V_L^2)}{4 \cdot \Delta i_{Lp} \cdot f \cdot V_H \cdot (V_H + 3 \cdot V_L)}, \tag{5.12}$$

$$W_{L3} = \frac{L_3 \cdot I_{L3}^2}{2} = \frac{I_L \cdot V_L^2 \cdot (V_H - V_L)}{r_i \cdot f \cdot V_H \cdot (V_H + 3 \cdot V_L)}. \tag{5.13}$$

The total inductor energy from the BHSISC is calculated with:

$$W_{LTot} = \sum W_{Li} = \sum \frac{L_i \cdot I_{Li}^2}{2} = 2 \cdot W_{L1} + W_{L3}, \tag{5.14}$$

and final result is:

$$W_{LTot} = \frac{I_L \cdot V_L \cdot (V_H - V_L)}{2 \cdot r_i \cdot f \cdot V_H}. \tag{5.15}$$

The inductor currents are defined as a time function, in order to calculate the capacitances:

$$i_{L1}(t) = i_{L2}(t) = \begin{cases} I_{L1} + \Delta i_{L1} \cdot (t / t_{on} - 1/2), & t \in [0, t_{on}) \\ I_{L1} + \Delta i_{L1} \cdot ((T - t) / t_{off} - 1/2), & t \in [t_{on}, T] \end{cases} \tag{5.16}$$

$$i_{L3}(t) = \begin{cases} I_{L3} + \Delta i_{L3} \cdot (t / t_{on} - 1/2), & t \in [0, t_{on}) \\ I_{L3} + \Delta i_{L3} \cdot ((T - t) / t_{off} - 1/2), & t \in [t_{on}, T] \end{cases} \tag{5.17}$$

Similar to the CBBB converter from 1.3.1, a voltage ripple percentage is considered:

$$r_v = \frac{\Delta v_{CH}}{V_{CH}} = \frac{\Delta v_{CL}}{V_{CL}} = \frac{\Delta v_{Csw}}{V_{Csw}}. \tag{5.18}$$

The currents from the capacitors are defined as the following time functions:

$$i_{CL} = \begin{cases} i_{L1} - I_L, & t \in [0, t_{on}) \\ 2 \cdot i_{L1} + i_{L3} - I_L, & t \in [t_{on}, T] \end{cases} \tag{5.19}$$

$$i_{CH} = I_H - i_{L3}, \tag{5.20}$$

$$i_{Csw} = \begin{cases} (i_{L3} - i_{L1}) / 2, & t \in [0, t_{on}) \\ i_{L3} & t \in [t_{on}, T] \end{cases} \tag{5.21}$$

Applying the voltage-current dependency of an ideal capacitor, the following are used to calculate the capacitances:

$$C_L = \frac{-1}{\Delta v_{CL}} \int_0^{t_{on}} (i_{L1} - I_L) dt, \tag{5.22}$$

$$C_H = \frac{1}{\Delta v_{CH}} \int_{t_{on}/2}^{t_{on}+t_{off}/2} (i_{L3} - I_H) dt, \tag{5.23}$$

$$C_1 = C_2 = C_{sw} = \frac{-1}{\Delta v_{Csw}} \int_0^{t_{on}} \frac{i_{L3} - i_{L1}}{2} dt, \tag{5.24}$$

The final values of the capacitances are calculated as:

$$C_L = \frac{2 \cdot I_L \cdot (V_H - V_L)}{r_v \cdot f \cdot V_H \cdot (V_H + 3 \cdot V_L)}, \tag{5.25}$$

$$C_H = \frac{r_i \cdot I_L \cdot V_L}{8 \cdot r_v \cdot f \cdot V_H^2}, \tag{5.26}$$

$$C_{sw} = \frac{2 \cdot I_L \cdot V_L \cdot (V_H - V_L)}{r_v \cdot f \cdot V_H \cdot (V_H^2 + 4 \cdot V_L \cdot V_H + 3 \cdot V_L^2)}. \tag{5.27}$$

The total capacitor energy is calculated with:

$$W_{CTot} = \sum W_{Ci} = \sum \frac{C_i \cdot V_{Ci}^2}{2} = W_{CL} + W_{CH} + 2 \cdot W_{Csw}, \tag{5.28}$$

and the energy for each capacitor is:

$$W_{CH} = \frac{r_i \cdot I_L \cdot V_L}{16 \cdot r_v \cdot f}, \tag{5.29}$$

$$W_{CL} = \frac{I_L \cdot V_L^2 \cdot (V_H - V_L)}{r_v \cdot f \cdot V_H \cdot (V_H + 3 \cdot V_L)}, \tag{5.30}$$

$$W_{Csw} = \frac{I_L \cdot V_L \cdot (V_H^2 - V_L^2)}{4 \cdot r_v \cdot f \cdot V_H \cdot (V_H + 3 \cdot V_L)}. \tag{5.31}$$

The total capacitor energy is calculated as:

$$W_{CTot} = \frac{I_L \cdot V_L \cdot (V_H \cdot (8 + r_i) - 8 \cdot V_L)}{16 \cdot r_v \cdot f \cdot V_H}. \tag{5.32}$$

Even if the BHSISC has a number of four capacitors, and three of them have a relatively large current ripple, the total capacitor energy is identical to that of the CBBB converter.

The total active switch stress for the four switches is equal to:

$$S = \sum_{j=1}^{4} V_{Sj} \cdot I_{Sj}, \tag{5.33}$$

and is calculated by using the switches voltage and current stresses:

$$V_{S1} = V_{S2} = V_{S3} / 2 = V_{S4} / 2 = \frac{V_{Csw} + V_L}{2} = \frac{V_H + 3 \cdot V_L}{4}, \tag{5.34}$$

$$I_{S1} / 2 = I_{S2} / 2 = I_{S3} = I_{S4} = \frac{I_{L1} + I_{L3}}{2} = \frac{I_L \cdot (V_H + 3 \cdot V_L)}{4 \cdot V_H}. \tag{5.35}$$

From the voltage and current stresses of the switches, the total active switch stress is calculated:

$$S = V_{S1} \cdot I_{S1} + V_{S2} \cdot I_{S2} + V_{S3} \cdot I_{S3} + V_{S4} \cdot I_{S4} = \frac{I_L \cdot (V_H + 3 \cdot V_L)^2}{2 \cdot V_H}. \tag{5.36}$$

Compared with the converters from section 1.3 and chapters 2-4, it can be concluded that the BHSISC converter has the lowest active switch stress, while also achieving a very wide conversion ratio.

5.4. Dynamic analysis

The dynamic modeling of the BHSISC is performed by applying the SSA method, in a similar way to the BHSC1 converter analysis from 2.4. The general form of the state equation is considered:

$$\dot{x} = A_i \cdot x + B_i \cdot u, \tag{5.37}$$

where i=1 and i=2 for the equations corresponding to t_{on} and t_{off} intervals, respectively.

The state vector, x, containing the state variables (the two different inductor currents and the capacitor voltages), and the input vector u containing the system inputs (voltages on the two sides):

$$x = \begin{bmatrix} i_{L1} \\ i_{L3} \\ v_{Csw} \\ v_{CL} \\ v_{CH} \end{bmatrix}, \quad u = \begin{bmatrix} V_L \\ V_H \end{bmatrix}, \tag{5.38}$$

The state (A_i) and input (B_i) matrices are expressed as follows:

$$A_i = \begin{bmatrix} a_{11_i} & a_{12_i} & a_{13_i} & 0 & a_{15_i} \\ a_{21_i} & a_{22_i} & a_{23_i} & a_{24_i} & a_{25_i} \\ a_{31_i} & a_{32_i} & 0 & 0 & 0 \\ 0 & a_{42_i} & 0 & a_{44_i} & 0 \\ a_{51_i} & a_{52_i} & 0 & 0 & a_{55_i} \end{bmatrix}, \quad B_i = \begin{bmatrix} 0 & b_{12_i} \\ b_{21_i} & b_{22_i} \\ 0 & 0 \\ b_{41_i} & 0 \\ 0 & b_{52_i} \end{bmatrix}. \tag{5.39}$$

The BHSISC converter with the parasitic resistances, required for an improved model, is shown in Fig. 5.5.

The two equivalent schematics for the t_{on} and t_{off} switching states, are presented in Fig. 5.6 and Fig. 5.7, respectively.

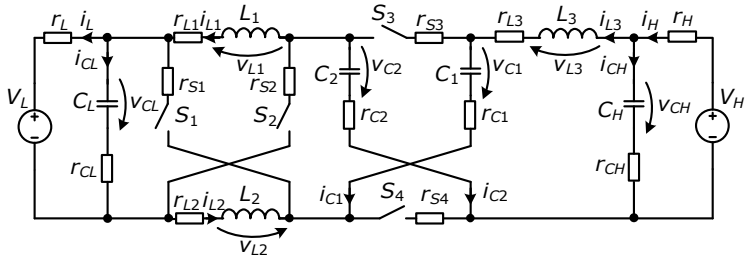

Fig. 5.5. BHSISC schematic used for the SSA analysis. The schematic includes the following parasitic components: r_{L1}, r_{L2}, r_{L3} – inductor ESRs; r_{CH}, r_{CL}, r_{C1}, r_{C2} – capacitor ESRs; r_{S1}-r_{S4} – switch on-state resitances; r_H, r_L – high and low voltage bus resistances. Component values are provided in Table 5.1

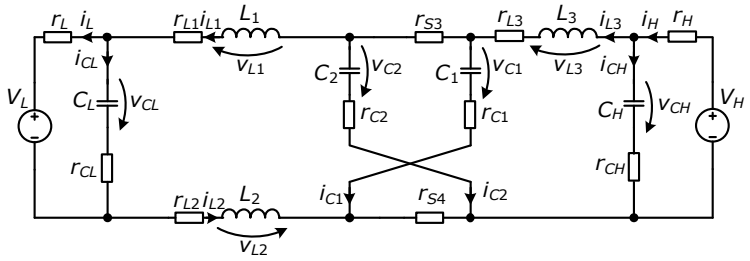

Fig. 5.6. BHSISC equivalent schematic during t_{on} interval used for SSA

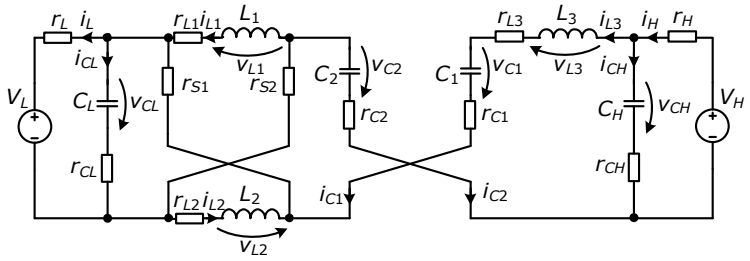

Fig. 5.7. BHSISC equivalent schematic during t_{off} interval used for SSA

From the equations (5.37), (5.38), (5.39) and the schematic from Fig. 5.6, the elements of the state matrix (A_1), for t_{on} switching interval, are expressed:

$$a_{11_1} = -\frac{\frac{r_{C1}}{4} + r_{L_1} + \frac{r_{S3}}{4} + \frac{r_{CL} \cdot r_L}{2 \cdot (r_{CL} + r_L)}}{L_1},\ a_{12_1} = \frac{r_{C1} - r_{S3}}{4 \cdot L_1}, \tag{5.40}$$

$$a_{13_1} = \frac{1}{2 \cdot L_1},\ a_{15_1} = -\frac{r_L}{2 \cdot L_1 \cdot (r_{CL} + r_L)}, \tag{5.41}$$

$$a_{21_1} = \frac{r_{C1} - r_{S3}}{2 \cdot L_3},\ a_{22_1} = \frac{\frac{r_{C1}}{2} + r_{L3} + \frac{r_{S3}}{2} + \frac{r_{CH} \cdot r_H}{r_{CH} + r_H}}{L_3}, \tag{5.42}$$

$$a_{23_1} = -\frac{1}{L_3},\ a_{24_1} = \frac{r_H}{L_3 \cdot (r_{CH} + r_H)},\ a_{25_1} = 0, \tag{5.43}$$

$$a_{31_1} = -\frac{1}{2 \cdot C_1},\quad a_{32_1} = \frac{1}{2 \cdot C_1}, \tag{5.44}$$

$$a_{42_1} = -\frac{r_H}{C_H \cdot (r_{CH} + r_H)},\ a_{44_1} = -\frac{1}{C_H \cdot (r_{CH} + r_H)}, \tag{5.45}$$

$$a_{51_1} = \frac{r_L}{C_L \cdot (r_{CL} + r_L)},\quad a_{52_1} = 0,\quad a_{55_1} = -\frac{1}{C_L \cdot (r_{CL} + r_L)}, \tag{5.46}$$

With the same considerations, the elements of the input matrix (B_1), are:

$$b_{12_1} = -\frac{r_{CL}}{2 \cdot L_1 \cdot (r_{CL} + r_L)},\ b_{21_1} = \frac{r_{CH}}{L_3 \cdot (r_{CH} + r_H)}, \tag{5.47}$$

$$b_{41_1} = \frac{1}{C_H \cdot (r_{CH} + r_H)},\quad b_{52_1} = \frac{1}{C_L \cdot (r_{CL} + r_L)}, \tag{5.48}$$

From the equations (5.37), (5.38), (5.39) and the schematic from Fig. 5.7, the elements of the state matrix (A_2), for t_{off} switching interval, are expressed as:

$$a_{11_2} = -\frac{r_{L1} + r_{S1} + \frac{2 \cdot r_{CL} \cdot r_L}{r_{CL} + r_L}}{L_1},\ a_{12_2} = -\frac{r_{S1} + \frac{r_{CL} \cdot r_L}{r_{CL} + r_L}}{L_1}, \tag{5.49}$$

$$a_{13_2} = 0,\ a_{15_2} = -\frac{r_L}{L_1 \cdot (r_{CL} + r_L)}, \tag{5.50}$$

$$a_{21_2} = -\frac{2 \cdot r_{S1} + \frac{2 \cdot r_{CL} \cdot r_L}{r_{CL} + r_L}}{L_3},\ a_{22_2} = \frac{2 \cdot r_{C1} + r_{L3} + 2 \cdot r_{S1} + \frac{r_{CH} \cdot r_H}{r_{CH} + r_H} + \frac{r_{CL} \cdot r_L}{r_{CL} + r_L}}{L_3}, \tag{5.51}$$

$$a_{23_2} = -\frac{2}{L_3},\quad a_{24_2} = \frac{r_H}{L_3 \cdot (r_{CH} + r_H)},\quad a_{25_2} = -\frac{r_L}{L_3 \cdot (r_{CL} + r_L)}, \tag{5.52}$$

$$a_{31_2} = 0,\quad a_{32_2} = \frac{1}{C_1}, \tag{5.53}$$

$$a_{42_2} = -\frac{r_H}{C_H \cdot (r_{CH} + r_H)},\quad a_{44_2} = -\frac{1}{C_H \cdot (r_{CH} + r_H)}, \tag{5.54}$$

$$a_{51_2} = \frac{2 \cdot r_L}{C_L \cdot (r_{CL} + r_L)},\quad a_{52_2} = \frac{r_L}{C_L \cdot (r_{CL} + r_L)},\quad a_{55_2} = -\frac{1}{C_L \cdot (r_{CL} + r_L)}, \tag{5.55}$$

The elements of the input matrix (B_2), are:

$$b_{12_2} = -\frac{r_{CL}}{L_1 \cdot (r_{CL} + r_L)},\ b_{21_2} = \frac{r_{CH}}{L_3 \cdot (r_{CH} + r_H)},\ b_{22_2} = -\frac{r_{CL}}{L_3 \cdot (r_{CL} + r_L)}, \tag{5.56}$$

$$b_{41_2} = \frac{1}{C_H \cdot (r_{CH} + r_H)}, b_{52_2} = \frac{1}{C_L \cdot (r_{CL} + r_L)}, \tag{5.57}$$

The system from (5.37) is averaged by using a dynamic duty cycle, d, and the following continuous and nonlinear system is written:

$$\dot{x} = (d \cdot A_1 + (1-d) \cdot A_2) \cdot x + (d \cdot B_1 + (1-d) \cdot B_2) \cdot u, \tag{5.58}$$

The system is linearized by introducing small signal variations around a steady state point, for the state variables, x, duty cycle, d, and outputs, y:

$$x = X + \tilde{x}, \quad d = D + \tilde{d}, \quad y = Y + \tilde{y}. \tag{5.59}$$

The linearized system is expressed as:

$$\begin{cases} \dot{\tilde{x}} = A_e \cdot \tilde{x} + B_e \cdot \tilde{d} \\ \tilde{y} = C_e \cdot \tilde{x} \end{cases}, \tag{5.60}$$

with the equivalent state (A_e) and input (B_e) matrices:

$$A_e = (A_1 \cdot D + A_2 \cdot (1-D)), \tag{5.61}$$

$$B_e = ((A_1 - A_2) \cdot X + (B_1 - B_2) \cdot u). \tag{5.62}$$

The output matrices, C_{e1} and C_{e2}, defined to output the i_{L1} or the i_{L3} current, are:

$$C_{e1} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \end{bmatrix}, C_{e2} = \begin{bmatrix} 0 & 1 & 0 & 0 & 0 \end{bmatrix}, \tag{5.63}$$

and the respective transfer functions are:

$$G_{P1}(s) = \frac{\tilde{y}}{\tilde{d}} = \frac{\tilde{i}_{L1}}{\tilde{d}}, \tag{5.64}$$

$$G_{P2}(s) = \frac{\tilde{y}}{\tilde{d}} = \frac{\tilde{i}_{L3}}{\tilde{d}}, \tag{5.65}$$

The two transfer functions are calculated using:

$$\tilde{y} = C_e \cdot (s \cdot I - A_e)^{-1} \cdot B_e \cdot \tilde{d}. \tag{5.66}$$

The passive components were sized according to 5.3, and values of the components are summarized in Table 5.1, with initial design values in parentheses. As the stability of the converter can be affected because of the low values of ESRs of capacitors (1-3 mΩ), as it is discussed in [64], the values of the poles and zeros of the system were evaluated and presented in Table 5.2. A new set of electrolytic capacitors were chosen, with higher ESR, in order to improve the stability of the design, and the new poles and zeros are shown in Table 5.3. The final capacitors were chosen in order to withstand the maximum RSM current.

Table 5.1. BHSISC parameters for the dynamic analysis (initial values in parentheses)

Element	Value	Unit	Description
V_H	400	V	Nominal voltage at the high voltage side
V_L	50	V	Nominal voltage at the low voltage side
C_H	680 (0.39)	μF	Capacitance of the high voltage side capacitor
C_L	47.6 (0.159)	mF	Capacitance of the low voltage side capacitor
C_1, C_2	4.8 (0.017)	mF	Capacitance of the switched capacitors
r_v	2	%	Capacitance voltage ripple percentage
L_1, L_2	47	μH	Inductance of the low voltage side inductor
L_3	470	μH	Inductance of the high voltage side inductor
r_i	20	%	Inductor current ripple percentage
r_{S1}, r_{S2}	15	mΩ	On-state resistance of the S_1, S_2 switches
r_{S3}, r_{S4}	50	mΩ	On-state resistance of the S_3, S_4 switches
r_H	160	mΩ	Parasitic resistance of the supply line at V_H
r_L	2.1	mΩ	Parasitic resistance of the supply line at V_L
r_{CH}	160 (3)	mΩ	Equivalent series resistance of C_H
r_{CL}	2.1 (1)	mΩ	Equivalent series resistance of C_L
r_{C1}	23.8 (1)	mΩ	Equivalent series resistance of C_1
r_{L1}, r_{L2}	4	mΩ	Low voltage side inductor resistance
r_{L3}	53	mΩ	High voltage side inductor resistance
T	12.5	μs	Switching period
D	0.372	-	Duty cycle of the steady state operation point
I_{L1}	40	A	Steady state value of the L_1 inductor current

Table 5.2. Poles and zeros of the process with initial values

Transfer function	Poles	Zeros
$G_{P1}(s)$	-427350424.158; -3144639.569; -479.867; -59.595 ± 14213.481i	-427350424.158; -3145225.33; **1118.105 ± 13945.656i**
$G_{P2}(s)$	-427350424.158; -3144639.569; -479.867; -59.595 ± 14213.481i	-427350427.35; -3144866.448; -5210.839 + 14239.223i

Table 5.3. Poles and zeros of the process with final values

Transfer function	Poles	Zeros
$G_{P1}(s)$	-4867.665; -4404.637; -635.816; -235.456 ± 834.977i	-4904.408; -4410.393; -270.533 ± 820.508i
$G_{P2}(s)$	-4867.665; -4404.637; -635.816; -235.456 ± 834.977i	-4883.926; -4595.588; -123.419 + 909.120i

As shown in Table 5.2, if low ESR capacitors are used (values in parentheses from Table 5.1), a RHPZ appears for the $G_{P1}(s)$ transfer function. If higher ESR capacitors are used, the RHPZ is eliminated from the transfer function as shown in Table 5.3. This aspect was also demonstrated for a different topology in [64].

The transfer functions, calculated with (5.64) and (5.65), for the final design values from Table 5.1, are:

$$G_{P1}(s) = \frac{2.91 \cdot 10^6 \cdot s^4 + 2.88 \cdot 10^{10} \cdot s^3 + 8.01 \cdot 10^{13} \cdot s^2 + 5.45 \cdot 10^{16} \cdot s + 4.71 \cdot 10^{19}}{s^5 + 1.04 \cdot 10^4 \cdot s^4 + 3.27 \cdot 10^7 \cdot s^3 + 3.39 \cdot 10^{10} \cdot s^2 + 2.69 \cdot 10^{13} \cdot s + 1.03 \cdot 10^{16}}, \quad (5.67)$$

$$G_{P2}(s)=\frac{5.86\cdot10^{5}\cdot s^{4}+5.7\cdot10^{9}\cdot s^{3}+1.5\cdot10^{13}\cdot s^{2}+7.92\cdot10^{15}\cdot s+1.11\cdot10^{19}}{s^{5}+1.04\cdot10^{4}\cdot s^{4}+3.27\cdot10^{7}\cdot s^{3}+3.39\cdot10^{10}\cdot s^{2}+2.69\cdot10^{13}\cdot s+1.03\cdot10^{16}}, \tag{5.68}$$

A current control method is desired similar to the BHSI, BHSC1 and BHSC2 converters, therefore the i_{L1} current is chosen as control variable, as it is larger than i_{L3}. The bode plots of the two transfer functions, G_{P1}(s) and G_{P2}(s), are shown in Fig. 5.8, together with the Bode plots obtained by simulating the switching model of the BHSISC converter, and a good resemblance is found between them.

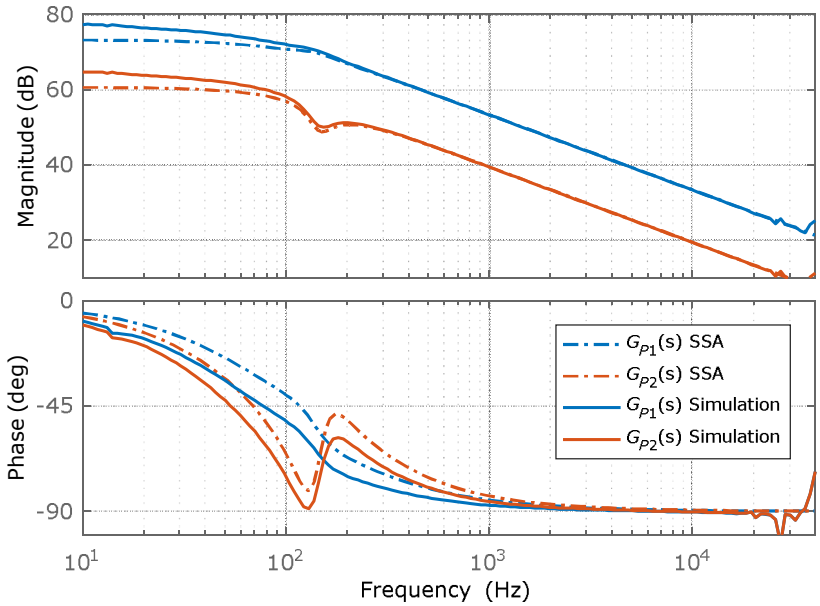

Fig. 5.8. Open loop Bode plots of the BHSISC dynamic model: continuous time model of G_{P1}(s) and G_{P2}(s), obtained by SSA method or from the simulation of the converter switching model realized in PSIM software

5.5. Controller design

Based on the Bode plots obtained by SSA modeling, a controller was designed for the BHSISC converter. The requirements for the controller were: fast response, zero steady state error, reduced overshoot(≤2%) which is achievable with a phase margin (*PM*) of approximately 80°, a gain margin (*GM*) greater or close to 10dB, and a cutoff frequency (f_c) lesser than 25% of the switching frequency.

The controller was designed by directly shaping the Bode plot of the open loop system. The design was performed by using the controlSystemDesigner application from MATLAB software. In order to eliminate steady state error, a pole was added in the origin, and an additional zero was added while adjusting the gain of the controller. The resulting transfer function of the controller is:

$$G_C(s)=\frac{0.042814\cdot(s+1.478\cdot10^{4})}{s}. \tag{5.69}$$

The Bode plot of the open loop system, $G_C(s) \cdot G_{P1}(s)$, from Fig. 5.9, confirms the performance of the system, achieving a phase margin of 83.5° at the cutoff frequency of 20kHz. The Bode plot of the controller is shown in Fig. 5.10.

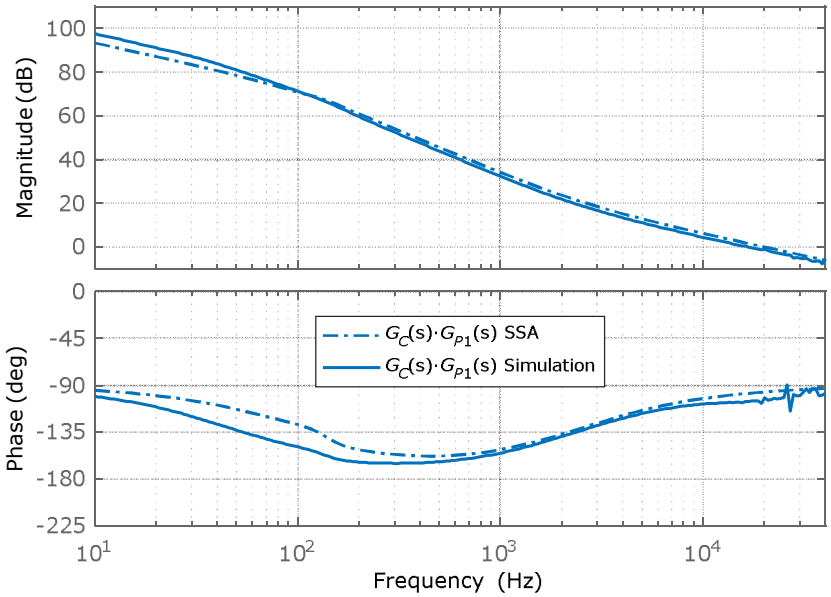

Fig. 5.9. Open loop Bode plots of the BHSISC model controlled by $G_C(s)$: response of the SSA model, $G_C(s) \cdot G_{P1}(s)$; the Model Simulation with analog controller and switching model of the BHSISC⇒ PM=83.5°, f_c=20kHz

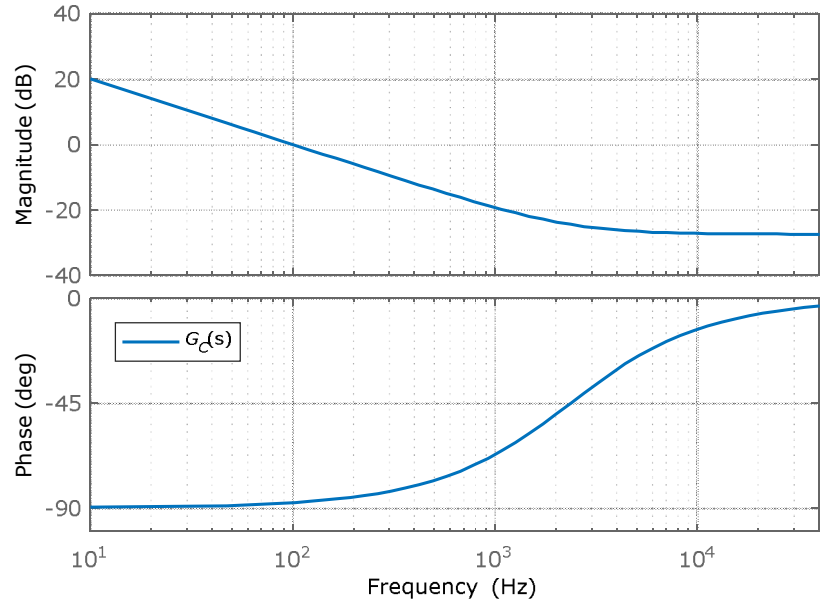

Fig. 5.10. Bode plots of the $G_C(s)$ controller designed for the BHSISC converter

5.6. Simulation results

Steady state and transient simulation results are presented for the BHSISC converter in Fig. 5.11 and Fig. 5.12, respectively. The simulation results for steady state operation in Fig. 5.11 are in good correspondence to the theoretical waveforms from Fig. 5.4.

The results for the transient operation of the BHSISC, controlled by $G_C(s)$, are presented in Fig. 5.12. The converter operates in both step-up and step-down modes, having a fast transition between the two modes, with reduced oscillations on the i_{L3} inductor current which is not directly controlled. In contrast to the BHSC1, the BHSISC is designed by taking the dynamic results from section 5.4 into account. Because of this the controller does not require an LPF on the reference, and the resulting oscillations are insignificant.

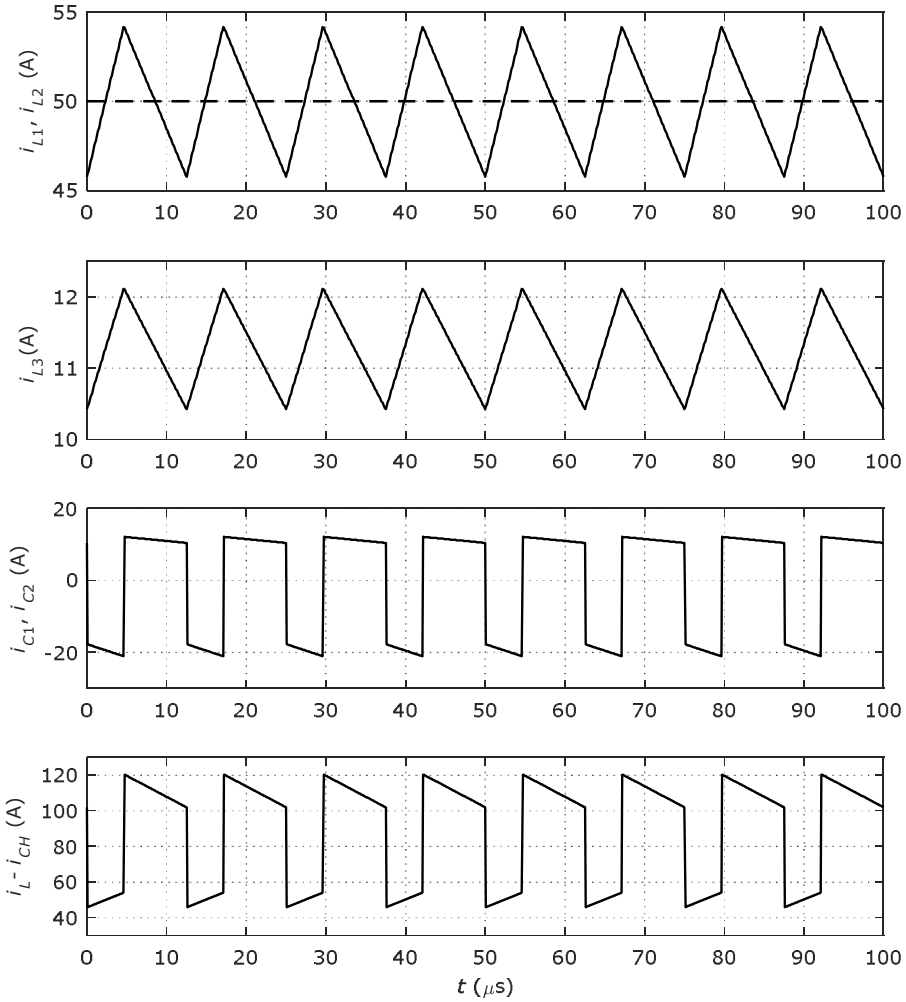

Fig. 5.11. Simulation waveforms for steady state operation of the BHSISC: i_{L1}=50A, V_L=50V, V_H=400V, P_{in}=2.5kW, (i_{L1}, i_{L2}, i_{L3} are the currents from L_1, L_2 and L_3 inductors, respectively, i_{C1}, i_{C2} are the currents on the switched capacitors, respectively, i_L - i_{CH} is the output current with the capacitor ripple)

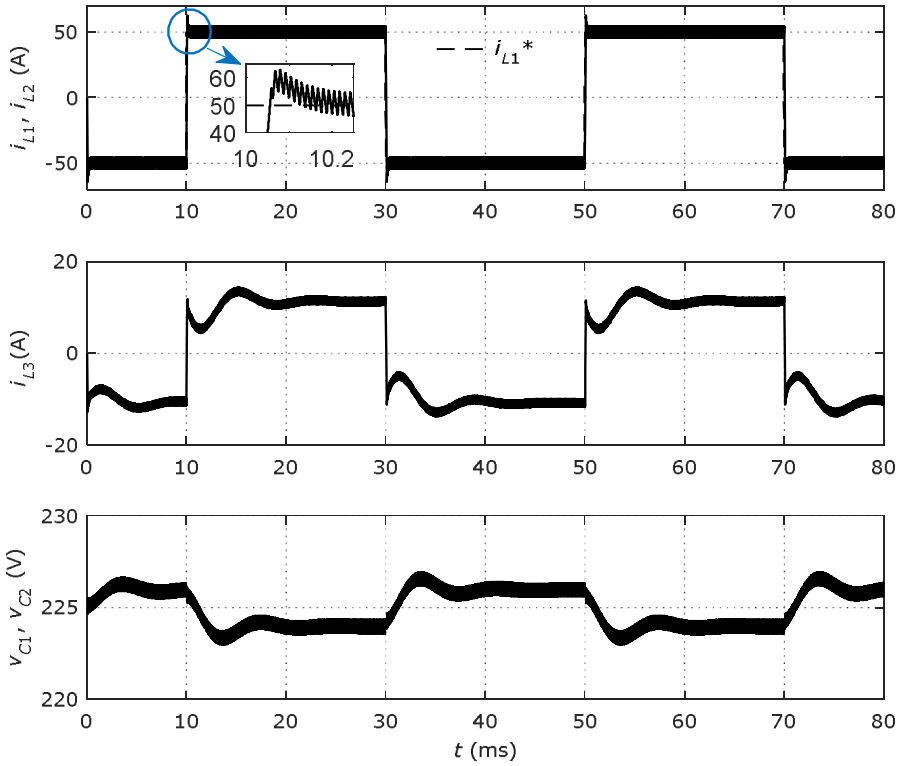

Fig. 5.12. Simulation waveforms for transient operation of the BHSISC, controlled by the G_C(s) controller: i_{L1} =±50A, V_L=50V, V_H=400V, P_{in}=±2.5kW, (i_{L1}, i_{L2}, i_{L3} are the currents from L_1, L_2 and L_3 inductors, respectively, v_{C1}, v_{C2} are the voltages on the switched capacitors)

5.7. Topology improvements

As the BHSISC converter is inspired by the BHSI and BHSC1 converter, it is expected to apply the same concepts in order to improve their schematic. Therefore, the tendency might be to cascade the two converters, as shown in Fig. 5.13. The cascaded schematic has more switches and inductors, and the conversion ratio will be the product between the conversion ratio of the two, and this appears to be far from the actual BHSISC converter. Nevertheless, this topology might achieve good performances.

A different way of applying the principles for improving the BHSI and BHSC1 converter into achieving an improved BHSISC (I-BHSISC), is presented in Fig. 5.14. The topology uses inductors on both terminals of the V_H supply which can be or uncoupled for simplicity and availability or coupled in order to reduce the size of the overall inductor. The purpose of the split inductors is to eliminate the high frequency voltage that appears in the standard BHSISC, between the two voltage inputs. The switched inductors are also coupled, with the intent of eliminating any possible inductor voltage oscillations, as it happens with the BHSI, Fig. 4.38.

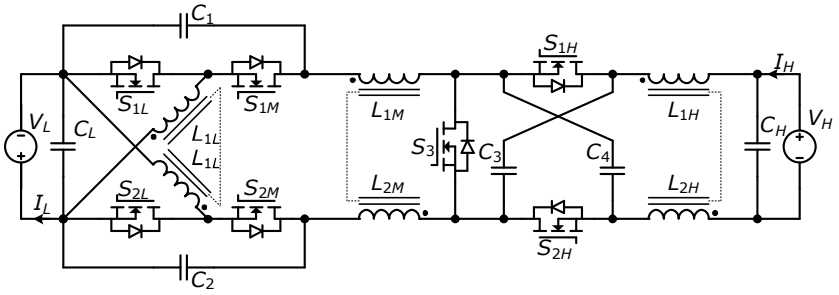

Fig. 5.13. Cascaded I-BHSI and I-BHSC1 converters

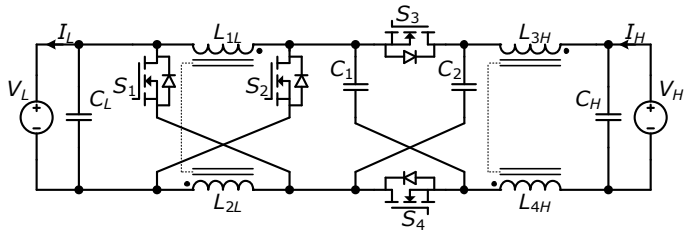

Fig. 5.14. The Improved Bidirectional Hybrid Switched Inductor Switched Capacitor converter (I-BHSISC)

5.8. Conclusions

The BHSISC converter was analytically examined in steady state operation, and in addition, a dynamic model was also realized. Comparing this topology to other converters, from the perspective of the metrics obtained by steady state analysis, a good performance is observed. The dynamic modelling was used in order to make a stable design for this converter, and also to design a current controller required to control the power flow. Even if only one inductor current is controlled, no significant oscillations appear in the other inductors. Simulation results are used to confirm the dynamic model and to present the operation of the BHSISC converter in steady state and transient operations.

An improved version of the BHSISC converter is also proposed, which should further improve the characteristics of this topology.

6. TOPOLOGIES COMPARISON

6.1. Abstract

As the literature presents many converter topologies under the same category of bidirectional non-isolated converters, different means to compare the topologies are needed. This chapter presents a comparison between the different hybrid topologies presented in chapters 2 to 5, and other topologies proposed in literature, described in sections 1.3.1 to 1.3.9. The topologies are compared in terms of step-up and step-down conversion ratios, total inductor energy, total capacitor energy and total active switch stress. The conversion ratios provide an overall information about the performance of the converter, as it shows the operation range for the two inputs. The total inductor energy and total capacitor energy gives information about the size and costs of these passive components. The total active switch stress provides information about the cost or the losses in the active switches.

6.2. Topologies overview

The characteristics of the different topologies presented in this work, are summarized in Table 6.1. Characteristics, such as step-down and step-up conversion ratios, the number of the active switches (transistors and diodes), and references to the total inductor or capacitor energy required by each converter or the active switch stress, that can be found in the chapters of this work. The following sections of this chapter present a comparison between the main characteristics of each converter.

Table 6.1. Converter comparison table

Conv. No.	Ref.	Chap.	Step-down ratio	Step-up ratio	Switch count Tr./D.	Ind. Energy	Cap. Energy	Stress
0. CBBB		1.3.1	D	$1/(1-D')$	2/2	(1.14)	(1.28)	(1.32)
1. BHSISC	[73]	5	$\frac{D}{4-3\cdot D}$	$\frac{1+3\cdot D'}{1-D'}$	4/4	(5.15)	(5.32)	(5.36)
2. BHSI	[81]	4	$\frac{D}{2-D}$	$\frac{1+D'}{1-D'}$	3/3	(4.12)	(4.24)	(4.28)
3. BHSC1	[67]	2	idem 2	idem 2	3/3	(2.15)	(2.32)	(2.36)
4. BHSC2	[71]	3	idem 2	idem 2	5/5	(3.15)	(3.32)	(3.36)
5. BSQZ	[53]	1.3.2	idem 2	idem 2	3/3	Table 1.3		
6.CBQ	[54]	1.3.3	D^2	$\frac{1}{(1-D')^2}$	4/4	Table 1.4		
7. BQ1	[55]	1.3.4	idem 6	idem 6	4/4	Table 1.5		
8. BQ2	[56]	1.3.5	idem 6	idem 6	4/4	Table 1.6		
9. BQ3	[57]	1.3.6	idem 6	idem 6	3/5	Table 1.7		
10. BTMM	[58]	1.3.7	$\frac{D^2}{D^2-D+1}$	$\frac{D'^2-D'+1}{(1-D')^2}$	6/6	Table 1.8		
11. BSC1	[59]	1.3.8	$D/2$	$2/(1-D')$	4/4	Table 1.9		
12. BSC2	[60]	1.3.9	$\frac{D}{1+D}$	$\frac{2-D'}{1-D'}$	3/3	Table 1.10		

6.3. Conversion ratio comparisons

The conversion ratios represent the ratio between the low voltage (V_L) and the high voltage (V_H), or vice versa, in steady state operation and in continuous conduction mode, and is calculated with respect to the duty ratio. As described in 1.3.1, the step-down duty ratio is D and the step-up duty ratio is D', as they are proportional to their respective conversion ratio.

The conversion ratios from Table 6.1, for each converter, are presented in the step-down and step-up forms, in Fig. 6.1 and Fig. 6.2, respectively. A graphical representation is more advantageous since it conveys the information in a more easily understandable manner. The step-up and step-down modes are identical in terms of converter operation, it differs only in the mathematical form in which is written.

In step-down operation (V_L / V_H), the topologies are evaluated starting from the lowest conversion ratio achieved by the lowest duty cycle. Therefore, the quadratic converters, CBQ, BQ1, BQ2 and BQ3, and the BTMM achieve the lowest conversion ratio for a duty cycle lower than 30%.

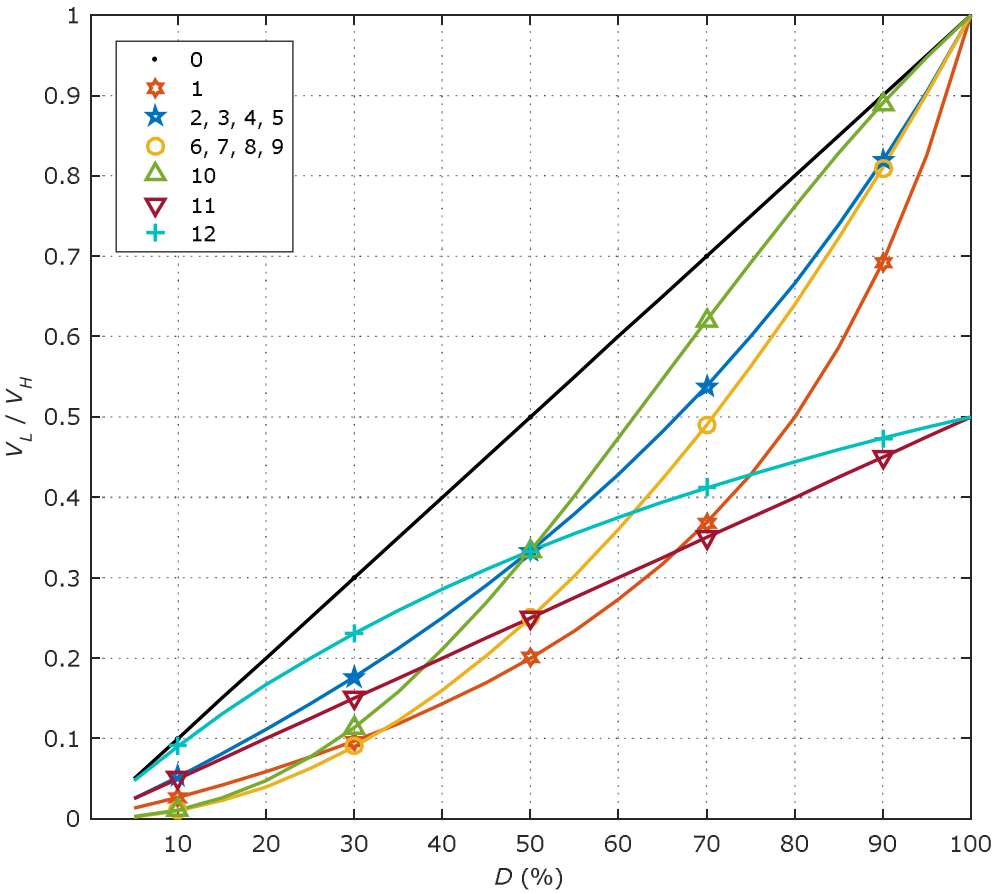

Fig. 6.1. Step-down conversion ratio comparison between previousely presented topologies: 0. CBBB 1. BHSISC, 2. BHSI, 3. BHSC1, 4. BHSC2, 5. BSQZ, 6. CBQ, 7. BQ1, 8. BQ2, 9. BQ3, 10. BTMM, 11. BSC1, 12. BSC2. Details of the converters are highlighted in Table 6.1

The BTMM has a fast ascend to a higher conversion ratio, therefore if low conversion ratios are desired, it should be kept at a more lower duty cycle.

These converters are closely followed by the BHSISC converter, which manages to achieve a lower conversion ratio, until 70% duty cycle.

Following the BHSISC, are the rest of the hybrid converters, BHSI, BHSC1, BHSC2, and the BSQZ converter. They achieve a conversion ratio which is situated between the quadratic converters, and the CBBB converter, and for higher conversion ratios it is approaching the quadratic converters.

The BSC1 converter starts from the same conversion ratio as the hybrid converters, and it has a linear ascension up to the maximum 50%. This limitation must be taken into account if this topology is used.

The next topology is the BSC2 converter, which starts from the same point as the CBBB converter, but it is also limited at 50% maximum conversion ratio, having a very slow increase.

The last topology from the plot, is the conventional converter, the CBBB, used as a reference for the rest of the converters.

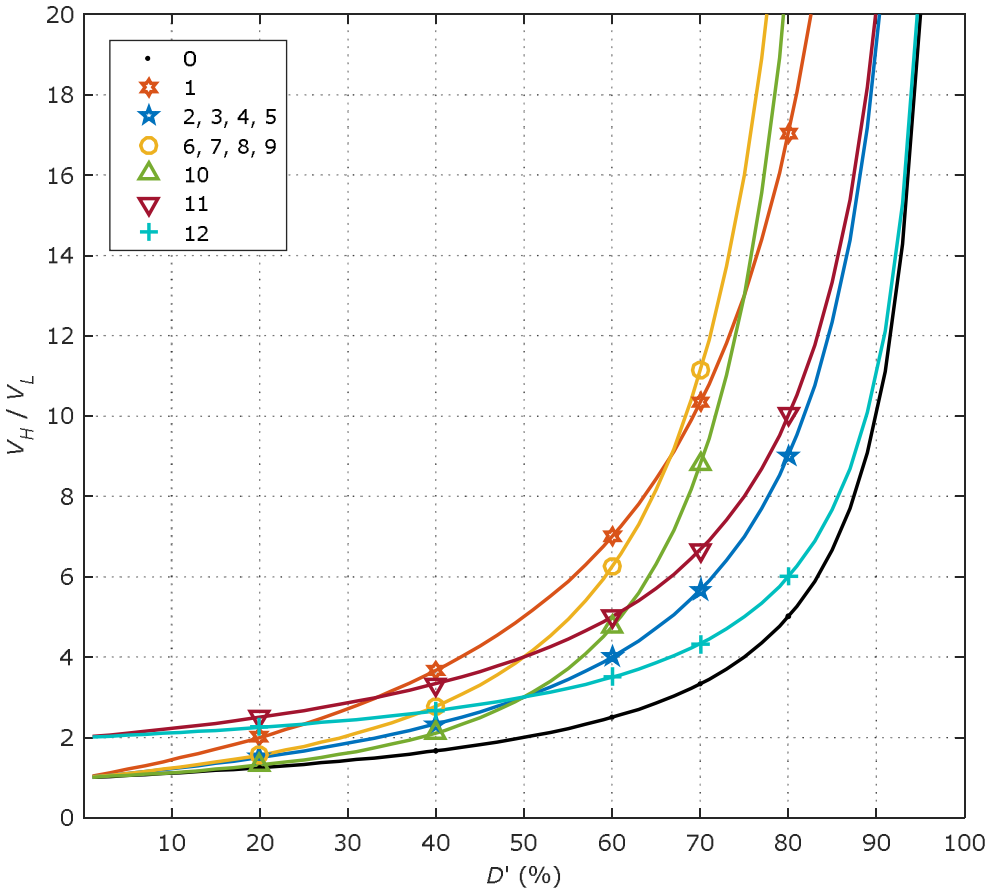

Fig. 6.2. Step-up conversion ratio comparison between previously presented topologies: 0. CBBB 1. BHSISC, 2. BHSI, 3. BHSC1, 4. BHSC2, 5. BSQZ, 6. CBQ, 7. BQ1, 8. BQ2, 9. BQ3, 10. BTMM, 11. BSC1, 12. BSC2. Details of the converters are highlighted in Table 6.1

For the step-up conversion ratio (V_H / V_L), the converters are analyzed starting from the one that achieves the highest conversion ratio with the lowest duty cycle, *D'*. The quadratic converters, CBQ, BQ1, BQ2 and BQ3, achieve the highest conversion ratios, achieving a static gain of 20 with a duty cycle slightly lower than 80%. In proximity is the BTMM converter which achieves almost the same performances. A slightly lower performance is achieved by the BHSISC, and it does not have such a steep decrease.

The next converters to achieve the static gain of 20 at around 90% duty cycle, are the BSC1 converter, the rest of the hybrid converters (the BHSI, BHSC1 and BHSC2), and the BSQZ converter. The BSC1 converter is limited in this case to a gain of minimum 2, therefore the two input voltages cannot be equal.

Lastly, the BSC2 converter, also limited to a minimum gain of 2, and the CBBB converters, achieve a static gain of 20 at almost 95% duty cycle.

6.4. Inductor energy comparisons

The total inductor energy equations for each of the converters previously presented in this work are referenced in Table 6.1. The total inductor energy for each converter is normalized to the energy of the CBBB converter. Therefore, the equation for the energy of each converter is divided by the equation of the energy for the CBBB converter, and then calculated for various step-down conversion ratios, between 5% to 25%. The step-down and step-up conversion ratios are equivalent, but the step-down is more easily comprehendable, therefore it is used in the graphs. The conversion ratio is only presented up to 25% (in step-down operation) as a lower range is generaly of most interest for wide voltage conversion ratio converters. Appart for the conversion ratio, no other values are needed for the calculation, as the terms simplify through the normalization. As a reference, at V_H=400V, a variation of 5-25% will result in a variation for V_L between 20V to 100V, which is optimum for microgrid applications with supercapacitor storage, applications which are described in the next chapter.

The calculated results are presented in Fig. 6.3. As shown here, the converters BSC1, and BSC2 require a lower inductor energy, compared to the CBBB, as their line is always lower than unity. The required energy does increase close to 1 at lower voltage conversion ratios. As shown in 1.3.8 and 1.3.9, these converters operate by connecting in parallel capacitors with different voltages which introduce unwanted effects in their operation, such as large current spikes. These spikes are not accounted in the total active switch stress comparison and can result in a decreased life of the converter.

Placed on the unity line, the four hybrid converters, BHSISC, BHSI, BHSC1 and BHSC2, show that they require the same inductor energy as the CBBB converter, which is unexpected given the fact that the hybrid converters are capable of a much wider conversion ratio, and, as it is shown in the next section, lower switch stress.

The next converter, with aproximately 40% larger requirement for inductors energy compared to the CBBB, is the BSQZ converter. Close to the BSQZ are the quadratic converters, the CBQ, BQ1, BQ2 and BQ3, which require up to 60% more inductor energy, at lower conversion ratios. Finally, the BTMM converter requires the largest inductor energy, up to 80% more than the CBBB converter.

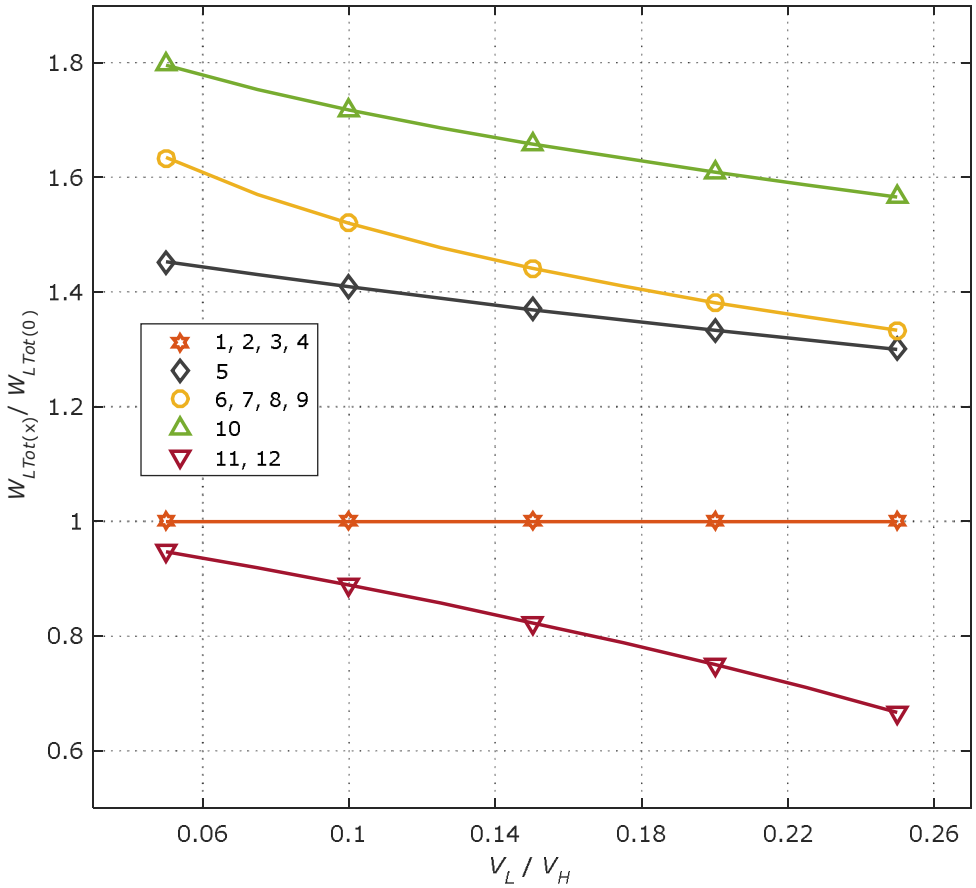

Fig. 6.3. Total inductor energy comparison between previousely presented topologies: x = 1. BHSISC, 2. BHSI, 3. BHSC1, 4. BHSC2, 5. BSQZ, 6. CBQ, 7. BQ1, 8. BQ2, 9. BQ3, 10. BTMM, 11. BSC1, 12. BSC2, normalized to 0. CBBB.
Details of the converters are highlighted in Table 6.1

6.5. Capacitor energy comparisons

The total capacitor energy is normalized for each of the converters from Table 6.1 to the CBBB converter, similarly to the normalization of the inductor energy. The results are presented in Fig. 6.4.

The lowest capacitor energy is for the BSC2 converter, but as previously mentioned, this converter operates by connecting in parallel capacitors with different voltages which introduces unwanted effects in the operation of the converter.

Close to the CBBB converter, are the hybrid topologies, from lowest to highest: the BHSI, the BHSISC, the BHSC1 and BHSC2 converters. The slight difference from the topologies, comes from the r_i factor, which is not reduced from the total capacitor energy and is considered equal to 20% for this comparison. Even if the BHSI and BHSISC converters have apparently larger capacitor current ripples, overall, the required capacitance energy is not increased, resulting the same, or almost the same required energy as the CBBB.

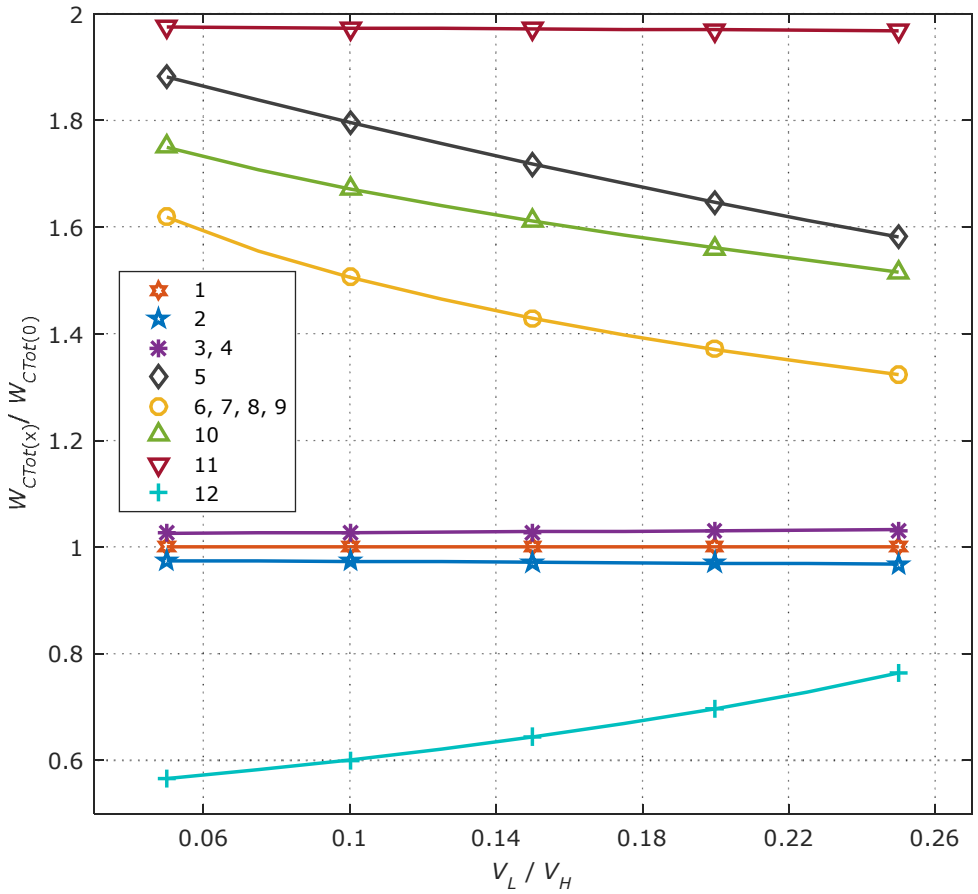

Fig. 6.4. Total capacitor energy comparison between previousely presented topologies: x = 1. BHSISC, 2. BHSI, 3. BHSC1, 4. BHSC2, 5. BSQZ, 6. CBQ, 7. BQ1, 8. BQ2, 9. BQ3, 10. BTMM, 11. BSC1, 12. BSC2, normalized to 0. CBBB.
Details of the converters are highlighted in Table 6.1

The rest of the converters require larger capacitor energies than the CBBB converter, first being the quadratic converters, CBQ, BQ1, BQ2 and BQ3, requiring up to 60% more capacitor energy than the CBBB or the hybrid converters.

The quadratic converters are followed by the BTMM converter, the BSQZ and finally the BSC1 converter, with almost 200% the required energy of the CBBB converter.

Even if capacitors may not be sized according to the relations provided in their correspoding section because of low ESR which can produce instability in operation, the relations are still relevant for the comparison.

6.6. Total active switch stress comparisons

The total active switch stress for each of the converters from Table 6.1 is normalized in a similar fashion to the total active switch stress of the CBBB converter. As presented in Fig. 6.5, the lowest stress, for the 5-25% conversion ratio, is achieved

by the BHSISC. Even if this topology has four switches, the stress, on lower conversion ratio, can be as low as 30% of the CBBB stress. For low conversion ratio values, the three quadratic converters, CBQ, BQ1 and BQ2, are approaching 40%, but increase quickly on larger conversion ratio. The hybrid converters, BHSI, BHSC1, and converters BSQZ and BSC1 are also close to the BHSISC, but do not achieve the same low stress at low conversion ratios. Following a similar path, the BTMM converter is slightly worse than the quadratic converters, and for conversion ratios greater than approximately 18% it has a stress higher than the CBBB converter. The BSC2 converter seems to decrease its relative stress, when increasing the conversion ratio, contrary to the rest of the topologies, and at higher ratios is close to the BHSISC, BSC1, BHSI, BHSC1 and BSQZ.

Even if BHSC2 has a hybrid structure, and at least analytically is very similar to the BHSC1, it has higher stress, even higher than the CBBB, but it can achieve good conversion ratios.

Converter BQ3 has the worst stress, with up to 80% higher stress compared to the CBBB, most influenced by the larger number of switches.

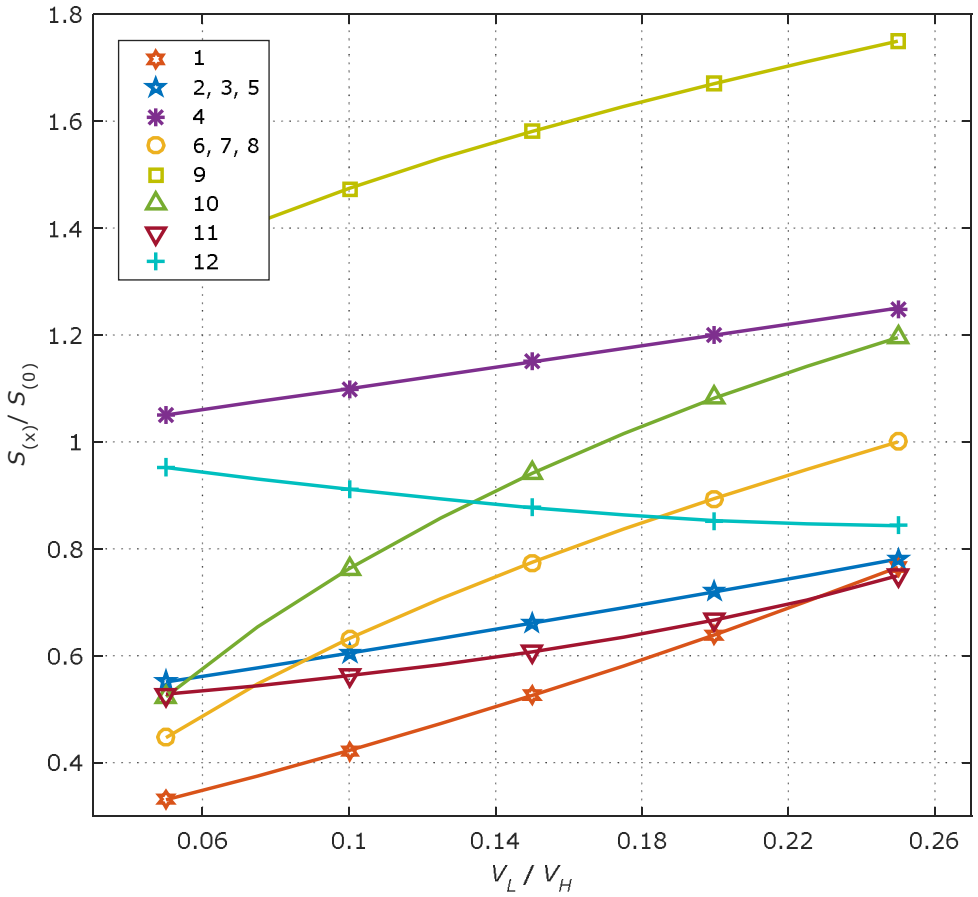

Fig. 6.5. Total active switch stress comparison between previousely presented topologies: x = 1. BHSISC, 2. BHSI, 3. BHSC1, 4. BHSC2, 5. BSQZ, 6. CBQ, 7. BQ1, 8. BQ2, 9. BQ3, 10. BTMM, 11. BSC1, 12. BSC2, normalized to 0. CBBB.
Details of the converters are highlighted in Table 6.1

6.7. Conclusions

Overall, each topology may be more suitable for a specific application, depending on the range of the voltage ratio, number of switches, or the total active switch stress, passive components size, or the costs of the components.

In terms of conversion ratio, the quadratic converters offer the widest conversion ratios, but they are closely followed by the BHSISC converter. The rest of the hybrid converters are situated between the quadratic and the conventional converter, and this aspect can be beneficial if these are the conversion ratios that are desired.

In terms of total inductor and total capacitor energy, the switched capacitor converters BSC1 and BSC2 offer very good performance but with the cost of current spikes while charging and discharging capacitors with different voltages by connecting them in parallel. Next, the hybrid converters offer good characteristics in this aspect, similar to the conventional converter but with much wider conversion ratios. The rest of the topologies have much larger requirements for capacitors or inductors.

Regarding the total active switch stress, the BHSISC converter and the rest of the hybrid topologies achieve the best results, much lower than the conventional converter, and followed by the rest of the topologies.

An interesting conclusion that can be drawn for the quadratic converters, is that the characteristics of the converters considered for this analysis, are identical for under almost all aspects, regardless of their schematic.

Overall, the hybrid topologies, especially the BHSISC converter, offer good characteristics which make them good candidates for applications where a wide voltage conversion ratio is desired.

7. MICROGRID POWER SHARING CONTROL STRATEGIES FOR BIDIRECTIONAL CONVERTERS

7.1. Abstract

This chapter presents an overview of the microgrid control strategies, with applications for DC-DC bidirectional wide ratio converters. A classification of the microgrid control strategies is initially presented, based on the type of communication between the microgrid devices (centralized, distributed and decentralized) and the hierarchy in which the control structures are classified (tertiary, secondary or primary). This work focuses on the decentralized strategies, with applications in droop controlled microgrids, useful for nanogrid control, or as local controllers for the centralized or distributed strategies. Droop control methods for power sharing in supercapacitor storage methods are presented, based on different virtual impedances, with simulation and experimental validation.

7.2. Introduction

Many applications for bidirectional converters are for storage purposes in renewable energy applications, which are usually integrated in microgrid structures [33], [87]–[94]. A means of managing the power flow withing the grid by controlling the converters is required in order to manage the source of production or storage, to reduce energy costs, increase efficiency, or increase reliability [95], [96].

As shown in Fig. 7.1, the microgrid control strategies are usually classified by scientific literature, such as [97]–[101], from the communication perspective (by where the energy management decisions are taken) in three types: centralized, distributed, and decentralized. The example diagram is for a DC microgrid, but the same is applicable in AC, or hybrid grids. The representation considers multiple distributed generators (DG_1 to DG_n) each connected with a DC-DC converter to the common voltage DC bus.

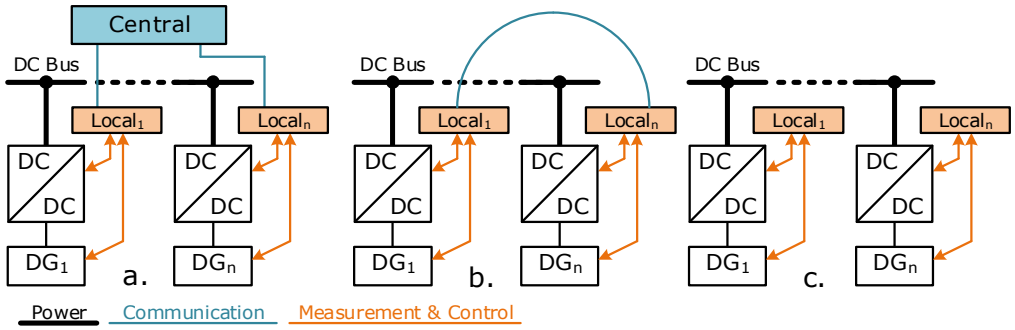

Fig. 7.1. DC Microgrid control strategies, categorized from the communication perspective (location of the energy management computations): a. Centralized control (in a central unit), b. Distributed control (distributed among controllers which communicate), c. Decentralized control (decisions taken locally by measuring bus parameters, without communication) [97]–[101] (DG - distributed generators)

In a centralized system, data from each unit is acquired in a single centralized place, it is processed, and commands are sent back to each local controller. In a distributed control a coordinated control is realized, and the energy management strategy is processed locally. In the decentralized control, the only means of exchanging information between the units, is by modifying parameters of the grid, usually the voltage in DC grids (there are also cases where a frequency is injected in the grid as in [102], [103]).

Usually centralized systems achieve greater performances, but with the disadvantage of having a decreased reliability as there is only one central control system. The distributed systems solve the problem of reliability by using multiple controllers, which also makes them better for large networks offering resilience against single points of failure. Nevertheless, an appropriate algorithm is required for communication among them.

Decentralized control, such as [104], [105], is the simplest control since it is limited to measuring the parameters of the DG, converter and grid voltage, and is mainly based on droop control or other similar power sharing algorithm. It has the advantage of being easy to implement, but also disadvantages because it is limited in the information about neighbor DGs. Because of these reasons, the decentralized control is most common in nanogrid structures.

The control of the microgrid is divided based on their purpose, and their response time, in a hierarchy: the primary, the secondary and the tertiary controllers and their functions are briefly enumerated in Table 7.1, according to [97]–[101].

Each converter has a local controller, which is also the primary controller and is responsible for a few main objectives: voltage & current regulation, power sharing (which can be performed with droop control), local supervisions, and islanding detections. The local controller is also responsible for other functions dependent on the DG, such as the charge/discharge control for storage units, maximum peak power point tracking for solar, wind or even hydro power, and other specific functions that require to be managed locally. Being the closest to the converter, its response time is the fastest and is hierarchically controlled by the Secondary controller. In a centralized system (Fig. 7.1. a), each local controller receives its reference from the central system, which in some cases can take the function of power sharing as well.

Table 7.1. Hierarchy of the microgrid controls

Control level	**Functions**
Tertiary (part of the host grid)	To coordinate to the host grid, or neighbor microgrids It is a part of the utility management system Responsible with the management, optimization and the system regulations
Secondary (Microgrid EMS)	Solve system level issues Coordination between DGs (i.e. regarding SoC) Power Flow control Synchronization to outer grid Power quality control Compensating the primary control deviations Economical & reliable operation by using energy price forecasts The EMS minimizes microgrid operational cost & maximizes reliability Set points for Droop control
Primary (Local)	Voltage & Current control, Power Sharing control (i.e. droop control) Local supervision Islanding detection

In a distributed system, the secondary controller is closely connected to the local controller. In decentralized systems, the local controller is the only controller available, and the power sharing strategy is responsible for controlling the microgrid.

The secondary controller has the functions of the Energy Management System (EMS), and includes system level attributes such as: coordination between the DGs (i.e. based on the SoC in case of batteries), power flow control, synchronization to the outer grid, power quality control, compensating eventual deviations caused by the primary controller, economical & reliability purposes (such as energy price forecasts, minimizing operational costs). These functions are realized by generating power/current references for the local controller, or, various set points for the droop power sharing control. For decentralized controllers, in some cases the local controller also has the function of an EMS.

The tertiary control has purposes such as coordination of the microgrid to the neighboring microgrids, ancillary services, overall system regulations, and it is usually a subsystem of the utility distribution management system from the host grid, not the actual microgrid.

This work focuses on the decentralized strategies, as they are the most suited for small scale, small power applications, and the droop power sharing methods used for these strategies can be upgraded in centralized [106]–[109], or distributed structures [110]–[113].

An important part in microgrid structures are the storage elements so the charge/discharge strategy needs to take into account the energy flow to the storage elements as well, in order to achieve the best performances and maximum life for the storage elements [114].

The droop control was developed as a power sharing strategy, by emulating the droop characteristic of synchronous generators [115], [116], and was later used for DC converters where parallel operation of multiple modules was required [117]–[122]. The method was also used in various papers as a decentralized control method for nanogrids [104], [105].

The standard droop method in DC voltage, controls the converter so that it has a voltage variation (ΔV), proportional to its output current, around the prescribed voltage (V_d), similar to an ideal voltage source with a series resistor connected at the output, as shown in Fig. 7.2. This control feature is done by lowering the output voltage reference, with respect to the output current. The actual characteristic of this method is presented in Fig. 7.3.

This work is focused on bidirectional hybrid DC-DC converters that achieve a wide voltage conversion ratio. As it was also mentioned in chapter 1, these types of converters are especially beneficial in supercapacitor (SC) storage, as a better utilization is made for the SC energy when wide voltage variations are possible.

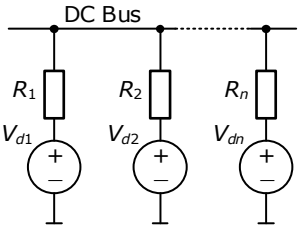

Fig. 7.2. Equivalent schematic of the conventional droop methods
(V_{d1} - V_{dn} are ideal voltage sources that emulate the constant voltage operation of a converter, R_1 - R_n are the droop resistors emulated by the converter operation, within its control loop)

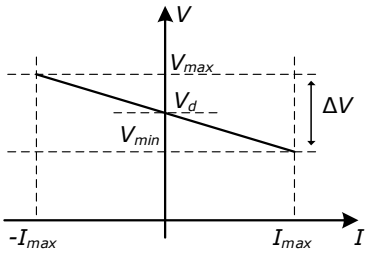

Fig. 7.3. Standard droop control voltage-current static characteristic of the converter (V_d – nominal grid voltage; V_{min}, V_{max}, $\pm I_{max}$ – voltage-current range, ΔV – voltage variation)

The following sections present different power sharing strategies for SC storage with simple or more complex implementation methods that are decentralized and based on the standard droop control method.

7.3. Nonlinear droop

A simple power sharing strategy based on two nonlinear droop methods were initially designed in [123] for SC storage applications. The methods were inspired by other nonlinear droop methods such as [104], [124], and were further analyzed for their benefits in [125]–[127].

The requirement was to create a control method that will limit the charge and discharge of the SC in the usual voltage operation range and increase its charging currents when approaching the bus voltage limits. To achieve this requirement, the droop methods with the characteristics from Fig. 7.4 were developed.

An initial nonlinear droop method (Fig. 7.4. a) uses a larger droop resistor (R_A), and two Zener diodes (D_{Z1}, D_{Z2}), ND-LRZD, connected in series to each other, and in parallel to the resistor. With this schematic, the method operates similarly to the conventional droop, but when the voltage limits dictated by the Zener diodes are approached, a larger current will limit further variations on the bus by charging or discharging the SC. An important aspect to mention, is that the ideal voltage source, V_{dA}, is a current limited voltage source when implemented in the converter.

The nonlinear method can be implemented using a nonlinear resistor, R_B, as shown in Fig. 7.4. b, ND-NR. This virtual resistor can be mathematically designed to resemble the ND-LRZD method, with different mathematical functions. The static characteristics for the two methods are presented in Fig. 7.5.

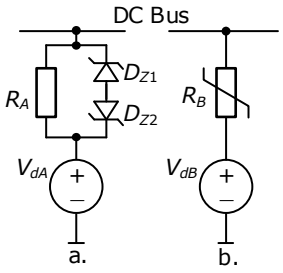

Fig. 7.4. Equivalent schematic of the nonlinear droop methods using: a. Linear resistor (R_A) and Zenner diodes (D_{Z1}, D_{Z2}) – ND-LRZD; b. A nonlinear resistor (R_B) – ND-NR [123] (V_{dA}, V_{dB} are current limited voltage sources)

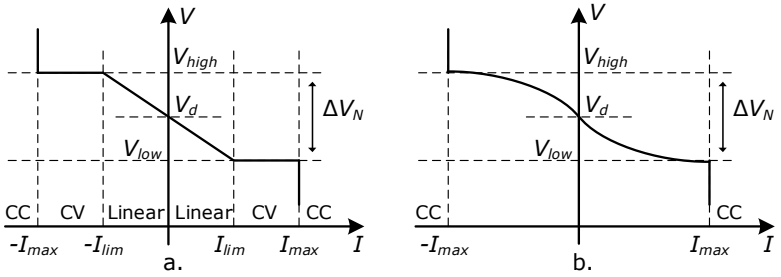

Fig. 7.5. Static characteristics of the: a. ND-LRZD (Fig. 7.4.a); b.ND-NR (Fig. 7.4.b), for a converter operating in constant current (CC), constant voltage (CV) or with linear voltage-current dependency (V_d – nominal grid voltage; V_{min}, V_{max}, $\pm I_{max}$ – voltage-current range, ΔV – voltage variation, $\pm I_{lim}$ maximum current range for linear operation)

As mentioned above, the ND-LRZD, operates in a linear region, up until the voltage is limited by the two ideal Zener diodes, after which it will operate in the constant voltage mode (CV). The nonlinear resistor characteristic used for the ND-NR, is shaped so that its static characteristic resembles that of the ND-LRZD. Therefore, various mathematical relations can be used. Above the maximum current limits, I_{max}, the converter operates in constant current mode (CC) for both ND-LRZD and ND-NR methods.

As a virtual varistor can be used for modeling the R_B resistor, a power function is considered for its current-voltage dependency:

$$I_{RB} = sgn(V_{RB}) \cdot k_V \cdot |V_{RB}|^{a_V}, \tag{7.1}$$

where k_V and a_V are the gain and power coefficients, respectively, that help shape the function.

A different function that achieves a similar shape is the inverse tangent function:

$$V_{RB} = k_1 \cdot \text{atan}(k_2 \cdot I_{RB}), \tag{7.2}$$

where k_1 and k_2 are the output and input gain coefficients, respectively, that help shape the function.

The two functions, (7.1) and (7.2), together with a linear resistor, are presented in Fig. 7.6 for comparison.

In order to implement the control for the two methods, an additional voltage controller is required, apart for the current controller from chapter 2, in order to obtain a cascaded current-voltage control. The voltage controller is designed by trial and error, and the following transfer function is obtained:

$$G_{CV}(z) = \frac{0.11 \cdot z - 0.1}{z - 1}. \tag{7.3}$$

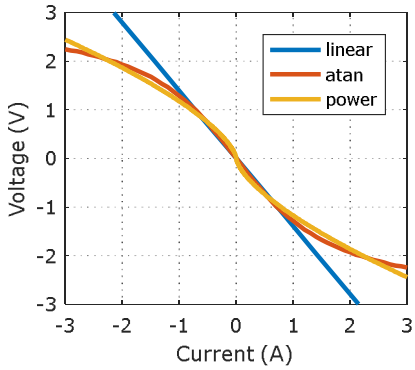

Fig. 7.6. Static characteristics for: linear droop (R_{droop}=1.4Ω), ND-NR with power function (7.1) (k_V=0.7857, a_V=1.5) and ND-NR with atan function (7.2) (k_2=0.8, k_1=1.91)

The control implementation for the ND-LRZD is presented in Fig. 7.7. The control loop uses a cascaded current-voltage control with a saturation block, Sat. 1, to limit the i_{L1} maximum reference current, from the inner current control loop. The actual droop implementation contains the R_A and the Sat. 2 saturation block, applied for the i_{L2} current (which can be approximated to the current from the voltage bus, I_H). The R_A gain represents the actual resistor from Fig. 7.4. a, and Sat. 2 is used to simulate the breakdown voltages of the Zener diodes. The voltage droop (ΔV_{RA}) is added to the bus voltage (subtracted from the reference), which, in this case, is connected to the high voltage output of the BHSC1, V_H.

The ND-NR method is implemented in a similar way to the ND-LRZD, as presented in Fig. 7.8. The cascaded current-voltage control is used, with the additional change in the calculation of the droop voltage, ΔV_{RB}, which is performed with (7.2). The inverse tangent function is used, as this function is already implemented in the core of some microcontrollers, such as the TMS320F28335, and this will result in faster calculation for the controller. The i_{L2} current is used here as well, as an approximation of I_H current.

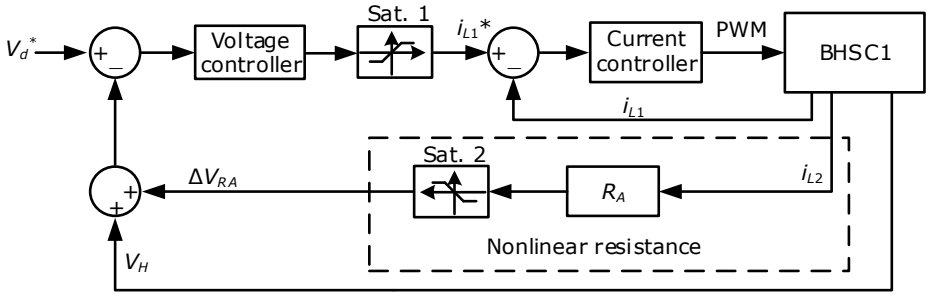

Fig. 7.7. ND-LRZD control method implementation (Fig. 7.4.a) for the BHSC1 converter (Ch. 2) using cascaded current-voltage control, with the nonlinear resistance implemented by the R_A gain and Sat. 2 saturation block (V_d^* - DC bus voltage reference; V_H – the high voltage output of the BHSC1; ΔV_{RA} – resistance voltage drop; i_{L1}, i_{L2} – converter inductor currents, Sat. 1 – saturation block for limiting i_{L1}^* current)

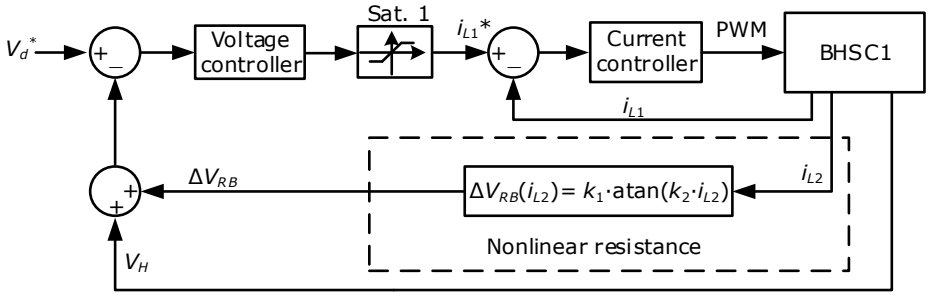

Fig. 7.8. ND-NR control method implementation (Fig. 7.4.b) for the BHSC1 converter (Ch. 2) using cascaded current-voltage control, with the nonlinear resistance implemented by the R_B arctangent function (V_d* - DC bus voltage reference; V_H – the high voltage output of the BHSC1; ΔV_{RB} – resistance voltage drop; i_{L1}, i_{L2} – converter inductor currents; Sat. 1 – saturation block for limiting i_{L1}* current; k_1, k_2 – atan function coefficients)

The parameters for testing the two methods are enumerated in Table 7.2, for both nonlinear droop methods. These parameters are used in the static gain characteristics, in Fig. 7.5, and in the control loop implementations, in Fig. 7.7 and Fig. 7.8.

The BHSC1 converter is used for testing the droop methods, as it has inductors on each output, and the currents are already available for measurements as they are state variables and were considered for control purposes from the initial design. The test setup used for this method is shown in Fig. 7.9, and it consists of a supercapacitor bank with C_{SC} capacitance, the BHSC1 converter, a bus capacitance, C_{bus}, a real droop resistance, R_{droop}, and a parallel combination between an electronic load and a DC source, connected though a diode. The purpose of the R_{droop} and the parallel combination of the source and electronic load, is to emulate a conventional droop controlled grid and a real resistor is used for the grid side in order to reduce the complexity of the test setup, while the nonlinear resistors are programmed in the microcontroller. The specifications of the equipment used in the test setup are presented in Table 7.3.

Table 7.2. Nonlinear droop method parameters for the ND-LRZD and the ND-NR

Element	**Value**	**Unit**	**Description**
General parameters			
V_d*	350	V	Nominal grid voltage reference
V_{high}	360	V	Upper bus voltage limit
V_{low}	340	V	Lower bus voltage limit
ΔV_N	20	V	Nominal bus voltage variation
I_{max}	7.1	A	Maximum output (I_H) converter current
ND-LRZD (Fig. 7.7) parameters			
R_A	3	Ω	Linear droop resistance
I_{lim}	3.33	A	Current limit between CV and Linear operation
ND-NR (Fig. 7.8) parameters			
k_1	7.9577	V	Output gain for the atan function
k_2	0.5	A^{-1}	Input gain for the atan function

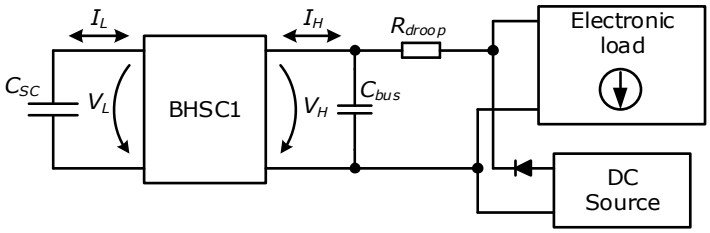

Fig. 7.9. Experimental test setup consisting of a supercapacitor bank (C_{SC}), the BHSC1 converter (Ch. 2), a bus capacitor (C_{bus}), an electronic voltage load in parallel to a DC source and a real droop resistor (R_{droop}) (for DC bus emulation).
All parameters are presented in Table 7.3

Table 7.3. Experimental setup equipment for testing the droop methods

Element	**Device**	**Manufacturer**	**Characteristics**
C_{SC} (two series)	BMOD0063 P125 B04	Maxwell	63F, 125V, 1900A, 1.7kW/kg, 2.3Wh/kg
Electronic load	EA-EL 9400-50	Elektro-Automatik	0-2.4kW, 0-400V, 0-50A
DC Source	TC.P.10.400.400.S	Regatron	0-10kW, 0-400V, 0-50A
C_{bus}	-	-	10mF
R_{droop}	-	-	0-4.4 Ω

Simulation and experimental results are presented for the two methods in Fig. 7.10 and Fig. 7.11, for the ND-LRZD, and Fig. 7.12 and Fig. 7.13 for the ND-NR. As the dynamic characteristic is not important for these characteristics, an initial R_{droop} was shorted (R_{droop}=0), and current limitation was used for both the source and the electronic load, for a simple operation. A voltage variation was prescribed to the load and source, in order to emulate transitions between the two operation modes with current limitation.

The results from Fig. 7.10, show the operation for the "Linear" range with the ND-LRZD, for currents between $\pm I_{lim}$, i_{L2}=±2A, and a smooth operation is achieved. When operating in CV mode, at i_{L2}=±5A, damped oscillation are shown for the currents of the converter in Fig. 7.11, which is expected as in this range the virtual resistance is considered to be null. In this case, the bus voltage is limited at 340V or 360V.

The ND-NR achieves similar results under the same conditions, with either lower currents, i_{L2}=±2A in Fig. 7.12, or higher currents, i_{L2}=±4A in Fig. 7.13. With this method the same voltages are achieved during the two regions, with the difference that for the second method the current or voltage oscillations are greatly reduced, and a smoother transition is realized. Therefore, the ND-NR method does not introduce the same oscillations during the charge/discharge transitions.

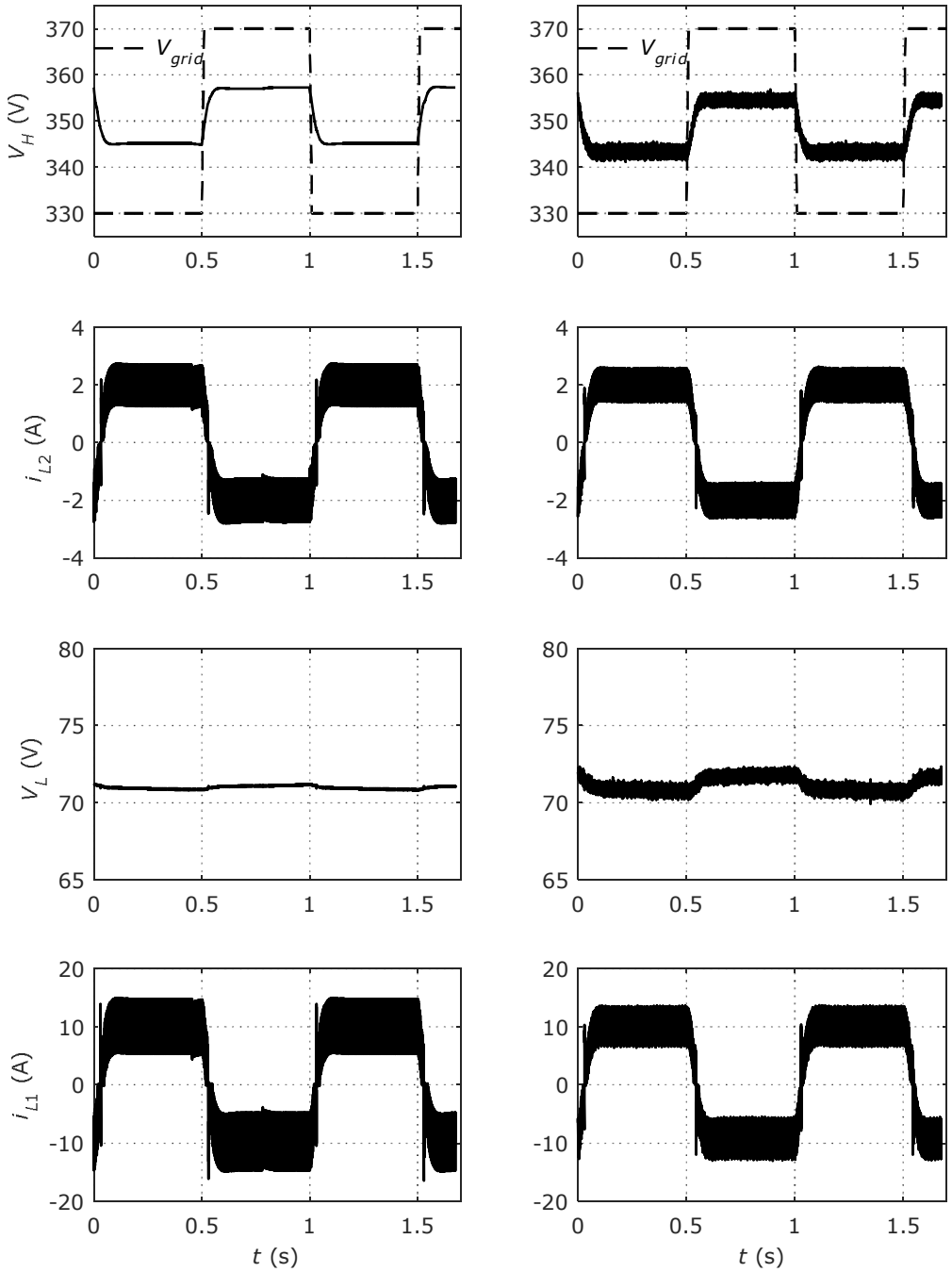

Fig. 7.10. BHSC1 simulation (left) and experimental (right) waveforms for transient operation, controlled by the ND-LRZD (in "Linear" region): transition for V_{grid}=V_d±20V, i_{L2}=±2A (limited by source/load), V_L=71V, P_{in}=±0.7kW, R_{droop}=0 Ω (i_{L1}, i_{L2}, are the currents from L_1 and L_2 inductors, respectively, V_L, V_H are the low and high voltage inputs, respectively)

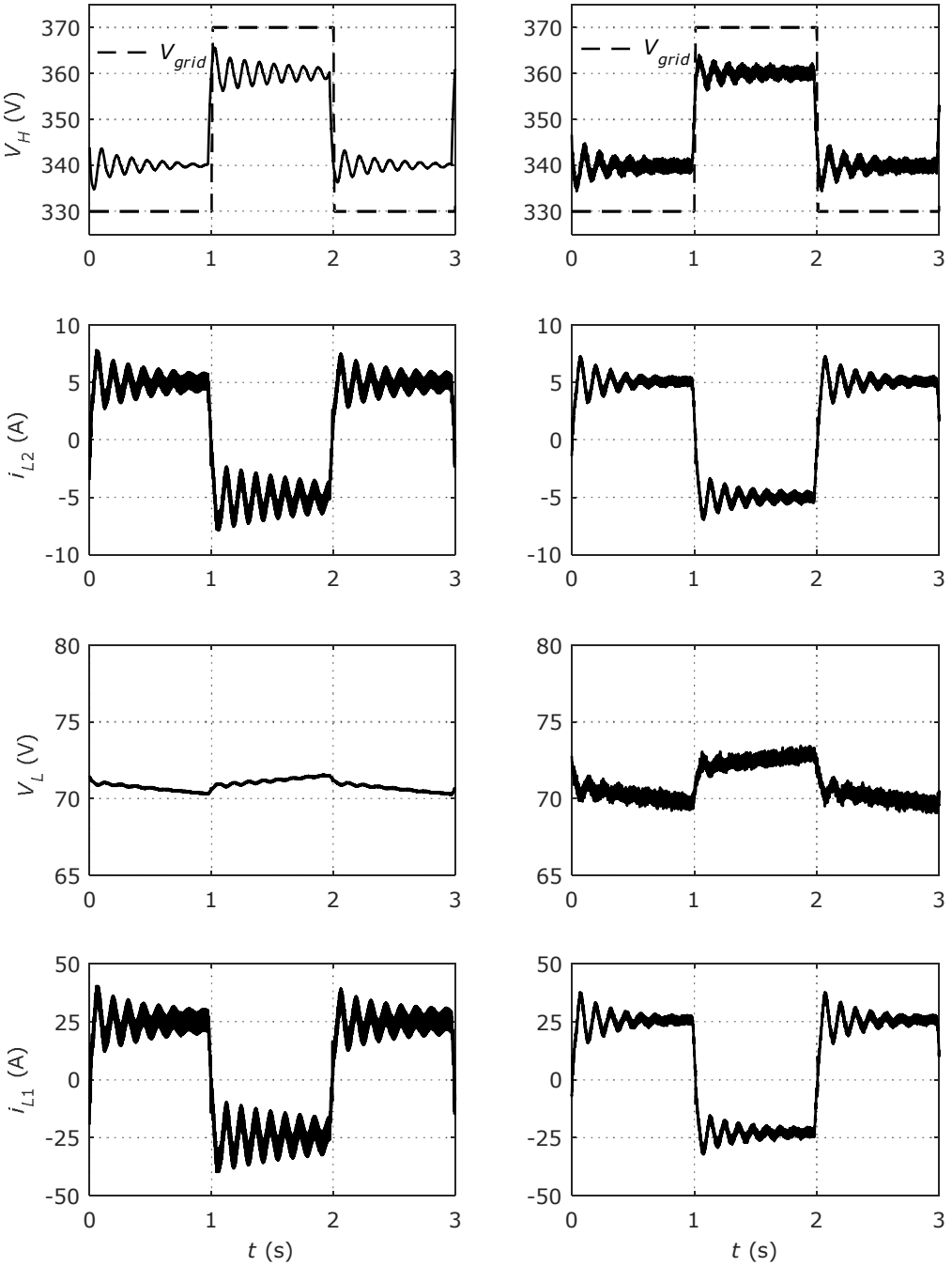

Fig. 7.11. BHSC1 simulation (left) and experimental (right) waveforms for transient operation, controlled by the ND-LRZD (in "CV" region): transition for V_{grid}=V_d±20V, i_{L2}=±5A (limited by source/load), V_L=71V, P_{in}=±1.78kW, R_{droop}=0 Ω (i_{L1}, i_{L2}, are the currents from L_1 and L_2 inductors, respectively, V_L, V_H are the low and high voltage inputs, respectively)

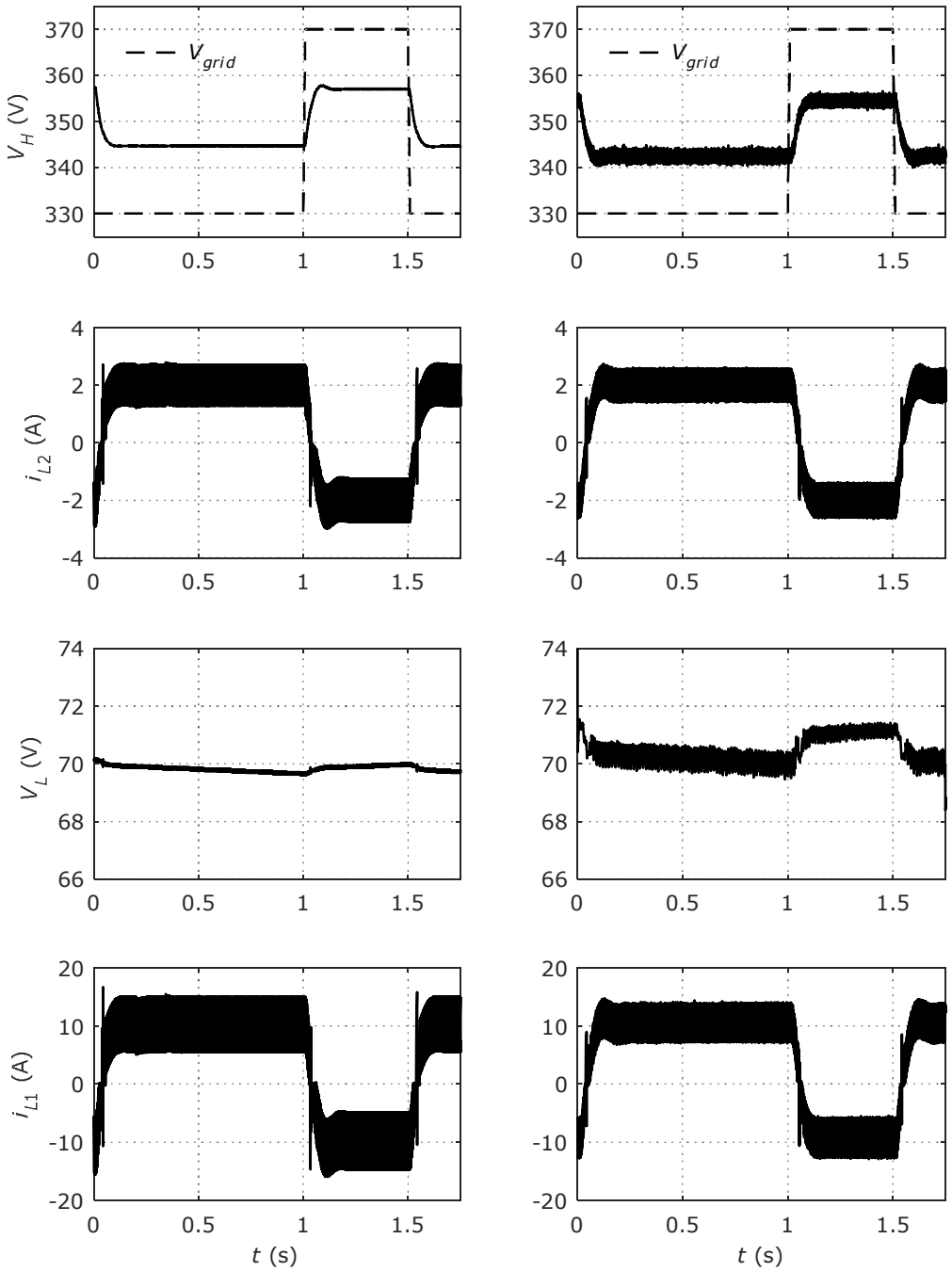

Fig. 7.12. BHSC1 simulation (left) and experimental (right) waveforms for transient operation, controlled by the ND-NR: transition for V_{grid}=V_d±20V, i_{L2}=±2A (limited by source/load), V_L=70V, P_{in}=±0.7kW, R_{droop}=0 Ω (i_{L1}, i_{L2}, are the currents from L_1 and L_2 inductors, respectively, V_L, V_H are the low and high voltage inputs, respectively)

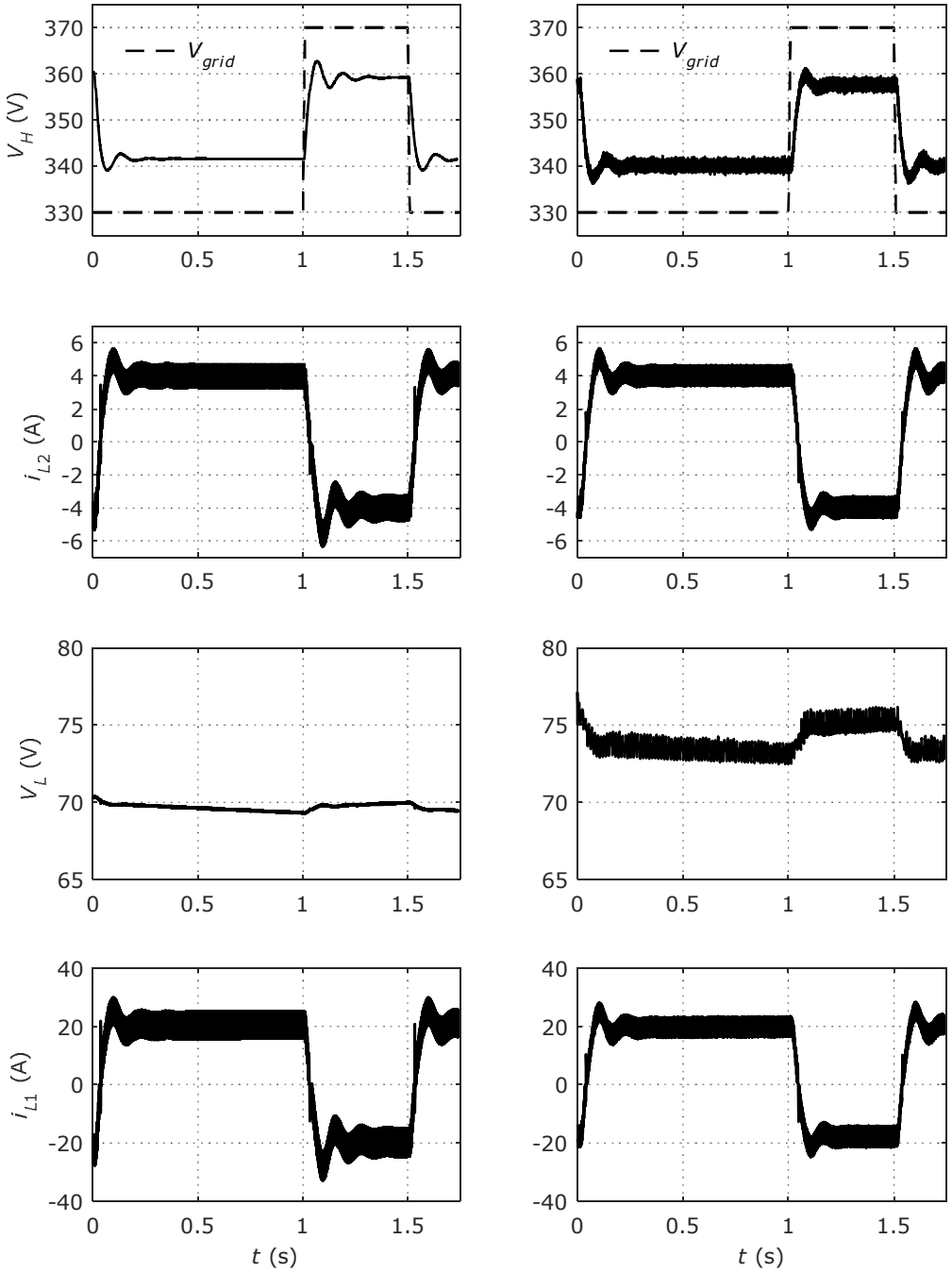

Fig. 7.13. BHSC1 simulation (left) and experimental (right) waveforms for transient operation, controlled by the ND-NR: transition for V_{grid}=V_d±20V, i_{L2}=±4A (limited by source/load), V_L=70V, P_{in}=±1.4kW, R_{droop}=0 Ω (i_{L1}, i_{L2}, are the currents from L_1 and L_2 inductors, respectively, V_L, V_H are the low and high voltage inputs, respectively)

The static characteristics of the two methods are presented in Fig. 7.14 and Fig. 7.15, for the ND-LRZD and ND-NR, respectively. A good correspondence is shown between them, with the exception of the CC operation for ND-LRZD method. The difference for CC operation comes from the fact that the i_{L2} current is not limited but actually the i_{L1} current, as shown in Fig. 7.7. The I_{max} limits from Fig. 7.5, are calculated based on fixed limits for i_{L1} current, and a maximum power limitation. With these conditions, the I_{max} values are variable within a small range when the voltages at the two inputs are drastically changed as the duty ratio are also changed. The limits are to be considered as a safety feature for protecting the converter.

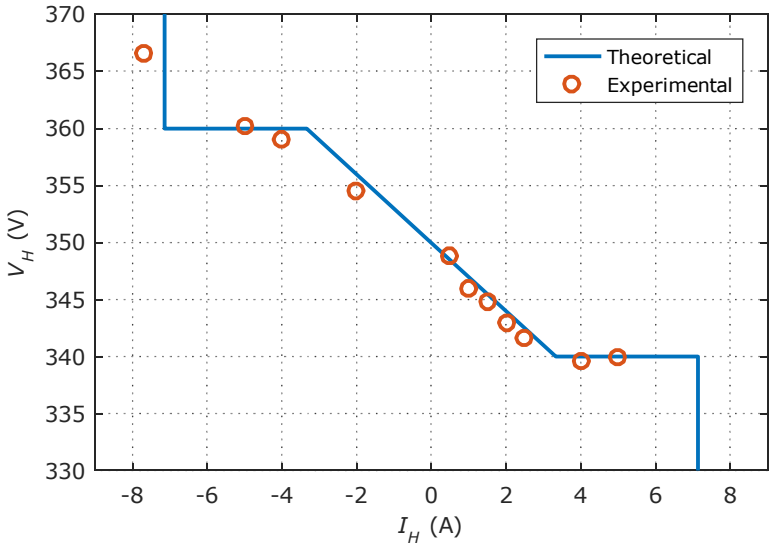

Fig. 7.14. Theoretical vs experimental static characteristic of the ND-LRZD method with parameters from Table 7.2

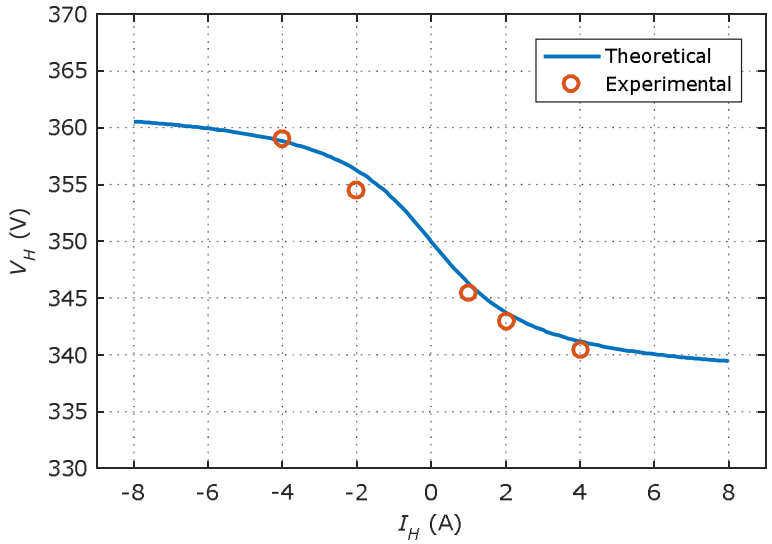

Fig. 7.15. Theoretical vs experimental static characteristic of the ND-NR method with parameters from Table 7.2

7.4. Nonlinear virtual impedance

Newer methods for introducing SC storage in droop controlled microgrids, [128]–[131], propose the use of virtual impedances in place of the conventional droop resistors, achieving a virtual impedance droop control method (VID) as a power sharing controller. The equivalent schematic of the VID, placed in a conventional droop-controlled grid, is presented in Fig. 7.16. a. The commonly used impedance for this method is a series resistor-capacitor circuit, achieving a high-pass filter for the currents flowing to the converter. With this filter, only high frequency variations from the DC bus will charge/discharge the SC, while the low frequency currents will flow to the rest of the grid.

Based on the VID and the ND-NR, presented in the previous section, we proposed a nonlinear virtual impedance droop control method (NVID) in [132], with the schematic presented in Fig. 7.16. b. This method works similarly to the VID, with the difference that the nonlinear resistor makes possible for achieving a variable cutoff frequency, dependent on the amplitude of the voltage. The variable cutoff frequency will make the charge/discharge process to operate at currents depending on the voltage variation, and implicitly the power fluctuations in the grid. If lower power variations are present at a specific moment (and implicitly lower voltage variations), the SC influence can be designed to be lower. Another option is to maintain normal operation at lower power variations but increase the effect on higher power variations. Similar to the ND-NR, the NVID can use different types of nonlinear resistors, and the inverse tangent function is used here as well.

The control loop implementation is similar to the implementation for the ND-LRZD and ND-NR, in the sense that it has a cascade voltage-current control, and the virtual impedance is used in the place of the nonlinear resistor.

Firstly, the VID control implementation is realized in a similar fashion, in order to be compared to the NVID, and it is presented in Fig. 7.17. Here the voltage on the virtual filter resistor (R_F) and virtual capacitor (C_F) are added as they are connected in series. The resistor voltage drop is calculated simply, and the capacitor voltage drop is calculated considering the transfer function, in *s* domain, of an ideal capacitor:

$$\frac{v_C(s)}{i_C(s)} = \frac{1}{s \cdot C}. \tag{7.4}$$

The implementation of the NVID control method is similar to the VID implementation, with the difference that the linear filter resistance is replaced by the arctangent function, defined in a similar fashion to the ND-NR method. The control loop implementation of the NVID is presented in Fig. 7.18.

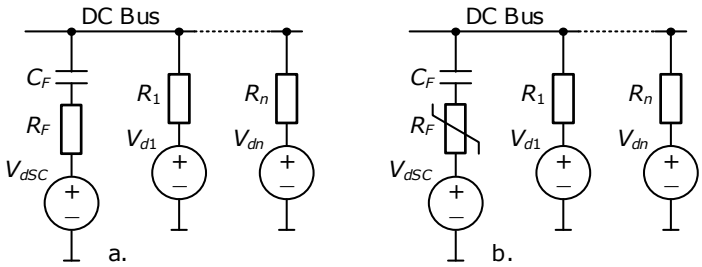

Fig. 7.16. Equivalent schematics of the: a. Virtual Impedance Droop control method (VID) using a RC impedance; b. Nonlinear Virtual Impedance Droop control method (NVID) which uses a nonlinear resistor for the RC impedance, both schematics presented in a conventional droop-controlled grid

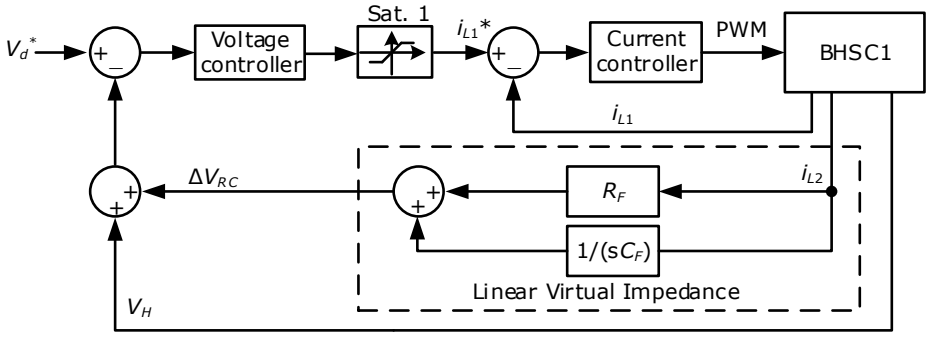

Fig. 7.17. VID control method implementation (Fig. 7.16.a) for the BHSC1 converter (Ch. 2) using cascaded current-voltage control, with the virtual impedance implemented by the R_F gain and $1/(sC_F)$ transfer function (V_d* - DC bus voltage reference; V_H – the high voltage output of the BHSC1; ΔV_{RC} –virtual impedance voltage drop; i_{L1}, i_{L2} – converter inductor currents, Sat. 1 – saturation block for limiting i_{L1}* current)

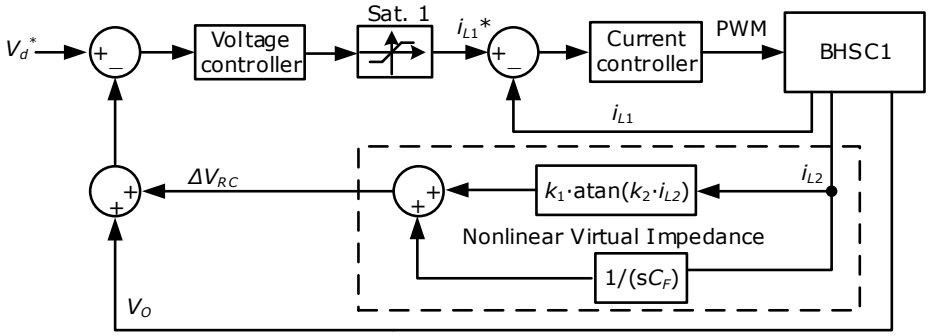

Fig. 7.18. NVID control method implementation (Fig. 7.16.b) for the BHSC1 converter (Ch. 2) using cascaded current-voltage control, with the virtual impedance implemented by the atan function and $1/(sC_F)$ transfer function (V_d* - DC bus voltage reference; V_H – the high voltage output of the BHSC1; ΔV_{RC} –virtual impedance voltage drop; i_{L1}, i_{L2} – converter inductor currents, Sat. 1 – saturation block for limiting i_{L1}* current, k_1, k_2 – atan function coefficients)

Using the parameters of Table 7.4, the two methods were implemented and tested with the setup from Fig. 7.9 and the equipment described in Table 7.3. Initial simulation and experimental results confirm the correspondence between the two results, as shown in Fig. 7.19. A total time of 2 seconds was used as the simulation results will result in a very large size if larger simulation times are used and it becomes difficult to process. Nevertheless, larger times are required in order to test the operation of the two methods, therefore the experimental results are presented in Fig. 7.20 to Fig. 7.23 using acquisition times of 10s. The VID and NVID methods are compared for voltage variations applied to the grid, of V_d±10V in Fig. 7.20 and Fig. 7.21, respectively, and with voltage of V_d±30V in Fig. 7.22 and Fig. 7.23. The design in Table 7.4 was performed such that the NVID methods has a small influence in the grid at small voltage variations, but at larger voltage variations it performs similar to the VID method.

As shown in Fig. 7.20 and Fig. 7.21, at a small voltage variation, the NVID method charges/discharges the SC with 66% the power vehiculated by the VID method. The comparison between Fig. 7.22 and Fig. 7.23 shows that at a higher voltage variation, the operation of the two methods is similar, achieving the same charge/discharge power for the SC. This method of operating gives the NVID an advantage when the operation of the converter is not required for low powers, but a higher influence is required by the converter at higher powers. The NVID method also has an advantage for centralized system, where it gives the possibility to adjust multiple coefficients by the higher system, for an optimized operation specific to different operations.

Table 7.4. Virtual impedance parameters for the VID and NVID

Element	**Value**	**Unit**	**Description**
General parameters			
V_d*	350	V	Nominal grid voltage reference
*VID (*Fig. 7.17*) parameters*			
R_F	3	Ω	Virtual linear filter resistance
C_F	1	F	Virtual filter capacitor
*NVID (*Fig. 7.18*) parameters*			
k_1	8.59	V	Output gain for the atan function
k_2	1.7	A^{-1}	Input gain for the atan function
C_F	1	F	Virtual filter capacitor

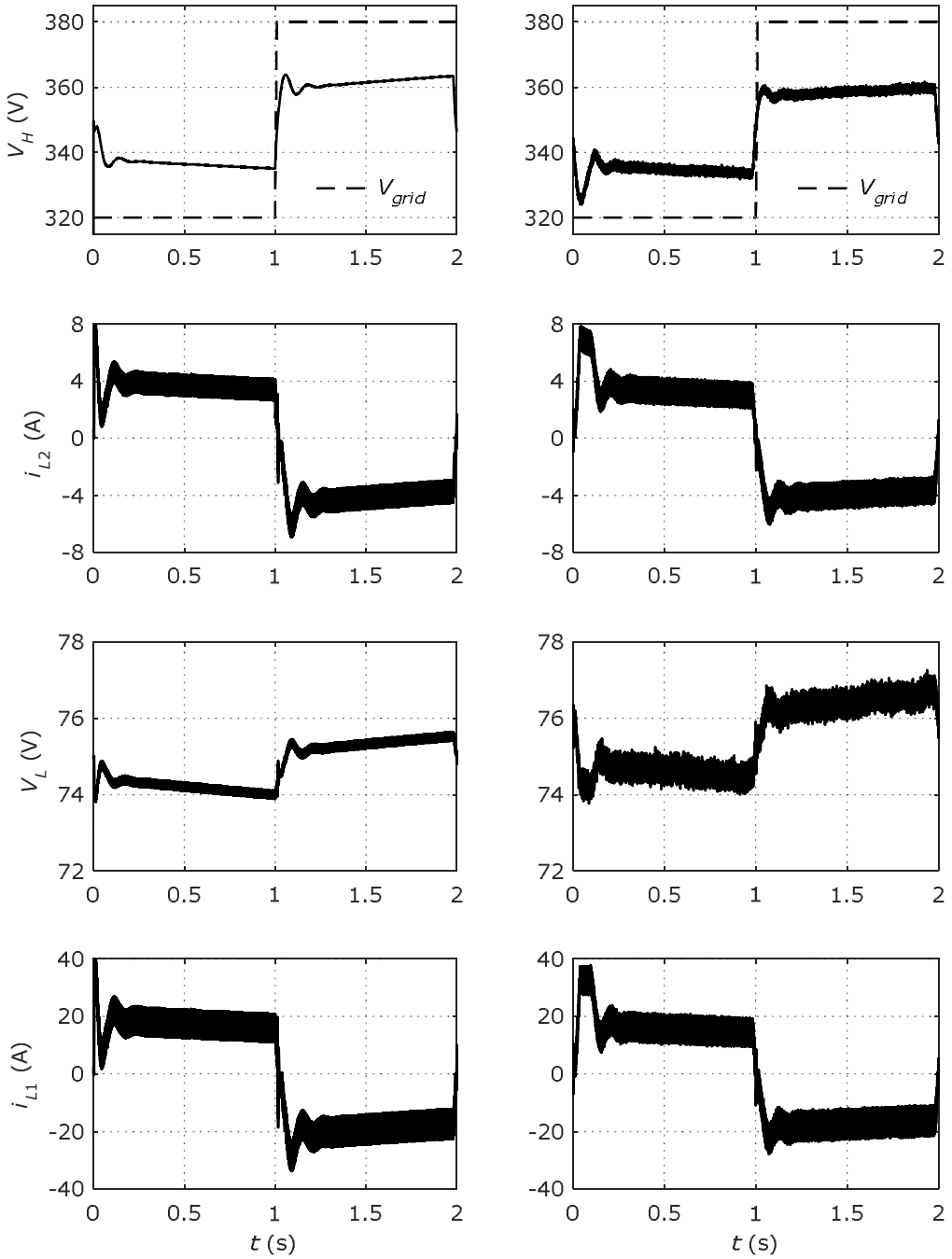

Fig. 7.19. BHSC1 simulation (left) and experimental (right) waveforms for transient operation, controlled by the NVID: transition for V_{grid}=V_d±30V, i_{L2}≈±4A, V_L≈75V, P_{in}≈±1.5kW, R_{droop}=4.4 Ω (i_{L1}, i_{L2}, are the currents from L_1 and L_2 inductors, respectively, V_L, V_H are the low and high voltage inputs, respectively)

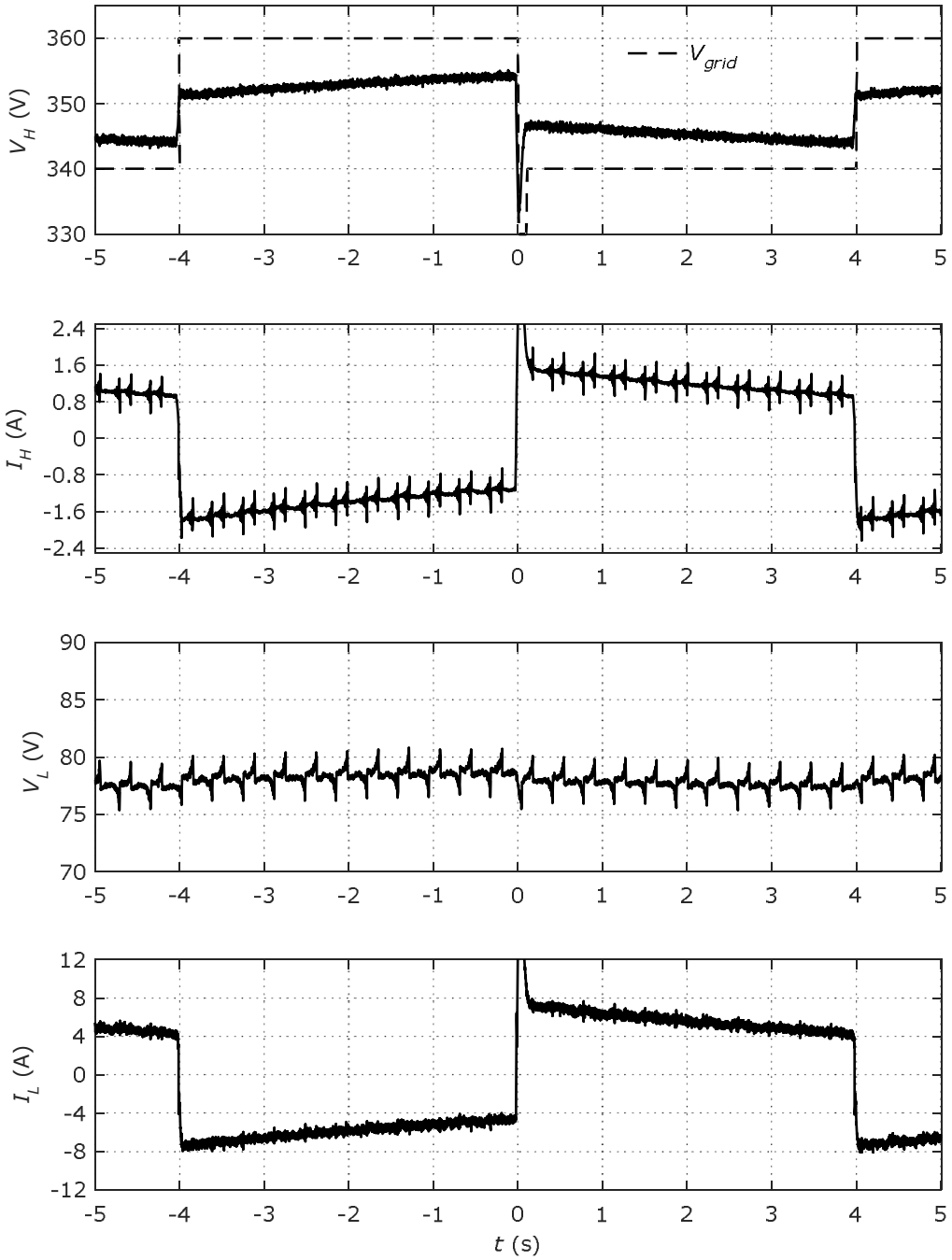

Fig. 7.20. Experimental waveforms for transient operation of the BHSC1, controlled by the VID: transition for V_{grid}=V_d±10V (+ voltage impulse at 0s), I_H≈±1.5A, V_L≈77V, P_{in}≈±450W, R_{droop}=4.4 Ω (V_L, V_H are the low and high voltage inputs, respectively, I_L, I_H are the low and high voltage side currents, respectively)

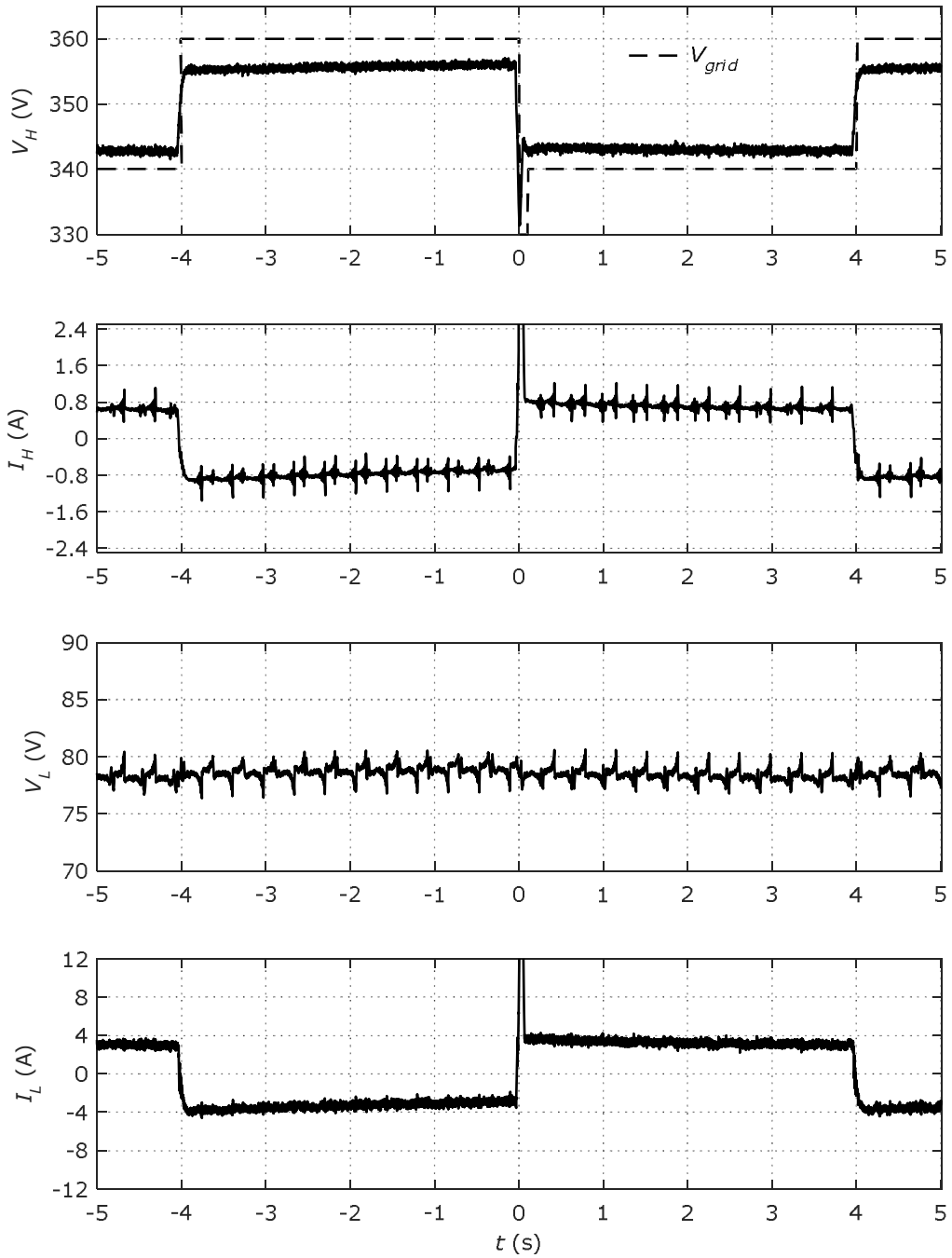

Fig. 7.21. Experimental waveforms for transient operation of the BHSC1, controlled by the NVID: transition for V_{grid}=V_d±10V (+ voltage impulse at 0s), I_H≈±0.7A, V_L≈77V, P_{in}≈±300W, R_{droop}=4.4 Ω (V_L, V_H are the low and high voltage inputs, respectively, I_L, I_H are the low and high voltage side currents, respectively)

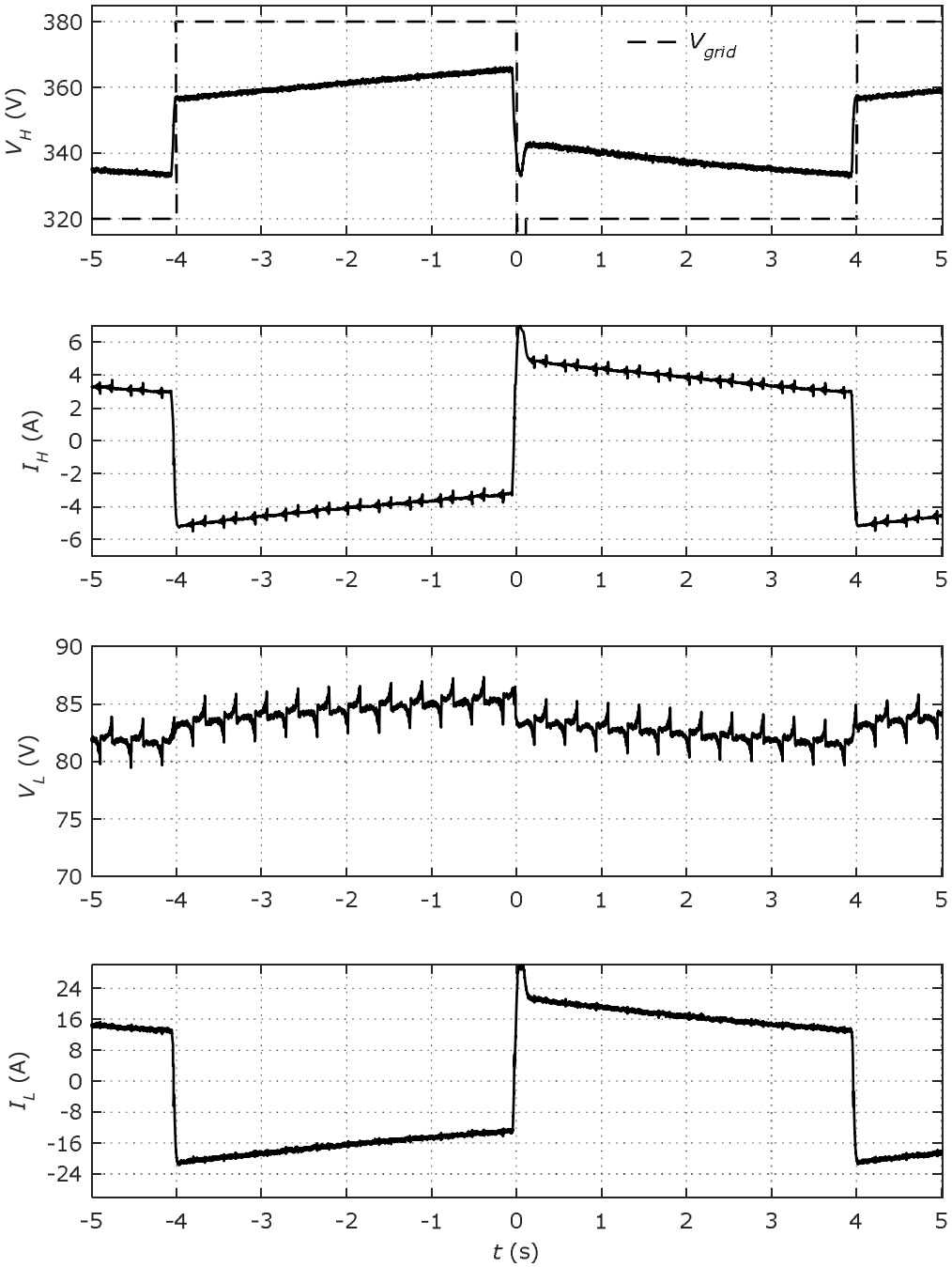

Fig. 7.22. Experimental waveforms for transient operation of the BHSC1, controlled by the VID: transition for V_{grid}=V_d±30V (+ voltage impulse at 0s), I_H≈±4 A, V_L≈83V, P_{in}≈±1.3kW, R_{droop}=4.4 Ω (V_L, V_H are the low and high voltage inputs, respectively, I_L, I_H are the low and high voltage side currents, respectively)

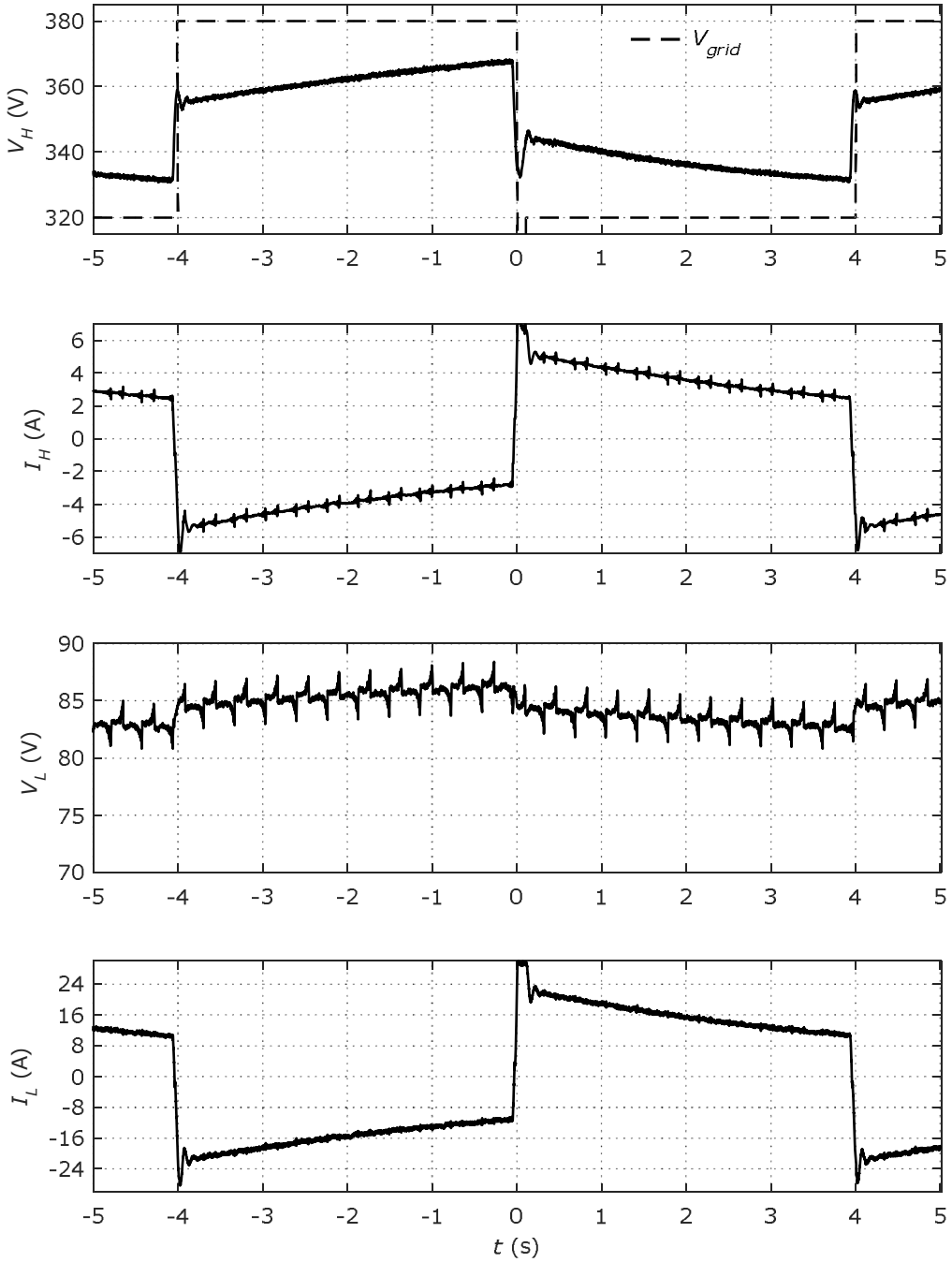

Fig. 7.23. Experimental waveforms for transient operation of the BHSC1, controlled by the NVID: transition for V_{grid}=V_d±30V (+ voltage impulse at 0s), I_H≈±4 A, V_L≈83V, P_{in}≈±1.3kW, R_{droop}=4.4 Ω(V_L, V_H are the low and high voltage inputs, respectively, I_L, I_H are the low and high voltage side currents, respectively)

7.5. Conclusions

This chapter presents an overview on the management energy strategies available for microgrid applications, with an emphasis on the decentralized, droop control methods.

Energy management strategies are considered for the charge/discharge control of supercapacitors, used in DC microgrid applications, and for this purpose two simple nonlinear characteristics for a droop control are analyzed. The nonlinear droop methods are considered as a simple alternative to the conventional centralized methods for supercapacitor storage.

The state-of-the-art virtual impedance methods are also considered, which offer good performance for decentralized methods. The virtual impedance method was improved by using a nonlinear characteristic for the filter, achieving the advantage of a variable influence of the storage system, based on the amplitude of grid voltage variation. In other words, a variable cutoff filter frequency was achieved with the benefit of having more parameters to be controlled by a higher, centralized energy management system, or different influences depending on the voltage variation on the grid when the system has this requirement.

8. Conclusions and Contributions

8.1. Conclusions

This thesis is focused on bidirectional DC-DC converters which achieve wide voltage conversion ratios by using hybrid capacitive or inductive switching cells, initially proposed for unidirectional topologies. Four topologies are thoroughly studied, from which 3 are proposed by the author. The studied schematics are two switched-capacitor topologies, one switched-inductor topology, and one combined switched-inductor and switched-capacitor topology.

The analysis of the hybrid converters is performed analytically in order to obtain their performance metrics: the energy required to be stored by the passive components, and the total active switch stress of the transistors.

An in-depth comparison is realized between the studied topologies and other 9 state-of-the-art structures that can be classified in the same category: wide ratio, non-isolated, without coupled inductors, with a reduced number of switches (≤6), requiring a simple driving scheme, utilizing two switching states and no multilevel or multiphase structures, as most structures can be upgraded to operate similarly. From this comparison it results that the hybrid converters achieve good performances, when compared to the rest of the topologies.

The dynamic analysis is performed for each topology, in order to assess its stability, to improve the converter design, and to design a stable controller. All topologies are tested with simulations for bidirectional operation with current controllers, while two topologies are extensively tested experimentally, obtaining similar results compared to the simulations. All proposed converters have a stable operation with current controllers.

Detailed experimental results are obtained from a switched-capacitor and a switched-inductor topology, the first being built with IGBTs and the latter built in two prototypes, one with conventional MOSFETs, and one with GaN-FETs in order to assess their performances and influences on the topology. Efficiency calculations were realized using a novel method and were compared to the experimental results. Not only that the GaN-FETs switches achieve a better efficiency, but also a reduction in the oscillations that might appear in the topology.

Methods for improving the schematics for each of the four topologies are presented, in order to eliminate common high frequency voltages between inputs, or to improve a topology in a multilevel structure.

Finally, the switched-capacitor topology is used as a platform for employing 3 new power sharing control strategies for supercapacitor storage in microgrid applications, proposed by the author.

8.2. Contributions

The following list summarizes the contributions of the author:

- General overview of supercapacitor storage in microgrid applications, their technologies, and benefits of wide-ratio converters for these applications.

- Literature review for bidirectional wide-ratio converters, that fall under the category of converters with wide voltage conversion ratio, with non-isolated structures, without coupled inductors, with reduced switch count (≤6), that use simple driving schemes (two switching states, without multilevel or multiphase operation), and with analytical descriptions of the topologies.
- Thorough analysis of a hybrid switched capacitor converter, with steady state and dynamic analysis, employing three different types of controllers: valley current mode control, an analog controller, and a digital controller. Experimental tests of the converter are validated through simulations. An improved topology is proposed in order to eliminate high frequency common voltage.
- A common ground bidirectional hybrid switched capacitor converter is proposed and analyzed in steady state and dynamic operation. The dynamic analysis is used as a means to study the stability of the topology and to improve it from the design of the passive components. A current controller was designed based on the dynamic analysis, and simulation results are used to validate the operation. Benefiting from the advantage of the common ground, an improved multilevel topology is proposed based on this structure.
- A bidirectional hybrid switched inductor converter is proposed and analyzed for steady state and dynamic operation. The dynamic model of the converter has a reduced order system while maintaining its wide conversion ratio. Based on the dynamic model, a digital current controller was designed. Two prototypes of the topology were built using conventional MOSFETs and wide-bandgap GaN-FETs, and their influence in the operation and efficiency was analyzed. Efficiency is calculated with a novel method and compared to experimental results. An improved topology is also proposed for this structure, and tested by means of digital simulation.
- A combined bidirectional hybrid switched-inductor and switched-capacitor converter is proposed, that achieves even wider conversion ratios. The converter is described analytically, from the steady state and dynamic analysis. The converter design is improved in terms of stability by using the dynamic analysis results, which are also used for the current controller design. Simulation results are used to confirm the performances of the topology. An improved topology is proposed in order to eliminate the high frequency voltage between inputs.
- A comprehensive comparison between the 4 studied converters and 9 state-of-the-art topologies is realized, in terms of step-down or step-up conversion ratios, total capacitive and inductive energy required in the converter, and total active switch stress.
- Three nonlinear droop power sharing methods are proposed and implemented in a bidirectional hybrid converter, for supercapacitor storage in a microgrid applications.

8.3. Future work

This work is focused on the hybrid topologies presented, and few paths are open for progress, such as:

- Testing in practical implementation the two hybrid topologies which are verified by simulation only, and the improved topologies presented for each of the four hybrid topologies.
- Advanced comparison methods can be developed in order to optimize the selection of a topology depending on the application. The comparison method can take into account components costs, efficiency, size, all parametrized on voltage and power levels.
- As most of the wide ratio converters are modeled dynamically by a higher order system, a better method than the conventional single current controller should be evaluated.
- The power sharing strategies can be improved and analyzed for their stability operation. The strategies can be upgraded and tested in a centralized system.
- New ways to improve the bidirectional hybrid topologies can be assessed, such as into multiphase, multilevel, or multi-input structures.

9. REFERENCES

[1] L. E. Zubieta, "Are Microgrids the Future of Energy?: DC Microgrids from Concept to Demonstration to Deployment," *IEEE Electrification Magazine*, vol. 4, no. 2, pp. 37–44, Jun. 2016, doi: 10.1109/MELE.2016.2544238.

[2] D. Schnitzer, D. S. Lounsbury, J. P. Carvallo, R. Deshmukh, J. Apt, and D. M. Kammen, "A critical review of best practices based on seven case studies," p. 120.

[3] A. Al-Hafri, H. Ali, A. Ghias, and Q. Nasir, "Transformer-less based solid state transformer for intelligent power management," in *2016 5th International Conference on Electronic Devices, Systems and Applications (ICEDSA)*, Dec. 2016, pp. 1–4, doi: 10.1109/ICEDSA.2016.7818507.

[4] R. P. Londero, A. P. C. de Mello, and G. S. da Silva, "Comparison between conventional and solid state transformers in smart distribution grids," in *2019 IEEE PES Innovative Smart Grid Technologies Conference - Latin America (ISGT Latin America)*, Sep. 2019, pp. 1–6, doi: 10.1109/ISGT-LA.2019.8895327.

[5] C. Liu, K. T. Chau, D. Wu, and S. Gao, "Opportunities and Challenges of Vehicle-to-Home, Vehicle-to-Vehicle, and Vehicle-to-Grid Technologies," *Proceedings of the IEEE*, vol. 101, no. 11, pp. 2409–2427, Nov. 2013, doi: 10.1109/JPROC.2013.2271951.

[6] S.-A. Amamra and J. Marco, "Vehicle-to-Grid Aggregator to Support Power Grid and Reduce Electric Vehicle Charging Cost," *IEEE Access*, vol. 7, pp. 178528–178538, 2019, doi: 10.1109/ACCESS.2019.2958664.

[7] F. M. Shakeel and O. P. Malik, "Vehicle-To-Grid Technology in a Micro-grid Using DC Fast Charging Architecture," in *2019 IEEE Canadian Conference of Electrical and Computer Engineering (CCECE)*, May 2019, pp. 1–4, doi: 10.1109/CCECE.2019.8861592.

[8] S. Kowal, A. Dhand, H. Khurana, A. Ahmad, and A. Emadi, "The Missing Health Link: How a transition to electrified vehicles may benefit more than just the environment," *IEEE Electrification Magazine*, vol. 7, no. 3, pp. 76–80, Sep. 2019, doi: 10.1109/MELE.2019.2925765.

[9] Y. Tahir, M. F. Nadeem, A. Ahmed, I. A. Khan, and F. Qamar, "A Review on Hybrid Energy Storage Systems in Microgrids," in *2020 3rd International Conference on Computing, Mathematics and Engineering Technologies (iCoMET)*, Jan. 2020, pp. 1–7, doi: 10.1109/iCoMET48670.2020.9073919.

[10] A. Etxeberria, I. Vechiu, H. Camblong, J. M. Vinassa, and H. Camblong, "Hybrid Energy Storage Systems for renewable Energy Sources Integration in microgrids: A review," in *2010 Conference Proceedings IPEC*, Oct. 2010, pp. 532–537, doi: 10.1109/IPECON.2010.5697053.

[11] V. A. Boicea, "Energy Storage Technologies: The Past and the Present," *Proceedings of the IEEE*, vol. 102, no. 11, pp. 1777–1794, Nov. 2014, doi: 10.1109/JPROC.2014.2359545.

[12] W. Jing, C. H. Lai, S. H. W. Wong, and M. L. D. Wong, "Battery-supercapacitor hybrid energy storage system in standalone DC microgrids: areview," *IET Renewable Power Generation*, vol. 11, no. 4, pp. 461–469, 2017, doi: 10.1049/iet-rpg.2016.0500.

[13] X. Chang, Y. Li, X. Li, and X. Chen, "An Active Damping Method Based on a Supercapacitor Energy Storage System to Overcome the Destabilizing Effect of Instantaneous Constant Power Loads in DC Microgrids," *IEEE Transactions on Energy Conversion*, vol. 32, no. 1, pp. 36–47, Mar. 2017, doi: 10.1109/TEC.2016.2605764.

[14] Y. Yan, Q. Li, W. Chen, B. Su, J. Liu, and L. Ma, "Optimal Energy Management and Control in Multimode Equivalent Energy Consumption of Fuel Cell/Supercapacitor of Hybrid Electric Tram," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 8, pp. 6065–6076, Aug. 2019, doi: 10.1109/TIE.2018.2871792.

[15] R. E. Araújo, R. de Castro, C. Pinto, P. Melo, and D. Freitas, "Combined Sizing and Energy Management in EVs With Batteries and Supercapacitors," *IEEE Transactions on Vehicular Technology*, vol. 63, no. 7, pp. 3062–3076, Sep. 2014, doi: 10.1109/TVT.2014.2318275.

[16] A. González, E. Goikolea, J. A. Barrena, and R. Mysyk, "Review on supercapacitors: Technologies and materials," *Renewable and Sustainable Energy Reviews*, vol. 58, pp. 1189–1206, May 2016, doi: 10.1016/j.rser.2015.12.249.

[17] G. Gautham Prasad, N. Shetty, S. Thakur, Rakshitha, and K. B. Bommegowda, "Supercapacitor technology and its applications: a review," *IOP Conf. Ser.: Mater. Sci. Eng.*, vol. 561, p. 012105, Nov. 2019, doi: 10.1088/1757-899X/561/1/012105.

[18] J. Schindall, "The Charge of the Ultracapacitors," *IEEE Spectrum*, vol. 44, no. 11, pp. 42–46, Nov. 2007, doi: 10.1109/MSPEC.2007.4378458.

[19] Poonam, K. Sharma, A. Arora, and S. K. Tripathi, "Review of supercapacitors: Materials and devices," *Journal of Energy Storage*, vol. 21, pp. 801–825, Feb. 2019, doi: 10.1016/j.est.2019.01.010.

[20] A. Berrueta, A. Ursúa, I. S. Martín, A. Eftekhari, and P. Sanchis, "Supercapacitors: Electrical Characteristics, Modeling, Applications, and Future Trends," *IEEE Access*, vol. 7, pp. 50869–50896, 2019, doi: 10.1109/ACCESS.2019.2908558.

[21] W. Zuo, R. Li, C. Zhou, Y. Li, J. Xia, and J. Liu, "Battery-Supercapacitor Hybrid Devices: Recent Progress and Future Prospects," *Advanced Science*, vol. 4, no. 7, p. 1600539, 2017, doi: 10.1002/advs.201600539.

[22] P. Liu, R. Lv, Y. He, B. Na, B. Wang, and H. Liu, "An integrated, flexible aqueous Zn-ion battery with high energy and power densities," *Journal of Power Sources*, vol. 410–411, pp. 137–142, Jan. 2019, doi: 10.1016/j.jpowsour.2018.11.017.

[23] Z. Zhao *et al.*, "An easily assembled boltless zinc–air battery configuration for power systems," *Journal of Power Sources*, vol. 458, p. 228061, May 2020, doi: 10.1016/j.jpowsour.2020.228061.

[24] A. Mitra, S. Jena, S. B. Majumder, and S. Das, "Supercapacitor like behavior in nano-sized, amorphous mixed poly-anion cathode materials for high power density lithium and other alkali-metal ion batteries," *Electrochimica Acta*, vol. 338, p. 135899, Apr. 2020, doi: 10.1016/j.electacta.2020.135899.

[25] J. Hou, W. Wang, P. Feng, K. Wang, and K. Jiang, "A surface chemistry assistant strategy to high power/energy density and cost-effective cathode for sodium ion battery," *Journal of Power Sources*, vol. 453, p. 227879, Mar. 2020, doi: 10.1016/j.jpowsour.2020.227879.

[26] A. Burke, "Ultracapacitors: why, how, and where is the technology," *Journal of Power Sources*, vol. 91, no. 1, pp. 37–50, Nov. 2000, doi: 10.1016/S0378-7753(00)00485-7.

[27] J. Zhang, Z. Shi, and C. Wang, "Effect of pre-lithiation degrees of mesocarbon microbeads anode on the electrochemical performance of lithium-ion capacitors," *Electrochimica Acta*, vol. 125, pp. 22–28, Apr. 2014, doi: 10.1016/j.electacta.2014.01.040.
[28] E. Lim *et al.*, "Facile Synthesis of Nb2O5@Carbon Core–Shell Nanocrystals with Controlled Crystalline Structure for High-Power Anodes in Hybrid Supercapacitors," *ACS Nano*, vol. 9, no. 7, pp. 7497–7505, Jul. 2015, doi: 10.1021/acsnano.5b02601.
[29] A. Brandt, A. Balducci, U. Rodehorst, S. Menne, M. Winter, and A. Bhaskar, "Investigations about the Use and the Degradation Mechanism of LiNi0.5Mn1.5O4 in a High Power LIC," *J. Electrochem. Soc.*, vol. 161, no. 6, p. A1139, May 2014, doi: 10.1149/2.105406jes.
[30] J. Ding *et al.*, "Peanut shell hybrid sodium ion capacitor with extreme energy–power rivals lithium ion capacitors," *Energy Environ. Sci.*, vol. 8, no. 3, pp. 941–955, Mar. 2015, doi: 10.1039/C4EE02986K.
[31] S. Peng, L. Li, H. B. Wu, S. Madhavi, and X. W. (David) Lou, "Controlled Growth of NiMoO4 Nanosheet and Nanorod Arrays on Various Conductive Substrates as Advanced Electrodes for Asymmetric Supercapacitors," *Advanced Energy Materials*, vol. 5, no. 2, p. 1401172, 2015, doi: 10.1002/aenm.201401172.
[32] H. Xu, X. Hu, H. Yang, Y. Sun, C. Hu, and Y. Huang, "Flexible Asymmetric Micro-Supercapacitors Based on Bi2O3 and MnO2 Nanoflowers: Larger Areal Mass Promises Higher Energy Density," *Advanced Energy Materials*, vol. 5, no. 6, p. 1401882, 2015, doi: 10.1002/aenm.201401882.
[33] H. Choi, M. Jang, M. Ciobotaru, and V. G. Agelidis, "Hybrid energy storage for large PV systems using bidirectional high-gain converters," in *2016 IEEE International Conference on Industrial Technology (ICIT)*, Mar. 2016, pp. 425–430, doi: 10.1109/ICIT.2016.7474790.
[34] Y. Song, J.-L. Xu, and X.-X. Liu, "Electrochemical anchoring of dual doping polypyrrole on graphene sheets partially exfoliated from graphite foil for high-performance supercapacitor electrode," *Journal of Power Sources*, vol. 249, pp. 48–58, Mar. 2014, doi: 10.1016/j.jpowsour.2013.10.102.
[35] H. Yang, S. Kannappan, A. S. Pandian, J.-H. Jang, Y. S. Lee, and W. Lu, "Graphene supercapacitor with both high power and energy density," *Nanotechnology*, vol. 28, no. 44, p. 445401, Oct. 2017, doi: 10.1088/1361-6528/aa8948.
[36] S. Zhang, X. Shi, R. Wróbel, X. Chen, and E. Mijowska, "Low-cost nitrogen-doped activated carbon prepared by polyethylenimine (PEI) with a convenient method for supercapacitor application," *Electrochimica Acta*, vol. 294, pp. 183–191, Jan. 2019, doi: 10.1016/j.electacta.2018.10.111.
[37] J. Cai *et al.*, "High-Performance Supercapacitor Electrode Materials from Cellulose-Derived Carbon Nanofibers," *ACS Appl. Mater. Interfaces*, vol. 7, no. 27, pp. 14946–14953, Jul. 2015, doi: 10.1021/acsami.5b03757.
[38] S. Ratha *et al.*, "Supercapacitors based on patronite–reduced graphene oxide hybrids: experimental and theoretical insights," *J. Mater. Chem. A*, vol. 3, no. 37, pp. 18874–18881, Sep. 2015, doi: 10.1039/C5TA03221K.
[39] M. Farhadi and O. Mohammed, "Energy Storage Technologies for High-Power Applications," *IEEE Transactions on Industry Applications*, vol. 52, no. 3, pp. 1953–1961, May 2016, doi: 10.1109/TIA.2015.2511096.
[40] E. Rodriguez-Diaz, F. Chen, J. C. Vasquez, J. M. Guerrero, R. Burgos, and D. Boroyevich, "Voltage-Level Selection of Future Two-Level LVdc Distribution Grids:

A Compromise Between Grid Compatibiliy, Safety, and Efficiency," *IEEE Electrification Magazine*, vol. 4, no. 2, pp. 20–28, Jun. 2016, doi: 10.1109/MELE.2016.2543979.

[41] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Switched-capacitor (SC)/switched inductor (SL) structures for getting hybrid step-down Cuk/Sepic/Zeta converters," in *2006 IEEE International Symposium on Circuits and Systems*, May 2006, pp. 4 pp.-, doi: 10.1109/ISCAS.2006.1693770.

[42] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Switched-Capacitor/Switched-Inductor Structures for Getting Transformerless Hybrid DC–DC PWM Converters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 2, pp. 687–696, Mar. 2008, doi: 10.1109/TCSI.2008.916403.

[43] T. Dragičević, X. Lu, J. C. Vasquez, and J. M. Guerrero, "DC Microgrids—Part II: A Review of Power Architectures, Applications, and Standardization Issues," *IEEE Transactions on Power Electronics*, vol. 31, no. 5, pp. 3528–3549, May 2016, doi: 10.1109/TPEL.2015.2464277.

[44] J. Ma, M. Zhu, X. Cai, and Y. W. Li, "Configuration and operation of DC microgrid cluster linked through DC-DC converter," in *2016 IEEE 11th Conference on Industrial Electronics and Applications (ICIEA)*, Jun. 2016, pp. 2565–2570, doi: 10.1109/ICIEA.2016.7604026.

[45] Y. Karimi, H. Oraee, M. S. Golsorkhi, and J. M. Guerrero, "Decentralized Method for Load Sharing and Power Management in a PV/Battery Hybrid Source Islanded Microgrid," *IEEE Transactions on Power Electronics*, vol. 32, no. 5, pp. 3525–3535, May 2017, doi: 10.1109/TPEL.2016.2582837.

[46] B. R. Naidu, G. Panda, and P. Siano, "A Self-Reliant DC Microgrid: Sizing, Control, Adaptive Dynamic Power Management, and Experimental Analysis," *IEEE Transactions on Industrial Informatics*, vol. 14, no. 8, pp. 3300–3313, Aug. 2018, doi: 10.1109/TII.2017.2780193.

[47] Q. Xu, C. Zhang, Z. Xu, P. Lin, and P. Wang, "A Composite Finite-Time Controller for Decentralized Power Sharing and Stabilization of Hybrid Fuel Cell/Supercapacitor System with Constant Power Load," *IEEE Transactions on Industrial Electronics*, pp. 1–1, 2020, doi: 10.1109/TIE.2020.2967660.

[48] Q. Li *et al.*, "A State Machine Control Based on Equivalent Consumption Minimization for Fuel Cell/ Supercapacitor Hybrid Tramway," *IEEE Transactions on Transportation Electrification*, vol. 5, no. 2, pp. 552–564, Jun. 2019, doi: 10.1109/TTE.2019.2915689.

[49] F. C. Dezza, V. Musolino, L. Piegari, and R. Rizzo, "Hybrid battery–supercapacitor system for full electric forklifts," *IET Electrical Systems in Transportation*, vol. 9, no. 1, pp. 16–23, 2019, doi: 10.1049/iet-est.2018.5036.

[50] ROHM Semiconductor, "Inductor Calculation for Buck converter IC." ROHM, 2012, [Online]. Available: http://rohmfs.rohm.com/en/products/databook/applinote/ic/power/switching_regulator/inductor_calculation_appli-e.pdf.

[51] He Li-gao and Wu Jian, "Selection of the current ripple ratio of converters and optimal design of output inductor," in *2010 5th IEEE Conference on Industrial Electronics and Applications*, Jun. 2010, pp. 1163–1167, doi: 10.1109/ICIEA.2010.5515878.

[52] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. Springer US, 2001.

[53] Y. Zhang, Q. Liu, J. Li, and M. Sumner, "A Common Ground Switched-Quasi-Z -Source Bidirectional DC–DC Converter With Wide-Voltage-Gain Range for

EVs With Hybrid Energy Sources," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 6, pp. 5188–5200, Jun. 2018, doi: 10.1109/TIE.2017.2756603.

[54] A. Ahmad, R. K. Singh, and R. Mahanty, "Bidirectional quadratic converter for wide voltage conversion ratio," in *2016 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, Dec. 2016, pp. 1–5, doi: 10.1109/PEDES.2016.7914538.

[55] H. Ardi, R. R. Ahrabi, and S. N. Ravadanegh, "Non-isolated bidirectional DC amp;#8211;DC converter analysis and implementation," *IET Power Electronics*, vol. 7, no. 12, pp. 3033–3044, 2014, doi: 10.1049/iet-pel.2013.0898.

[56] H. Ardi, A. Ajami, F. Kardan, and S. N. Avilagh, "Analysis and Implementation of a Nonisolated Bidirectional DC–DC Converter With High Voltage Gain," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 8, pp. 4878–4888, Aug. 2016, doi: 10.1109/TIE.2016.2552139.

[57] V. F. Pires, D. Foito, and J. F. Martins, "Bidirectional DC-DC converter with high voltage gain for the charge/discharge control of storage systems," in *2016 15th Biennial Baltic Electronics Conference (BEC)*, Oct. 2016, pp. 191–194, doi: 10.1109/BEC.2016.7743761.

[58] K. Filsoof and P. W. Lehn, "A Bidirectional Modular Multilevel DC–DC Converter of Triangular Structure," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 54–64, Jan. 2015, doi: 10.1109/TPEL.2014.2307004.

[59] Y. Zhang, Y. Gao, L. Zhou, and M. Sumner, "A Switched-Capacitor Bidirectional DC–DC Converter With Wide Voltage Gain Range for Electric Vehicles With Hybrid Energy Sources," *IEEE Transactions on Power Electronics*, vol. 33, no. 11, pp. 9459–9469, Nov. 2018, doi: 10.1109/TPEL.2017.2788436.

[60] S. Li, K. M. Smedley, D. R. Caldas, and Y. W. Martins, "Hybrid Bidirectional DC–DC Converter With Low Component Counts," *IEEE Transactions on Industry Applications*, vol. 54, no. 2, pp. 1573–1582, Mar. 2018, doi: 10.1109/TIA.2017.2785760.

[61] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Transformerless DC-DC converters with a very high DC line-to-load voltage ratio," in *Proceedings of the 2003 International Symposium on Circuits and Systems, 2003. ISCAS '03.*, May 2003, vol. 3, pp. III–III, doi: 10.1109/ISCAS.2003.1205049.

[62] H. Nomura, K. Fujiwara, and M. Y. Kochi, "A new DC-DC converter circuit with larger step-up/down ratio," in *2006 37th IEEE Power Electronics Specialists Conference*, Jun. 2006, pp. 1–7, doi: 10.1109/pesc.2006.1712228.

[63] Yan Zhang, Chaoyi Zhang, Jinjun Liu, and Yujie Cheng, "Comparison of conventional dc-dc converter and a family of diode-assisted dc-dc converter," in *Proceedings of The 7th International Power Electronics and Motion Control Conference*, Jun. 2012, vol. 3, pp. 1718–1723, doi: 10.1109/IPEMC.2012.6259095.

[64] Y. Zhang, J. Liu, and X. Ma, "Using RC type damping to eliminate right-half-plane zeros in high step-up DC-DC converter with diode-capacitor network," in *2013 IEEE ECCE Asia Downunder*, Jun. 2013, pp. 59–65, doi: 10.1109/ECCE-Asia.2013.6579074.

[65] O. Cornea, E. Guran, N. Muntean, and D. Hulea, "Bi-directional hybrid DC-DC converter with large conversion ratio for microgrid DC busses interface," in *Automation and Motion 2014 International Symposium on Power Electronics, Electrical Drives*, Jun. 2014, pp. 695–700, doi: 10.1109/SPEEDAM.2014.6872065.

[66] D. Hulea, N. Muntean, and O. Cornea, "Valley current mode control of a bi-directional hybrid DC-DC converter," in *2015 Intl Aegean Conference on Electrical*

Machines Power Electronics (ACEMP), 2015 Intl Conference on Optimization of Electrical Electronic Equipment (OPTIM) 2015 Intl Symposium on Advanced Electromechanical Motion Systems (ELECTROMOTION), Sep. 2015, pp. 274–279, doi: 10.1109/OPTIM.2015.7427024.

[67] O. Cornea, G. Andreescu, N. Muntean, and D. Hulea, "Bidirectional Power Flow Control in a DC Microgrid Through a Switched-Capacitor Cell Hybrid DC–DC Converter," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 4, pp. 3012–3022, Apr. 2017, doi: 10.1109/TIE.2016.2631527.

[68] C. Basso, *Switch-Mode Power Supplies Spice Simulations and Practical Designs*, 1 edition. New York: McGraw-Hill Professional, 2008.

[69] G. M. L. Chu, D. D. C. Lu, and V. G. Agelidis, "Practical application of valley current mode control in a flyback converter with a large duty cycle," *IET Power Electronics*, vol. 5, no. 5, pp. 552–560, May 2012, doi: 10.1049/iet-pel.2011.0225.

[70] N. Muntean, O. Cornea, O. Pelan, and C. Lascu, "Comparative evaluation of buck and hybrid buck DC-DC converters for automotive applications," in *2012 15th International Power Electronics and Motion Control Conference (EPE/PEMC)*, Sep. 2012, p. DS2b.3-1-DS2b.3-6, doi: 10.1109/EPEPEMC.2012.6397272.

[71] D. Hulea, N. Muntean, M. Gireada, and O. Cornea, "A Bidirectional Hybrid Switched-Capacitor DC-DC Converter with a High Voltage Gain," in *2019 International Aegean Conference on Electrical Machines and Power Electronics (ACEMP) 2019 International Conference on Optimization of Electrical and Electronic Equipment (OPTIM)*, Aug. 2019, pp. 289–296, doi: 10.1109/ACEMP-OPTIM44294.2019.9007160.

[72] F. S. Garcia, J. A. Pomilio, and G. Spiazzi, "Comparison of non-insulated, high-gain, high-power, step-up DC-DC converters," in *2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Feb. 2012, pp. 1343–1347, doi: 10.1109/APEC.2012.6165994.

[73] D. Hulea, N. Muntean, M. Gireada, O. Cornea, and E. Serban, "Bidirectional Hybrid Switched-Inductor Switched-Capacitor Converter Topology with High Voltage Gain," in *2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe)*, Sep. 2019, p. P.1-P.10, doi: 10.23919/EPE.2019.8915535.

[74] O. Cornea, O. Pelan, and N. Muntean, "Comparative study of buck and hybrid buck 'switched-inductor' DC-DC converters," in *2012 13th International Conference on Optimization of Electrical and Electronic Equipment (OPTIM)*, May 2012, pp. 853–858, doi: 10.1109/OPTIM.2012.6231912.

[75] I. Rezaei and M. Akhbari, "Transformerless hybrid buck converter with wide conversion ratio," in *2011 2nd Power Electronics, Drive Systems and Technologies Conference*, Feb. 2011, pp. 599–603, doi: 10.1109/PEDSTC.2011.5742489.

[76] L. Yang, T. Liang, and J. Chen, "Transformerless DC–DC Converters With High Step-Up Voltage Gain," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 8, pp. 3144–3152, Aug. 2009, doi: 10.1109/TIE.2009.2022512.

[77] E. Babaei, A. Mofidi, and S. Laali, "Calculation of switching current stress in high voltage gain boost dc-dc converter," in *2015 International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles (ESARS)*, Mar. 2015, pp. 1–6, doi: 10.1109/ESARS.2015.7101516.

[78] Y. Tang and T. Wang, "Study of An Improved Dual-Switch Converter With Passive Lossless Clamping," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 2, pp. 972–981, Feb. 2015, doi: 10.1109/TIE.2014.2341608.

[79] Y. Tang, D. Fu, T. Wang, and Z. Xu, "Analysis of Active-Network Converter With Coupled Inductors," *IEEE Transactions on Power Electronics*, vol. 30, no. 9, pp. 4874–4882, Sep. 2015, doi: 10.1109/TPEL.2014.2363662.

[80] H. Liu and F. Li, "A Novel High Step-up Converter With a Quasi-active Switched-Inductor Structure for Renewable Energy Systems," *IEEE Transactions on Power Electronics*, vol. 31, no. 7, pp. 5030–5039, Jul. 2016, doi: 10.1109/TPEL.2015.2480115.

[81] D. Hulea, B. Fahimi, N. Muntean, and O. Cornea, "High Ratio Bidirectional Hybrid Switched Inductor Converter Using Wide Bandgap Transistors," in *2018 20th European Conference on Power Electronics and Applications (EPE'18 ECCE Europe)*, Sep. 2018, p. P.1-P.10.

[82] D. Christen and J. Biela, "Analytical Switching Loss Modeling Based on Datasheet Parameters for mosfets in a Half-Bridge," *IEEE Transactions on Power Electronics*, vol. 34, no. 4, pp. 3700–3710, Apr. 2019, doi: 10.1109/TPEL.2018.2851068.

[83] D. Hulea, M. Gireada, D. Vitan, O. Cornea, and N. Muntean, "An Improved Bidirectional Hybrid Switched Inductor Converter," in *2020 22nd European Conference on Power Electronics and Applications (EPE '20 ECCE Europe)*, to be published.

[84] J. K. Jorgensen *et al.*, "Loss Prediction of Medium Voltage Power Modules: Trade-offs between Accuracy and Complexity," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2019, pp. 4102–4108, doi: 10.1109/ECCE.2019.8913066.

[85] A. B. Jørgensen, T.-H. Cheng, D. Hopkins, S. Beczkowski, C. Uhrenfeldt, and S. Munk-Nielsen, "Thermal Characteristics and Simulation of an Integrated GaN eHEMT Power Module," in *2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe)*, Sep. 2019, p. P.1-P.7, doi: 10.23919/EPE.2019.8915012.

[86] N. Fichtenbaum, M. Giandalia, S. Sharma, and J. Zhang, "Half-Bridge GaN Power ICs: Performance and Application," *IEEE Power Electronics Magazine*, vol. 4, no. 3, pp. 33–40, Sep. 2017, doi: 10.1109/MPEL.2017.2719220.

[87] Y. Du, X. Zhou, S. Bai, S. Lukic, and A. Huang, "Review of non-isolated bi-directional DC-DC converters for plug-in hybrid electric vehicle charge station application at municipal parking decks," in *2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Feb. 2010, pp. 1145–1151, doi: 10.1109/APEC.2010.5433359.

[88] A. A. Fardoun, E. H. Ismail, A. J. Sabzali, and M. A. Al-Saffar, "Bi-directional converter with low input/output current ripple for renewable energy applications," in *2011 IEEE Energy Conversion Congress and Exposition*, Sep. 2011, pp. 3322–3329, doi: 10.1109/ECCE.2011.6064217.

[89] C. Lai, Y.-C. Lin, and Y.-J. Lin, "Newly-constructed bidirectional DC/DC converter topology with high voltage conversion ratio for vehicle to DC-microgrid (V2DCG) system," in *2015 IEEE 2nd International Future Energy Electronics Conference (IFEEC)*, Nov. 2015, pp. 1–8, doi: 10.1109/IFEEC.2015.7361383.

[90] M. M. Chen and K. W. E. Cheng, "A new bidirectional DC-DC converter with a high step-up/down conversion ratio for renewable energy applications," in *2016 International Symposium on Electrical Engineering (ISEE)*, Dec. 2016, pp. 1–6, doi: 10.1109/EENG.2016.7845991.

[91] K. Tytelmaier, O. Husev, O. Veligorskyi, and R. Yershov, "A review of non-isolated bidirectional dc-dc converters for energy storage systems," in *2016 II*

International Young Scientists Forum on Applied Physics and Engineering (YSF), Oct. 2016, pp. 22–28, doi: 10.1109/YSF.2016.7753752.

[92] V. F. Pires, D. Foito, and A. Cordeiro, "Bidirectional boost/buck quadratic converter for distributed generation systems with electrochemical storage systems," in *2016 IEEE International Conference on Renewable Energy Research and Applications (ICRERA)*, Nov. 2016, pp. 879–884, doi: 10.1109/ICRERA.2016.7884462.

[93] K. K. Gokul, B. P. Emmanuel, S. Ashok, and S. Kumaravel, "Design and control of non-isolated bidirectional DC-DC converter for energy storage application," in *2017 2nd IEEE International Conference on Recent Trends in Electronics, Information Communication Technology (RTEICT)*, May 2017, pp. 289–293, doi: 10.1109/RTEICT.2017.8256603.

[94] P. S. Tomar, A. K. Sharma, and K. Hada, "Energy storage in DC microgrid system using non-isolated bidirectional soft-switching DC/DC converter," in *2017 6th International Conference on Computer Applications In Electrical Engineering-Recent Advances (CERA)*, Oct. 2017, pp. 439–444, doi: 10.1109/CERA.2017.8343370.

[95] E. Harmon, U. Ozgur, M. H. Cintuglu, R. de Azevedo, K. Akkaya, and O. A. Mohammed, "The Internet of Microgrids: A Cloud-Based Framework for Wide Area Networked Microgrids," *IEEE Transactions on Industrial Informatics*, vol. 14, no. 3, pp. 1262–1274, Mar. 2018, doi: 10.1109/TII.2017.2785317.

[96] N. Kanwar, N. Gupta, K. R. Niazi, and A. Swarnkar, "Optimal distributed resource planning for microgrids under uncertain environment," *IET Renewable Power Generation*, vol. 12, no. 2, pp. 244–251, 2018, doi: 10.1049/iet-rpg.2017.0085.

[97] D. E. Olivares *et al.*, "Trends in Microgrid Control," *IEEE Transactions on Smart Grid*, vol. 5, no. 4, pp. 1905–1919, Jul. 2014, doi: 10.1109/TSG.2013.2295514.

[98] S. Parhizi, H. Lotfi, A. Khodaei, and S. Bahramirad, "State of the Art in Research on Microgrids: A Review," *IEEE Access*, vol. 3, pp. 890–925, 2015, doi: 10.1109/ACCESS.2015.2443119.

[99] T. Dragičević, X. Lu, J. C. Vasquez, and J. M. Guerrero, "DC Microgrids—Part I: A Review of Control Strategies and Stabilization Techniques," *IEEE Transactions on Power Electronics*, vol. 31, no. 7, pp. 4876–4891, Jul. 2016, doi: 10.1109/TPEL.2015.2478859.

[100] L. Meng *et al.*, "Review on Control of DC Microgrids and Multiple Microgrid Clusters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 3, pp. 928–948, Sep. 2017, doi: 10.1109/JESTPE.2017.2690219.

[101] Z. Cheng, J. Duan, and M. Chow, "To Centralize or to Distribute: That Is the Question: A Comparison of Advanced Microgrid Management Systems," *IEEE Industrial Electronics Magazine*, vol. 12, no. 1, pp. 6–24, Mar. 2018, doi: 10.1109/MIE.2018.2789926.

[102] S. Peyghami, H. Mokhtari, and F. Blaabjerg, "Decentralized Load Sharing in a Low-Voltage Direct Current Microgrid With an Adaptive Droop Approach Based on a Superimposed Frequency," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 3, pp. 1205–1215, Sep. 2017, doi: 10.1109/JESTPE.2017.2674300.

[103] S. Peyghami, P. Davari, H. Mokhtari, and F. Blaabjerg, "Decentralized Droop Control in DC Microgrids Based on a Frequency Injection Approach," *IEEE Transactions on Smart Grid*, vol. 10, no. 6, pp. 6782–6791, Nov. 2019, doi: 10.1109/TSG.2019.2911213.

[104] J. Bryan, R. Duke, and S. Round, "Decentralized generator scheduling in a nanogrid using DC bus signaling," in *IEEE Power Engineering Society General Meeting, 2004.*, Jun. 2004, pp. 977-982 Vol.1, doi: 10.1109/PES.2004.1372983.
[105] J. Schonbergerschonberger, R. Duke, and S. D. Round, "DC-Bus Signaling: A Distributed Control Strategy for a Hybrid Renewable Nanogrid," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 5, pp. 1453–1460, Oct. 2006, doi: 10.1109/TIE.2006.882012.
[106] Q. Li, T. Wang, C. Dai, W. Chen, and L. Ma, "Power Management Strategy Based on Adaptive Droop Control for a Fuel Cell-Battery-Supercapacitor Hybrid Tramway," *IEEE Transactions on Vehicular Technology*, vol. 67, no. 7, pp. 5658–5670, Jul. 2018, doi: 10.1109/TVT.2017.2715178.
[107] M. Mokhtar, M. I. Marei, and A. A. El-Sattar, "An Adaptive Droop Control Scheme for DC Microgrids Integrating Sliding Mode Voltage and Current Controlled Boost Converters," *IEEE Transactions on Smart Grid*, pp. 1–1, 2018, doi: 10.1109/TSG.2017.2776281.
[108] J. Zhang, J. Ning, L. Huang, H. Wang, and J. Shu, "Adaptive droop control for accurate power sharing in islanded microgrid using virtual impedance," in *IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society*, Oct. 2017, pp. 2383–2388, doi: 10.1109/IECON.2017.8216401.
[109] X. Yu, X. She, X. Ni, and A. Q. Huang, "System Integration and Hierarchical Power Management Strategy for a Solid-State Transformer Interfaced Microgrid System," *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 4414–4425, Aug. 2014, doi: 10.1109/TPEL.2013.2289374.
[110] J. Hu, J. Duan, H. Ma, and M. Chow, "Distributed Adaptive Droop Control for Optimal Power Dispatch in DC Microgrid," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 1, pp. 778–789, Jan. 2018, doi: 10.1109/TIE.2017.2698425.
[111] S. M. Kaviri, H. Hajebrahimi, M. Pahlevani, P. Jain, and A. Bakhshai, "A hybrid adaptive droop control technique with embedded DC-bus voltage regulation for single-phase microgrids," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Oct. 2017, pp. 3359–3366, doi: 10.1109/ECCE.2017.8096604.
[112] P. Huang, P. Liu, W. Xiao, and M. S. E. Moursi, "A Novel Droop-Based Average Voltage Sharing Control Strategy for DC Microgrids," *IEEE Transactions on Smart Grid*, vol. 6, no. 3, pp. 1096–1106, May 2015, doi: 10.1109/TSG.2014.2357179.
[113] P. Wang, C. Jin, D. Zhu, Y. Tang, P. C. Loh, and F. H. Choo, "Distributed Control for Autonomous Operation of a Three-Port AC/DC/DS Hybrid Microgrid," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 2, pp. 1279–1290, Feb. 2015, doi: 10.1109/TIE.2014.2347913.
[114] A. Gupta, S. Doolla, and K. Chatterjee, "Hybrid AC amp;#x2013;DC Microgrid: Systematic Evaluation of Control Strategies," *IEEE Transactions on Smart Grid*, vol. 9, no. 4, pp. 3830–3843, Jul. 2018, doi: 10.1109/TSG.2017.2727344.
[115] R. M. Wright, "Understanding modern generator control," *IEEE Transactions on Energy Conversion*, vol. 4, no. 3, pp. 453–458, Sep. 1989, doi: 10.1109/60.43248.
[116] M. C. Chandorkar, D. M. Divan, and R. Adapa, "Control of parallel connected inverters in standalone AC supply systems," *IEEE Transactions on Industry Applications*, vol. 29, no. 1, pp. 136–143, Jan. 1993, doi: 10.1109/28.195899.
[117] Zhihong ye, D. Boroyevich, Kun Xing, and F. C. Lee, "Design of parallel sources in DC distributed power systems by using gain-scheduling technique," in

30th Annual IEEE Power Electronics Specialists Conference. Record. (Cat. No.99CH36321), Jul. 1999, vol. 1, pp. 161–165 vol.1, doi: 10.1109/PESC.1999.788997.

[118] P. Karlsson and J. Svensson, "DC bus voltage control for a distributed power system," *IEEE Transactions on Power Electronics*, vol. 18, no. 6, pp. 1405–1412, Nov. 2003, doi: 10.1109/TPEL.2003.818872.

[119] C. Quinn and P. Nikkel, "Droop Compensation Versus Ideal Regulation," *Power Electronics*, Nov. 01, 2004. https://www.powerelectronics.com/content/article/21854778/droop-compensation-versus-ideal-regulation (accessed May 17, 2020).

[120] M. Lee, D. Chen, K. Huang, C.-W. Liu, and B. Tai, "Modeling and Design for a Novel Adaptive Voltage Positioning (AVP) Scheme for Multiphase VRMs," *IEEE Transactions on Power Electronics*, vol. 23, no. 4, pp. 1733–1742, Jul. 2008, doi: 10.1109/TPEL.2008.924822.

[121] C.-J. Chen, D. Chen, C.-S. Huang, M. Lee, and E. K.-L. Tseng, "Modeling and Design Considerations of a Novel High-Gain Peak Current Control Scheme to Achieve Adaptive Voltage Positioning (AVP) for DC Power Converters," *IEEE Transactions on Power Electronics*, vol. 24, no. 12, pp. 2942–2950, Dec. 2009, doi: 10.1109/TPEL.2009.2021604.

[122] H.-H. Huang, C.-Y. Hsieh, J.-Y. Liao, and K.-H. Chen, "Adaptive Droop Resistance Technique for Adaptive Voltage Positioning in Boost DC–DC Converters," *IEEE Transactions on Power Electronics*, vol. 26, no. 7, pp. 1920–1932, Jul. 2011, doi: 10.1109/TPEL.2010.2095508.

[123] D. Hulea, O. Cornea, and N. Muntean, "Nonlinear droop charging control of a supercapacitor with a bi-directional hybrid DC-DC converter," in *2016 IEEE 16th International Conference on Environment and Electrical Engineering (EEEIC)*, Jun. 2016, pp. 1–6, doi: 10.1109/EEEIC.2016.7555540.

[124] F. Chen, R. Burgos, D. Boroyevich, and W. Zhang, "A nonlinear droop method to improve voltage regulation and load sharing in DC systems," in *2015 IEEE First International Conference on DC Microgrids (ICDCM)*, Jun. 2015, pp. 45–50, doi: 10.1109/ICDCM.2015.7152008.

[125] Q. T. T. Tran, H. Shehadeh, E. R. Sanseverino, S. Favuzza, and M. L. D. Silvestre, "Nonlinear droop control for minimum power losses operation in islanded microgrids," in *2017 IEEE International Conference on Environment and Electrical Engineering and 2017 IEEE Industrial and Commercial Power Systems Europe (EEEIC / I CPS Europe)*, Jun. 2017, pp. 1–5, doi: 10.1109/EEEIC.2017.7977874.

[126] P. Prabhakaran, Y. Goyal, and V. Agarwal, "Novel Nonlinear Droop Control Techniques to Overcome the Load Sharing and Voltage Regulation Issues in DC Microgrid," *IEEE Transactions on Power Electronics*, vol. 33, no. 5, pp. 4477–4487, May 2018, doi: 10.1109/TPEL.2017.2723045.

[127] F. Chen, R. Burgos, D. Boroyevich, J. C. Vasquez, and J. M. Guerrero, "Investigation of Nonlinear Droop Control in DC Power Distribution Systems: Load Sharing, Voltage Regulation, Efficiency, and Stability," *IEEE Transactions on Power Electronics*, vol. 34, no. 10, pp. 9404–9421, Oct. 2019, doi: 10.1109/TPEL.2019.2893686.

[128] Y. Gu, W. Li, and X. He, "Frequency-Coordinating Virtual Impedance for Autonomous Power Management of DC Microgrid," *IEEE Transactions on Power Electronics*, vol. 30, no. 4, pp. 2328–2337, Apr. 2015, doi: 10.1109/TPEL.2014.2325856.

[129] X. Zhao, Y. W. Li, H. Tian, and X. Wu, "Energy Management Strategy of Multiple Supercapacitors in a DC Microgrid Using Adaptive Virtual Impedance," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 4, pp. 1174–1185, Dec. 2016, doi: 10.1109/JESTPE.2016.2601097.

[130] Y. Zhang and Y. W. Li, "Energy Management Strategy for Supercapacitor in Droop-Controlled DC Microgrid Using Virtual Impedance," *IEEE Transactions on Power Electronics*, vol. 32, no. 4, pp. 2704–2716, Apr. 2017, doi: 10.1109/TPEL.2016.2571308.

[131] Q. Xu *et al.*, "A Decentralized Dynamic Power Sharing Strategy for Hybrid Energy Storage System in Autonomous DC Microgrid," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 7, pp. 5930–5941, Jul. 2017, doi: 10.1109/TIE.2016.2608880.

[132] D. Hulea, O. Cornea, and N. Muntean, "Energy Management Strategy for Supercapacitor Storage Using a Nonlinear Virtual Impedance," in *2018 IEEE 18th International Power Electronics and Motion Control Conference (PEMC)*, Aug. 2018, pp. 375–380, doi: 10.1109/EPEPEMC.2018.8521858.