DUAL INPUT DC-DC CONVERTERS FOR RENEWABLE ENERGY PROCESSING

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Abstract

The present thesis wishes to offer a possible solution to the problem of interconnecting two or more energy sources through a multi-input DC-DC converter. A brief presentation of the main multi-input DC-DC converters proposed in literature and a comparative study of them has been presented in the thesis. New dual input DC-DC converters with classical cell and hybrid inductor/ capacitors structures have been proposed. Analytical study, operating modes, simulation and experimental results have been included in the thesis. After a comparative study of the proposed converters one topology has been chosen and a complete description with boundary conduction mode analysis has been given. Finally an application with renewable energy sources has been proposed for the integration of the chosen converter. Operation strategy, system description and a adequate control strategy has been given. Two simulation have been carried out for the proposed system: a cosimulation between Matlab and Plecs for the specific study of the converter behavior, and a simulation only in Matlab for the experimental implementation of the system. A prototype of the system has been built and preliminary results are given. The proposed converter can be used in automotive industry for the interconnection of the multiple energy sources used for the automobils.

TABLE OF CONTENT

NOMENCLATURE

Abbreviations

AC	Alternating Current
ACL	AC load
ADC	Analog-To-Digital Converter
B	Battery
BCM	Boundary Conduction Mode
CAN	Controller Area Network
CCM	Continuous Conduction Mode
CMOS	Complementary Metal–Oxide–Semiconductor
CPU	Central Processing Unit
DBR	Diode Bridge Rectifier
DC	Direct Current
DCM	Discontinuous Conduction Mode
DSP	Digital Signal Processing
DR	Dumping Resistor
e.g.	For example
ECC	Energy Control Centre
EG	Electric Generator
EMCU	Energy Management Control Unit
EMI	Electromagnetic Interference
EV	Electric Vehicle
EPRI	Electric Power Research Institute
FLC	Fuzzy Logic Controller
HBC	Buck/ Hybrid Buck with switched capacitors C converter
HBCL	Hybrid Buck C/ Hybrid Buck L converter
HBL	Buck/ Hybrid Buck with switched inductors L converter
HBLC	Hybrid Buck L/ Hybrid Buck C converter
IGBT	Insulated-Gate Bipolar Transistor
IV	PV panel Current Voltage curve
MIC	Multi-Input Converter
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
MPP	Maximum Power Point

MPPT	Maximum Power Point Tracking
PCB	Printed Circuit Board
PCSC	Pulsating Current Source Cell
PFM	Power Flow Management
PM	Permanent Magnet
PR	Power Regulation
PV	Photovoltaic
PVSC	Pulsating Voltage Source Cell
PWM	Pulse Width Modulation
RG	Switch
SG	Synchronous Generator
SOC	State Of Charge
TELECOM	Telecommunications
TTL	Transistor–transistor logic
UC	Ultracapacitor
USA	United States of America
WPVS	Wind and PV energy generation system
ZVS	Zero Voltage Switching

Symbols

A	Exponential voltage from the battery model [V]
A_C	Cross-sectional area from the transformer [mm^2]
B	Exponential capacity used from the battery model[$(Ah)^{-}$]
C, C_1, C_2, C_3	Converter topologies capacitors [μF]
C_4, C_5, C_6	Converter topologies capacitors [μF]
C_P	Wind turbine power coefficient
d, d_1, d_2	Converter topologies duty cycles [%]
D_1, D_2, D_3, D_4	Converter topologies diodes
D_5, D_6, D_7, D_8	Converter topologies diodes
D_9, D_{10}, D_{11}, D_{12}	Converter topologies diodes
E_0	Constant voltage from the battery model[V]
E_{Batt}	Nonlinear voltage from the battery model[V]
Exp(s)	Exponential zone dynamics from the battery model[V]
f	Switching frequency [kHz]
F1	Short-circuit fuse protection from the renewable energy system
F_T	Magnetomotive force of the coupled transformers [Nm]
i	Battery current from the battery model[A]
i*	Low frequency current dynamics from the battery model[A]
I'_L	Demanded current from the AC loads reflected to the DC bus side [A]
i_0	Output current of the battery model[A]
i_1, i_2	Converters input sources current [A]

I_B	Battery current [A]
I_{bat_ch}	Charging battery bank current [A]
I_{bat_dis}	Battery discharging current [A]
i_C	Capacitor current [A]
I_{D1}	PV panel first diode current [A]
I_{D2}	PV panel second diode current [A]
I_{EG}	Electric generator current [A]
I_{Gin}	Injected current into the grid [A]
I_{Gout}	Input current from the grid [A]
I_{HBLC}	Output current of the HBLC [A]
I_{in1}	Wind turbine current [A]
I_{in2}	PV panel current [A]
i_L, i_{L1}, i_{L2}	Converter topologies inductor currents [A]
I_{lim}, $I_{L1,lim1}$, $I_{L1,lim2}$	Limit values of the inductor L_1 current [A]
$I_{L1,A1}$, $I_{L1,B1,}$ $I_{L1,C1}$	Average values of the inductor L_1 current in the case $d_1>d_2$ [A]
$I_{L1,A2}$, $I_{L1,B2,}$ $I_{L1,C2}$	Average values of the inductor L_1 current in the case $d_1\leq d_2$ [A]
$I_{lim,pu}$	Relative values of the limit inductor current
$I_{lim,pu,max}$	Maximum value of the relative limit current
I_{max_ch}	Maximum charging current for the battery bank (according to the SOC) [A]
I_{max_dis}	Maximum discharging current for the battery bank (according to the SOC) [A]
I_{mp}	Maximum power point current [A]
I_{out}	Wind-PV panel system output current [A]
I_{PV}	PV panel current [A]
I_{ph}	Solar-induced current to the PV panel [A]
I_{ph0}	Measured solar-generated current of the PV panel [A]
I_{REF_PV}	Reference current for the PV panel [A]
I_{rr}	Irradiation [W/m^2]
I_{rr0}	Initial irradiation of the PV panel [W/m^2]
I_s	Saturation current of the first diode from the PV panel model[A]
i_{S1}, i_{S2}	Converter topologies power switches current [A]
I_{s2}	Saturation current of the second diode from the PV panel model [A]
I_{sc}	Short circuit current of the PV panel[A]
it	Extracted capacity from the battery model[Ah]
I_{T1}, I_{T2}	Primary winding currents of the transformer[A]
I_{UC}	Ultracapacitor current [A]
k	Ratio of the two input voltages [V]
k_p	Boltzmann constant
k_{opt}	Optimum coefficient for MPP determination of the wind turbine
K	Polarization constant [Ah^{-1}] or Polarization resistance [Ω] of the battery model
l_m	Magnetic length path of the transformer [mm]

L, L_1, L_2, L_3, L_4	Converter topologies inductors [μH]
L_{T1}, L_{T2}	Transformer windings inductance [μH]
N, N_2	Quality factor from the PV panel
n_1, n_2, n_3	Windings turns number of the transformer
P_1, P_2	Converters input powers [kW]
P_{link}	Load demanded power proportional to the link [W]
P_m	Mechanical power of the wind turbine[kW]
P_o	Converter output power [kW]
P_w	Wind power [kW]
Q	Maximum battery capacity from the battery model[Ah]
R	Converters resistance [Ω]
R_p	PV panel parallel resistance [Ω]
R_S	PV panel series Resistance [Ω]
R_t	Turbine blade radius [rad]
S_1, S_2, S_3, S_4	Converter topologies power switches
S_5, S_6, S_7, S_8	Converter topologies power switches
Sel(s)	Represents the battery mode: Sel(s) = 0 during battery discharge, Sel(s) = 1 during battery charging.
T	Power switches period[μs]
t, t_0, t_1, t_2	Converter times [μs]
T_1, T_2, T_3	Transformer windings
t_3, t_4, t_5, t_6	Converter times [μs]
t_{off}	Time period when the power switch is off [μs]
t_{on}	Conduction time [μs]
V	PV panel voltage from the model [V]
V_1, V_2	Converters input sources voltage [V]
v_C, v_{C1}, v_{C2}	Converters capacitors voltage [V]
v_{D1}, v_{D2}	Converters diodes voltage [V]
v_{gS1}, v_{gS2}	Power switches gate signal of the converters[V]
V_i	Converter input voltage [V]
v_L, v_{L1}, v_{L2}	Converter inductor voltage [V]
V_{link}	Converter DC link voltage [V]
V_o, V_{out}	Converters output voltage [V]
V_{oc}	Open circuit voltage
v_{S1}, v_{S2}	Converters power switches voltage [V]
V_t	Thermal voltage [V]
P_{MPP}	Maximum power point [W]
P_w	Wind power [kW]
P_{wind}	Wind turbine nominal power [W]
P_{PV}	PV panel power [W]

Greek Symbols

μ	Magnetic permeability [H/m]
Φ_1, Φ_2	Magnetic fluxes [Wb]
Θ_1, Θ_2	Phase shifts [rad]
v_r	Wind speed [m/s]
ω_r	Rotating speed [rpm]
λ	Tip-speed ratio
ρ	Air density [kg/m^3]
φ	Phase delay between the two duty cycles
π	pi

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CHAPTER 1
Introduction

1.1. Motivation

Energy technology is a main concern in a present, modern economy.

Energy sources are classified in two groups: nonrenewable and renewable.

Most of our energy comes from nonrenewable sources: oil, petroleum, natural gas, propane, and uranium. The main functions of them are to produce electricity or heat, to move our cars, and to manufacture all kinds of products.

Renewable energy sources are geothermal, biomass, hydropower, solar, and wind potential.

Figure 1.1 presents the global energy generation scenario in nowadays [1.1].

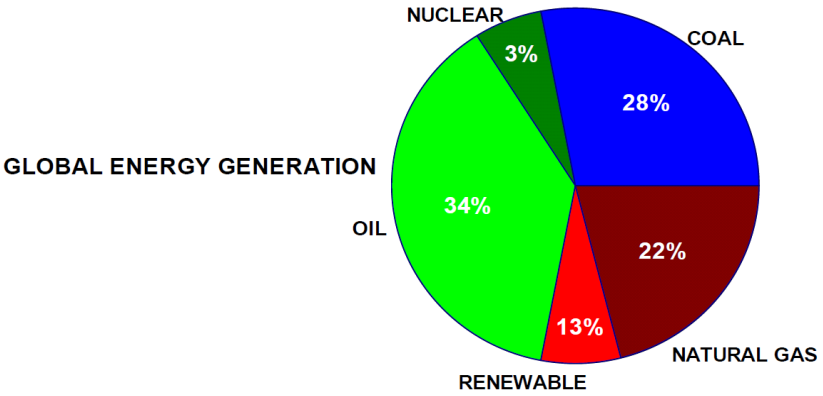

Figure 1.1. Global energy generation scenario.

According to EPRI (Electric Power Research Institute) statistics in 2011, only in USA 70% of electrical energy flows through power electronics [1.1, 1.2]. Prediction in this field says that soon 100% of the electrical energy transfer will be made through power electronics.

T. G. Wilson gives in [1.3] the following definition: "Power electronics is the technology associated with the efficient conversion, control and conditioning of electric power by static means, from its available input form into the desired electrical output forms". A block diagram with the place of power converters, in an energy flow, is presented in figure 1.2 [1.4]. The controller consists of linear integrated circuits and/or a digital signal processors. The evolution of power electronics devices has improved the voltage and current handling capabilities and the switching speed of power semiconductor devices.

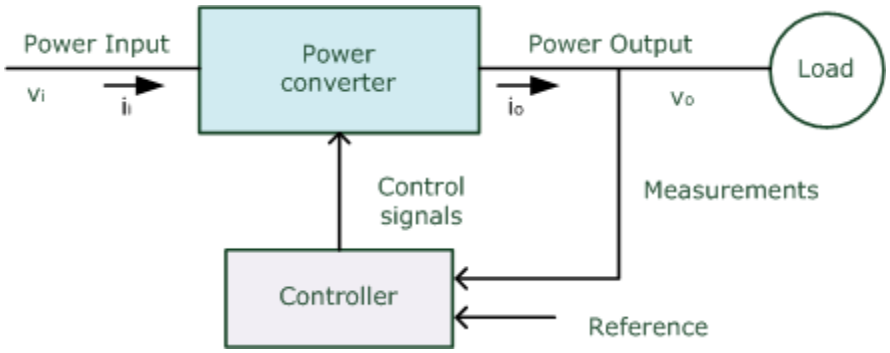

Figure 1.2. The place of a power converter.

In a DC-DC power converter the input voltage is converted to an output voltage having a larger or smaller magnitude, possible with opposite polarity or isolated (decoupled between sources, distribution system and loads) from the input side.

The DC-DC power converter can have common negative or common positive input and output terminals. Fixed and adjustable output voltage of the converter can be achieved with PWM techniques.

Common requirements of most power converters are: high efficiency, power density, and reliability at lower possible costs.

Renewable energy is based on sources that fluctuate during the course of any given day or season. Distributed energy resources systems are small-scale power generation technologies (typically in the range of 3 kW to 10,000 kW) used to provide an alternative to or an enhancement of the traditional electric power system. Their input sources can be of different types (e.g. renewables, conventional, storage) and interconnected to provide the needed flexibility and reliability [1.5, 1.6].

The next level is a microgrid, a discrete energy system consisting of distributed energy sources and loads capable of operating in parallel with, or independently from, the main grid [1.7-1.9]. The input energy and the loads need to be managed in order to obtain maximum efficiency and reliability. This is possible by using power converters associated with intelligent control.

1.2. The thesis outline

In this thesis dual input DC-DC converters with different topologies are proposed, studied analytically, with digital simulations, and validated through experiments. Then, a mixed photovoltaic and wind power generation system is analyzed, as application of the proposed converters.

The content of the next chapters is:

Chapter *two* is a review of the multi-input DC-DC converters and systems configurations, proposed in literature. A short description is given for each type and corresponding systems are evaluated.

Chapter *three* proposes different hybrid, dual input DC-DC converters topologies, with switched capacitors or/and switched inductors cell. The main structures are analytically studied and digital simulations are given. Experimental results validate the simulation for these types of converters.

One structure has been chosen, due to its advantages, and in chapter *four* a complete description with analytical study, operating modes, design parameters and boundary conduction operating mode analysis is given. The digital simulation results are validated by experiments obtained from a prototype.

The next step consists in the integration of the dual-input DC-DC converter into an application. Chapter *five* presents a mixed wind and photovoltaic energy conversion system, which includes the proposed converter, with all needed control strategies regarding the energy management. Operation strategy is given for on-grid and, especially, for off-grid connection. Extended digital simulations and preliminary experimental results validate the proposed control strategies, and open future work directions.

In chapter *six* the platform used for testing the prototypes, built for this scope, is briefly described.

The thesis ends with chapter *seven,* which summarizes the work in terms of conclusions. Original contributions of the author and future work are presented, too.

1.3. The thesis objectives

- to make a review of the main multi-input DC-DC converters and systems, developed in the literature;
- to present the main methods to generate multi-input DC-DC converters;
- to propose dual-input DC-DC converter topologies based on hybrid structures;
- to study analytically, and through digital simulation, the proposed converters;
- to build and test laboratory prototypes in order to validate the theoretical results;
- to integrate one of the proposed converter into a wind turbine and PV mixing energy system, and to propose an adequate control strategy studied with digital simulations;
- to presents some preliminary experimental results obtained with the proposed system.

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CHAPTER 2
Multi-Input DC-DC Converters and Systems – A General Review

2.1. Introduction

Different methods to generate multi input DC-DC converters and their constraints have been presented in literature [2.1-2.13]. The main methods consist in synthesizing DC-DC converters in multiple input converters [2.1-2.9], in interfacing input sources through a forward-conducting-bidirectional-blocking switch [2.10-2.12], in mixing several input DC sources by means of a DC link [2.30] or mixing them in "magnetic form" [2.39].

Several solutions and their control have been proposed in the literature if more than one DC source is used to feed the loads [2.14-2.58]. We make distinction between multi-input DC-DC converters and multi-input DC-DC systems.

Multi-input DC-DC converters are obtained from DC-DC converters coupled in a manner that does not permit the independent control of each one. There is only one output filter and one control system. The energy flow management unit is superposed on the control system of the converter.

Multi-input DC-DC systems, on the other hand, contain two or more DC-DC converters which can operate independently. There is one distinct energy management system that deals with the control of energy flow from the input sources to the load or from the load to the input, if at least one converter is bidirectional.

It is expected that the importance of multi-input converters and systems will grow in the future especially due to the integration of the renewable energy sources in many domains.

The multi-input DC-DC converters are used in many applications, like:

- renewable energy generation system (wind-PV-battery, wind-PV-fuel cell, PV-PV-battery, etc.) [2.16-2.18, 2.22, 2.25, 2.35, 2.46];
- automotive industry: to mix the power flowing from combined on-board energy sources [2.23, 2.32, 2.32, 2.47];
- systems which combines a fuel cell, a supercapacitor and the load with galvanic isolation between [2.42];
- coupling reactors for EV scooter traction AC drive [2.50];
- a fuel cell powered laptop [2.51];
- micro-grid based telecom power system [2.52];
- energy harvesting of the wireless body area network in heal care or telemedicine [2.53].

This chapter is an overview of the multi-input DC-DC converters and systems main topologies described in the literature. Synthesizing methods, circuit configurations, typical waveforms, and brief analytical descriptions are presented.

2.2. Synthesizing of multi-input DC-DC converters

A method to develop multi-input, PWM, DC-DC converters (MIC) is to add an extra pulsating voltage or current source to a classic DC-DC converter [2.1-2.4]. Two basic circuits, with different types of sources, are defined as the building cells, and used to generate MICs. One is the pulsating voltage source cell (PVSC) which consists of pulsating voltage source with a diode in parallel (figure 2.1.a) and the other one is the pulsating current source cell (PCSC) made from a pulsating current source in series with a diode (figure 2.2.a).

PVSC's can be connected only in series with one of the branches of a PWM converter for developing MIC. In figure 2.1 is presented the topologies of PVSC: Buck type (figure 2.1.b), Cuk type (figure 2.1.c), and Zeta type (figure 2.1.d).

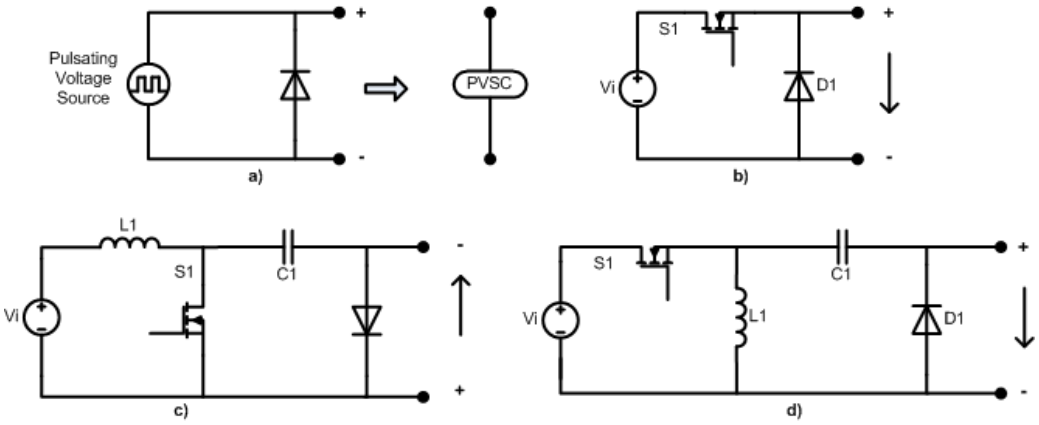

Figure 2.1. Circuit configurations for PVSC.

To insert a PCSC into a PWM converter to develop a MIC, the cell must be connected in series. Figure 2.2. presents the topologies for the PCSC: Boost type (figure 2.2.b), Buck-Boost type (figure 2.2.c) and SEPIC type (figure 2.2.d).

The rules to synthesizing MIC with PVSC are presented below:

- When a PVSC is introduced in the energy buffer zone of a classic PWM converter, it must be connected in series with a current buffer and have the current flow of the connected current buffer flowing out its positive end;
- When a PVSC is inserted into the output zone of a classic PWM converter, it must be connected in series with a current sink and have the current flow of the connected current sink flowing out its positive end;
- A PVCS must form a mesh with an output sink;

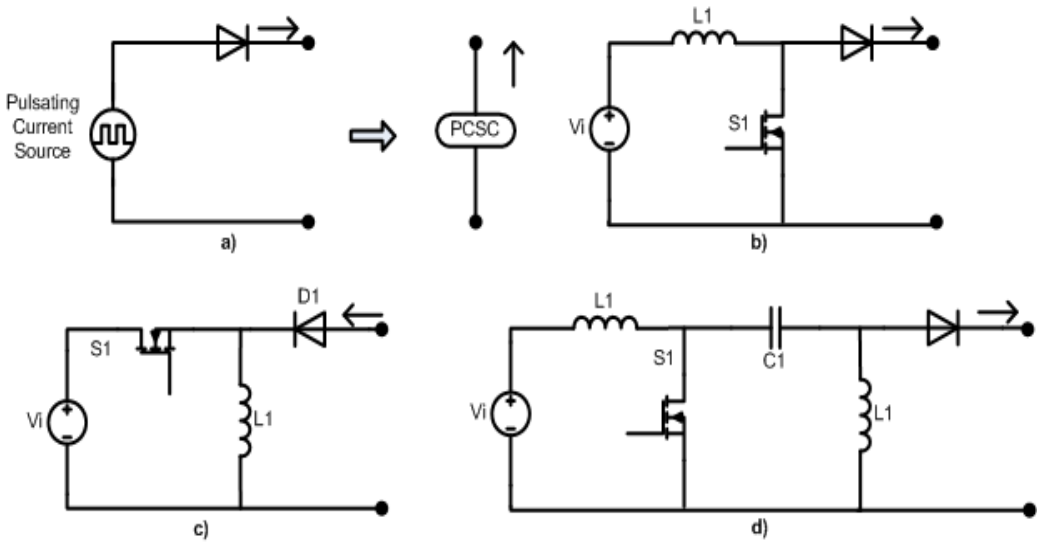

Figure 2.2. Circuit configurations for a PCSC.

The rules to connect a PCSC to a classic PWM converter to obtain MIC are described in the following:

- When PCSC is introduced in the energy buffer zone of a classic PWM converter, it must be connected in parallel with a voltage buffer and its out-going current terminal must tie to the positive end of the voltage buffer;
- When PCSC is inserted in the output zone of a classic PWM converter, it must be connected across a voltage sink with its outgoing current terminal tied to the positive end of the voltage sink;
- PCSC must form a mesh with an output sink.

To generate MIC with PVSC the next steps must be chosen:

- Step 1: PVSC topology from figure 2.1 must be chose;
- Step 2: one of the basic PWM topologies, which contains the current buffers or the current sink must be selected;
- Step 3: the chosen PVSC must be insert in the selected basic PWM converter according to the presented rules;
- Step 4: it must be verified if the inserted PVSC forms a mesh with an output sink.

Dual input integrated Buck/Buck and Buck/Buck-Boost converters where obtained with this approach.

Similarly, can be obtained a multi-input converter with PCSC by following the next steps:

- Step 1: PCSC topology from the figure 2.2 must be chosen;
- Step 2: one of the basic PWM topologies, which contains the voltage buffer or the voltage sink must be selected;
- Step 3: the chosen PCSC must be insert in the selected basic PWM converter according to the presented rules;

Step 4: iIt must be verified if the inserted PCSC forms a mesh with an output sink.

Three types of multi-input DC-DC converters are more often presented in the literature [2.13-2.27]:

- Dual-input integrated Buck/Buck-Boost converter;
- Dual-input integrated Buck/Buck converter;
- Dual-input integrated Buck-Boost/Buck-Boost Converter.

Each of these topologies is obtained integrating two DC-DC converters in one unit that has a single output filter and a single control system.

The number of power switching devices is equal to the sum of the integrated converter devices: two power transistors and two diodes. If each power switch and diode is replaced with an anti-parallel switch-diode pair, the multi-input converter will be bidirectional, allowing power transfer in both directions.

The MICs presented in this section are limited at two input sources, in order to simplify the steady-state analysis. More input sources can be added to the integrated converters, conforming to the rules mentioned above.

2.3. The integrated Buck/Buck converter

The integrated Buck/Buck converter is presented in figure 2.3. The input sources can provide power to the load simultaneously or individually [2.14-2.19].

The DC-DC converter has four operating modes, which are described below:

- **Mode I**: The switch S_1 is on and the switch S_2 is off. The energy demanded by the load is provided by the voltage source V_1 through the inductor L;
- **Mode II**: The switch S1 is off and the switch S_2 is on. The voltage source S_2 provides the power to the load through the inductor L;
- **Mode III**: Both power switches, S_1 and S_2, ore off. The magnetic energy stored in inductor L from the time when the energy was provided by the voltage sources is now released to the load
- **Mode IV**: Both switches, S_1 and S_2, are on. The voltage sources, V_1 and V_2, supply the demanded power to the load. They are connected in series.

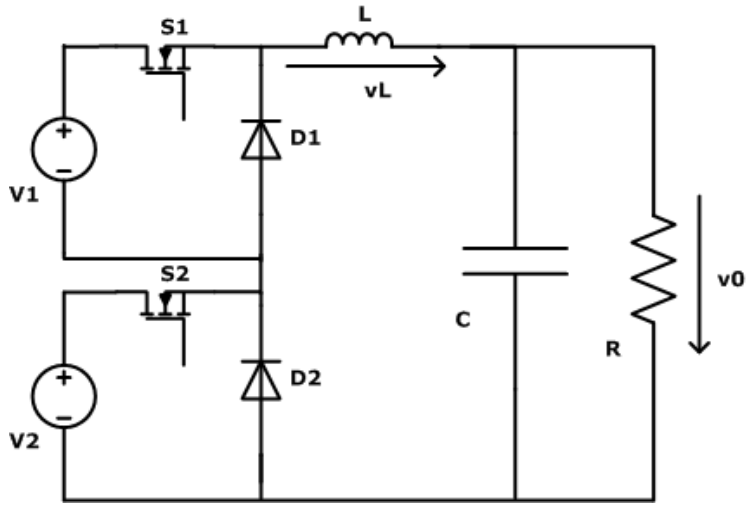

Figure 2.3. The topology of the integrated Buck/Buck converter.

The switches, S_1 and S_2, are operated with different on and off times, at the same switching frequency. Figure 2.4. presents the typical waveforms of the

converter: the S_1 and S_2 gate signals, the voltage across the inductor L, the inductor current, the S_1 and S_2 currents, and the unfiltered output current.

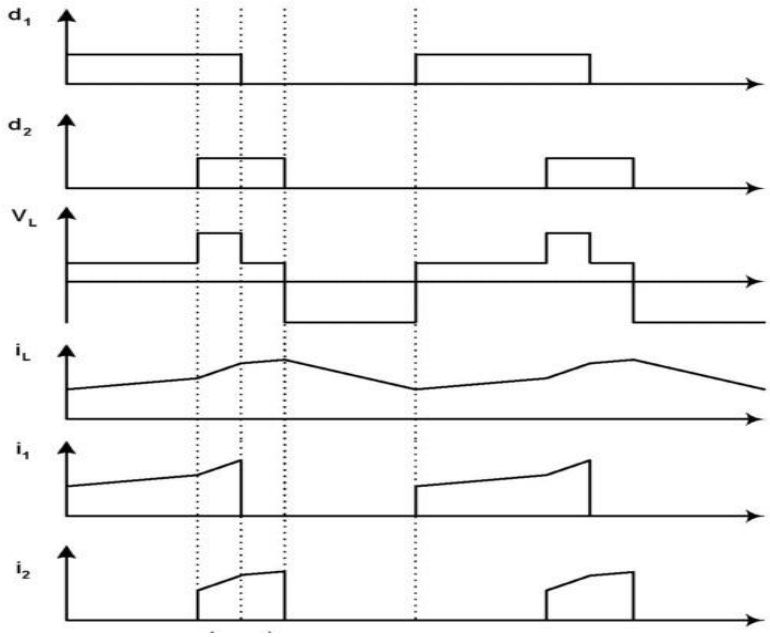

Figure 2.4. Typical waveforms of the integrated Buck/Buck converter.

Table.2.1. presents the voltage across the inductor L_1 for all four-operation modes.

Table.2.1. Voltage across the inductor in one period (for the integrated Buck/Buck converter)

	Mode I	**Mode II**	**Mode III**	**Mode IV**
S_1	1	0	1	0
S_2	0	1	1	0
V_L	V_1-V_0	V_2-V_0	V_1+V_2-V_0	-V_0

The output voltage is given by equation (2.1)

$$V_0 = d_1 V_1 + d_2 V_2 \tag{2.1}$$

where d_1 is the duty cycle of switch S_1 and d_2 is the duty cycle of switch S_2.

2.4. The integrated Buck/Buck-Boost converter

The circuit diagram of the double input integrated Buck/Buck-Boost converter is shown in figure 2.5. The voltage sources V_1 and V_2 can draw power to the load individually or simultaneously depending on the gate signals of the two power switches [2.14-2.16, 2.20-2.24].

By applying the PWM control to the switches S_1 and S_2, the converter has four different modes of operation:

- **Mode I**: The power switch S_1 is on and S_2 is off. The energy is provided to the load by the voltage source V_1 through the inductor L;
- **Mode II**: The power switch S_1 is off and S_2 is on. The voltage source V_2 charges the inductor L, while output capacitor C supplies the load;
- **Mode III**: Both power switches, S_1 and S_2, are off. The load is supplied from the energy stored in the inductor L and the capacitor C;
- **Mode IV**: Both power switches, S_1 and S_2, are on. The voltage sources V_1 and V_2 are working simultaneously and charging the inductor. The power for the load is provided by the capacitor C.

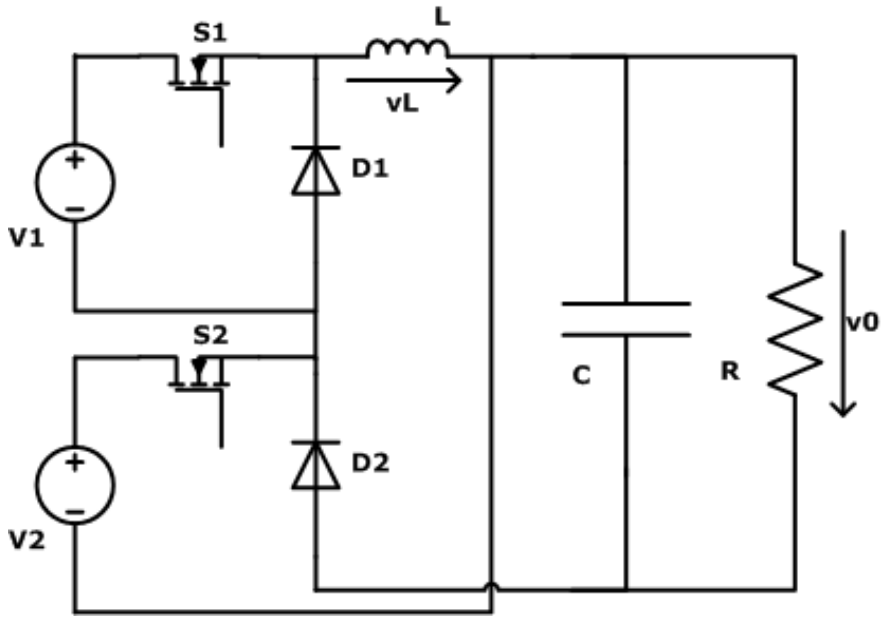

Figure 2.5. The topology of the Integrated Buck/Buck-Boost converter.

The switches S_1 and S_2 are driven at the same frequency. The signals can be synchronized at turn-on, or turn-off time. Figure 2.6. presents the gate signals (synchronized at turn-off time) and the main voltage and current waveforms of the converter: the inductor voltage and current, the input, output, and the capacitor currents.

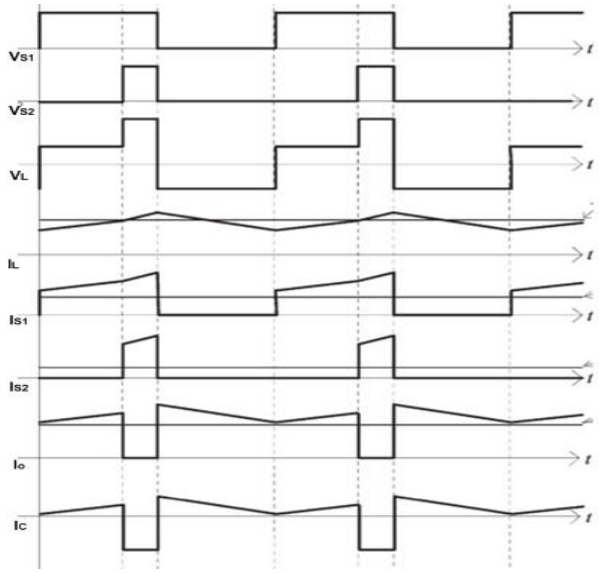

Figure 2.6. Waveforms of the main voltages and currents of the Buck/Buck-Boost converter.

Table.2.2. presents the voltage across the inductor L_1 for all four operation modes of the integrated Buck/Buck-Boost converter.

Table.2.2. Voltage across the inductor in one period (for the integrated Buck/Buck-Boost converter)

	Mode I	**Mode II**	**Mode III**	**Mode IV**
S_1	1	0	1	0
S_2	0	1	1	0
V_L	V_1-V_0	V_2	V_1+V_2	-V_0

The output voltage was obtained by applying the volt-second balance theorem and is given by equation (2.2), where d_1 is the duty cycle of the switch S_1, and d_2 is the duty cycle of the switch S_2:

$$V_0 = \frac{d_1}{1-d_1}V_1 + \frac{d_2}{1-d_2}V_2 \tag{2.2}$$

The power transfer from each input voltage source to the load can be controlled or undetermined. Taking into account this, the converter can work in three different cases:

- Case I: the load consumes the needed power, the voltage source V_1 supplies a limited power, and it is the main power source, the voltage source V_2 provides the rest of the demanded power;

- Case II: the voltage source V_2 supplies limited power and the voltage source V_1 provides the remained power demanded by the load;
- Case III: The load absorbs the power supplied by both voltage sources, both input currents are controlled, both voltage sources can always deliver their maximum power to the load.

By adding a passive soft switching cell, the switching loss of the power switches S_1 and S_2 will be reduced, and the converter efficiency will be improved. Figure 2.7. shows a double-input DC-DC converter with soft-switching cell [2.21].

The converter is proposed as a DC-DC unit for a grid-connected hybrid photovoltaic/wind power system followed by a full bridge DC-AC inverter.

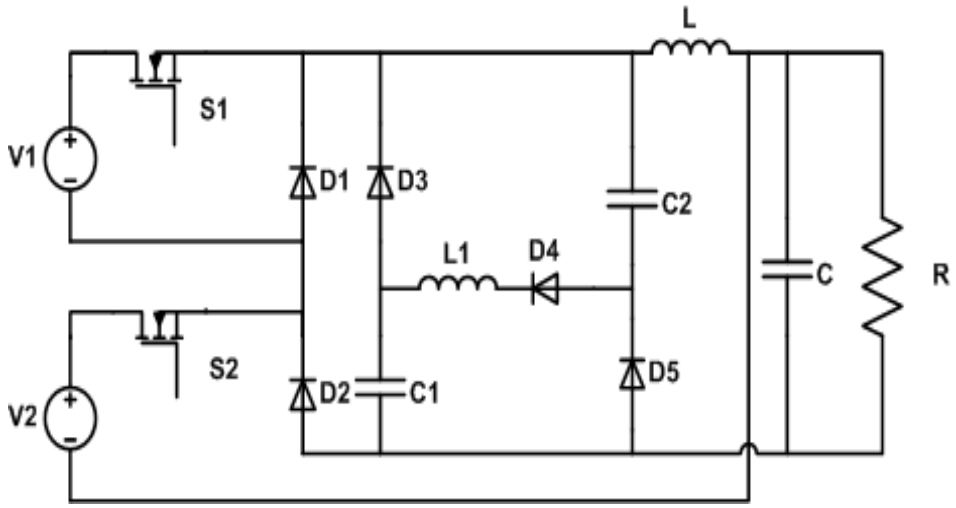

Figure 2.7. Double Input DC-DC converter with soft-switching cell.

2.5. The integrated Buck-Boost/Buck-Boost converter

Figure 2.8. presents the topology of the integrated Buck-Boost/Buck-Boost converter. In this case the voltage sources V_1 and V_2 cannot work simultaneously. When one voltage source transfers power to the load, the other will use the energy stored in the inductor [2.14-2.16, 2.25-2.27].

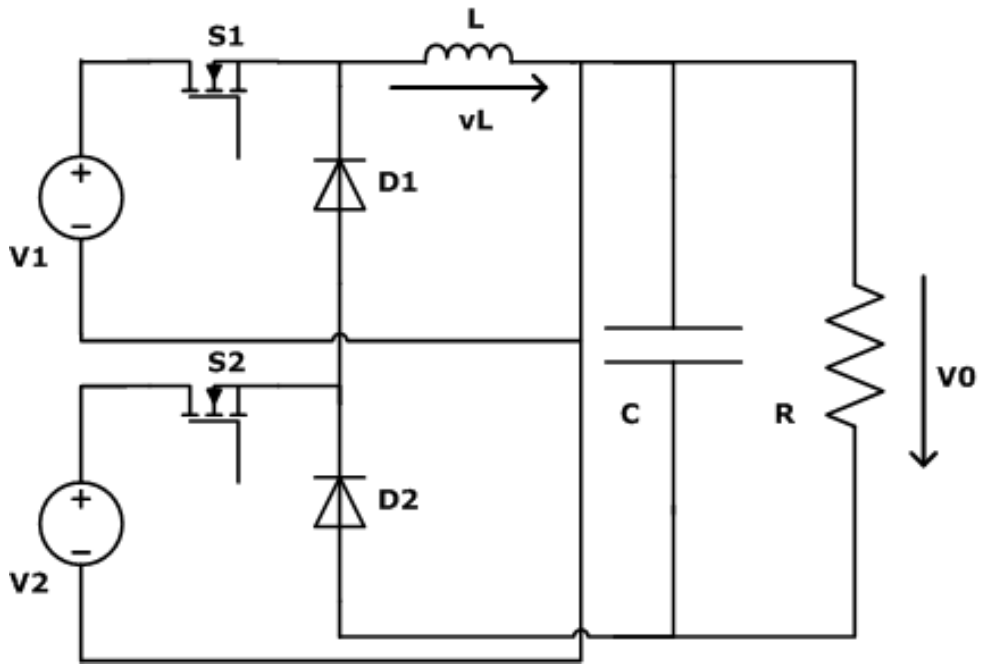

Figure 2.8. The topology of the integrated Buck-Boost/Buck-Boost converter.

When both S_1 and S_2 are off, the freewheeling diodes D_1 and D_2 provide the path for the inductor current. In this case the converter is working in three modes:

- **Mode I**: The switch S_1 is on and the switch S_2 is off. The voltage source V_1 provides power to the load through the inductor;

$$V_{D_2} + V_{D_1} = -V_1 - V_0 \tag{2.3}$$

- **Mode II**: The switch S_1 is off and the switch S_2 is on. The voltage source V_2 supplies all the demanded power;

$$V_{D_2} = -V_2 - V_0 \tag{2.4}$$

- **Mode III**: The switches S_1 and S_2 are off. The power demanded by the load is provided by the inductor L.

Typical waveforms of the switches gate signal, the inductor voltage and current, the input voltage sources currents, and the output current are presented in figure 2.9. The gate signals are synchronized so that the two power switches could not conduct in the same time.

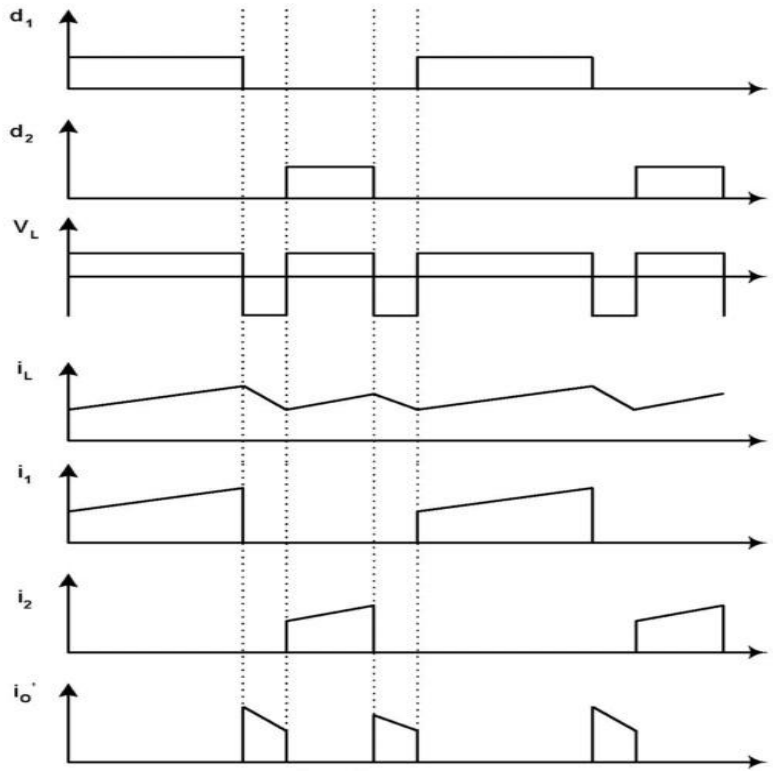

Figure 2.9. Typical vaweforms for the integrated Buck-Boost/Buck-Boost converter.

Table.2.3. presents the voltage across the inductor L_1 for all four-operation modes of the integrated Buck-Boost/Buck-Boost converter.

Table.2.3. Voltage across the inductor in one period (for the integrated Buck-Boost/Buck-Boost converter)

	Mode I	**Mode II**	**Mode III**	**Mode IV**
S_1	1	0	1	0
S_2	0	1	1	0
V_L	V_1	V_2	restricted	$-V_0$

The output voltage can be obtained using the equation (2.5).

$$V_0 = \frac{d_1}{1-d_1-d_2}V_1 + \frac{d_2}{1-d_1-d_2}V_2 \tag{2.5}$$

The bidirectional integrated Buck-Boost/ Buck-Boost converter is obtained by replacing each switch and diode with an anti-parallel pair of a switch and a diode.

This configuration can be used in automotive applications, for example in the drive train. In this case one input source is the battery, the second is an ultracapacitor and the converter output supplies a three phase inverter which feeds an induction motor.

2.6. The multi-input Ćuk converter

Figure 2.10 shows the integrated dual input Ćuk/Ćuk converter topology which has the advantages of continuous input current and high flexibility, allowing the integration of input sources that require a relatively constant current (fuel cell for example) [2.28].

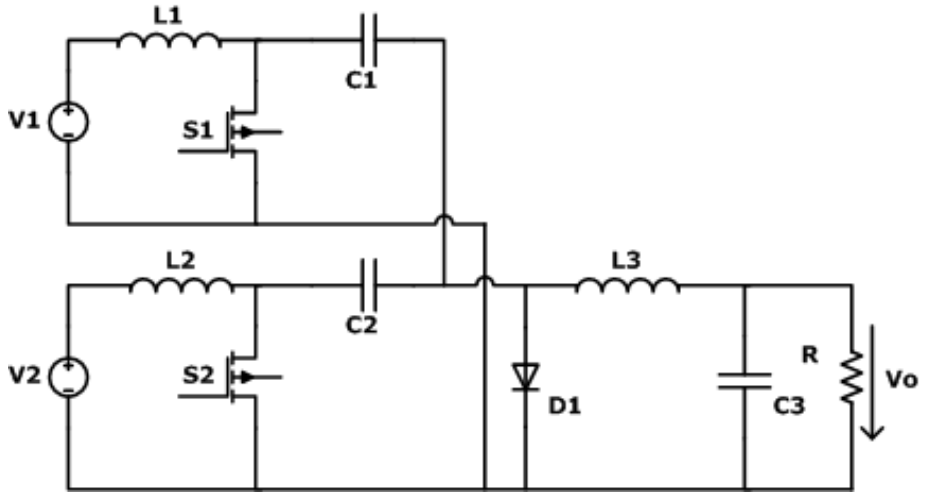

Figure 2.10. The topology of the Ćuk/Ćuk converter.

The output voltage of the converter is given by the next equation:

$$V_o = \frac{d_1}{1-d_2} V_1 + \frac{d_2 - d_1}{1-d_2} V_2 \qquad (2.6)$$

A three input Ćuk DC-DC converter is proposed in [2.29]. The topology of the converter is presented in figure 2.11. In this case the converters are connected in series and they don't have common elements. With the same principle the converter can have more than three inputs.

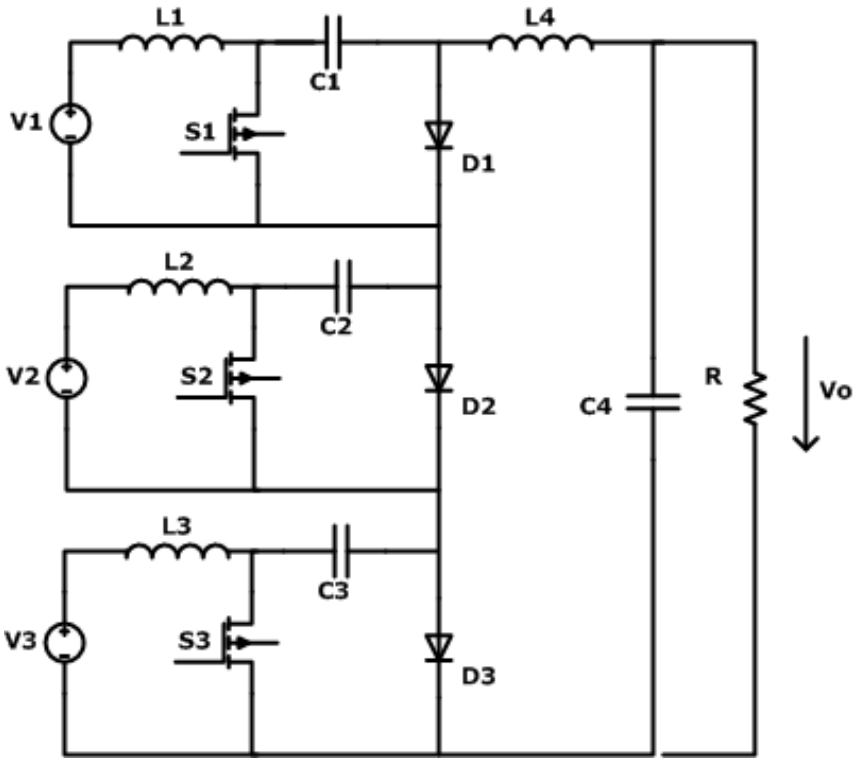

Figure 2.11. Topology of the three input Ćuk converter.

Figure 2.12 presents a three PV panel system which charges a 12V battery. A perturb and observe control algorithm of the system is implemented with a fuzzy logic controller [2.29].

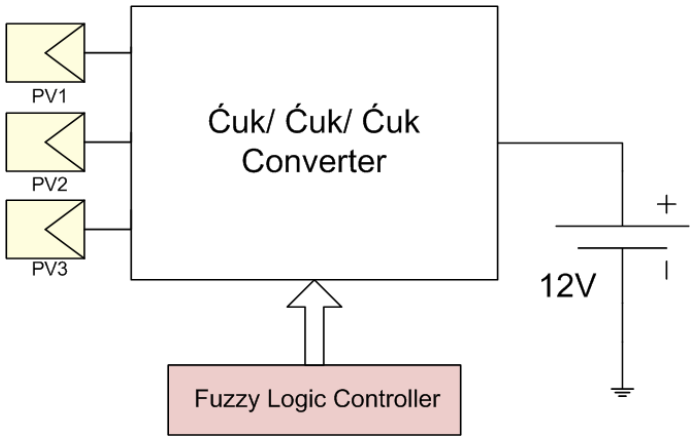

Figure 2.12. The diagram for the PV panel system.

2.7. Multi-input systems with a DC link

A multi input power electronic system configuration, which can be connected to a DC Link, is shown in figure 2.13. This topology is used for hybrid electric vehicles to combine different energy storage units with the electric generator [2.31, 2.32, 2.42].

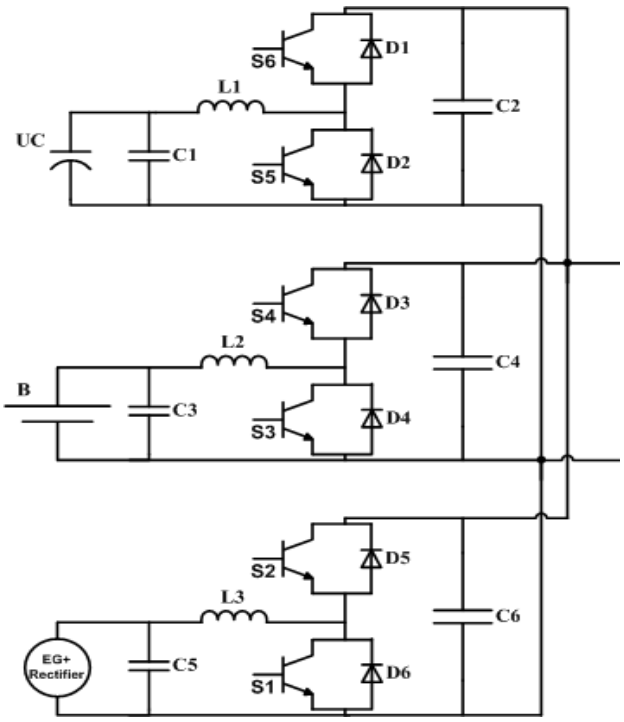

Figure 2.13. Multi-input system topology with a DC link.

The main energy source is the electric generator which is directly driven by the internal combustion engine and connected through an AC-DC converter to the multi-input system. The battery storage unit is sized in order to supply the traction power at light load, when the efficiency of the internal combustion engine combined with the electric generator is very poor; the ultracapacitor provides the requirements for acceleration and regenerative braking.

Each energy source is connected to the DC link through a bidirectional step-up/step-down converter; to transfer energy from one source to the DC link, its associated converter is used in the step-up mode, whereas to charge the battery unit or the ultracapacitor the converter is operated in the step-down mode.

In the case presented in figure 2.13, the third converter could be unidirectional because the energy flows only from the electric generator to the DC link but, for symmetry, a bidirectional converter was presented.

The system can be extended with other input sources and their associated converters. The implementation can be made using a commercial integrated three phase inverter bridge, already available on the market. This can be done even if one of the three converters operates only in the step-down mode.

The control of each converter can be made regarding the output voltage or current. For ultracapacitors, for example, the control depends on the input voltage and on the type of the voltage source.

The contribution of each source to the total power is made through its current. The power changed with the DC link is calculated with the equation 2.7.

$$\frac{dP_{link}}{dt} = V_{link}\left(\frac{dI_{EG}}{dt} + \frac{dI_{B}}{dt} + \frac{dI_{UC}}{dt}\right) \tag{2.7}$$

The power flow control is made through a Power Flow Management Unit (PFM) which acquires the system states and analyze them, in order to determinate the operating mode of each branch. The concept of the DC link management unit is presented in figure 2.14. The energy transfer between any voltage source and the DC-link can be unidirectional or bidirectional. If at least one voltage source can store energy, the transfer between the DC link and the load must be bidirectional.

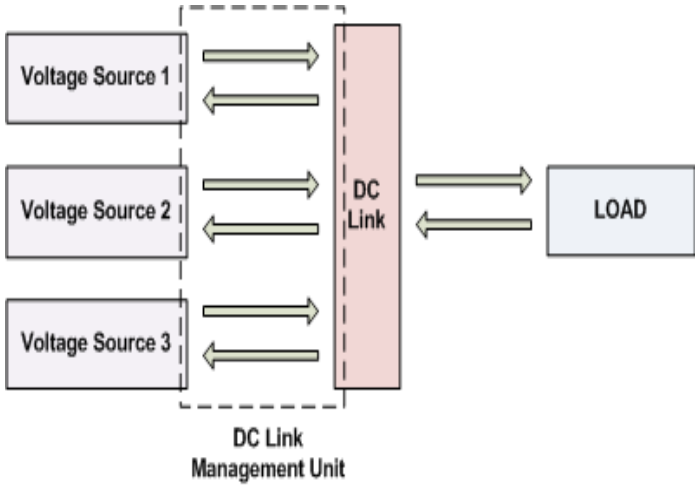

Figure 2.14. Power flow of the multi-input systemwith DC link.

2.8. Multi-input systems based on magnetic flux additivity

The DC-DC systems can combine two input sources not only in electric form, as seen in the previous section, but into magnetic form too, by adding the produced magnetic flux together in a magnetic core of a coupled transformer [2.32-2.43]. The leakage inductance of the transformer is used as energy storage and transfer element between the two sides (input and output) of the system.

The energy sources with different voltage levels connected through a multi-winding transformer can supply power to the load individually and simultaneously.

The sources connected through a multi-winding transformer and the loads are galvanic isolated, which can be an important requirement in some applications.

2.8.1 Two input current-fed Full-Bridge DC-DC system

The circuit diagram of a dual-input system is shown in figure 2.15. [2.33, 2.34]. It consists of two input current sources made with a DC voltage source in series with an inductor, a three-winding coupled transformer, and a common output circuit. The voltages of the DC sources can be different. The number of input sources is not limited. Other input sources can be added and coupled to the same transformer with a higher number of primary windings.

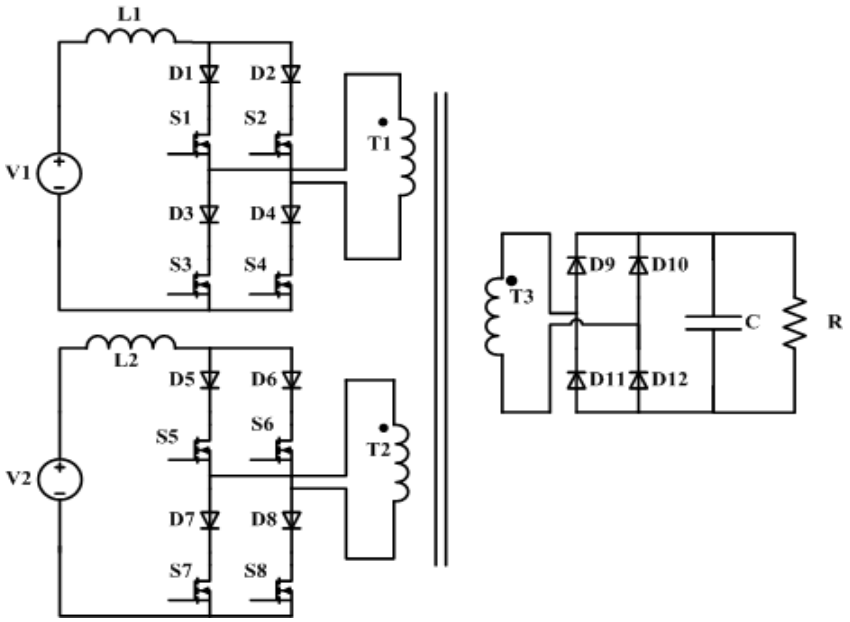

Figure 2.15. The topology of the two-input current-fed full-bridge system.

The power is transferred from the input sources to the load when two switches, located in diagonal position of the full bridge converters are turned on. When two switches of the right-leg or left-leg of the full bridge converter, in each input circuit, are turned on, no power is transferred to the load.

The presented two-input current-fed full-bridge DC-DC system has twelve different operating modes depending on the gate signals of power switches which are presented in figure 2.16. First six are explained below. It is taken into account that at least two switches must be in conduction at one time and no more than three switches of one converter can be turned on.

- **Mode I**, $t \in [t_0, t_{10})$: when $t=t_0$ the switch S_3 turns off. The demanded power is supply by the first source V_1 through the transformer. The current from the inductor L_2 and source V_2 is passing through the switches S_5 and S_7, and their body diodes. Because of the induced voltage in the transformer, winding T_3, the diodes D_9 and D_{12} will be turned on. The body diode of the switch S_8 will conduct;
- **Mode II**, $t \in [t_1, t_2)$: The switch S_8 is turned on but is not conducting current. The source V_1 is still suppling power to the load through the switches S_1 and S_4, and their body diodes;

- **Mode III**, t ϵ [t_2, t_3): The switch S_7 is turned off. The source V_2 starts to provide power to the load via the switches S_5 and S_8. At this time both sources are delivering power. The total magnetic flux in the coupled transformer increases;
- **Mode IV**, t ϵ [t_3, t_4): The switches S_2 an S_6 are turned on. The current from the input sources is passing through the switches S_2, S_4, S_6 and S_8, and their body diodes forming two low impedance circuit branches. No power is transferred from the input sources to the load, which will be supplied in this case by the capacitor C;
- **Mode V**, t ϵ [t_4, t_5): The switches S_1 and S_5 are turned off. The input sources cannot provide power and the load continues to be supplied by the capacitor C;
- **Mode VI**, t ϵ [t_5, t_6): The switch S_3 is turned on due to the clamped zero voltage across the first transformer winding T_1. The load power is still supplied by the capacitor C.

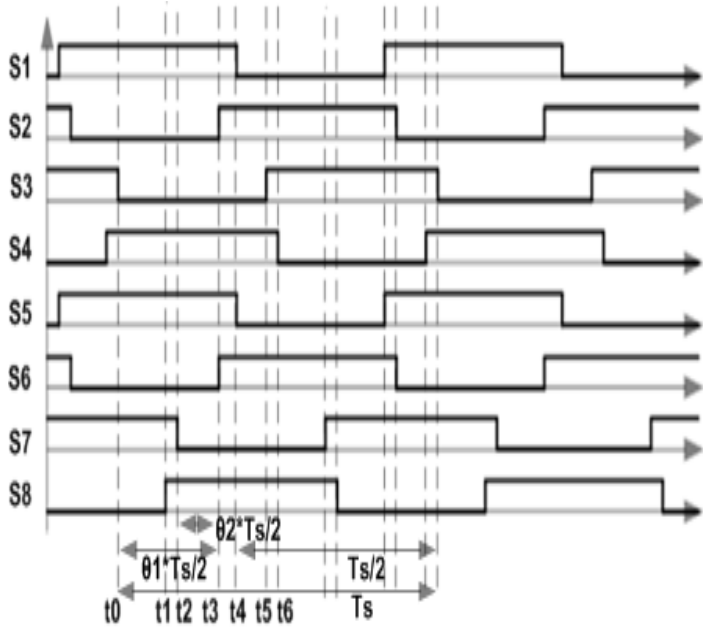

Figure 2.16. The gate signals of the power switches.

The rest of the operating modes are similar. Different is the polarity of the transformer voltages and currents.

The upper switches of each voltage source are operated with zero-current-switching and the lower switches are operated with zero-voltage-switching.

The net magnetomotive force of the coupled transformer can be expressed as:

$$F_T = (\phi_1 - \phi_2)\frac{l_m}{\mu A_C} \tag{2.8}$$

where $\emptyset_1$ and $\emptyset_2$ are the magnetic fluxes produced by the input currents, l_m is the magnetic length path of the transformer, μ is the magnetic permeability, and A_c is the cross-sectional area of the transformer.

The control of the output voltage can be made through phase shifting of the gate signals, θ_1 and θ_2. The output current is given by the equation (2.9).

$$I_0 = \frac{n_1}{n_3}\Theta_1 I_{T1} + \frac{n_2}{n_3}\Theta_2 I_{T2} \tag{2.9}$$

In the above equation, n_1, n_2 and n_3 are the number of turns of the windings T_1, T_2 and T_3, I_{T1} and I_{T2} are the primary winding currents.

A two-input current-fed full-bridge DC-DC system in which one input source is a PV array and the other is the rectified voltage of the utility grid is presented in literature. The system is implemented using the full-bridge converter connected to with the utility grid and a maximum power point tracking (MPPT) algorithm is implemented for the PV array.

2.8.2 Multi-input DC-DC system with zero voltage switching

The converter presented in figure 2.17 is bidirectional and consists of three half-bridges and a high-frequency multi-winding transformer. Adjusting the phase-shift angles of the voltages across the two sides of the transformer the power can flow in both directions from the input to the output. The soft switching can be achieved naturally using snubber capacitors and the transformer leakage inductances [2.36, 2.37].

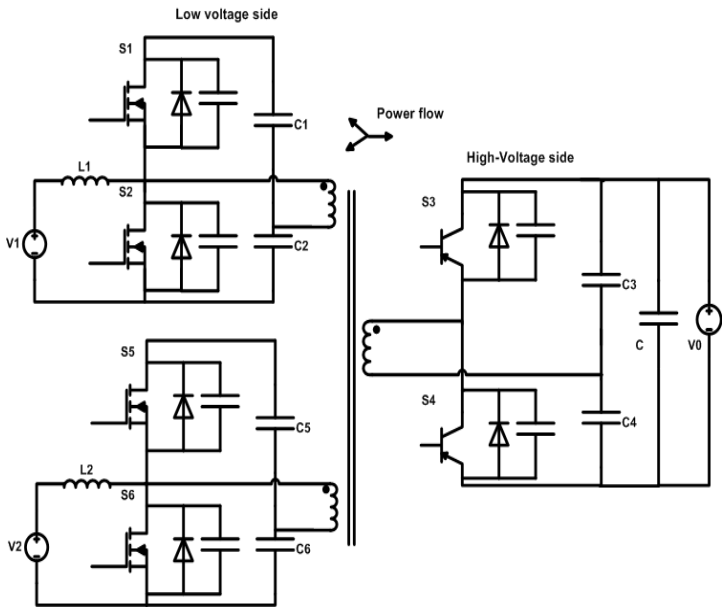

Figure 2.17. The topology of a multi input ZVS DC-DC converter.

At reverse power flow, the circuit will not achieve ZVS completely but realizes reducing switching losses by the decrease of the switch voltage at turn on.

The transformer functions are:

- To combine input DC sources in magnetic form;
- To step-up voltage from the low voltage side to the high voltage side;
- To step-up voltage in the power transfer from output to input.

The sources for the multi-input ZVS DC-DC converter in a hybrid electric vehicle can be the battery and the ultracapacitor and the output is the traction motor drive.

2.8.3. Multi-input bidirectional DC-DC systems with DC-Link and magnetic coupling

In the multi-input system topology, presented in figure 2.18., the input sources are interconnected through a DC Link bus and must have nearly equal operating voltages. The connection between the input sources and the load is made through a transformer. The leakage inductances of the transformer, L_{T1} and L_{T2}, are used as energy transfer elements [2.24].

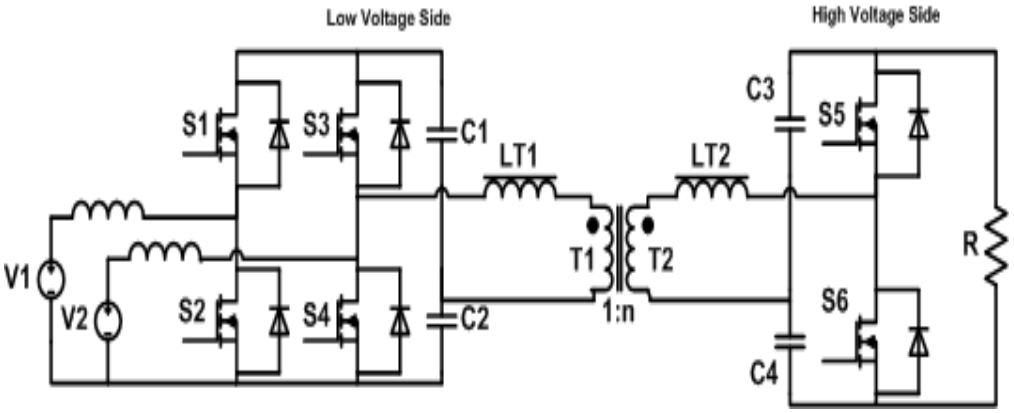

Figure 2.18. The circuit diagram for the multi-input converter with DC Link and magnetic coupling.

The converter has three ports, uses six power switches, and consists of a Boost-dual-half-bridge (S_3-S_4 and S_5-S_6), and a bidirectional direct-connected switching cell (S_1-S_2).

The switching cell S_1-S_2 operates in two modes:

- **Mode I**: The source V_1 sinks the surplus power;
- **Mode II**: The power flows from the source V_1 to the load.

Figure 2.19. presents the power switches gate signals. Each half-bridge are controlled with a pair of complementary gate signals. The switches S_3-S_4 and S_5-S_6 have a 50% fixed duty cycle. The gate signals of the pairs S_3-S_4 and S_5-S_6 are phase shifted to control the power flow between the DC Link capacitors C_1-C_2 and the load.

This converter is suitable for systems where the low operating voltage of the sources needs to be boosted to match the high voltage side of the load. A fuel cell

system for domestic applications build with a same DC-DC converter is presented in [2.42].

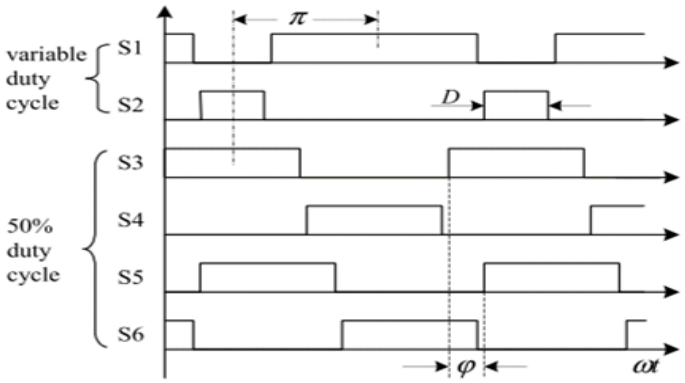

Figure 2.19. The power switches gate signals.

2.9. Multi-input systems with complex control

A typical example of a multiple input system with complex control is given in [2.53] and it is presented as a DC grid in a future home. Its block diagram is shown in figure 2.20. The term "grid" does mean here AC distribution. It is considered to be a small power system that uses a combination of different voltage level sources to supply small local loads [2.54, 2.55].

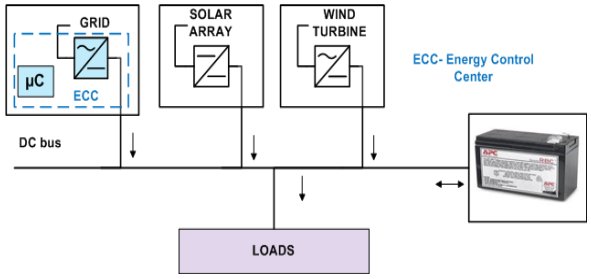

Figure 2.20. A intermediary DC grid in a future home.

The system inputs are considered to be the grid and renewable energy sources (PV and wind turbine). The power through the battery flows in both directions. Every energy source has its own AC-DC or DC-DC converter which connect it to the DC bus.

The control of the power flow is made with an energy control centre (ECC) which consists of a microcontroller and a full power bidirectional AC-DC converter. The DC bus of the system has a constant voltage. The voltage control uses the drop control based on the DC bus signaling technique. The power converter is used for power flow control, monitoring, diagnostic, and fault protection, as well as for voltage and frequency conversion.

Several grids can be connected in a hierarchically, organized system. If the intermediary grid has sufficient capacity for energy generation and storage, it can operate independent from the superior grid.

Figure 2.21. presents an example of an off-grid multi-input hybrid energy system. It has at least one renewable source, one additional source and one storage element. The ultracapacitor is directly connected to the DC bus to control its voltage level, which is not constant. The DC-DC converters can be controlled by a multi-agent fuzzy-logic based energy management unit [2.55]. In this case the system is a collection of autonomous and intelligent elements that collaborate to reach a global coordination. The advantage of such configuration is that when one element is changed, the others adapt its behavior, and the system continues to work without perturbation; the load is always supplied with high efficiency.

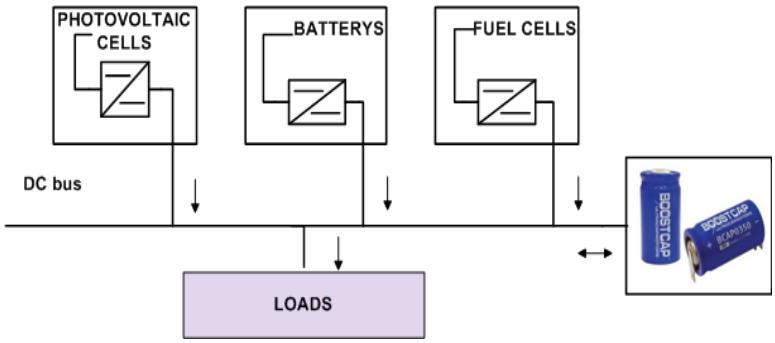

Figure 2.21. The general block diagram of a hybrid energy system.

2.10. Conclusions

Multi-input DC-DC converters and systems can be used when two or more energy sources have to be combined in one energy supply system. Several topologies were presented in the literature and a general overview of them was given in this chapter.

The advantages of combining two or more energy sources in one system are:

- less power electronic components are used in some cases;
- more power is available;
- continuous power flow in the system even if one input source is damaged.

A large scale of utilization of this type of multi-input DC-DC topologies is expected in the future due to the continuous growth of renewable energy importance and more requirements in energy flow management.

Table 2.5 shows the comparison of the integrated dual input converters. It can observe that they have the same number of elements but different performances.

Table 2.4. Comparison of the main integrated converters.

	The integrated Buck/Buck converter	The integrated Buck/Buck-Boost converter	The integrated Buck-Boost/Buck converter
No. of elements	5	5	5
Output voltage	$V_0 = d_1 V_1 + d_2 V_2$	$V_0 = \frac{d_1}{1-d_1} V_1 + \frac{d_2}{1-d_2} V_2$	$V_0 = \frac{d_1}{1-d_1-d_2} V_1 + \frac{d_2}{1-d_1-d_2} V_2$
Tested applications	PV/Wind system	Grid connected hybrid PV/Wind power system, Hybrid electric vehicles	-
Input sources work simultaneously	yes	yes	no

The multi-input converters connected in magnetic form have the following advantages:

- different magnitudes of the input sources;
- accessible soft-switching technology;
- electrical isolation naturally achieved.

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Chapter 3
Dual Input DC-DC Converters Using Classical and/or Hybrid Buck Structures

3.1. Introduction

The dual-input converters generated with the above presented methods have into their topologies classical Buck, Boost and Buck-Boost structures. The concept of synthesizing multi-input DC-DC [3.1-3.7] converters will be extended, from classical to hybrid structures [3.8-3.15], as a major contribution of this thesis. Analytical description, digital simulations and experimental results complete the content of this chapter.

Only four new topologies are proposed in this thesis but many more dual input DC-DC converters can be generated starting from the theoretical concepts presented in this chapter.

A table with the possible combination of the hybrid cells into a dual input DC-DC converter is presented too. The MIC can be generated with classical and hybrid cell or only with hybrid cells, depending on the proposed scope.

It is analytically demonstrated that a hybrid structure is characterized by a higher (or lower) input to output voltage conversion ratio compared to a classical Buck converter, in step-down (or Boost) mode. For this type of applications hybrid Buck DC-DC converters are needed.

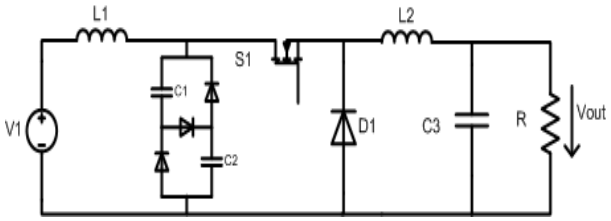
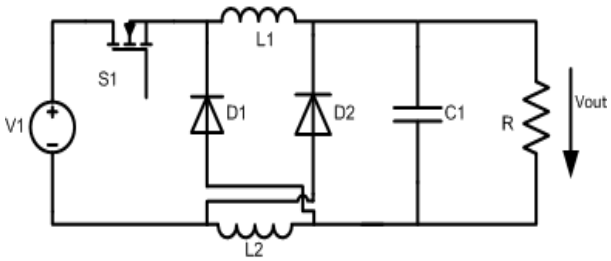
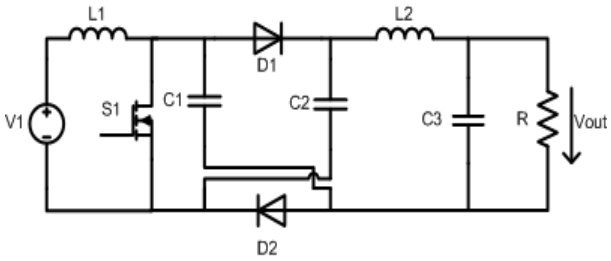
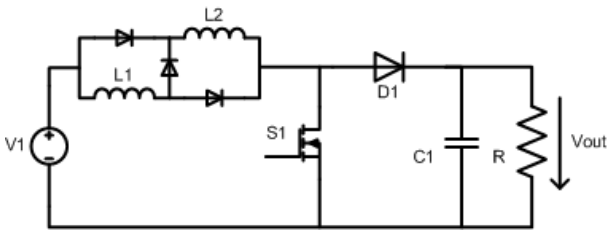
The hybrid DC-DC converters are made from classical structures (Buck, Boost, Buck-Boost, Ćuk, SEPIC, and ZETA topologies) by inserting switching cells as table 3.1 shows [3.8-3.14]. A switching cell can be an inductor, or a capacitor switch cell "assisted" by diodes. The relations between the input and output voltages, as a function of the duty cycle d, are also presented. The equations show that the output voltage of the presented converters is reduced/increased more times than in the classical structures.

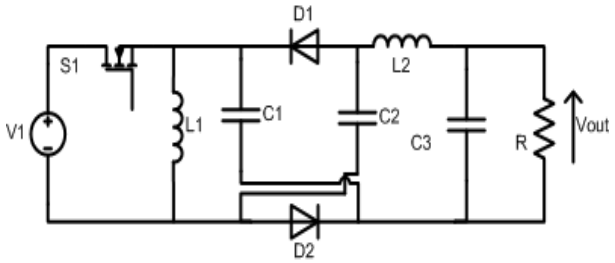
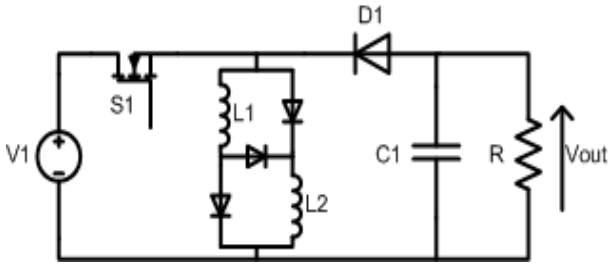
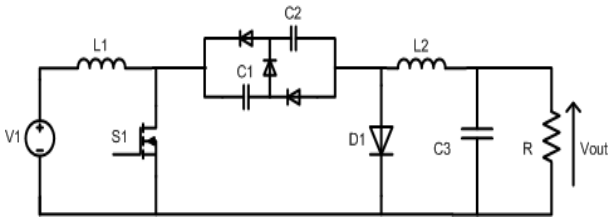
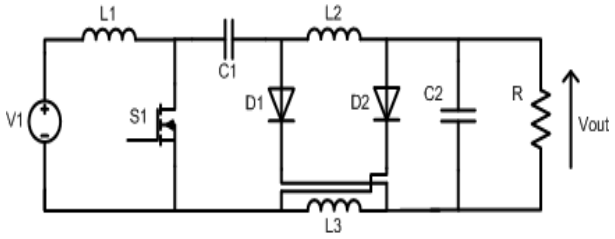
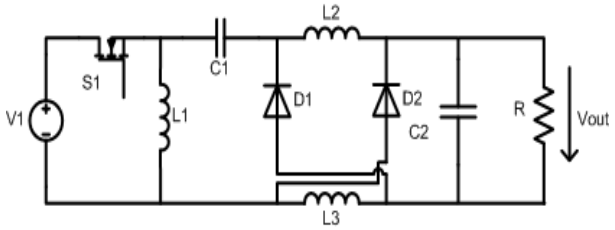
From table 3.1 the first two topologies (hybrid Buck L cell and hybrid Buck C cell) constitute the basic converters for the proposed dual input DC-DC structures. These circuits are analytically studied and simulation results are presented for them.

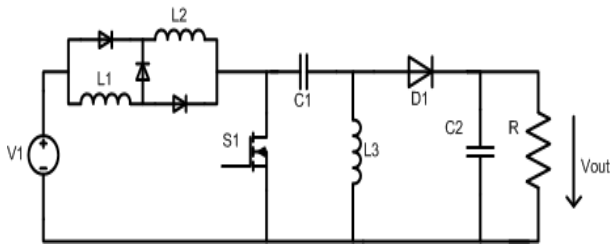
For all hybrid converters, when the power switch is on, the inductors and the capacitors in the switching cells are charged in series and discharged in parallel.

When the active power switch is off, these elements work in a reversed mode.

Table.3.1. Hybrid DC-DC converters.

Converter type	Converter topology	Output voltage
Hybrid Buck C converter		$V_{out}=\frac{d}{2-d}V_1$
Hybrid Buck L converter		$V_{out}=\frac{d}{2-d}V_1$
Hybrid Boost C converter		$V_{out}=\frac{1+d}{1-d}V_1$
Hybrid Boost L converter		$V_{out}=\frac{1+d}{1-d}V_1$

Hybrid Buck-Boost C converter		$V_{out}=\frac{2d}{1-d}V_1$
Hybrid Buck-Boost L converter		$V_{out}=\frac{2d}{1-d}V_1$
Hybrid Ćuk C converter		$V_{out}=\frac{2d}{2(1-d)}V_1$
Hybrid Ćuk L converter		$V_{out}=\frac{2d}{2(1-d)}V_1$
Hybrid ZETA L converter		$V_{out}=\frac{2d}{2(1-d)}V_1$

Hybrid SEPIC L converter		$V_{out} = \frac{d(1+d)}{1-d} V_1$

The hybrid Buck L converter is made from a classical Buck converter by inserting an inductors switched cell into its topology. Figure 3.1 presents the converter diagram with the corresponding t_{on} and t_{off} equivalent circuits (modes). While the power switch S_1 is on, the inductors are charged in series and the current slope is positive (figure 3.1.b). When the switch S_1 is off, the inductors current are discharged in parallel through the diodes D_1 and D_2 (figure 3.1.c).

The output voltage of the converter results from the voltage-second balanced theorem applied to the inductor L_1:

$$\frac{1}{2}(V_1 - V_0)d - V_0(1-d) = 0 \tag{3.1}$$

$$V_{out} = \frac{d}{2-d} V_1 \tag{3.2}$$

It can be seen from equation (3.2) that a lower conversion ration can be achieved, compared to classical Buck converter.

Digital simulations were made in PSim, simulation software embedded designed for power electronics and dynamic systems.

Figure 3.2 presents the simulated waveforms for the power switch S_1 gate signal (v_{gS1}), the current through the inductor L_1 (i_{L1}), the voltage across the inductor L_1 (v_{L1}), and the output voltage (v_{out}). The converter has been simulated for a duty cycle of 58% with an input voltage of 40V.

From the simulation results can be observed that the inductor current has two slopes corresponding to the conduction modes of the transistor. The output voltage, which is presented in figure 3.2 is 16V, which is reduced with (2-d) more times than in a classical Buck converter.

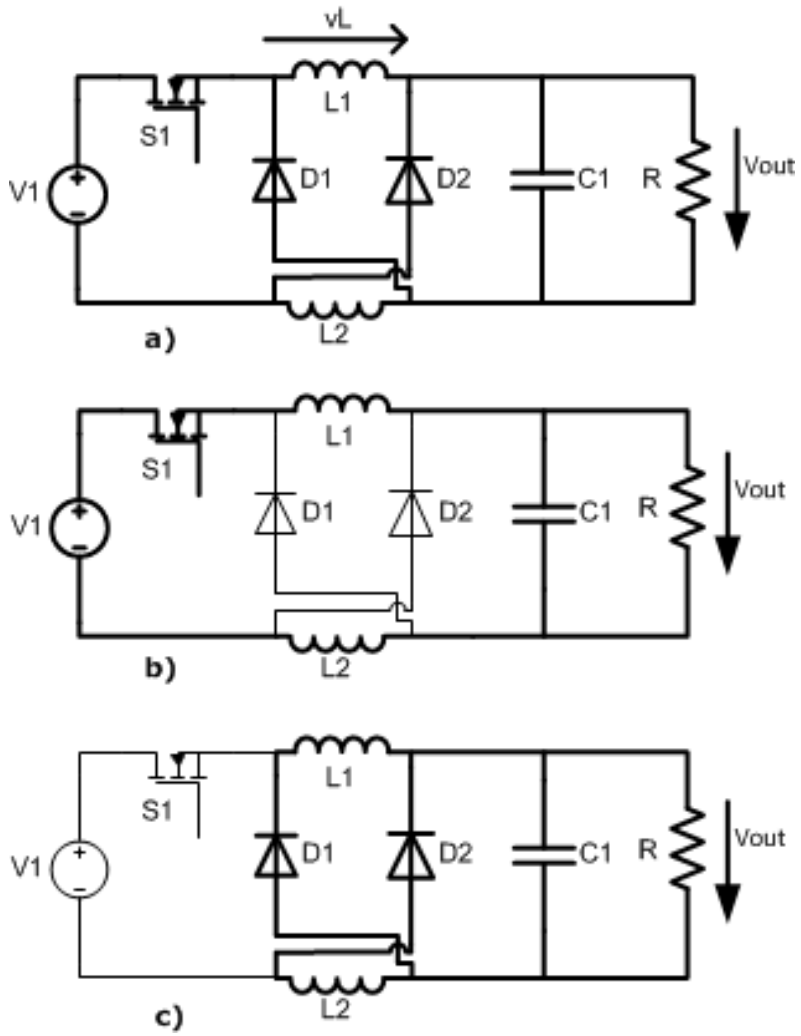


Figure 3.1. Hybrid Buck L converter: a) converter diagram; b) mode I (t_{on}); c) mode II (t_{off}).

The hybrid Buck C converter has a switched capacitor cell added in the topology. The diagram of the converter is presented in figure 3.3.a. Figure 3.3.b presents the operating modes: when the power switch S_1 is on, the capacitors are connected in parallel, and the voltage source V_1 will supply the load; when the power switch is off, the capacitors are charged in series.

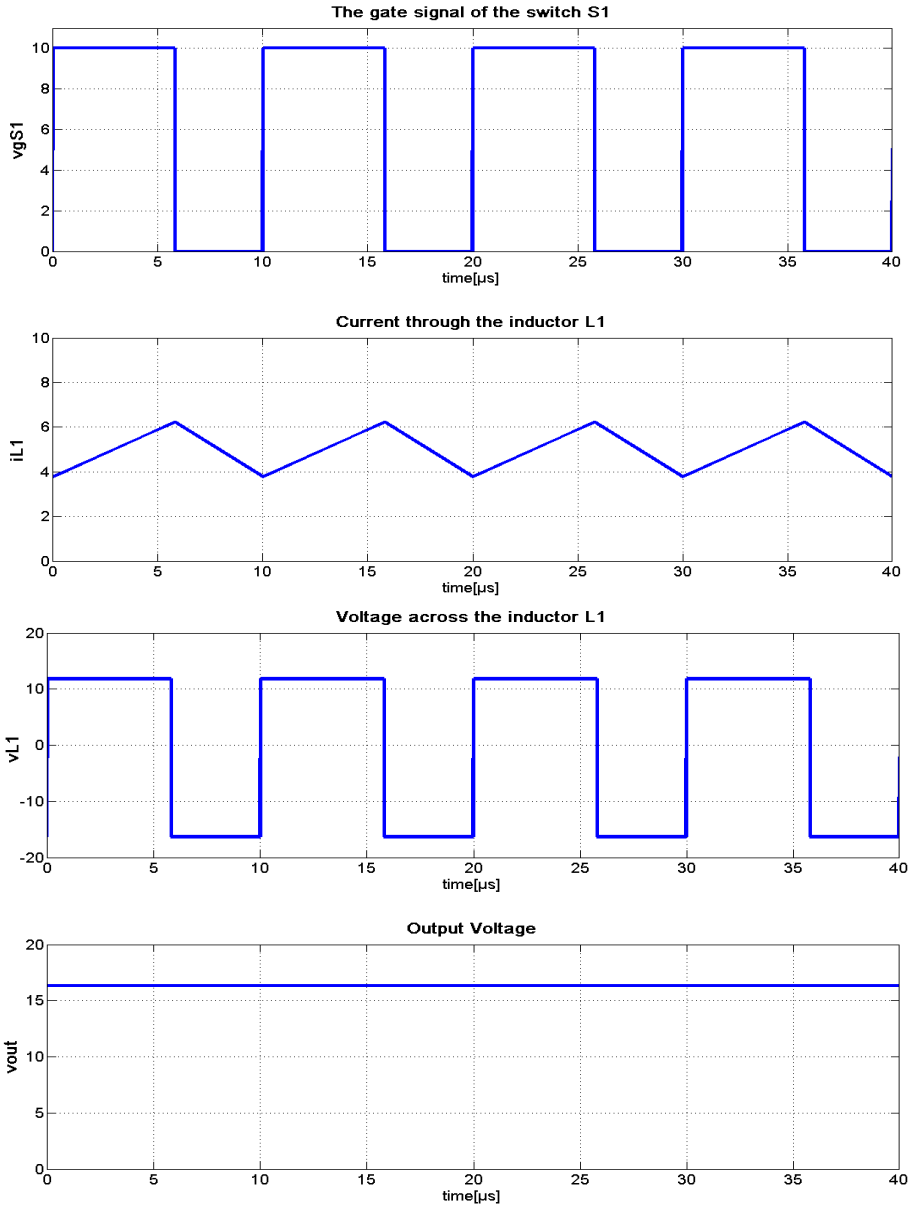


Figure 3.2. Simulation results for the hybrid Buck L converter.

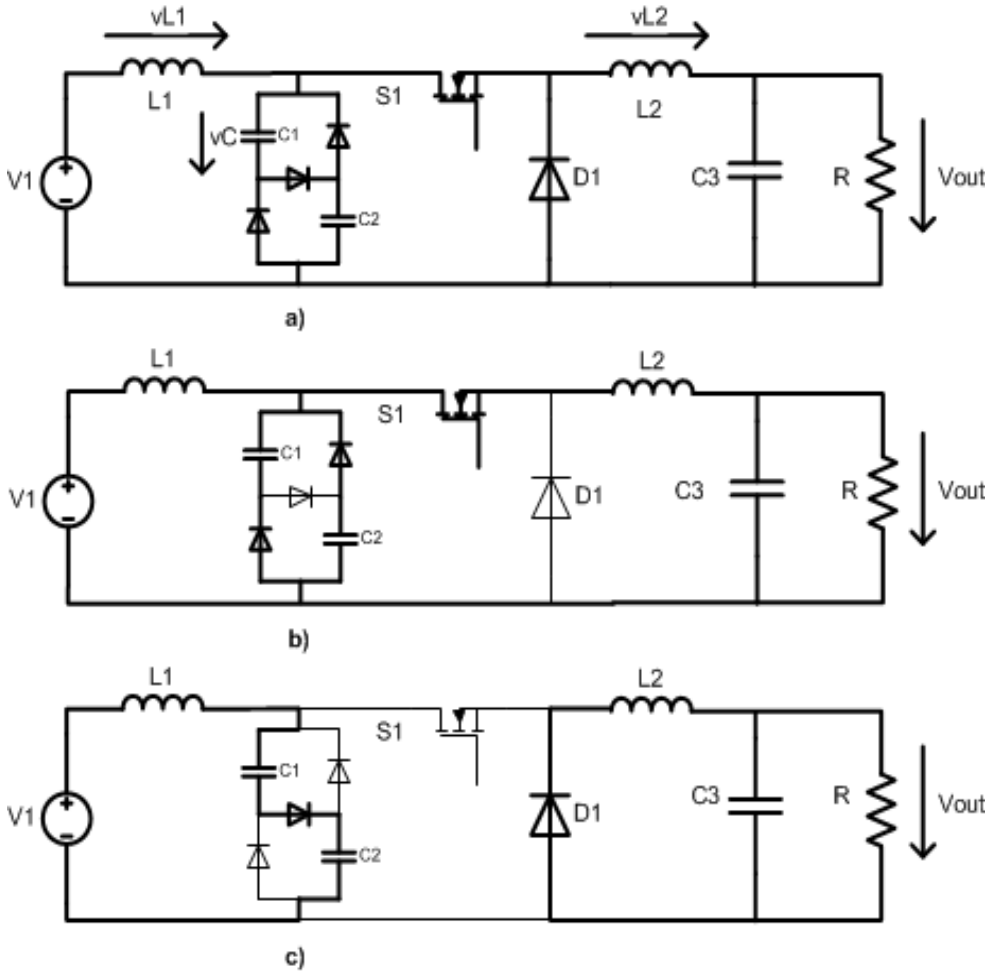


Figure 3.3. Hybrid Buck C converter: a) the converter topology; b) mode I (t_{on}); c) mode II (t_{off}).

The output voltage of the converter results from the voltage-second balanced theorem applied to the inductors L_1 and L_2:

$$(V_1 - V_C)d + (V_1 - 2V_C)(1-d) = 0 \tag{3.3}$$

$$(V_C - V_{out})d - V_{out}(1-d) = 0 \tag{3.4}$$

Where V_c is the voltage across the capacitors C_1 and C_2.
From equations (3.5) a relation between V_C and V_1 can be obtained:

$$V_C = \frac{1}{2-d} V_1 \tag{3.5}$$

The output converter voltage is given by:

$$V_{out} = \frac{d}{2-d} V_1 \tag{3.6}$$

Simulation results have been carried out using PSim. The simulation results are presented in figure 3.4 for an input voltage of 40V and a duty cycle of 50%.

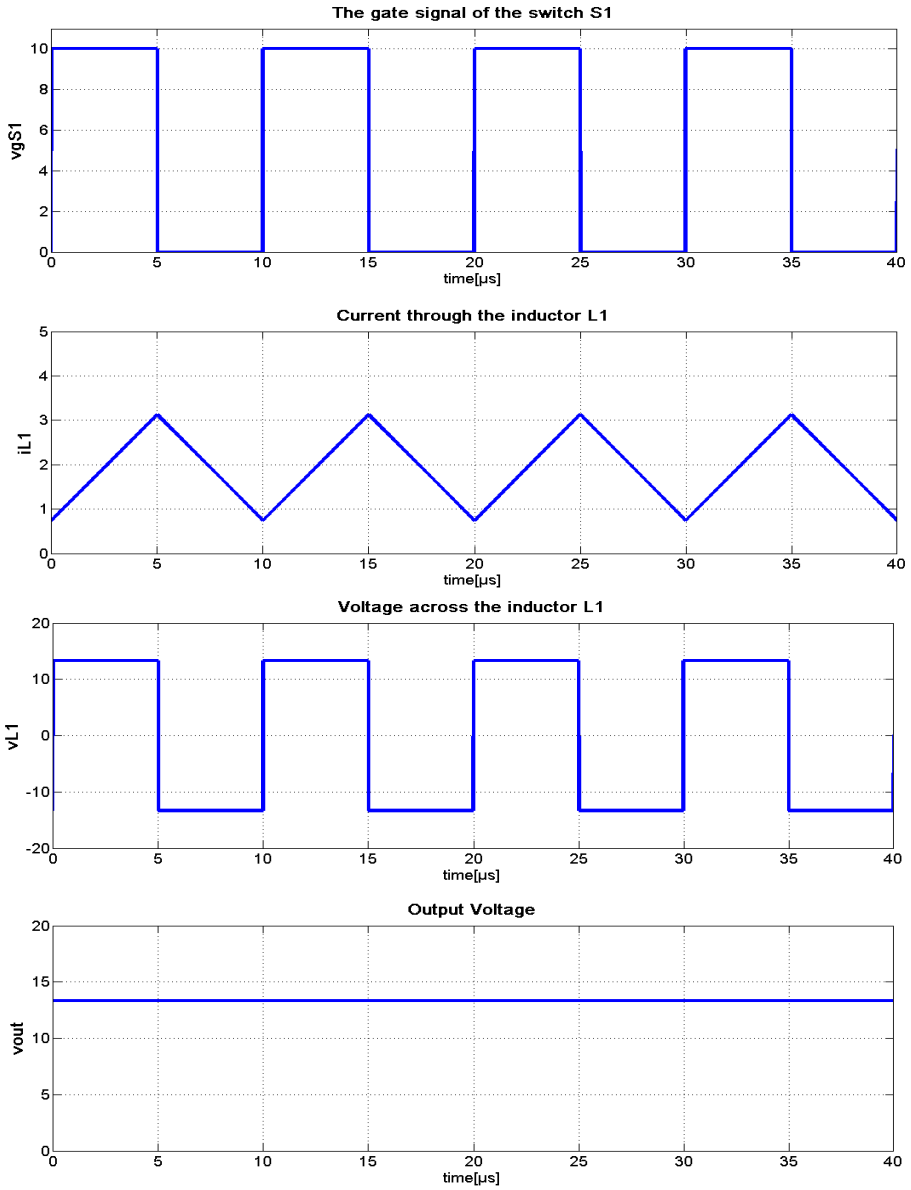


Figure 3.4. Simulation results for the hybrid Buck C converter.

For the hybrid Buck converter topologies study, some assumptions need to be made:

- The circuit operates in the continuous-conduction mode (CCM), the inductors current flows continuously;
- The capacitors from the switching capacitors cell are equals and relatively large, so that the voltage across them contains negligible ripple;
- The inductors from the switching inductors cell are equals so that the voltage across them is equal, too;
- The power switches are working at the same frequency, with different duty cycles.

Four configurations of multi-input hybrid Buck DC-DC converter topologies are proposed for application with two input voltage sources. Two of them are combinations between classical Buck and hybrid Buck converters and the others are mixing topologies of hybrid Buck structures:

- Dual input Buck/hybrid Buck L converter made from a classical Buck cell and a hybrid Buck inductor cell (figure 3.5.c);
- Dual input Buck/ hybrid Buck C converter consisting of a classical Buck cell and a hybrid Buck capacitor cell (figure 3.5.b);
- Dual input hybrid Buck C/ hybrid Buck L converter made from a hybrid Buck inductor and a hybrid Buck capacitor cell;
- Dual input hybrid Buck L/ hybrid Buck C converter, the previous reverse topology.

The principle of inductor volt-second balance (in steady-state, the net volt-seconds applied to an inductor must be zero knowing that the initial and final value of the inductor current are equal), is used later in this chapter for the proposed dual-input hybrid Buck DC-DC converters. The volt-second balanced principle is general and was applied to all proposed converters [3.15-3.20].

$$i_L(T) - i_L(0) = \frac{1}{L}\int_0^T v_L(t)dt \tag{3.7}$$

$$0 = \int_0^T v_L(t)dt \tag{3.8}$$

This chapter presents first an analytical study, validate through digital simulations, for three configurations made from a classical Buck and/or a hybrid Buck structure (dual input Buck/ hybrid Buck L converter, dual input Buck/ hybrid Buck C converter, and dual input hybrid Buck C/hybrid Buck L converter).

The dual input hybrid Buck L/hybrid Buck C converter will be studied in detail, with theoretical results validated through experiments.

The dual input hybrid Buck L/hybrid Buck C converter uses the switched inductor cell has an output filter, too. The advantage of having hybrid Buck C structure connected to a common ground (one input voltage source and the output have a common potential) makes the converter suitable to be integrated in many applications.

3.2. Synthesizing dual-input DC-DC converters using hybrid Buck structures

The hybrid DC-DC converters presented in the previous section will be classified as PVSC (hybrid Buck C converter) and a PCSC (hybrid Buck L converter).

Figure 3.5 presents the PVSC's made from hybrid DC-DC converters excluding the output part.

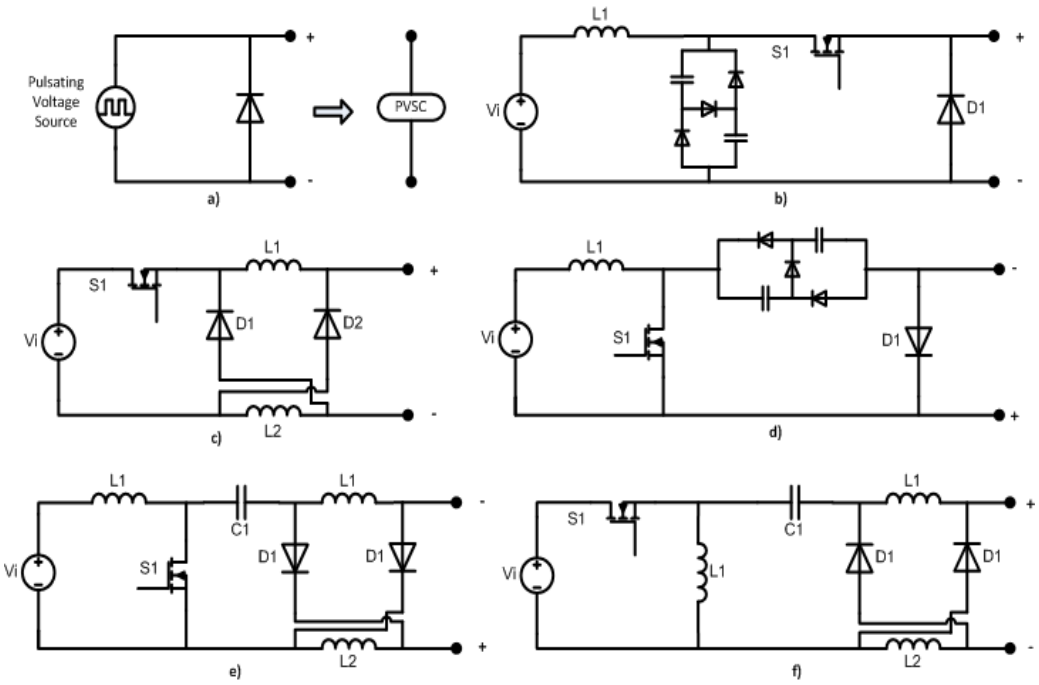


Figure 3.5. Circuit configurations of the PVSC: a) conceptual diagram of the PVSC ; b) Buck C type PVSC; c) Buck L type PVSC; d) Ćuk C type PVSC; e) Ćuk L type PVSC; f) ZETA L type PVSC.

Figure 3.6 presents the PCSC made from hybrid DC-DC converters, excluding the output part.

The rules to generate multi-input DC-DC converters are the same as presented in the previous chapter. When a PVSC is inserted into a basic converter, it must be connected in series with a current sink, as shown in figure 3.7.a. When a PCSC is inserted into a basic converter, it must be connected across a voltage sink, as shown in figure 3.7.b.

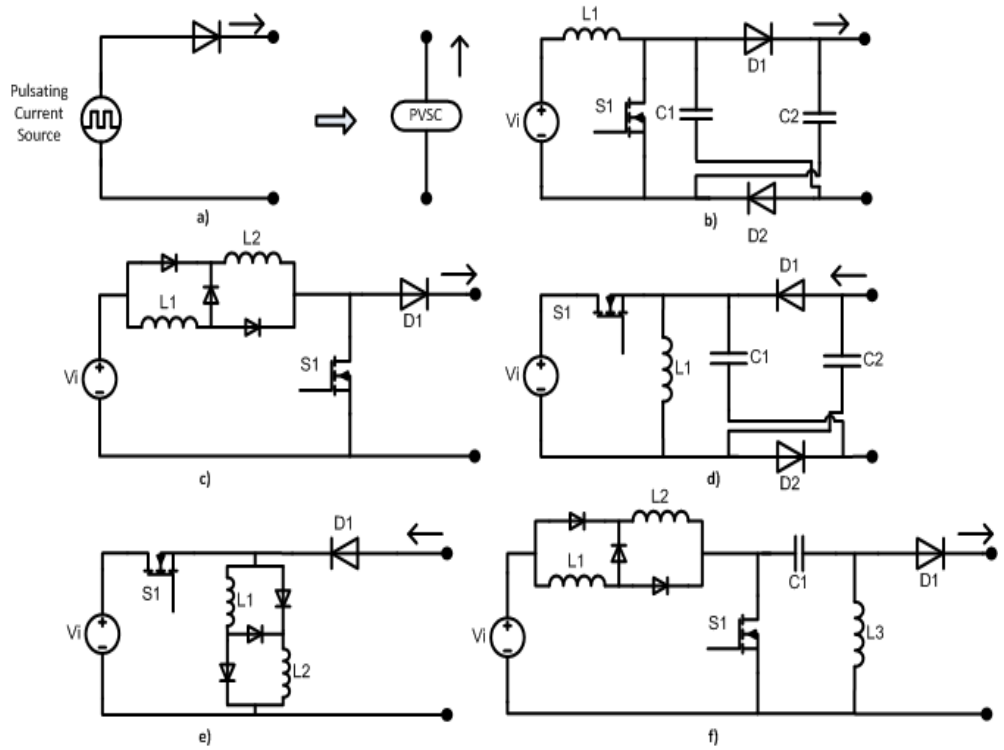


Figure 3.6. Circuit configurations of the PCSC: a) conceptual diagram of the PCSC ; b) Boost C type PCSC; c) Boost L type PCSC; d) Buck-Boost C type PCSC; e) Buck-Boost L type PCSC; f) SEPIC L type PCSC.

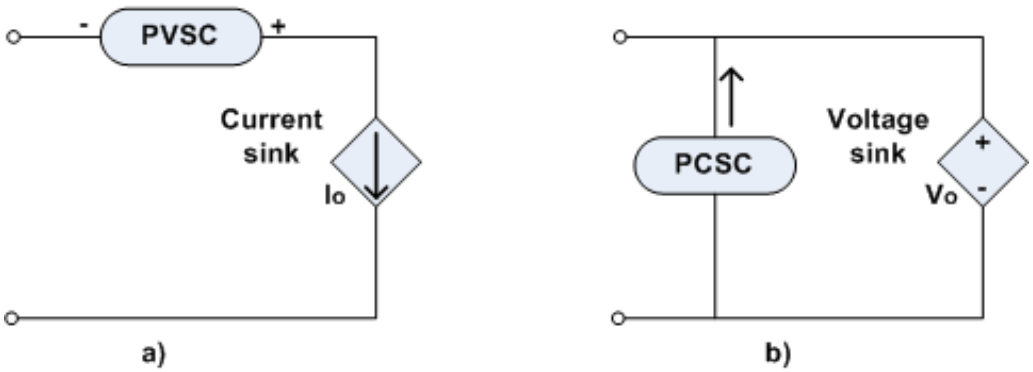


Figure 3.7. Circuit configuration of a PVSC/ PCSC connected to a basic converter.

Based on these rules, and using the hybrid DC-DC converters mentioned above, ten categories of dual input hybrid DC-DC converters have been presented (Table 3.2.). Some of the converter combinations are not possible and they are marked with "NO".

Tabel.3.2. Possible combinations of dual input hybrid DC-DC converters.

Basic converter	Pulsating source cell	Hybrid buck C	Hybrid buck L	Hybrid boost C	Hybrid boost L	Hybrid buck-boost C	Hybrid buck-boost L	Hybrid Cuk C	Hybrid Cuk L	Hybrid Zeta L	Hybrid Sepis L
PVSC	Hybrid buck C	YES	YES	NO	NO	YES	YES	YES	YES	YES	YES
	Hybrid buck L	YES	YES	NO	NO	YES	YES	YES	YES	YES	YES
	Hybrid cuk C	YES	YES	NO	NO	YES	YES	YES	YES	YES	YES
	Hybrid cuk L	YES	YES	NO	NO	YES	YES	YES	YES	YES	YES
	Hybrid zeta L	YES	YES	NO	NO	YES	YES	YES	YES	YES	YES
PCVS	Hybrid boost C	NO	NO	YES	YES	YES	YES	YES	YES	YES	YES
	Hybrid boost L	NO	NO	YES	YES	YES	YES	YES	YES	YES	YES
	Hybrid buck-boost C	NO	NO	YES	YES	YES	YES	YES	YES	YES	YES
	Hybrid buck-boost L	NO	NO	YES	YES	YES	YES	YES	YES	YES	YES
	Hybrid sepic C	NO	NO	YES	YES	YES	YES	YES	YES	YES	YES

3.3. Dual input Buck/hybrid Buck L converter

The dual input Buck/ hybrid Buck L converter (HBL) is essentially a series combination of a classical Buck and a hybrid Buck L converters, as it is shown in figure 3.8.

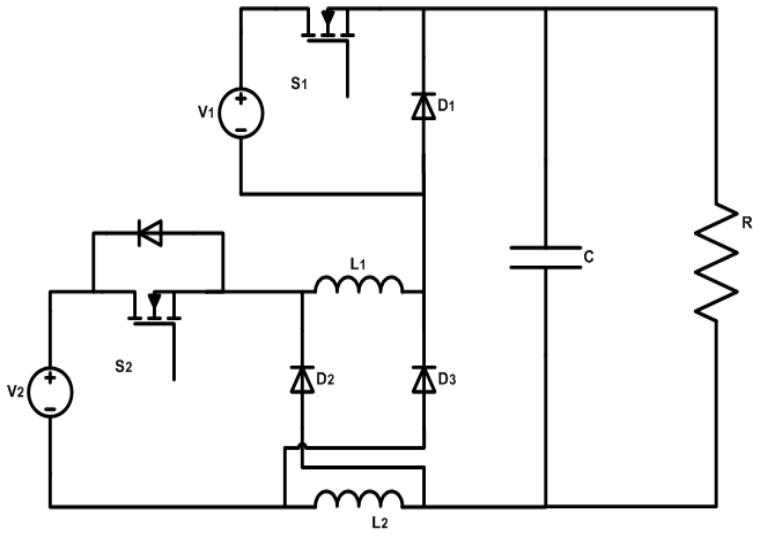


Figure 3.8. The Buck/hybrid Buck L converter topology.

HBL has four possible operating modes depending on the power switches status, as shown in figure 3.9. Depending on the relation between the duty cycle d_1 of the switch S_1, and the duty cycle d_2 of the switch S_2 the converter has only three operating modes during one period.

- **mode I**: The power switch S_1 is on and the power switch S_2 is off. The voltage source V_1 will supply all demanded power by the load and will charge the inductors L_1 and L_2 which are connected in parallel. From figure 3.9.a it can be seen that the diode D_1 is reverse biased and treated as an open circuit while the diodes D_2 and D_3 are connected in series with the inductors L_1 respectively L_2 to provide a current path.
- **mode II**: The power switch S_1 is off and the power switch S_2 is on. Figure 3.9.b presents the equivalent circuit. The voltage source V_2 will charge the inductors L_1 and L_2, which are connected in series and provide electrical energy to the load. The diode D_1 is forward biased and provides a by-pass for the inductors current while the diodes D_2 and D_3 are treated as an open circuit.
- **mode III**: The power switches S_1 and S_2 are on. The two input voltage sources V_1 and V_2 will work simultaneously to charge the inductors and supply the load, as shown in figure 3.9.d. The input sources are connected in series. The diodes from the circuit are reverse biased and treated as an open circuit.
- **mode IV**: The power switches S_1 and S_2 are off. Both input sources V_1 and V_2 are disconnected. The equivalent circuit for this operating mode is shown

in figure 3.9.c. The magnetic energy stored by the inductors L_1 and L_2 will supply the load. The diodes are forward biased providing a current path.

It is assumed that the gate signals of the power switches S_1 and S_2 are synchronized at turn on and have different conduction time ($d_1>d_2$ or $d_1\leq d_2$).

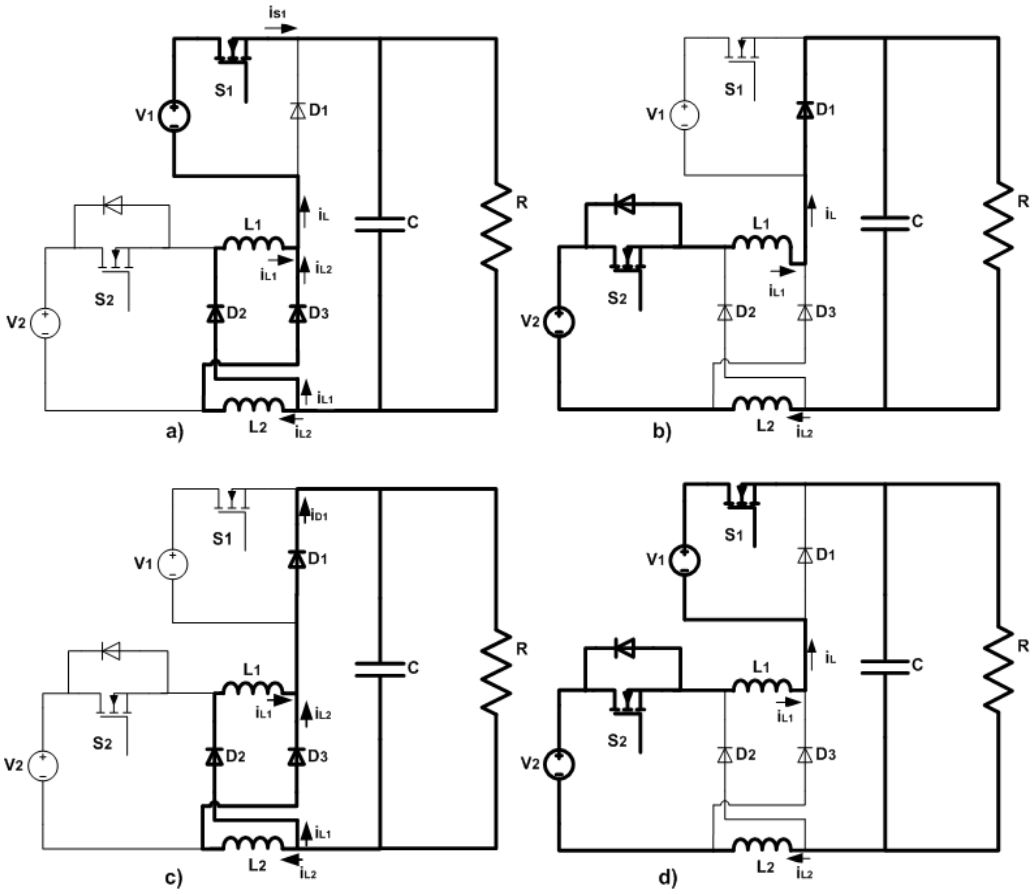


Figure 3.9. HBL operating modes: a) mode I; b) mode II; c) mode III; d) mode IV.

If the duty cycle $d_1>d_2$ the operating mode sequence is: mode IV, mode I and mode III, else the sequence is: mode IV, mode II and mode III.

Table 3.3 presents the voltage across one inductor (L_1 or L_2) during one period. The voltages are presented for all operating modes.

Table.3.3. Voltage across the inductor in one period (for the HBL)

	Mode I	**Mode II**	**Mode III**	**Mode IV**
S_1	1	0	0	1
S_2	0	1	0	1
$V_{L1}=V_{L2}$	V_1-V_0	$½(V_2-V_0)$	$-V_0$	$½(V_1+V_2-V_0)$

In the first case, when the $d_1>d_2$, by applying the volt – second balance theorem on the inductors L_1 or L_2, the following equation can be obtained:

$$\frac{1}{2}(V_1+V_2-V_0)d_2+(V_1-V_0)(d_1-d_2)-V_0(1-d_1)=0 \tag{3.9}$$

When d1 ≤ d2 the equation is:

$$\frac{1}{2}(V_1+V_2-V_0)d_1+\frac{1}{2}(V_2-V_0)(d_2-d_1)-V_0(1-d_2)=0 \tag{3.10}$$

From equations (3.9) and (3.10) the output voltage expressions for $d_1>d_2$, and $d_1\leq d_2$ respectively, can be obtained:

$$V_0=\frac{2d_1-d_2}{2-d_2}V_1+\frac{d_2}{2-d_2}V_2 \tag{3.11}$$

$$V_0=\frac{d_1}{2-d_2}V_1+\frac{d_2}{2-d_2}V_2 \tag{3.12}$$

Under normal operation, HBL can simultaneously provide electric energy from both input sources. If one of the voltage sources is disconnected, the other one can continue to deliver power to the load normally.

For the HBL extended study, digital simulations have been carried out in Psim with real elements with power losses consideration. The following parameters have been taken into account for the simulation:

Table.3.4. Simulation Parameters

Parameter	Value
Inductors L_1 and L_2	28μH
Output capacitor C	3960μF
Switching frequency	100kHz

3.3.1. Simulation results for $d_1>d_2$

Figures 3.10-3.13 present the case when d_1=50%, d_2=30%, V_1=45V, V_2=65V, and the load R=3.52Ω. The gate signals, v_{gS1} and v_{gS2}, are synchronized at turn on with $d_1>d_2$ (figure 3.10). The inductors current have three slopes, as can be seen in figure 3.11., corresponding to the operating modes IV, I and III. The output voltage obtained from simulation is 31V, similar to the value obtained from analytical calculation.

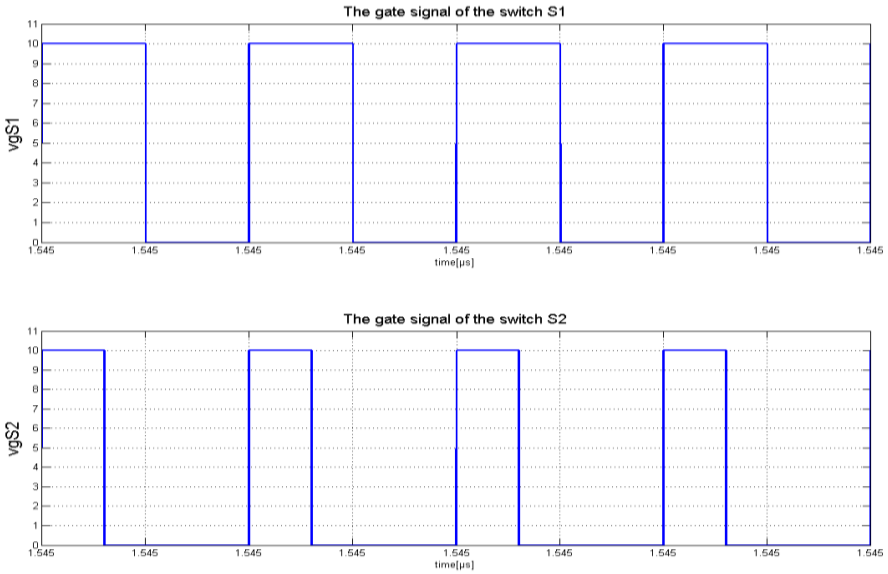


Figure 3.10. The control signals of the HBL when $d_1 > d_2$.

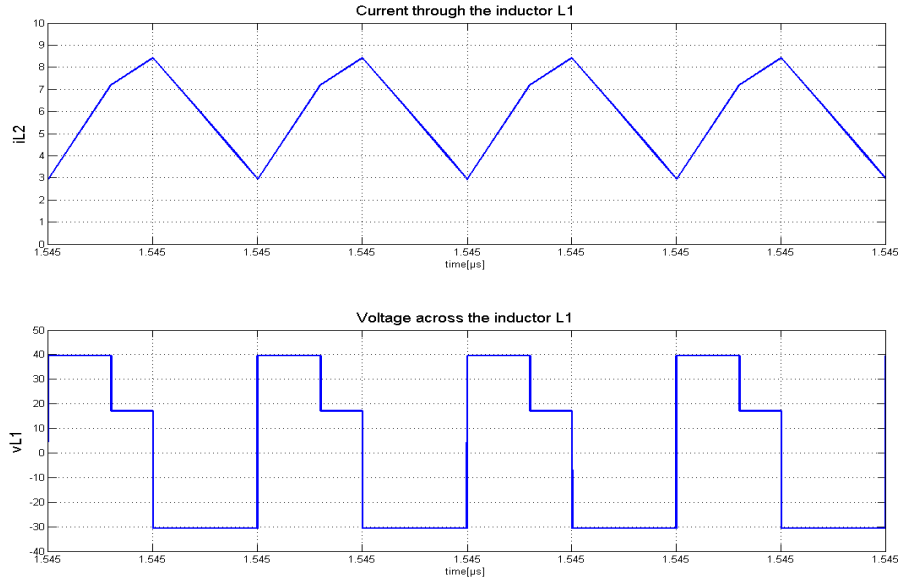


Figure 3.11. Inductor L_1 current and voltage when $d_1 > d_2$.

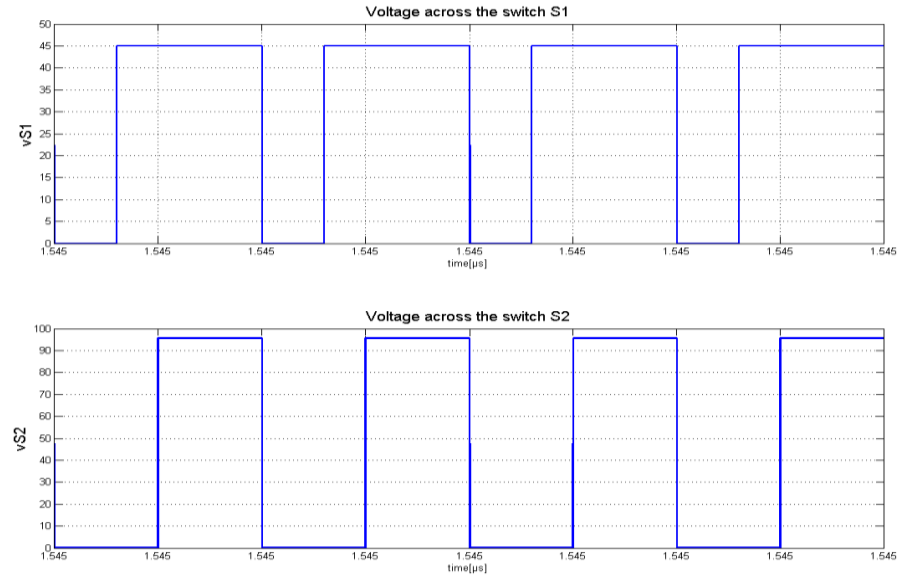


Figure 3.12. The voltages across the switches when $d_1>d_2$.

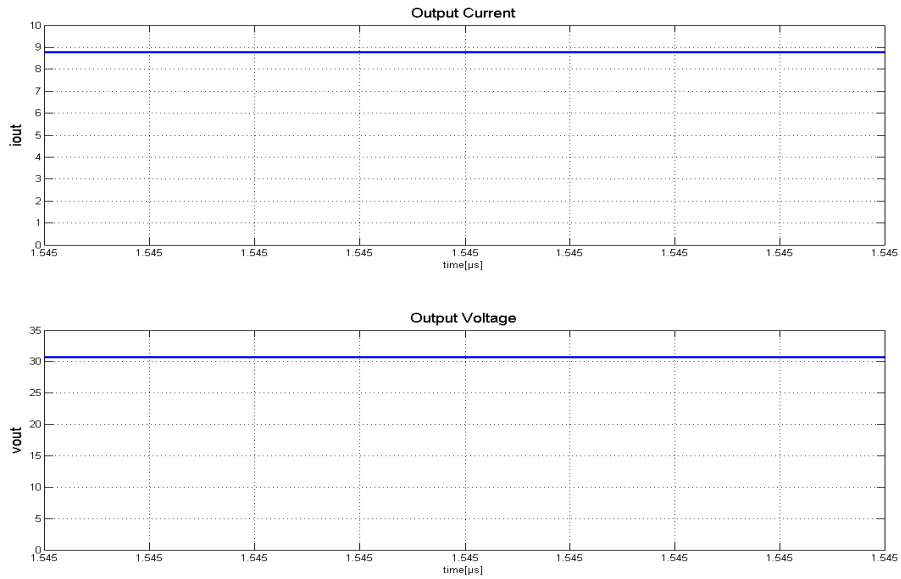


Figure 3.13. Output current and voltage when d_1=50% and d_2=30%.

3.3.2. Simulation results for $d_1 \leq d_2$

Figures 3.14.-3.17. present the simulation results when the input parameters are: d_1=45%, d_2=70%, V_1=60V, V_2=40V. It can be seen from figure 3.14. that the gate signals of the power switches are synchronized at turn on. The

output voltage is 48.3V which is close to the value obtained analytically, figure 3.17. The output resistance is R=3.2Ω.

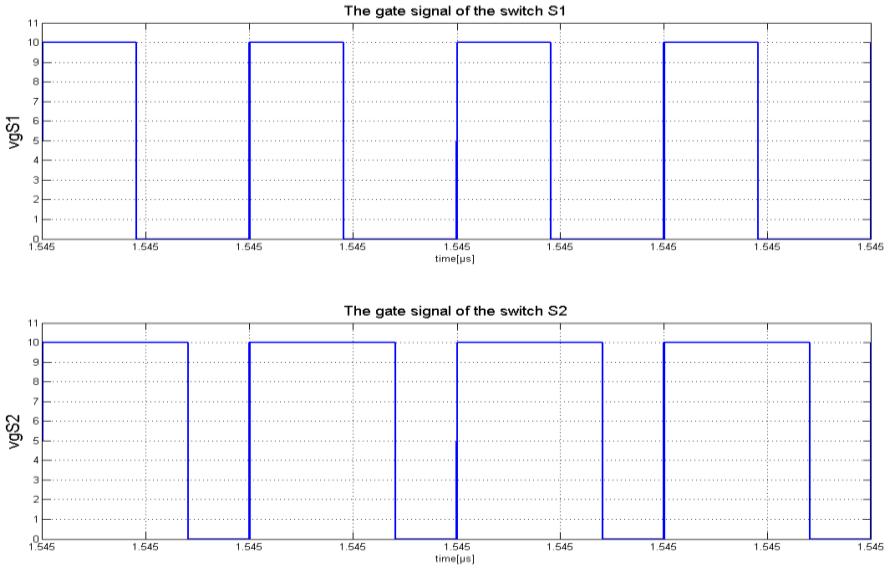


Figure 3.14. The control signals of the HBL converter when $d_1>d_2$.

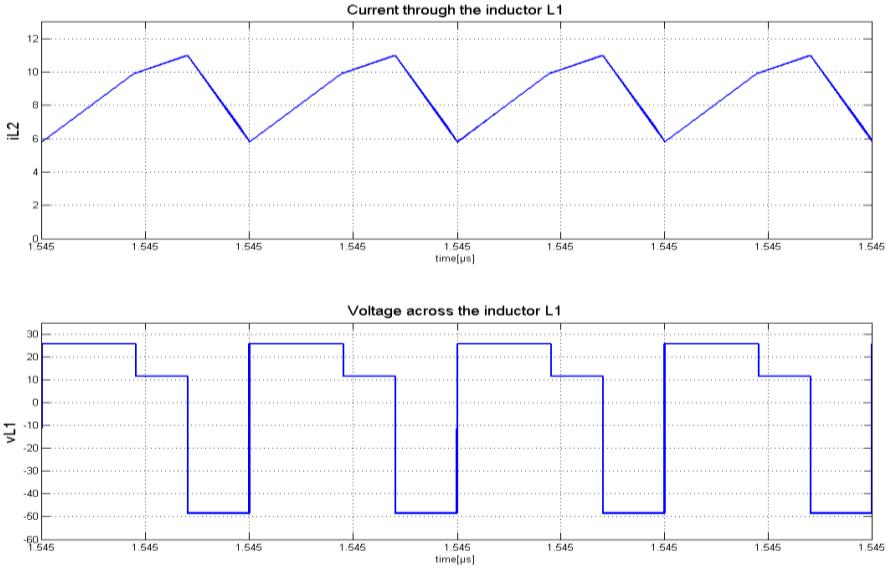


Figure 3.15. Inductor current and voltage when $d_1 \leq d_2$.

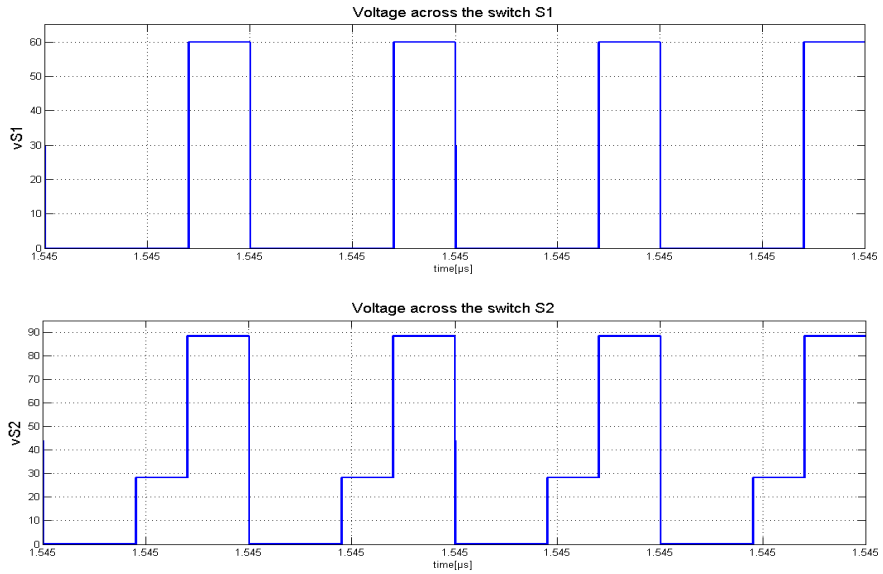


Figure 3.16. The voltages across the switches when $d_1 \leq d_2$.

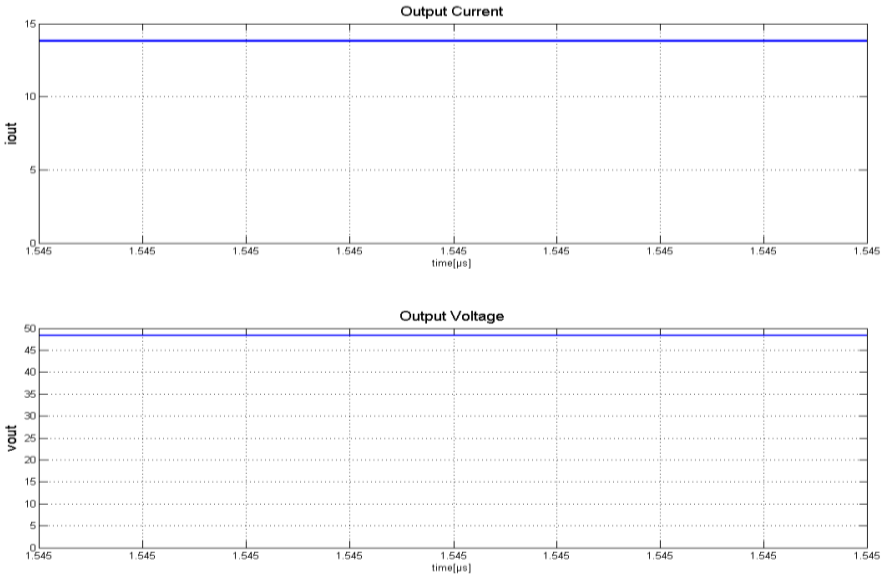


Figure 3.17. Output current and voltage when d_1=45% and d_2=70%.

Figure 3.18. presents the output voltage, as a function of the two duty cycles, in a three-dimensional representation. The input voltages are V_1=50V and V_2=30V. The output voltage has the maximum value $V_0=V_1+V_2$ (80V), when the input sources are connected in series and the duty cycle for each of them is 100%.

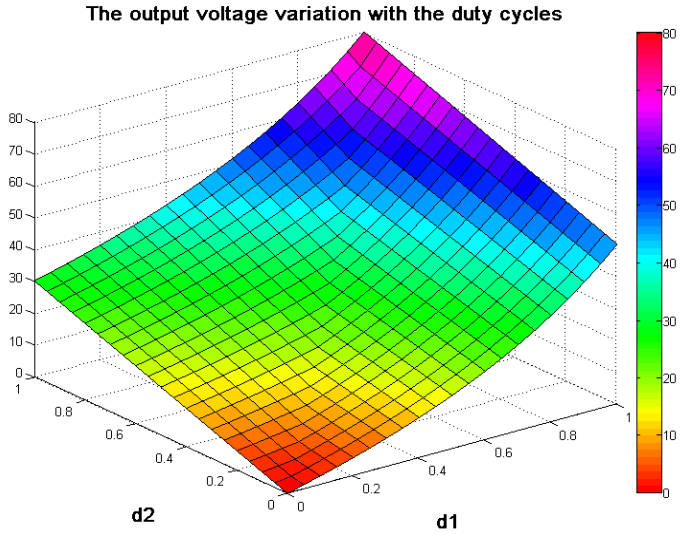


Figure 3.18. The output voltage as a function of the duty cycles.

HBL converter is suitable for application in which the voltage of source V_2 is much higher than the voltage of source V_1. Using the hybrid Buck L converter the input voltage is reduced $(2\text{-}d_2)$ times more than in the classical Buck, used in the upper part of the HBL structure.

3.4. Buck/hybrid Buck C converter

The Buck/hybrid Buck C converter (HBC) is made adding a hybrid Buck C structure to a classical Buck converter, as shown in figure 3.19.

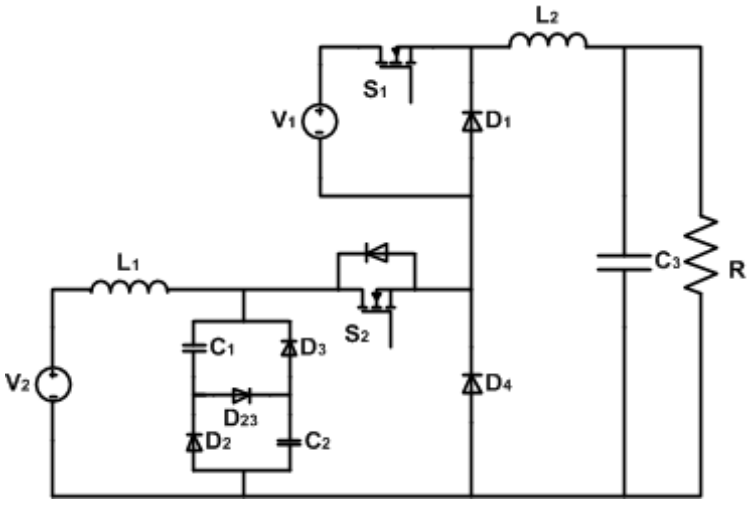


Figure 3.19. The Buck/hybrid Buck C converter topology.

The operating modes of HBC are:

- **mode I**: the power switch S_1 is on and the power switch S_2 is off. The input voltage V_1 will supply the demanded power by the load, as shown in figure 3.20.a. The capacitors C_1 and C_2 are connected in series trough the diode D_{23}. The diodes D_2, D_3 and D_1 are reverse biased and treated as an open circuit. The diode D_4 is forward biased and provides a current path for the source V_1.
- **mode II**: the power switch S_1 is off and the power switch S_2 is on, figure 3.20.b. All demanded power will be supplied by the input source V_2. The capacitors C_1 and C_2 are connected in parallel. The diodes D_2, D_3 and D_1 are forward biased. The diode D_1 provides the current path for the inductor current to flow continuously. The diodes D_{23} and D_4 are reverse biased and considered to be an open circuit.
- **mode III**: the power switches S_1 and S_2 are on, figure 3.20.c. The input sources V_1 and V_2 are supplying the load simultaneously. The source V_2 charges the inductor L_1 and capacitor C_1. The source V_1 charges the inductor L_2. The diodes D_2 and D_3 are forward biased and connected in series with a capacitor. The diodes D_{23}, D_1 and D_4 are reverse biased.
- **mode IV**: the power switches S_1 and S_2 are off, figure 3.20.d. The input source V_2 charges the inductor L_1 and the capacitors C_1 and C_2 while the magnetic energy stored in the inductor L_2 supplies the load. The diodes D_1 and D_4 provide the path for the inductor L_1 current to flow continuously.

The gate signals of the switches S_1 and S_2 are synchronized at turn on.

HBC is able to draw power from both input sources simultaneously or individually. If the switch S_2 is off for the entire switching period, HBC acts as a classical Buck converter.

Depending on the relation between d_1 and d_2 three operating modes are active during one period (for $d_1>d_2$ the operating modes are III, I, IV; for $d_1 \leq d_2$ the operating modes are III, II, IV).

Table 3.5 presents the voltage across the inductors L_1 and L_2 during one period, for all operating modes.

Table.3.5. Voltage across the inductors L_1 and L_2 in one period (for HBC converter)

	Mode I	**Mode II**	**Mode III**	**Mode IV**
S_1	1	0	1	0
S_2	0	1	1	0
V_{L1}	V_2-2V_C	V_2-V_C	V_2-V_C	V_2-2V_C
V_{L2}	V_1-V_0	V_C-V_0	V_1+V_C-V_0	-V_0

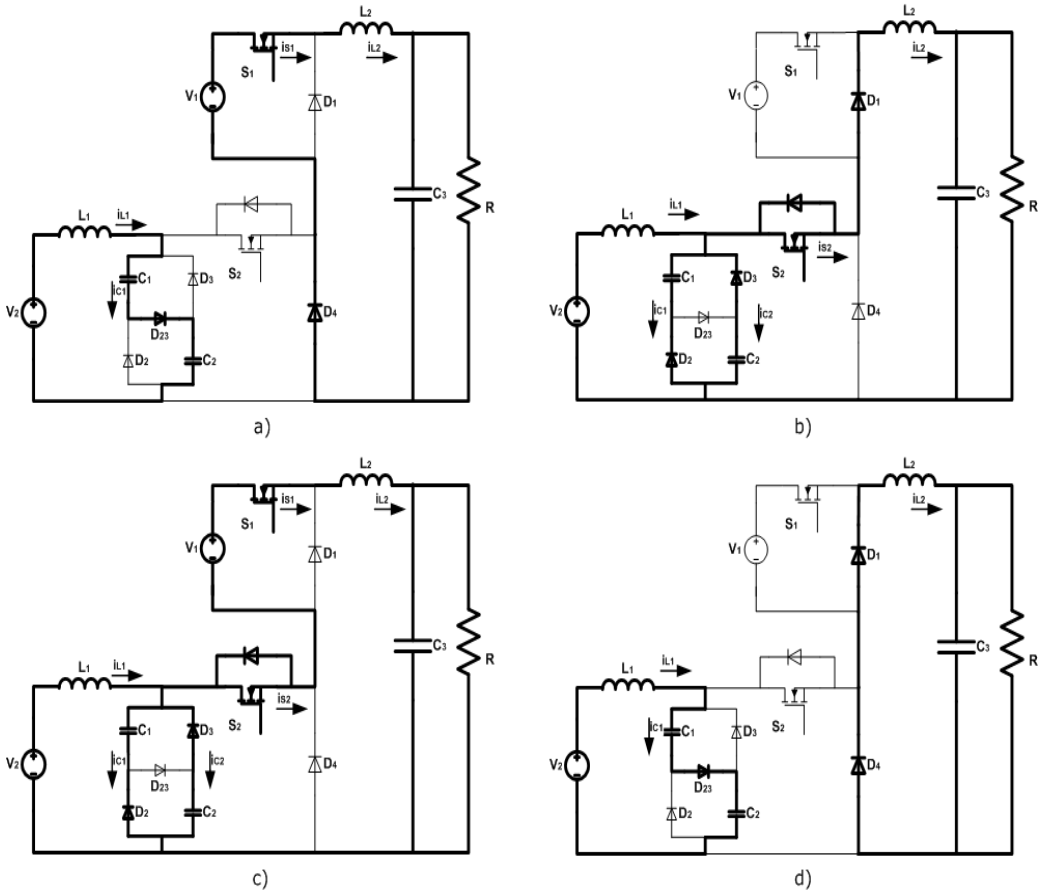


Figure 3.20. HBC operating modes: a) mode I; b) mode II; c) mode III; d) mode IV.

In the first case, when the $d_1>d_2$ the operating modes sequence during one period is III, I, IV. By applying the volt – second balance theorem on the inductors L_1 and L_2, the following equations can be written:

v_{L1}: $$(V_1+V_C-V_0)d_2T+(V_1-V_0)(d_1-d_2)T-V_0(1-d_1)T=0 \quad (3.13)$$

v_{L2}: $$(V_2-V_C)d_2T+(V_2-2V_C)(d_1-d_2)T+(V_2-2V_C)(1-d_1)T=0 \quad (3.14)$$

The voltage across the capacitors can be obtained from equation (3.14):

$$V_C = \frac{1}{2-d_2} V_2 \tag{3.15}$$

For $d_1 \le d_2$, by applying the volt-second balance theorem on the inductors, the following equations can be obtained:

v_{L1}: $$(V_1 + V_C - V_0)d_1 T + (V_C - V_0)(d_2 - d_1)T - V_0(1-d_2)T = 0 \tag{3.16}$$

v_{L2}: $$(V_2 - V_C)d_1 T + (V_2 - V_C)(d_2 - d_1)T + (V_2 - 2V_C)(1-d_2)T = 0 \tag{3.17}$$

From equation (3.17) results the same relation between V_C and V_2. The output voltage has the same expression for $d_1 > d_2$ and for $d_1 \le d_2$:

$$V_0 = d_1 V_1 + \frac{d_2}{2-d_2} V_2 \tag{3.18}$$

For HBC simulation, the system has been developed in Psim. The converter parameters are presented in table 3.6.

Table.3.6. Simulation Parameters

Parameter	Value
Inductor L_1	28μH
Inductor L_2	28 μH
Capacitors C_1 and C_2	2640 μF
Output capacitor C	3960μF
Switching frequency	100kHz

3.4.1. Simulation results for $d_1 > d_2$

Figure 3.21-3.25 presents the simulation results when the input parameters are: d_1=60%, d_2=25%, V_1=40V, V_2=20V and R=3.4Ω. It can be seen that the gate signals of the power switches are synchronized at turn on (figure 3.21). The output voltage is 27V which is similar to the value obtained from analytical calculation (figure 3.24).

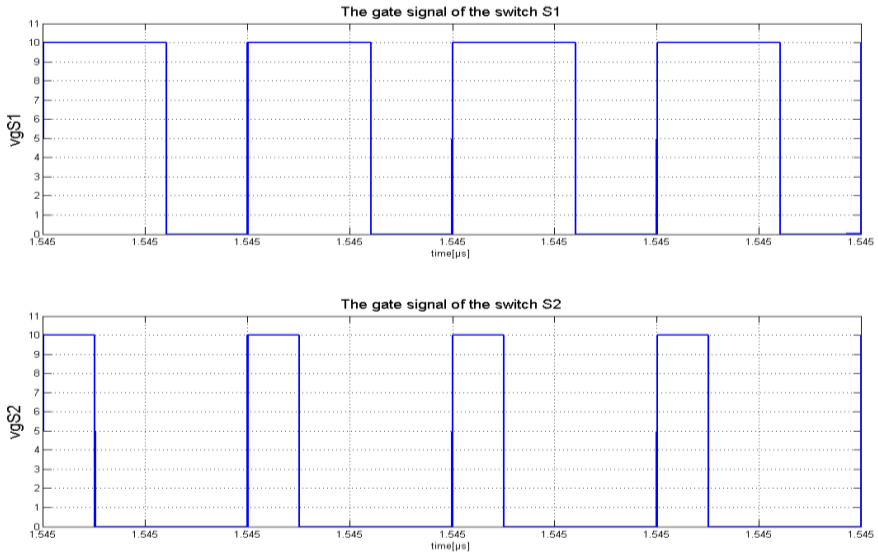


Figure 3.21. The control signals of HBC when $d_1>d_2$.

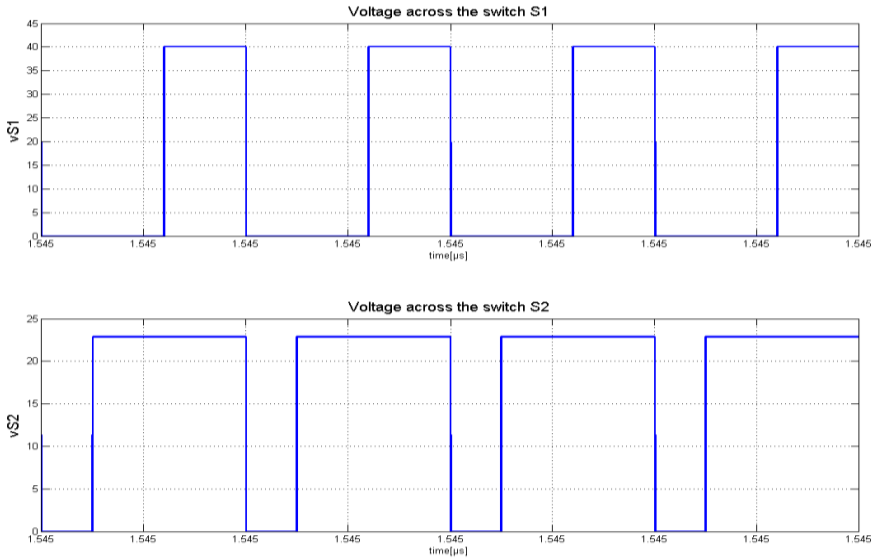


Figure 3.22.The voltage across the switches when $d_1>d_2$.

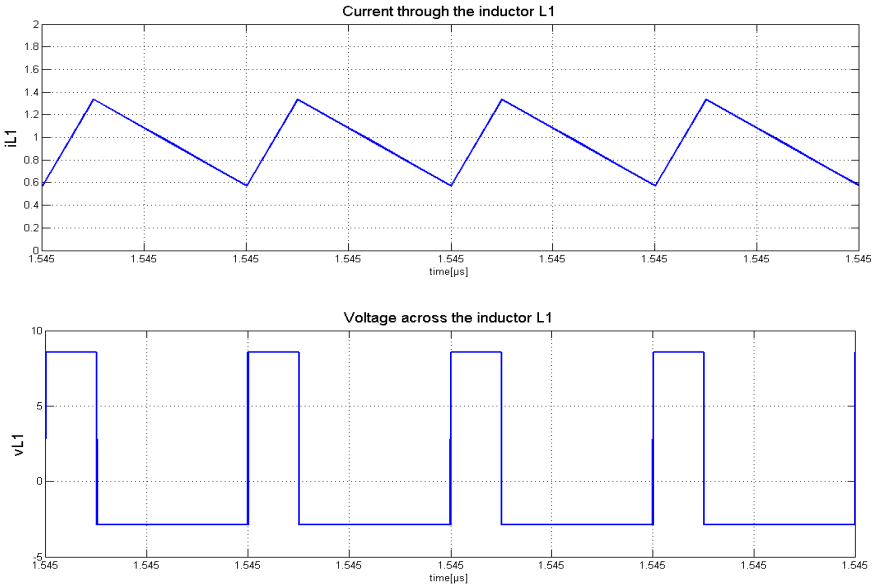


Figure 3.23. Inductor L_1 current and voltage when $d_1>d_2$.

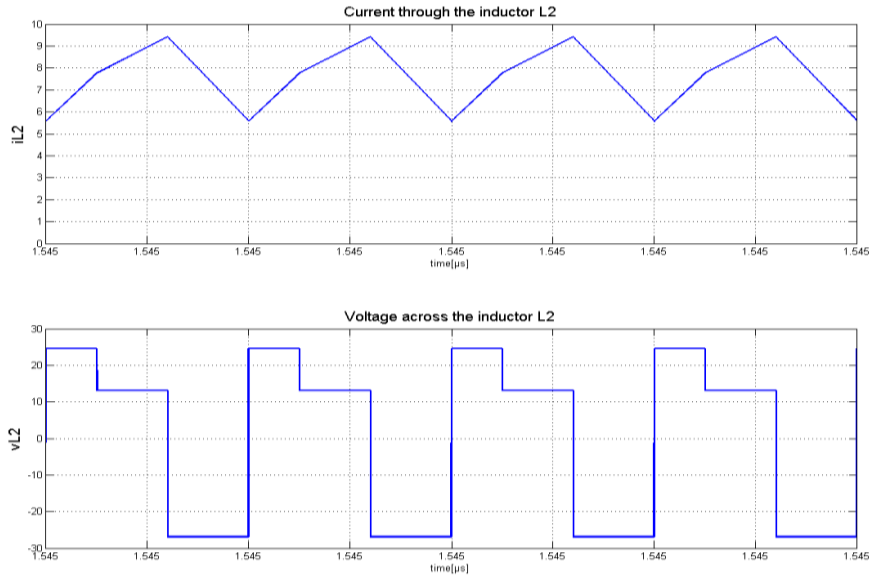


Figure 3.24. Inductor L_2 current and voltage when $d_1>d_2$.

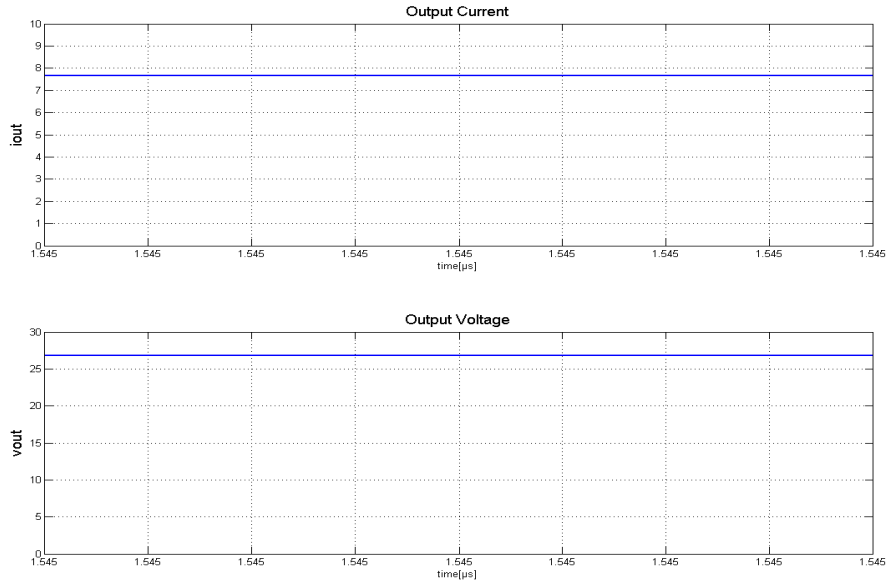


Figure 3.25. Output current and voltage when d_1=60% and d_2=25%.

3.4.2. Simulation results for $d_1 \leq d_2$

Figures 3.26-3.30 present the case with d_1=30%, d_2=70%, V_1=40V, V_2=60V and R=3.31Ω. The gate signals v_{gS1} and v_{gS2} are synchronized at turn on. The current through the inductors has three slopes as can be seen from fig 3.16, corresponding to three time operating modes III, II and IV.

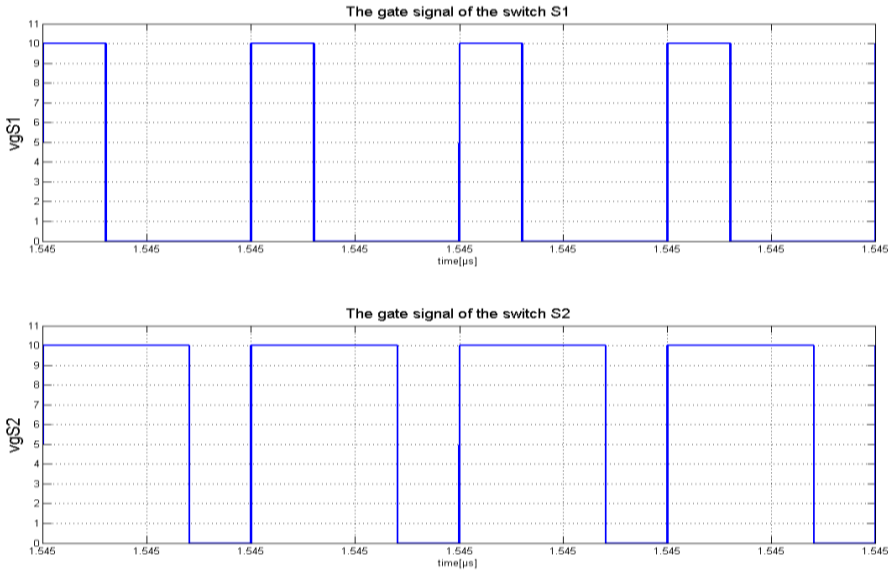


Figure 3.26. The control signals of the HBL when $d_1 \leq d_2$.

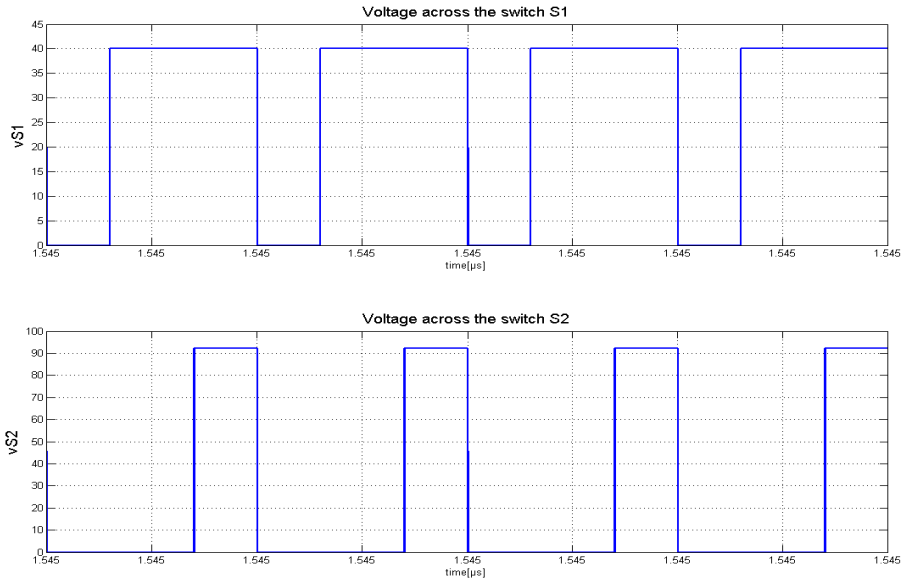


Figure 3.27. The voltage across the switches $d_1 \leq d_2$.

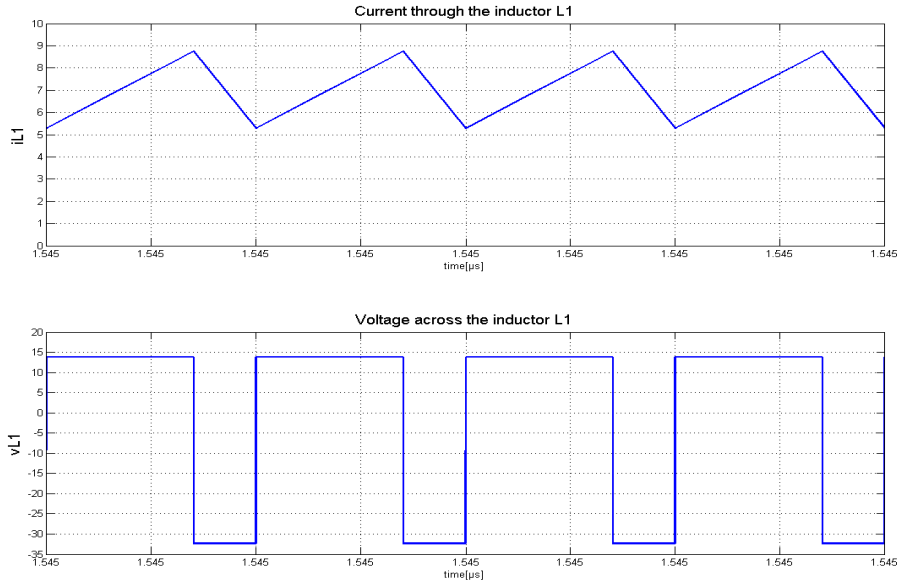


Figure 3.28. Inductor L_1 current and voltage when $d_1 \leq d_2$.

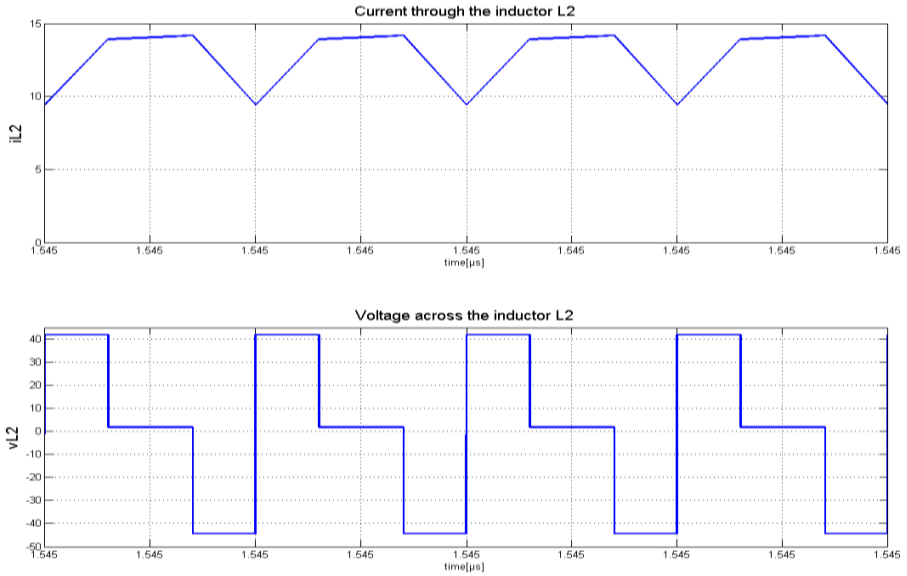


Figure 3.29. Inductor L_2 current and voltage when $d_1 \leq d_2$.

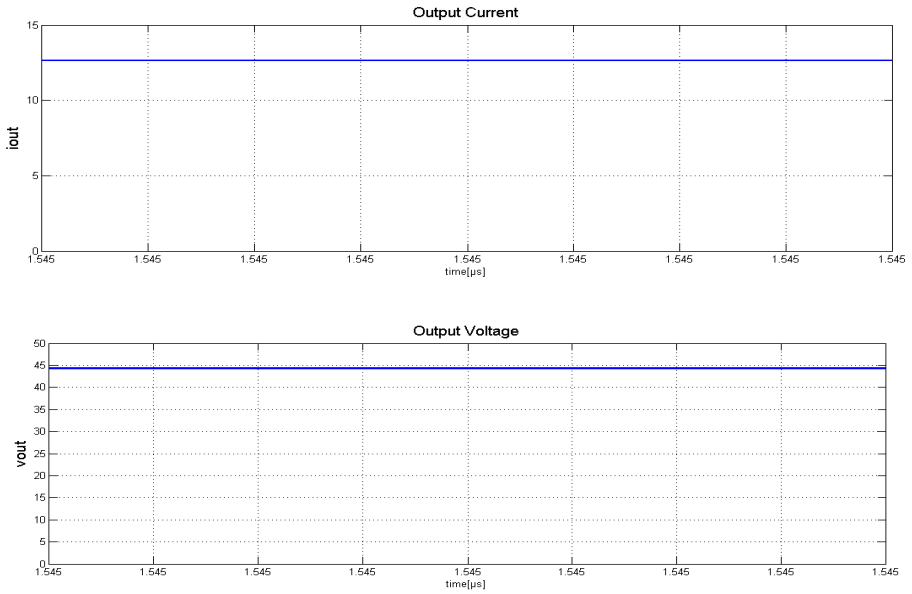


Figure 3.30. Output current and voltage when d_1=30% and d_2=70%.

Figure 3.31. presents the output voltage, as a function of the two duty cycles, in a three-dimensional representation. The input voltages are V_1=20V and V_2=40V. The output voltage has the maximum value $V_0=V_1+V_2=$60V, when the input sources are connected in series and the duty cycle for each of them is 100%.

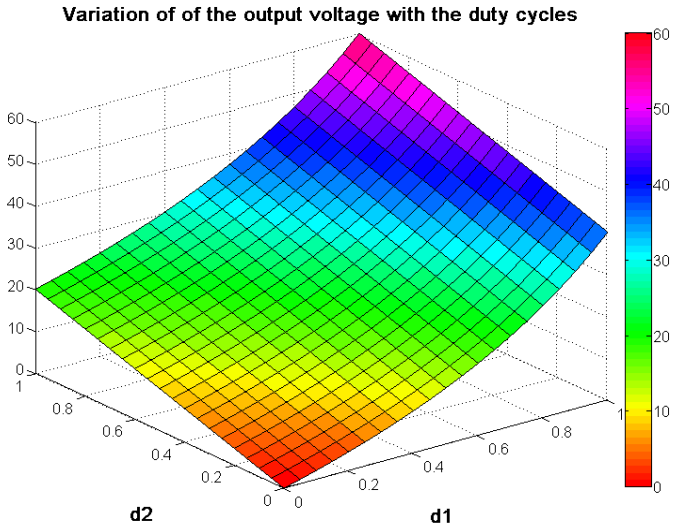


Figure 3.31. The output voltage as a function of the duty cycles.

3.5. Hybrid Buck C/hybrid Buck L converter

The proposed converter topology (figure 3.32) consists of two hybrids Buck structures (hybrid Buck L and hybrid Buck C).

By applying the PWM gate signals to the power switches S_1 and S_2 the hybrid Buck C/hybrid Buck L converter (HBCL) can draw power from the two voltage sources individually, or simultaneously.

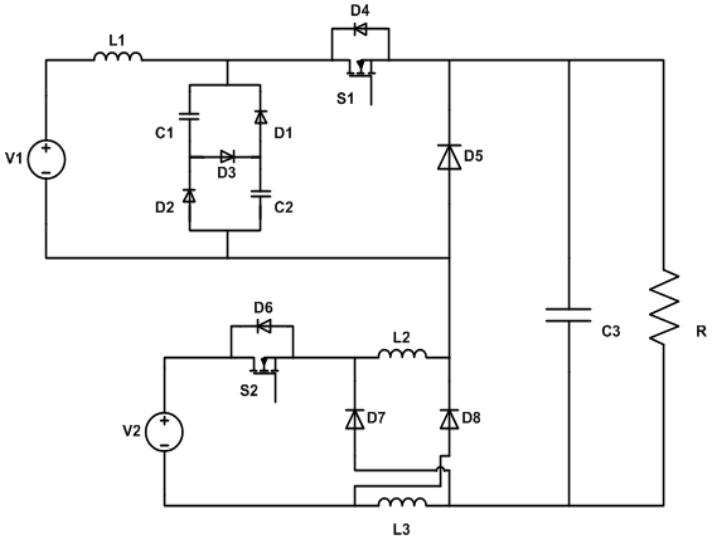


Figure 3.32. The topology of the HBCL.

The operating modes of HBCL are:

- **mode I:** the switch S_1 is on and the switch S_2 is off. The equivalent circuit is presented in figure 3.33.a. The capacitors C_1 and C_2 are connected in parallel. The diode D_3 and D_5 are reverse biased and treated as an open circuit, while D_1, D_2, D_7 and D_8 provide a bypass path for the inductors currents. In this mode, the voltage source V_1 will charge the inductors L_1 and provides the electrical energy to the load;
- **mode II:** the switch S_1 is off and the switch S_2 is on. Figure 3.33.b shows the equivalent circuit. The diodes D_1, D_2, D_7 and D_8 are reverse biased while D_3 and D_5 are forward biased. The voltage source V_2 will charge the inductors L_2 and L_3 and supply the load. The voltage source V_1 will charge the capacitors C_1 and C_2 (connected in series).
- **mode III:** the switches S_1 and S_2 are on. Figure 3.33.c presents the equivalent circuit. The diodes D_1 and D_2 together with C_1 and C_2 will provide the current path for the inductors L_2 and L_3. The voltage sources V_1 and V_2 will supply the load with the electric energy.
- **mode IV:** both switches, S_1 and S_2, are off. The equivalent circuit is shown in figure 3.33.d. The load will be supplied with the energy stored in the capacitor C_3 and inductors L_2 and L_3.

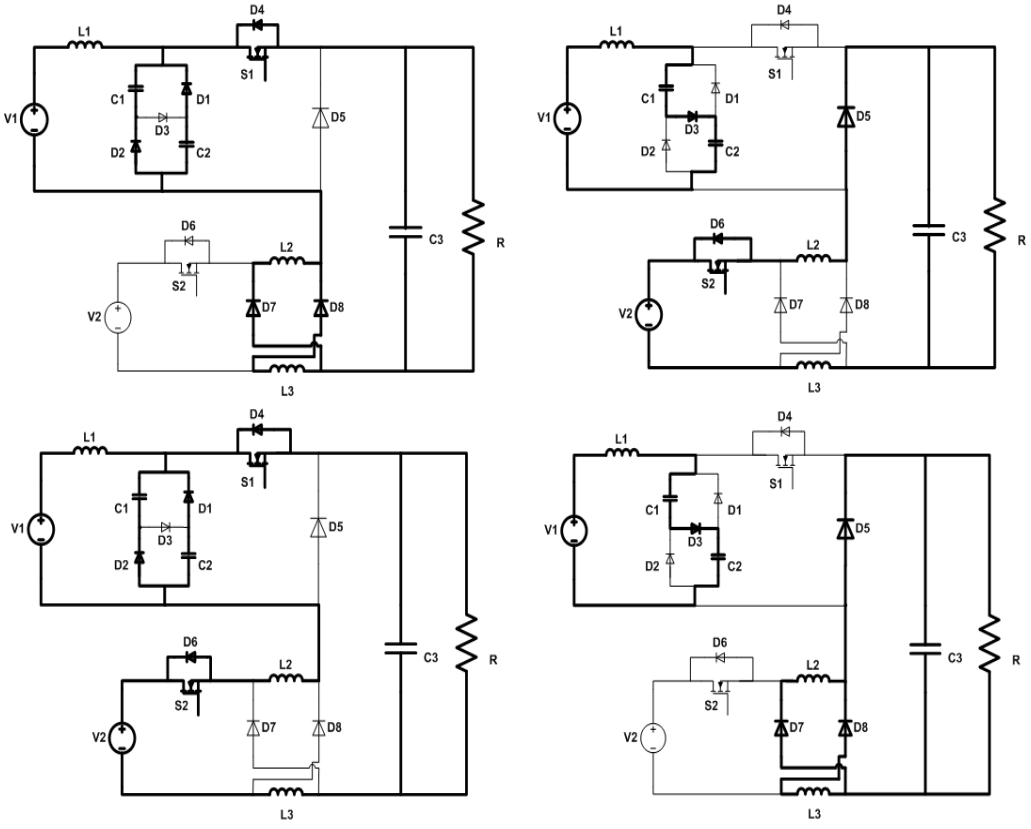


Figure 3.33. HBCL operating modes: a) mode I; b) mode II; c) mode III; d) mode IV.

The gate signals of the switches S_1 and S_2 are synchronized at turn on.

Depending on the relation between d_1 and d_2 three operating modes are active during one period (III, I, IV for $d_1>d_2$ and III, II, IV for $d_1\leq d_2$).

Table 3.7 presents the voltage across the inductors L_1 and L_2 during one period. The voltages are presented for all four operating modes.

Table.3.7. Voltage across the inductors L_1 and L_2 in one period (for HBCL)

	Mode I	**Mode II**	**Mode III**	**Mode IV**
S_1	1	0	1	0
S_2	0	1	1	0
v_{L1}	V_1-V_C	V_1-2V_C	V_1-V_C	V_1-2V_C
v_{L2}	V_C-V_0	½(V_2-V_0)	½(V_2+V_C-V_0)	-V_0

When the $d_1>d_2$ by applying the volt – second balance theorem on the inductors L_1 and L_2, the following equations can be obtained:

v_{L1}: $$V_1-V_C\ d_1T+\ V_1-2V_C\quad d_2-d_1\ T+\ V_1-2V_C\quad 1-d_2\ T=0 \tag{3.19}$$

v_{L2}: . $$\frac{1}{2}(V_2+V_C-V_0)d_2T+\ V_C-V_0\quad d_1-d_2\ T+\ -V_0\quad 1-d_1\ =0 \tag{3.20}$$

From the equation (3.19) the capacitor voltage can be written as:

$$V_C=\frac{1}{2-d_1}V_1 \tag{3.21}$$

If $d_1\leq d_2$, by applying the volt-second balance theorem on the inductors, the following equations can be obtained:

v_{L1}: $$V_1-V_C\ d_1T+\ V_1-2V_C\quad d_2-d_1\ T+\ V_1-2V_C\quad 1-d_2\ T=0 \tag{3.22}$$

v_{L2}: $$\frac{1}{2}\ V_2+V_C-V_0\ d_1T+\frac{1}{2}\ V_2-V_0\quad d_2-d_1\ T+\ -V_0\quad 1-d_2\ =0 \tag{3.23}$$

From equations (3.20) and (3.23) the output voltage expressions for $d_1>d_2$, and $d_1\leq d_2$ respectively, can be obtained:

$$V_0=\frac{2d_1-d_2}{(2-d_1)(2-d_2)}V_1+\frac{d_2}{2-d_2}V_2 \tag{3.24}$$

$$V_0 = \frac{d_1}{(2-d_1)(2-d_2)}V_1 + \frac{d_2}{2-d_2}V_2 \tag{3.25}$$

For HBCL digital simulations have been developed in Psim. The parameters used for simulations are presented in table 3.8.

Table.3.8. Simulation parameters for HBCL.

Parameter	Value
Inductors L_1	28µH
Inductors L_2 and L_3	28 µH
Capacitors C_1 and C_2	2640 µF
Output capacitor C	3960µF
Switching frequency	100kHz

3.5.1. Simulation results for $d_1>d_2$

Figures 3.34-3.38. present the simulation results when d_1=70%, d_2=35%, V_1=60V, V_2=30V. It can be seen that the gate signals of the power switches are synchronized at turn on. The output voltage is 40V, similar to the value obtained analytically.

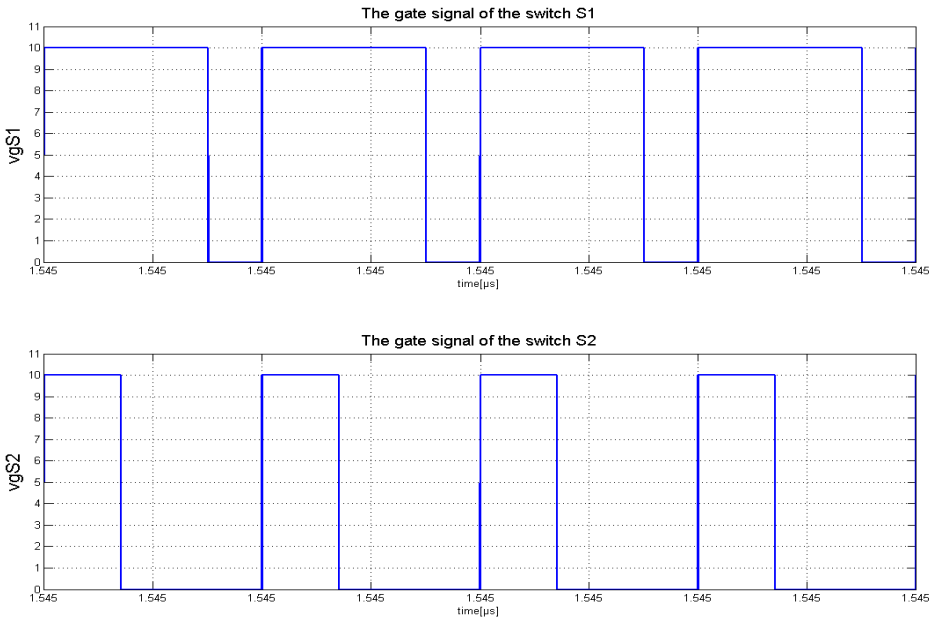


Figure 3.34. The control signals of the HBCL with $d_1>d_2$.

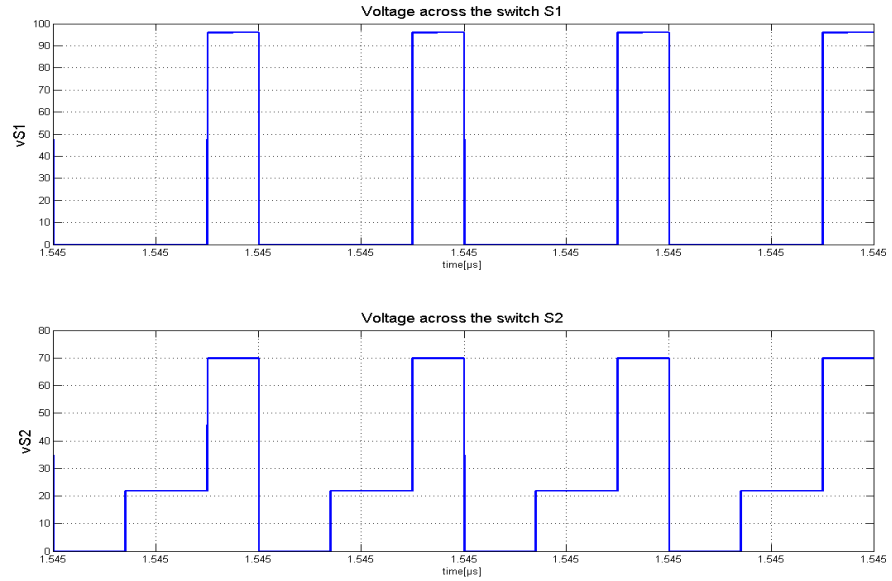


Figure 3.35. The voltage across the switches with $d_1>d_2$.

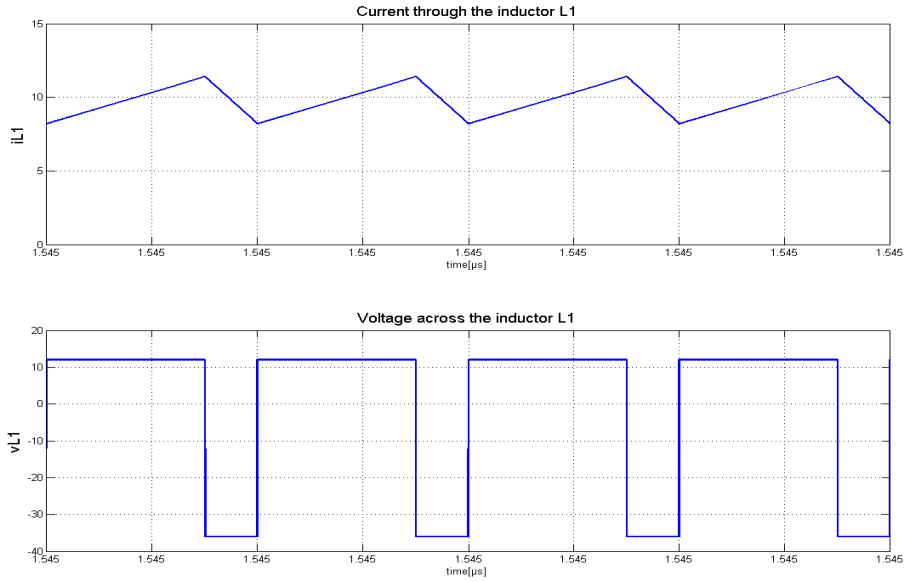


Figure 3.36. Inductor L_1 current and voltage with $d_1>d_2$.

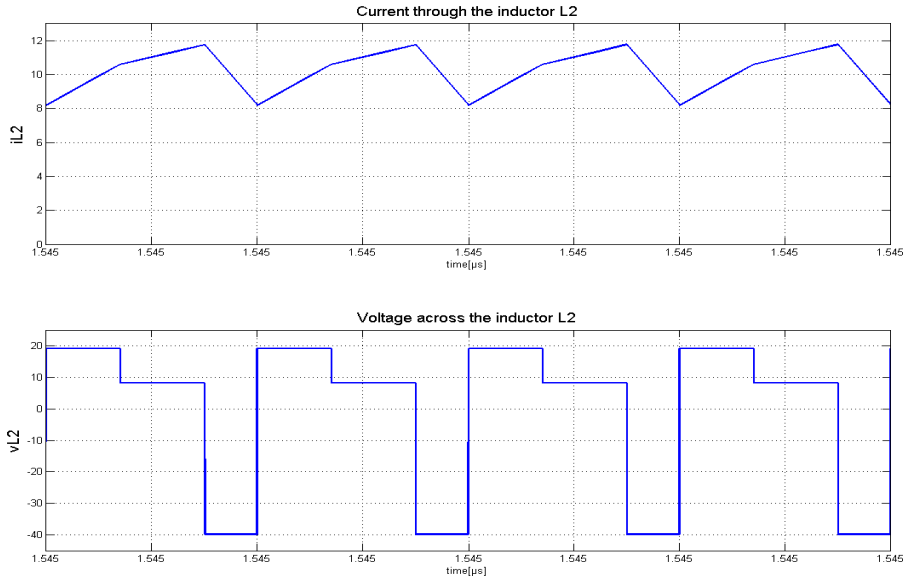


Figure 3.37. Inductor L_2 current and voltage with $d_1>d_2$.

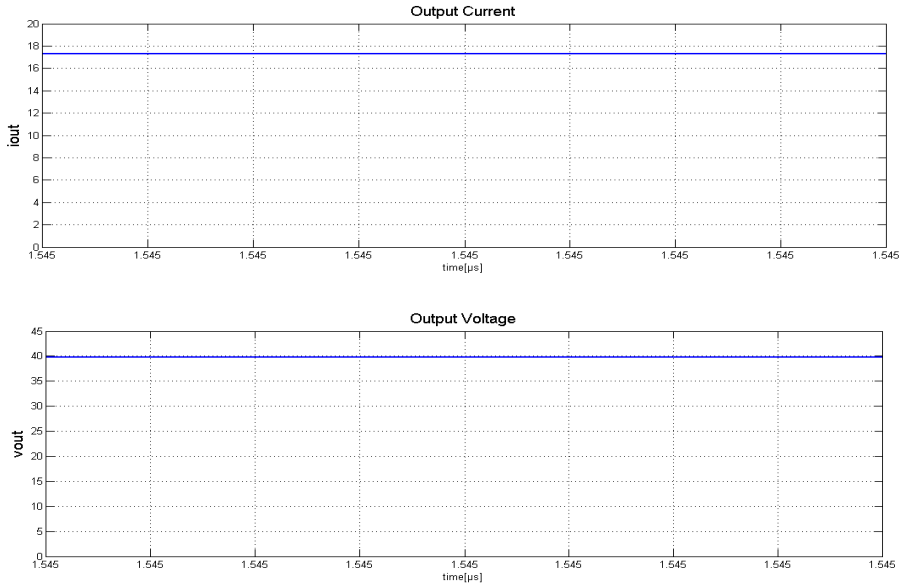


Figure 3.38. Output current and voltage with $d_1>d_2$.

3.5.2. Simulation results for $d_1 \leq d_2$

Figures 3.39.-3.43. present the case when d_1=25%, d_2=65%, V_1=45V and V_2=60V. It can be seen that the gate signals v_{gS1} and v_{gS2} are synchronized at turn on. The output voltage is 34.5V and the output current is 14.5A.

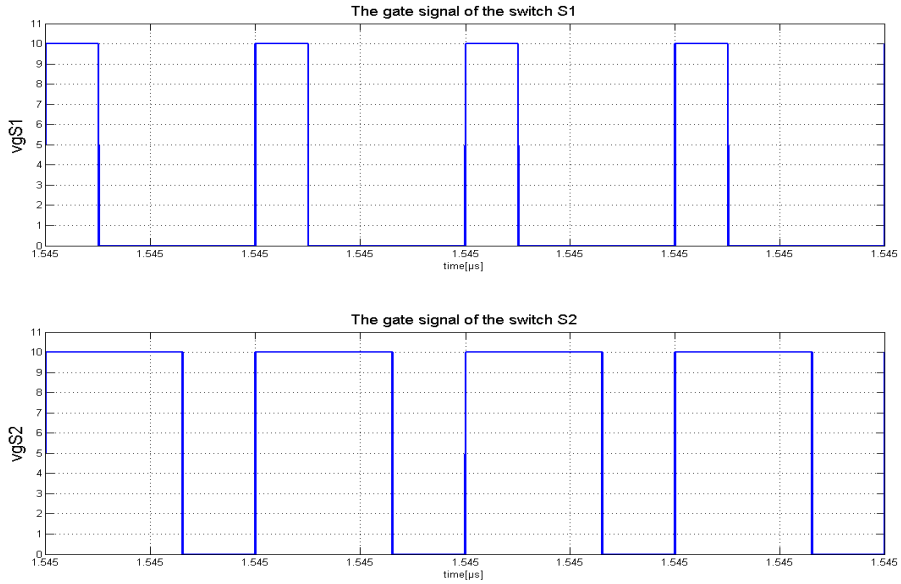


Figure 3.39. The control signals of the HBCL when $d_1 \leq d_2$.

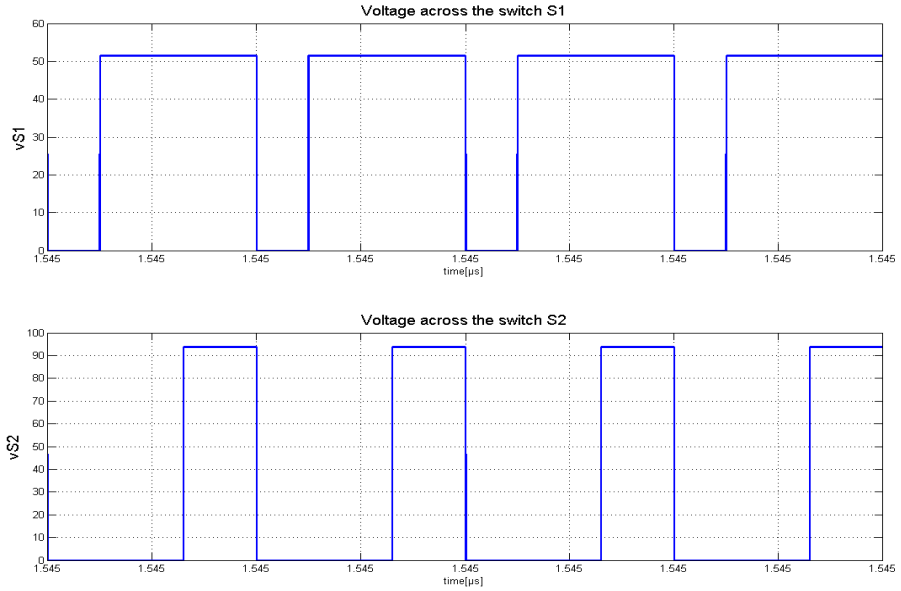


Figure 3.40. The voltage across the switches when $d_1 \leq d_2$.

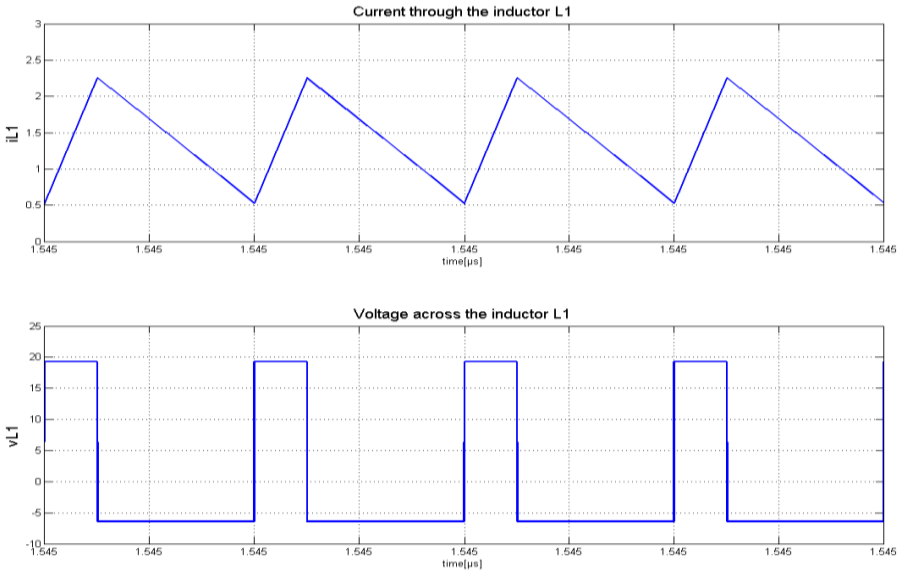


Figure 3.41. Inductor L_1 current and voltage when $d_1 \leq d_2$.

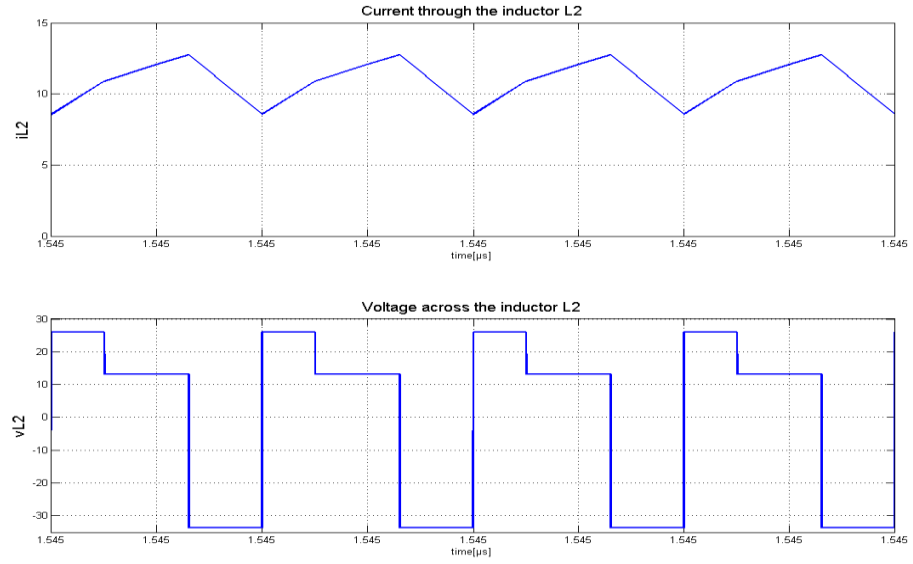


Figure 3.42. Inductor L_2 current and voltage when $d_1 \leq d_2$.

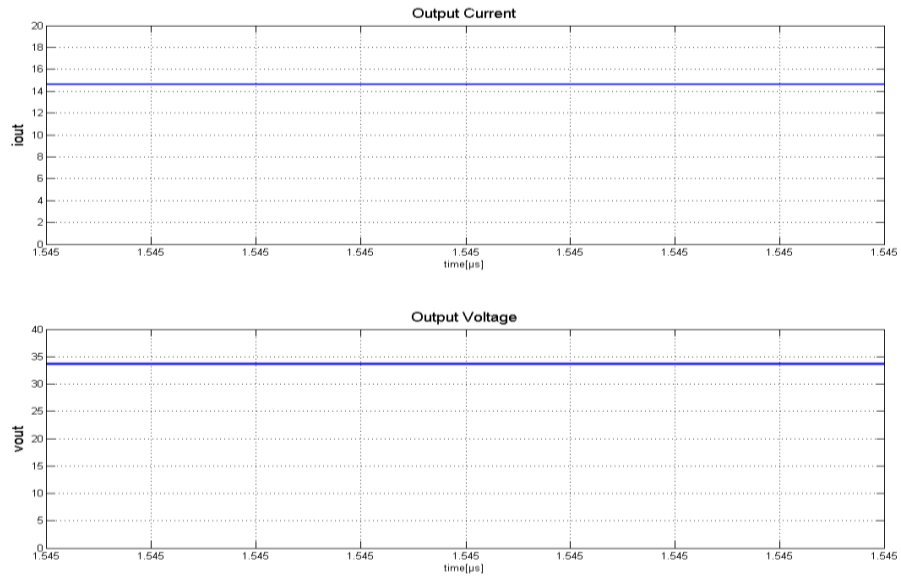


Figure 3.43. Output results when d_1=25% and d_2=65%.

Figure 3.44. presents the output voltage, as a function of the duty cycle in a three-dimensional representation. The input voltages are V_1=18V and V_2=60V. The output voltage has the maximum value $V_0=V_1+V_2$=78V, when the input sources are connected in series and the duty cycle for each of them is 100%.

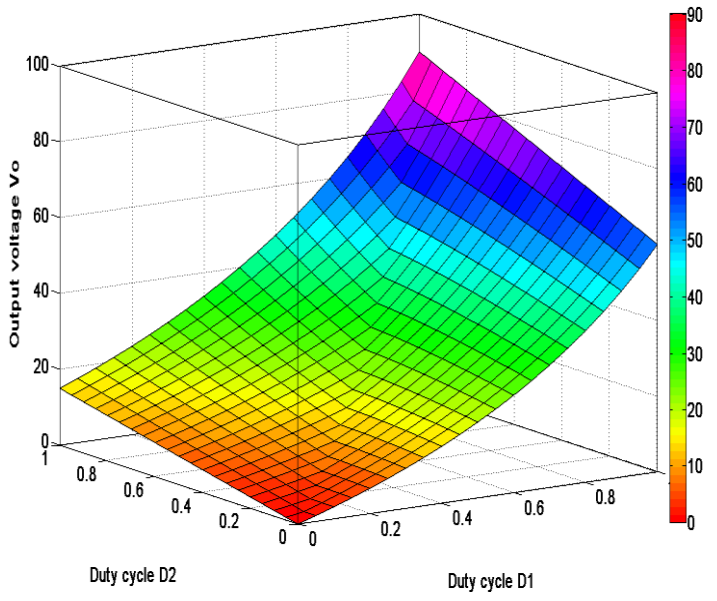


Figure 3.44. The output voltage as a function of the duty cycles.

From HBCL simulation with real components was obtained an average efficiency of 94%. The digital simulation was made in LTSpice, which has a very good database with real components models.

3.5.3. Experimental results

HBCL was implemented in laboratory in order to verify the analytical considerations and the simulation results. The prototype was build for a switching frequency of 7.8kHz.

The gate signals of the power switches S_1 and S_2 are synchronized at turn on with the duty cycles $d_1>d_2$ (d_1= 55% and d_2= 25%).

The input voltages are V_1=30V and V_2=60V.

A detailed presentation of the prototype is given in chapter 6 "Experimental Platform".

The experimental results are presented in figure 3.45. It can be seen the good correspondence with the simulations. The current through the inductor L_1 has two slopes corresponding to the conduction time of the power switches S_1. The current through the inductor L_2 has three slopes: one during the time when the power switches S_1 and S_2 are on, one for the time when only the power switch S_1 is on, and one for the time when the both power switches are off.

3.6. Conclusions

In this chapter dual input DC-DC converters, with hybrid structures, have been proposed and analyzed.

From the possible combinations of the classical with hybrid converters and hybrid with hybrid converters, only four dual input structures have been chosen:

- dual input Buck/ hybrid Buck L;
- dual input Buck/ hybrid Buck C;
- dual input hybrid Buck C/ hybrid Buck L;
- dual input hybrid Buck L/ hybrid Buck C.

An analytical study was presented for the first three configurations. Operating modes, the output voltage as function of the input voltages and duty cycles were expressed.

Digital simulations were carried out in Psim and a corresponding analysis was made for the obtained results.

HBCL was implemented in a laboratory prototype, at 7.8kHz. The good correspondence of the experimental and simulation results validates the theoretical considerations.

For efficiency estimation, the real circuit configuration, with components models, was simulated using LTSpice. An average efficiency of 94%, obtained at different duty cycles, proves thet HBCL is, from this point of view to, a viable solution in power electronics.

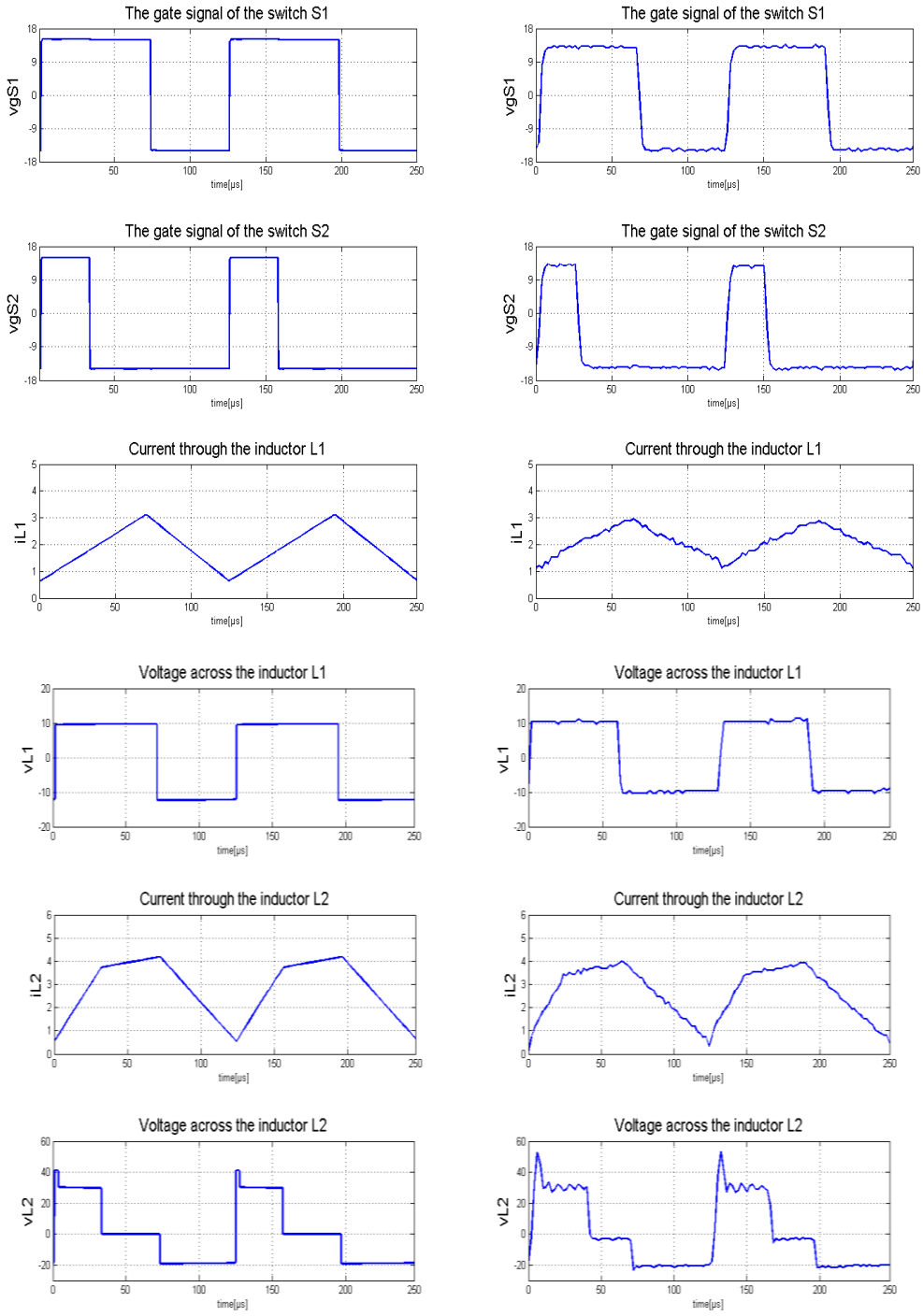


Figure 3.45. The simulation (left) and experimental results (right) for HBCL.

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CHAPTER 4
Dual Input, Hybrid Buck LC (HBLC), DC-DC Converters

4.1. Introduction

In the previous chapters, a systematic approach to synthesizing dual input DC-DC converters with hybrid and/or classical structures was presented.

In this chapter the dual input hybrid Buck LC converter (HBLC), generated with the synthesizing method [1-3], is proposed.

Compared with HBCL, HBLC has a major advantage: one converter input source and the output can have a common ground. This is the main reason in choosing this structure for a detailed study and, in the next chapter, for an application in the renewable energy conversion field.

A complete analysis of HBLC is made, including analytical description, and operating modes topology, at CCM and BCM.

Simulation results will come to validate the theoretical concepts.

Different simulations software were chosen (LTSpice and PLECS), depending on the intended scope (LTSpice for efficiency and PLECS for main waveform determination).

The theoretical results are validated through experiments, performed on a laboratory prototype.

As illustrated in figure 4.1 HBLC contains two hybrids Buck cells: a hybrid Buck L cell in the upper part, and a hybrid Buck C cell in the lower part [4-6].

Depending on the PWM gate signals applied to the power switches S_1 and S_2, HBLC can draw power from both input sources without any restriction.

For the same switching frequency, the power switches S_1 and S_2 can be synchronized at turn-on or turn-off time.

Figure 4.2 presents the typical voltage and current waveforms for the key components of the HBLC in CCM, under the turn on synchronization. From the top to the bottom, they are: the gate signal of the switch S_1 (v_{gS1}), the gate signal of the switch S_2 (v_{gS2}), the inductor L_1 current (i_{L1}), the voltage across the inductor L_1 (v_{L1}), the inductor L_2 current (i_{L2}), the voltage across the inductor L_2 (v_{L2}), the input current of the hybrid L converter (i_1), the input current of the hybrid C converter (i_2), the current through the switch S_1 (i_{S1}), and the current through the switch S_2 (i_{S2}).

It can be seen from figure 4.2 that the power switches S_1 and S_2 have different conduction times. In this case, the duty cycle for S_1 is smaller than the duty cycle of the switch S_2.

The voltage waveform across the inductor L_2 has three different levels, which are determined by the on-off status of the main power switches S_1 and S_2.

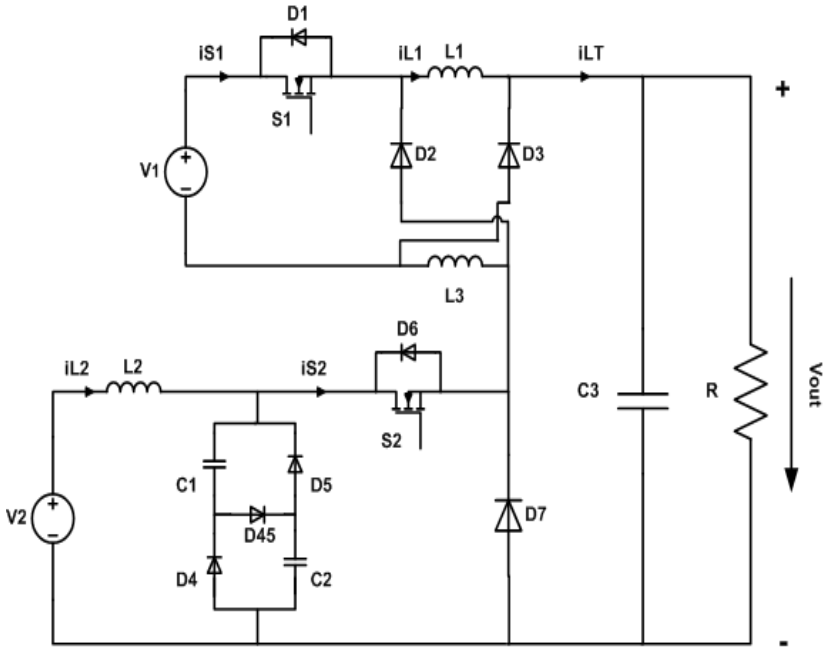

Figure 4.1. The topology of HBLC.

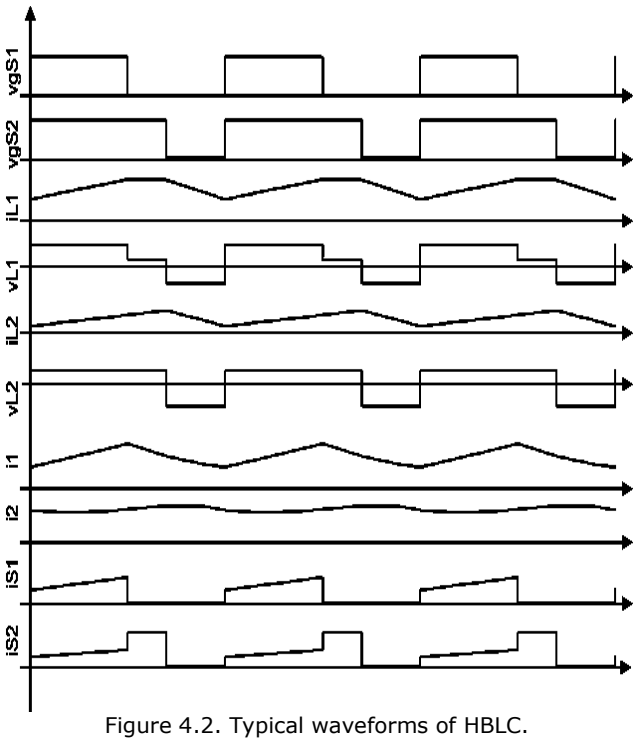

Figure 4.2. Typical waveforms of HBLC.

Considering that the inductors L_1 and L_3 have equal values, only the waveforms for the inductor L_1 will be presented. The inductor current waveform i_{L2} has three different slopes based on the three different inductor voltage values.

The current through the inductors L_2 has two slopes based on the on/off status of the power switch S_2. The input currents i_1 and i_2 represent the currents of the input sources V_1 and V_2.

The output capacitor C_3 is assumed to be very large in order to obtain a nearly constant output voltage. The capacitors C_1 and C_2 are considered to have the same capacitance.

Under normal operation, HBLC can provide electric energy from both input voltage sources simultaneously, but if one of the voltage sources is harmed, the other one can continue to deliver power to the load normally.

4.2. Operation principle of HBLC

According to the status of the power switches S_1 and S_2 the HBLC has four different operating modes, as figure 4.3 shows, which are presented as follows[7, 8]:

- **mode I**: The switch S_1 is on and the switch S_2 is off. The equivalent circuit of this mode is presented in figure 4.3. The capacitors C_1 and C_2 are connected in series. The diodes D_2, D_3, D_4 and D_5 are reverse biased and treated as an open circuit while D_7 and D_{45} provide a bypass path for the inductors currents. In this mode, the voltage source V_1 will charge the inductors L_1 and L_3, and provides the electrical energy to the load. The voltage source V_2 will charge the inductor L_2 and the capacitors C_1 and C_2;
- **mode II**: The switch S_1 is off and the switch S_2 is on. Figure 4.4 shows the equivalent circuit. The diodes D_{45} and D_7 are reverse biased while D_2, D_3, D_4 and D_5 are forward biased. The voltage source V_2 will charge the inductors L_1, L_2 and L_3 and supply the load. The capacitors C_1 and C_2 are connected in parallel.
- **mode III**: The switches S_1 and S_2 are on. Figure 4.5 presents the equivalent circuit. The diodes D_4 and D_5 are forward biased and the others are blocked. The voltage sources V_1 and V_2 will supply the load with energy.
- **mode IV**: Both switches, S_1 and S_2, are off. The equivalent circuit is shown in figure 4.6. The inductors L_1 and L_3 supply the demanded power. The source V_2 will charge the inductor L_2 and the capacitors C_1 and C_2.

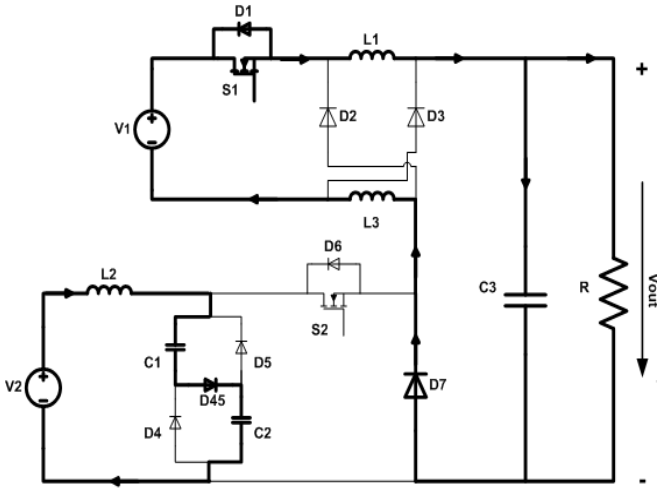

Figure 4.3. Operating mode topology for S_1 on.

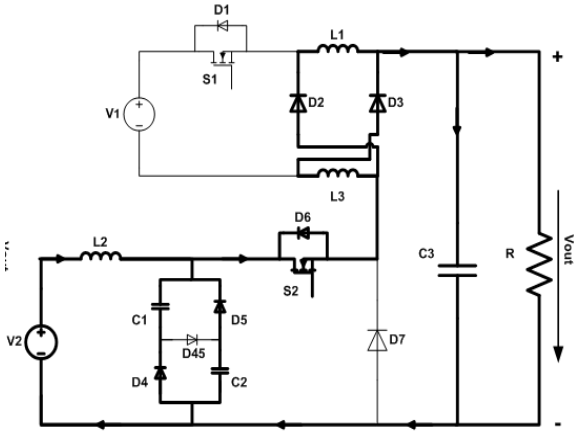

Figure 4.4. Operating mode topology for S_2 on.

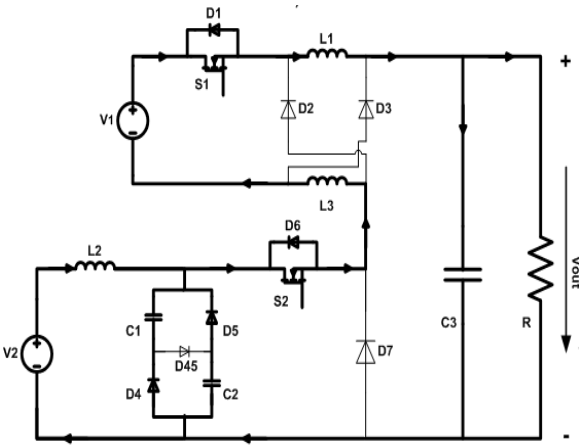

Figure 4.5. Operating mode topology for S_1 and S_2 on.

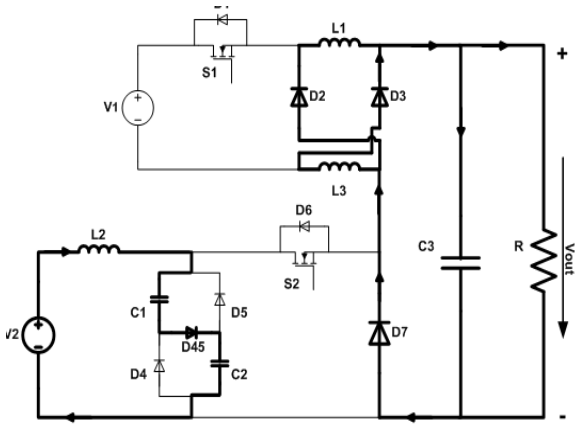

Figure 4.6. Operating mode topology for S_1 and S_2 off.

4.3. Output voltage

To calculate the input to output voltage ratio, it is assumed that the gate signals of the switches S_1 and S_2 are synchronized at turn on and have different conduction times.

If the power switch S_2 is off for the entire switching period HBLC acts as a hybrid Buck L converter, respectively hybrid Buck C converter if the power switch S_1 is off.

Depending on the relation between d_1 and d_2, three operating modes are active during one period $T = t_{on} + t_{off}$. The operating mode orders is exactly as the sequences presented for HBCL (for $d_1>d_2$ the operating mode order are III, I, IV; for $d_1 \leq d_2$ the operating mode are III, II, IV).

Table 4.1 presents the voltage across the inductor L_1 and L_2 during one period. In steady-state operation, the waveforms of HBLC are repeating. From figure 4.2 it can be seen that the inductor currents i_{L1} and i_{L2} flows continuous ($i_{L1}(t)>0$, $i_{L2}(t)>0$). The voltages across the inductors are presented for all operating modes.

Table.4.1. Voltage across the inductors L_1 and L_2 in one period (for HBLC)

	Mode I	**Mode II**	**Mode III**	**Mode IV**
S_1	1	0	1	0
S_2	0	1	1	0
V_{L1}	$½(V_1-V_0)$	V_C-V_0	$½(V_1+V_C-V_0)$	$-V_0$
V_{L2}	V_2-2V_C	V_2-V_C	V_2-V_C	V_2-2V_C

By applying the volt – second balance theorem, which implies that the integral of the inductor voltages over one period must be zero, on the inductors L_1 and L_2, the following equations can be obtained:

v_{L1}: $$\frac{1}{2}(V_1+V_C-V_0)d_2T+\frac{1}{2}(V_1-V_0)(d_1-d_2)T-V_0(1-d_1)T=0 \quad (4.1)$$

v_{L2}: $$(V_2-V_C)d_2T+(V_2-2V_C)(d_1-d_2)T+(V_2-2V_C)(1-d_1)T=0 \quad (4.2)$$

From equation (4.2), can be obtained the capacitor voltage $V_C = V_{C1} = V_{C2}$ as function of the input voltage V_1 and the duty cycle d_1:

$$V_C=\frac{1}{2-d_2}V_2 \quad (4.3)$$

For $d_1 \le d_2$ by applying the volt-second balance theorem on the inductors, the following equations can be obtained:

v_{L1}: $$\frac{1}{2}(V_1+V_C-V_0)d_1T+(V_C-V_0)(d_2-d_1)T-V_0(1-d_2)T=0 \quad (4.4)$$

v_{L2}: $$(V_2-V_C)d_1T+(V_2-V_C)(d_2-d_1)T+(V_2-2V_C)(1-d_2)T=0 \quad (4.5)$$

From equation (4.5) can be obtained the same expression for the capacitors voltage V_C as in the case when $d_1 > d_2$.

From equations (4.1) and (4.4) the output voltage expressions for $d_1 > d_2$, and $d_1 \le d_2$ respectively, can be obtained:

$$V_0=\frac{d_1}{2-d_1}V_1+\frac{d_2}{(2-d_1)(2-d_2)}V_2 \quad (4.6)$$

$$V_0=\frac{d_1}{2-d_1}V_1+\frac{2d_2-d_1}{(2-d_1)(2-d_2)}V_2 \quad (4.7)$$

Therefore, in CCM, the output voltage varies linearly with the duty cycle d_1 and d_2 for given input voltages. It not depends on any other circuit parameter.

Neglecting the power losses associated with the circuit elements, the output power equals the sum between the two input power P_1 and P_2.

$$P_o=P_1+P_2 \quad (4.8)$$

To demonstrate that HBLC has a high ratio of the output voltage figures 4.7, 4.8 show that the conversion ratio line of the HBLC is under the line of the dual input classical Buck converter variation. Two cases are presented:

- In the first case d_1 is constant and d_2 is variable;
- In the second case d_2 is constant and d_1 varies.

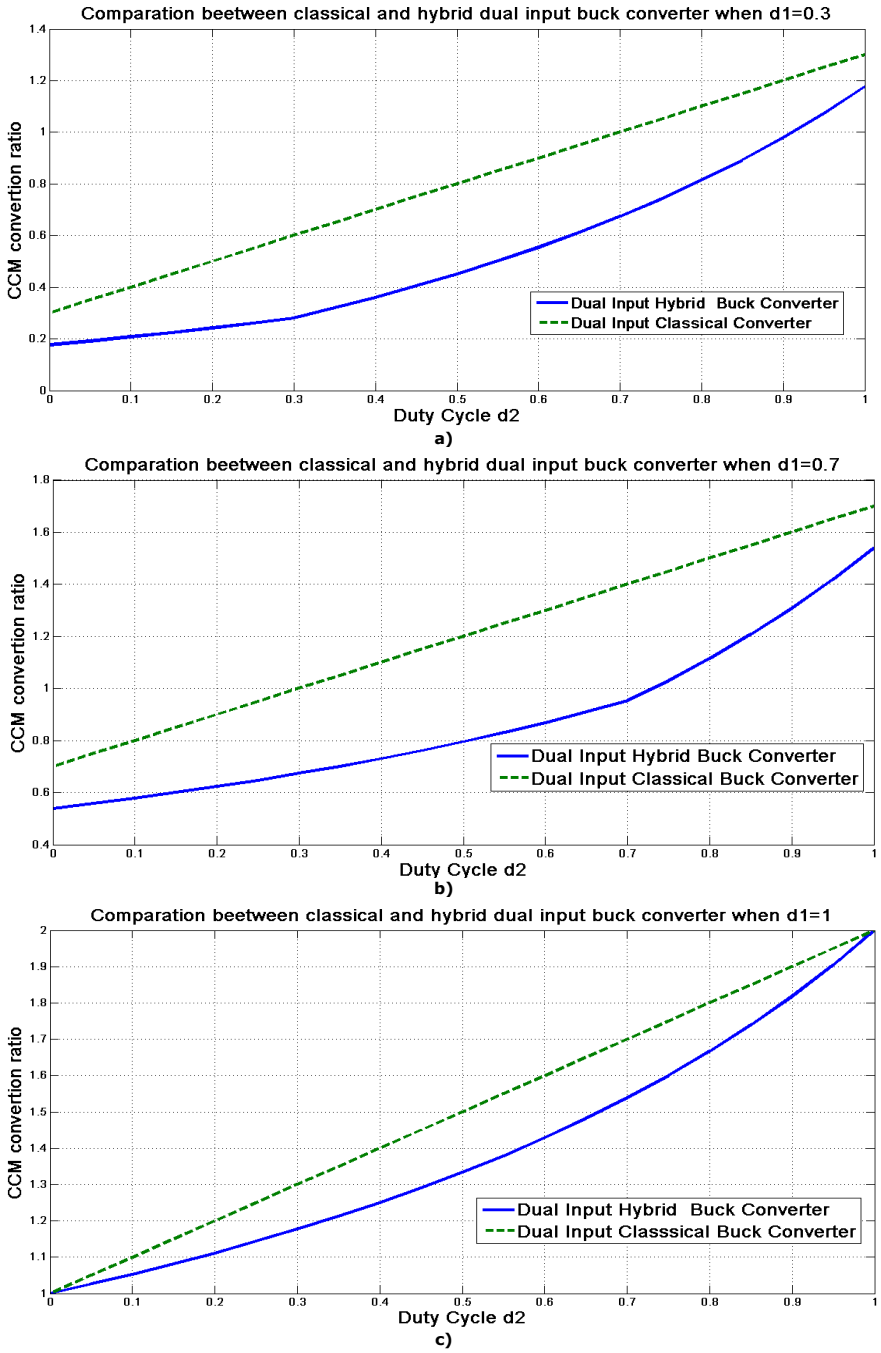

Figure 4.7. Comparison between classical Buck and HBLC when the duty cycle d_1 is kept constant.

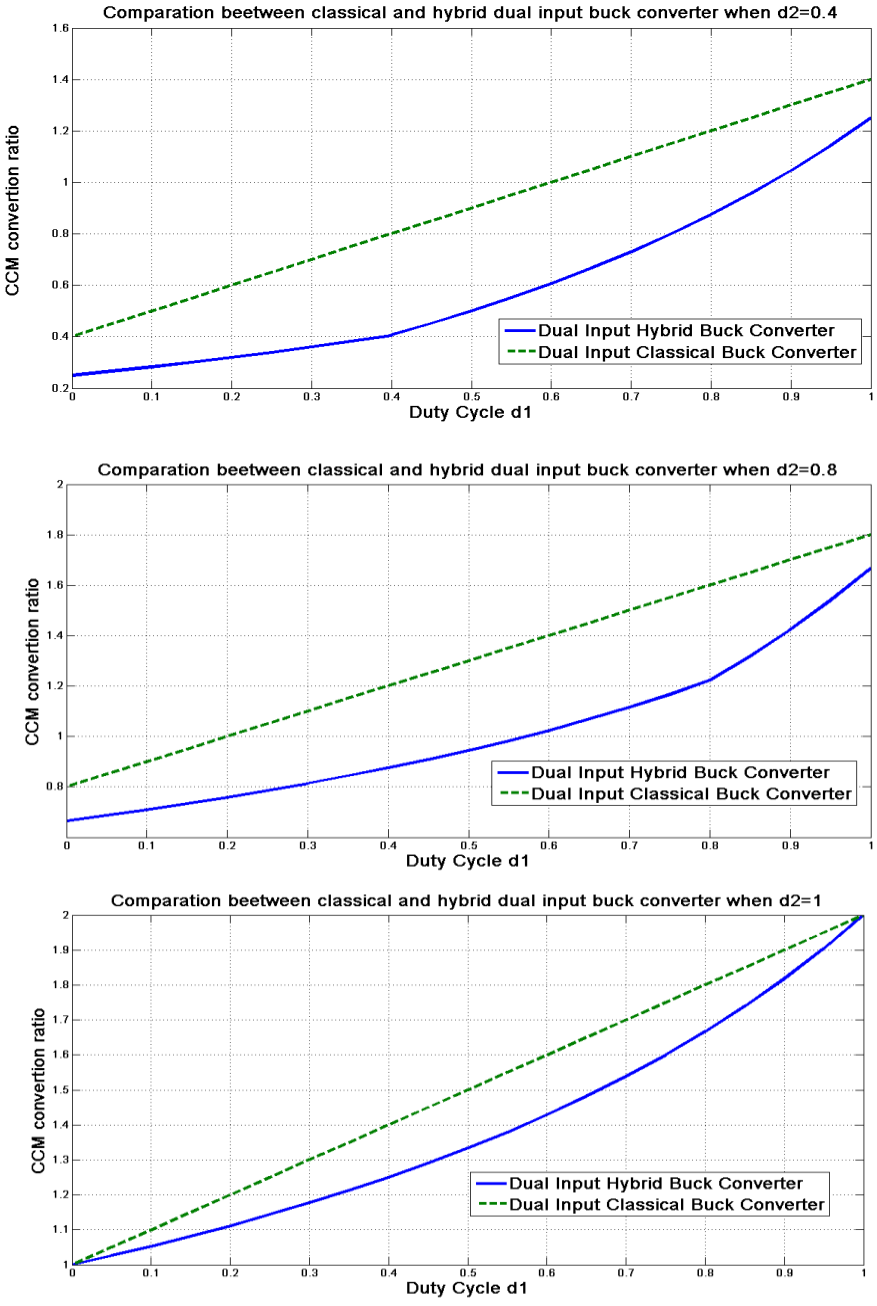

Figure 4.8. Comparison between classical Buck and HBLC when the duty cycle d_2 is kept constant.

Figure 4.9 presents the output voltage, as a function of the two duty cycles, in a three-dimensional representation. The input voltages are V_1=60V and V_2=30V. The output voltage has the maximum value $V_0=V_1+V_2$=90V, when the input sources are connected in series and the duty cycle for each of them is 100%.

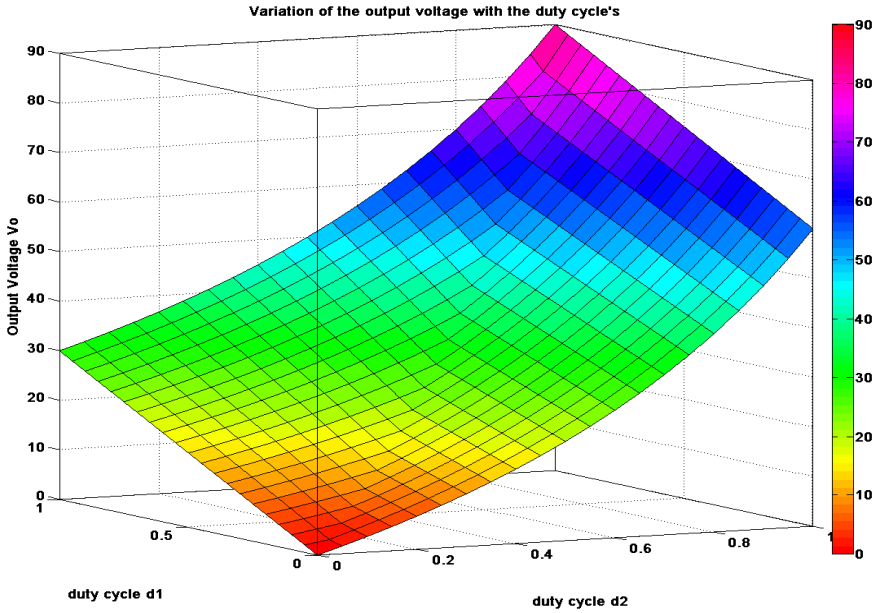

Figure 4.9. The output voltage as a function of the duty cycles.

4.4. HBLC study in BCM

In the previous sections HBLC has been analysed in CCM and the expression of the output voltage have been determined. In this section the study is extended for BCM, in order to obtain the output inductors value [4.9-4.11].

The first parameter used in HBLC BCM analysis is the power devices switching frequency (f).

The switching period (T) is given by equation (4.9):

$$T=\frac{1}{f}=10[\mu s] \tag{4.9}$$

At BCM, by definition, the output inductors current i_{L1} starts the switching period from zero and ends to zero. Figure 4.10 presents the HBLC waveforms at BCM, for $d_1>d_2$. From top to bottom they are: the gate signals of the power switch S_1 and S_2, the inductor L_1 current and voltage.

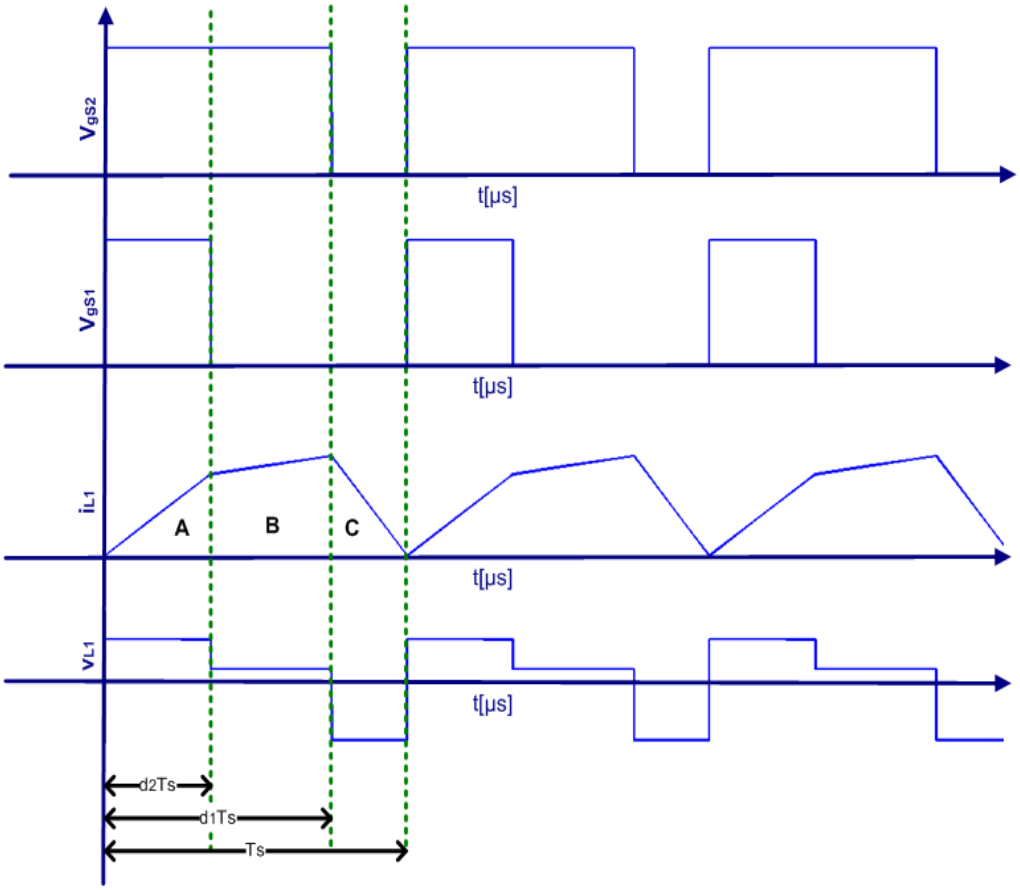

Figure 4.10. HBLC waveforms at BCM for $d_1>d_2$.

At BCM, for $d_1>d_2$, the average current ($I_{L1,lim1}$) has a minimum (limit) value from which the converter enters in DCM; it can be obtained by:

$$I_{L1,\text{lim1}} = \frac{1}{T}\int_0^T i_{L1}(t)dt = \frac{1}{2}(I_{L1,A1} + I_{L1,B1} + I_{L1,C1}) \tag{4.10}$$

In the next equations the average currents $I_{L1,A1}$, $I_{L1,B1}$ and $I_{L1,C1}$ corresponding to the sectors marked with A, B and C (figure 4.10) are determined:

$$I_{L1,A1} = \frac{1}{2T}\frac{\frac{1}{2}(V_1 + V_C - V_0)d_2T}{L}d_2T = \frac{T}{4L}(V_1 + V_C - V_0)d_2^2 \tag{4.11}$$

$$I_{L1,B1} = \frac{1}{2T}\frac{\frac{1}{2}(V_1 + V_C - V_0)d_2T + V_0(1-d_1)T}{L}(d_1 - d_2)T = \frac{T}{4L}[(V_1 + V_C - V_0)d_2 + 2V_0(1-d_1)](d_1 - d_2) \tag{4.12}$$

$$I_{L1,C1} = \frac{1}{2T}\frac{V_0(1-d_1)T}{L}(1-d_1)T = \frac{T}{4L}2V_0(1-d_1)^2 \tag{4.13}$$

The limit average current value is provided by the following equation:

$$I_{L1,\lim 1} = \frac{T}{4L}\{(V_1 + V_C - V_0)d_2^2 + [(V_1 + V_C - V_0)d_2 + + 2V_0(1-d_1)](d_1 - d_2) + 2V_0(1-d_1)^2\} \tag{4.14}$$

The same algorithm is applied for $d_1 \le d_2$. The waveforms for the L1 inductor current and voltage at BCM are presented in figure 4.8. To have a more compressive understanding of BCM, the gate signals of the two power switches S_1 and S_2 are presented too.

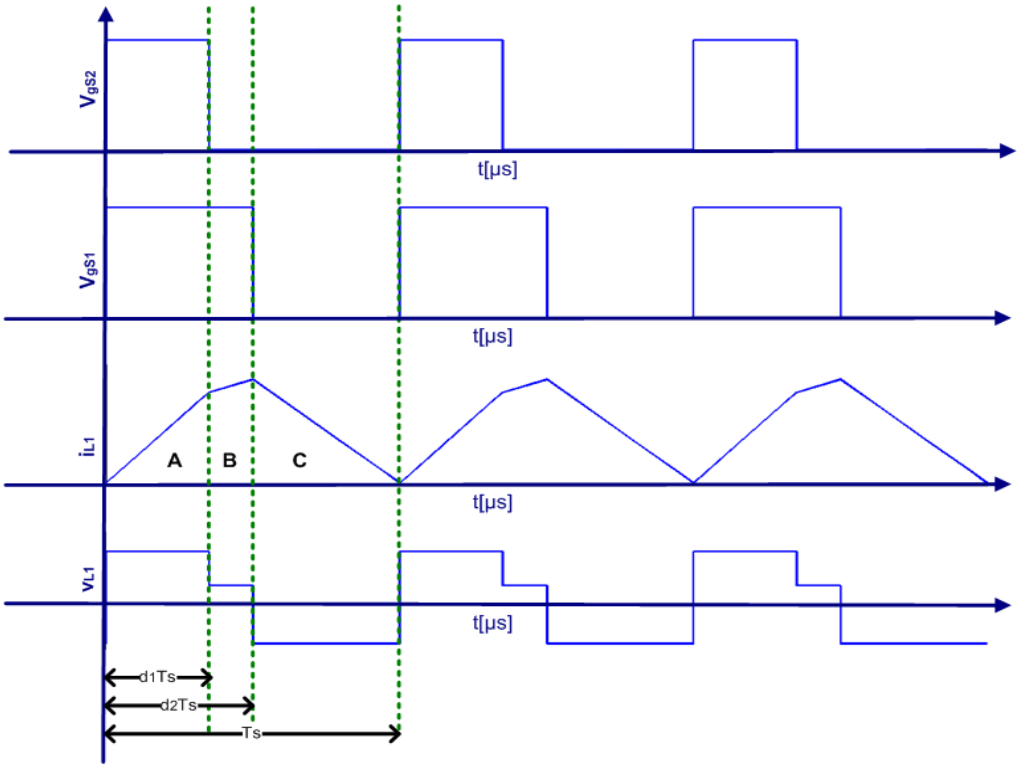

Figure 4.11. HBLC waveforms at BCM for $d_1 \le d_2$.

The average values for the inductor current i_{L1}, corresponding to the sectors A, B and C are given by the following equations:

$$I_{L1,A2} = \frac{1}{2T}\frac{\frac{1}{2}(V_1 + V_C - V_0)d_1 T}{L} d_1 T = \frac{T}{4L}(V_1 + V_C - V_0)d_1^2 \tag{4.15}$$

$$I_{L1,B2} = \frac{1}{2T}\frac{\frac{1}{2}(V_1 + V_C - V_0)d_1 T + V_0(1-d_2)T}{L}(d_2 - d_1)T = \frac{T}{4L}[(V_1 + V_C - V_0)d_1 + 2V_0(1-d_2)](d_2 - d_1) \tag{4.16}$$

$$I_{L1,C2} = \frac{1}{2T}\frac{V_0(1-d_2)T}{L}(1-d_2)T = \frac{T}{4L}2V_0(1-d_2)^2 \tag{4.17}$$

The average value of the inductor current i_{L1} in BCM ($I_{L1,lim2}$), for $d_1 \le d_2$, is given by the following equation:

$$I_{L1,\lim 2} = \frac{T}{4L}\{(V_1+V_C-V_0)d_1^2 + [(V_1+V_C-V_0)d_1 + + 2V_0(1-d_2)](d_2-d_1) + 2V_0(1-d_2)^2\} \tag{4.18}$$

In order to find out the duty cycles d_1 and d_2 for the limit current, will consider that the input source V_1 has constant voltage. A parameters k is used to express the input voltages ratio:

$$k = \frac{V_2}{V_1} \tag{4.19}$$

In equations (4.6) and (4.7), which gives the output voltage, the input voltage V_2 will be replaced with kV_1. A new set of equations for the output voltage have been obtained:

$$V_0 = V_1\frac{d_1(2-d_2)+kd_2}{(2-d_1)(2-d_2)} = V_1\frac{2d_1-d_1d_2+kd_2}{(2-d_1)(2-d_2)} \tag{4.20}$$

when $d_1 > d_2$ and

$$V_0 = V_1\frac{2d_1-d_1d_2+2kd_2-kd_1}{(2-d_1)(2-d_2)} \tag{4.21}$$

when $d_1 \le d_2$.

By replacing equation (4.20) in equation (4.14), results:

$$I_{L1,\lim 1} = \frac{TV_1}{4L}\frac{-4d_1^2+4d_1-2d_1d_2+(2-k)d_1^2d_2+kd_1d_2^2-2kd_2^2+2kd_2}{(2-d_1)(2-d_2)} \tag{4.22}$$

.

For $d_1 \le d_2$, equation (4.21) is introduced in equation (4.18). The average value for inductor current at BCM is now given by:

$$I_{L1,\lim 2} = \frac{TV_1}{4L}[\frac{-4d_1^{\ 2} + 4d_1 - 2d_1d_2 + (2-k)d_1^{\ 2}d_2}{(2-d_1)(2-d_2)} + \\ + \frac{+kd_1d_2^{\ 2} - 2kd_2^{\ 2} + 2kd_2}{(2-d_1)(2-d_2)}] \tag{4.23}$$

Two situations are presented next, depending on k values.
For k>1:

$$V_0 < V_1 < V_2, \tag{4.24}$$

hence,

$$V_0 < V_1 < kV_1. \tag{4.25}$$

Knowing that the output voltage has two expressions depending on the relation between d_1 and d_2, two directions will be taken. For $d_1>d_2$ the constraints takes the form presented below:

$$\frac{d_1}{2-d_1}V_1 + \frac{d_2}{(2-d_1)(2-d_2)}kV_1 < V_1 < kV_1 \tag{4.26}$$

hence,

$$\frac{d_1}{2-d_1} + \frac{d_2}{(2-d_1)(2-d_2)}k < 1 < k \tag{4.27}$$

For $d_1 \le d_2$ the relation between output voltage and the input voltage V_1 is:

$$\frac{d_1}{2-d_1} + \frac{2d_2 - d_1}{(2-d_1)(2-d_2)}k < 1 < k \tag{4.28}$$

For $0<k\le 1$:

$$V_0 < V_2 \le V_1 \tag{4.29}$$

hence

$$V_0 < kV_1 \le V_1 \tag{4.30}$$

For $d_1>d_2$:

$$\frac{d_1}{2-d_1}V_1+\frac{d_2}{(2-d_1)(2-d_2)}kV_1<kV_1\le V_1 \tag{4.31}$$

$$\frac{d_1}{2-d_1}+\frac{d_2}{(2-d_1)(2-d_2)}k<k\le 1 \tag{4.32}$$

For $d_1 \le d_2$:

$$\frac{d_1}{2-d_1}+\frac{2d_2-d_1}{(2-d_1)(2-d_2)}k<k\le 1 \tag{4.33}$$

Limit current expressions are complex and cannot be resolved analytically. In order to obtain the critical value for the output inductors the Wolfram Mathematica software has been used.

Only the inductor current p.u. value ($I_{lim,pu}$) has been mathematically analyzed in BCM:

$$I_{\lim,pu}=\frac{4L}{TV_1}I_{L1,\lim}\,. \tag{4.34}$$

The algorithm developed in this section computes a function which gives, the maximum of the equation (4.34), satisfying the constraint (4.27) if k>1 and (4.32) if k≤1.

In order to find the function which gives the maximum, we consider a three-dimensional regular grid for the variables d_1 in [0,1], d_2 in [0,1] and k in [0,1] (or [1,6], respectively), with 250 nodes per variable.

For each value of k the following steps have been performed:

- First, to simplify the computation, we exclude the values of d_1 and d_2, which do not satisfy the constraint;
- Next we sort the remaining triplets (k, d_1, d_2) in respect to the equation $I_{lim,pu}$ (k, d_1, d_2) and retain the one which gives the largest value, $I_{lim,pu,max}$(k, d_{1max}, d_{2max});

At the end of this computation, we obtain a list containing a set of values $I_{lim,pu,max}$(k, d_1, d_2) which maximizes the function.

Using a fitting procedure for this list we compute the polynomial function $I_{lim,pu,max}$ (k, d_1, d_2) and use it to determinate the inductor value:

$$L=\frac{TV_1}{4}I_{\lim,pu,\max} \tag{4.35}$$

Several polynomial definitions of the functions $I_{lim,pu,max}$ of degree 7, 8 and 9 were tested and the approximation error is very small.

3D plot surface of the functions $I_{lim,pu,max}$ for k=0.5 and for k=3 are presented in figures 4.12 and 4.13. It can be observed that every 3D surface has two sides corresponding to $d_1>d_2$ and $d_1\le d_2$, respectively. The x axe represents the duty cycle d_1 and the y axe represents the duty cycle d_2.

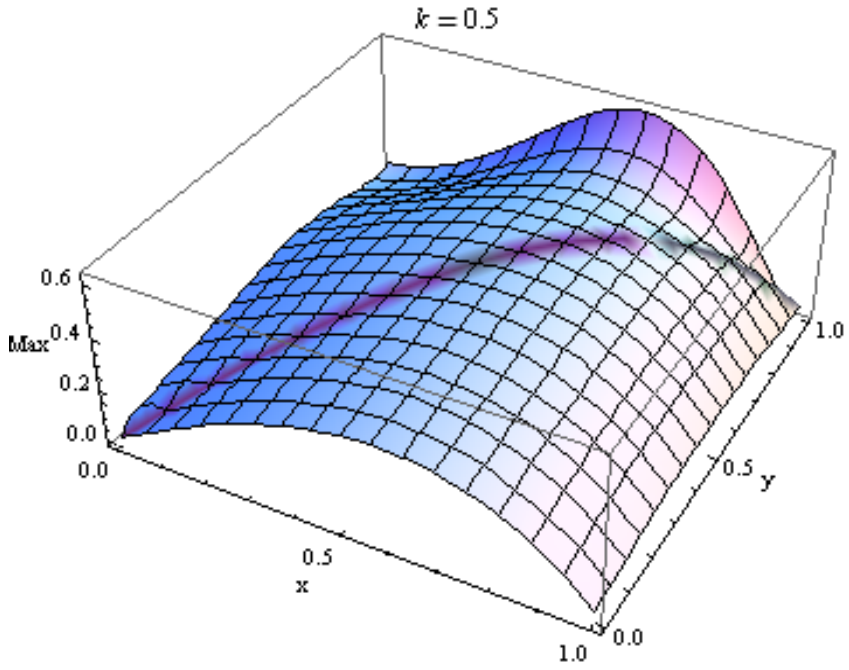

Figure 4.12. $I_{lim.pu,max}$ representation for k=0.5.

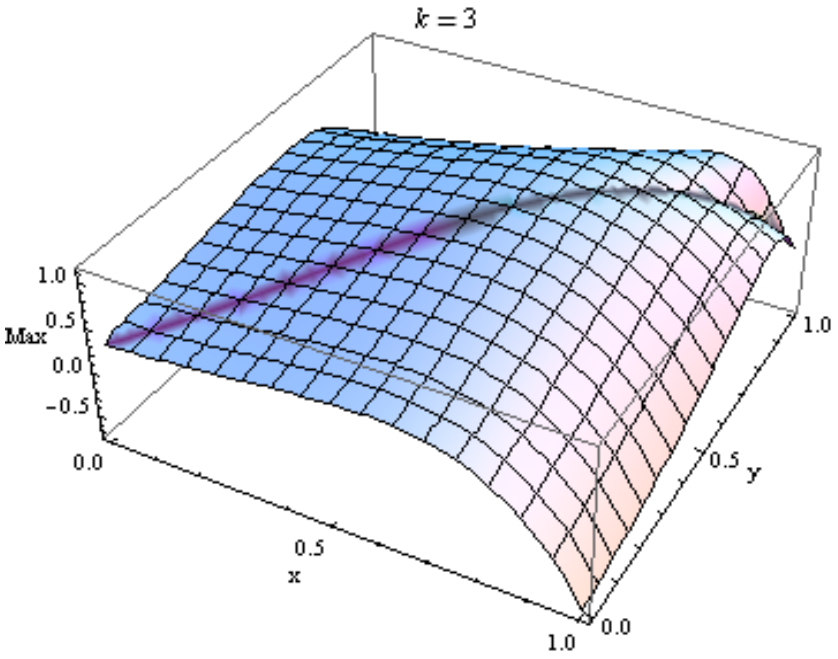

Figure 4.13. $I_{lim,pu,max}$ representation for k=3.

Table 4.2 presents $I_{lim,pu,max}$ for k taking values smaller, equal, and higher than 1.

Table 4.2. Selected values for the maximum inductor current.

k	d_{1max}	d_{2max}	$I_{lim,pu,max}$
0.1	0.16	0.374	0.164
0.2	0.283	0.457	0.284
0.3	0.38	0.521	0.363
0.4	0.457	0.571	0.42
0.5	0.52	0.61	0.461
0.7	0.585	0.647	0.491
0.9	0.585	0.647	0.516
1	0.585	0.712	0.541
2	0.534	0.635	0.566
3	0.459	0.529	0.597
4	0.405	0.458	0.837
4	0.405	0.458	1.005
5	0.364	0.405	1.219
6	0.331	0.364	1.292

4.5. Simulation results

For validate HBLC theoretical consideration, digital simulations have been developed in PLECS Block set under MATLAB. The PLECS software has been chosen due to the good communication with MATLAB. The parameters used for the simulations are presented in table 4.3.

Table.4.3. Simulation Parameters for HBLC

Parameter	Value
Inductors L_1	28μH
Inductor L_2	28 μH
Capacitors C_1 and C_2	2640 μF
Output capacitor C	3960μF
Switching frequency	100kHz

Two situations have been simulated: $d_1>d_2$ and $d_1\leq d_2$, with different values for the input sources voltages.

Figures 4.14-4.18 present the simulation results when d_1=70%, d_2=45%, V_1=60V, V_2=40V and R=2.28Ω. It can be seen that the gate signals of the power switches are synchronized at turn on. The output voltage is 48.3V, similar to the value obtained from analytical calculation. The current through the inductors has three slopes as can be seen from the figure 4.8, corresponding to the operation modes.

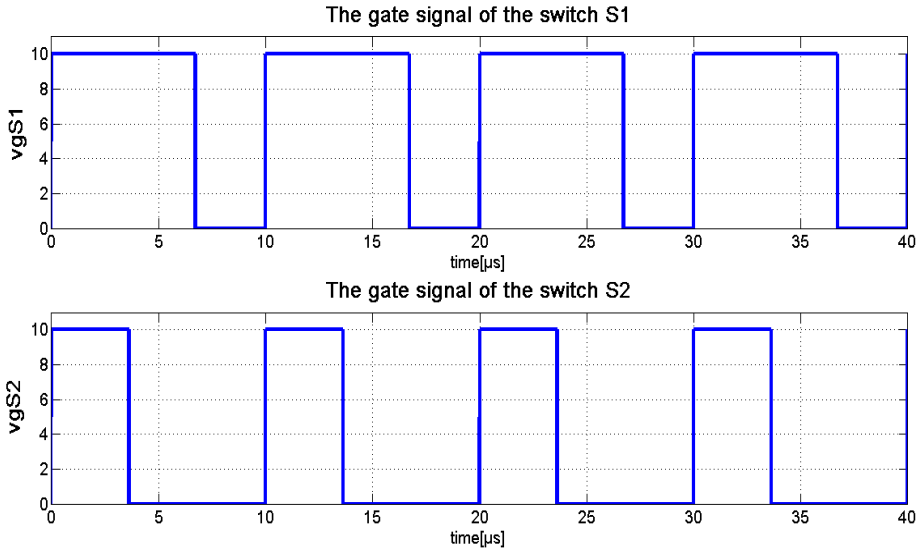

Figure 4.14. The gate signals of the HBLC when $d_1>d_2$.

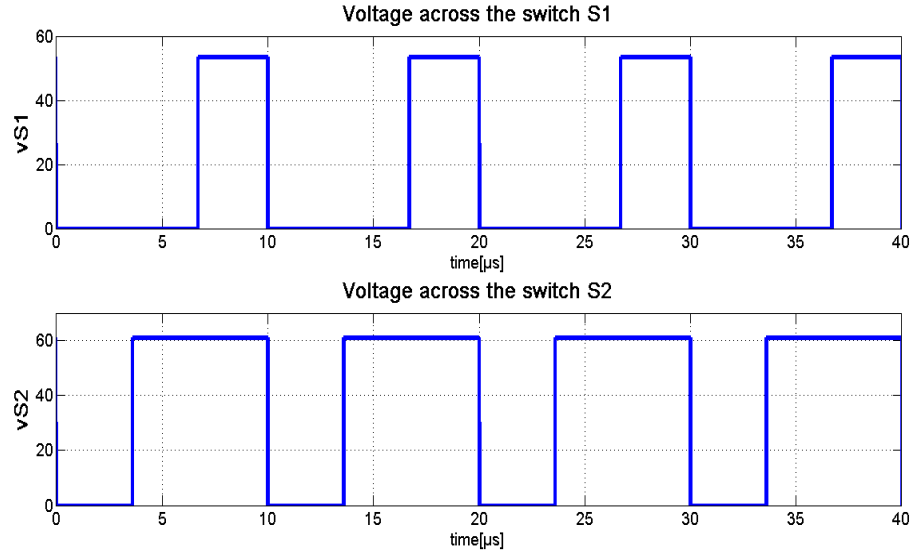

Figure 4.15. The voltage across the switches when $d_1>d_2$.

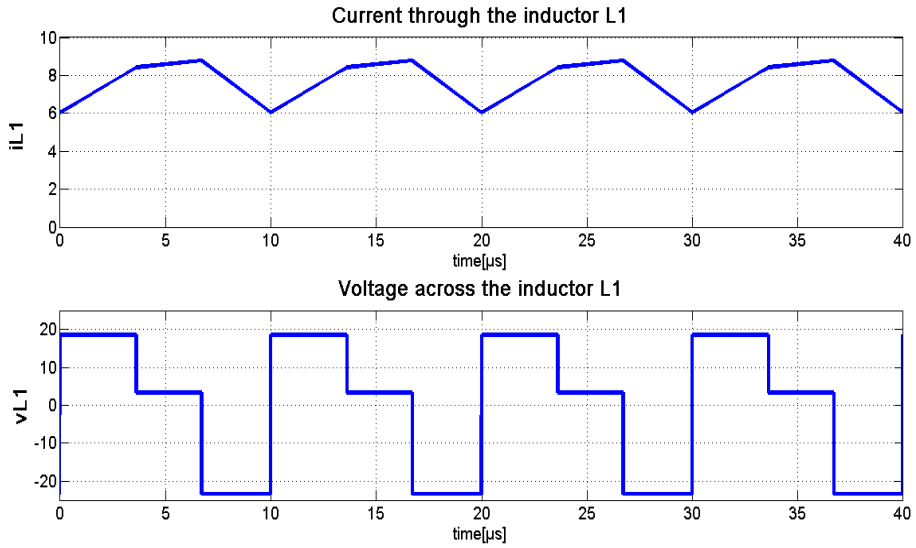

Figure 4.16. Inductor L_1 voltage and current when $d_1>d_2$.

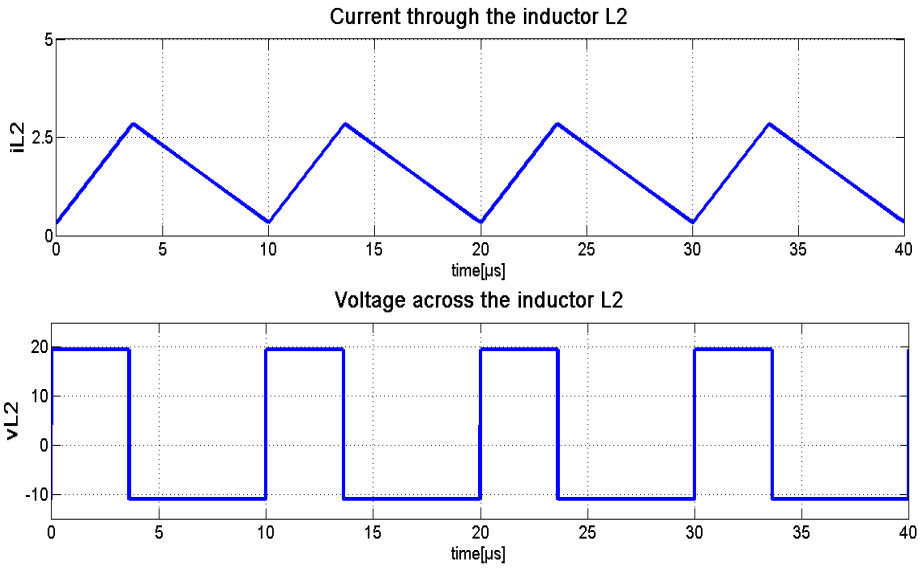

Figure 4.17. Inductor L_2 voltage and current when $d_1>d_2$.

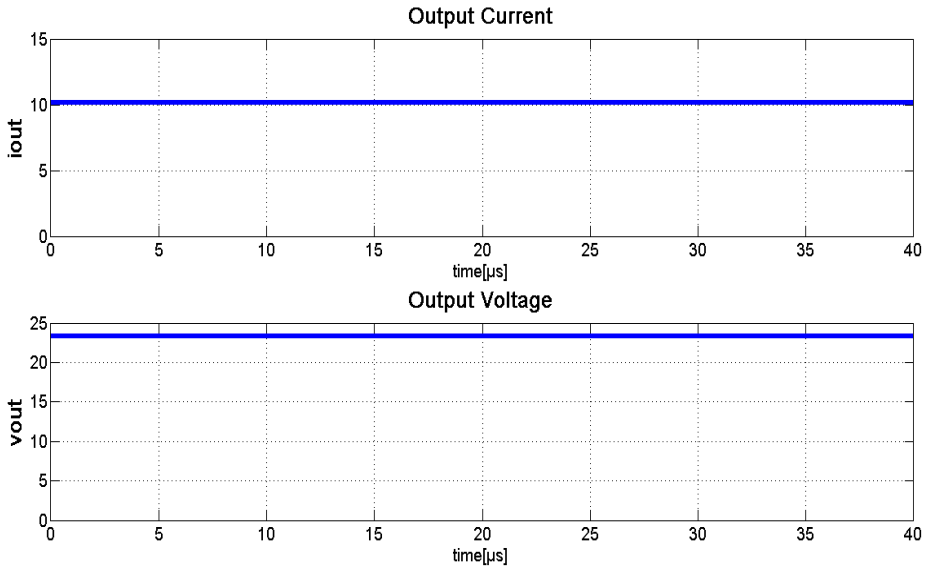

Figure 4.18. Output voltage and current when d_1=70% and d_2=45%.

Figures 4.19-4.23 present the case when d_1=30%, d_2=50%, V_1=45V, V_2=65V and R=2.3Ω. It can be seen that the gate signals v_{gS1} and v_{gS2} are synchronized at turn on time.

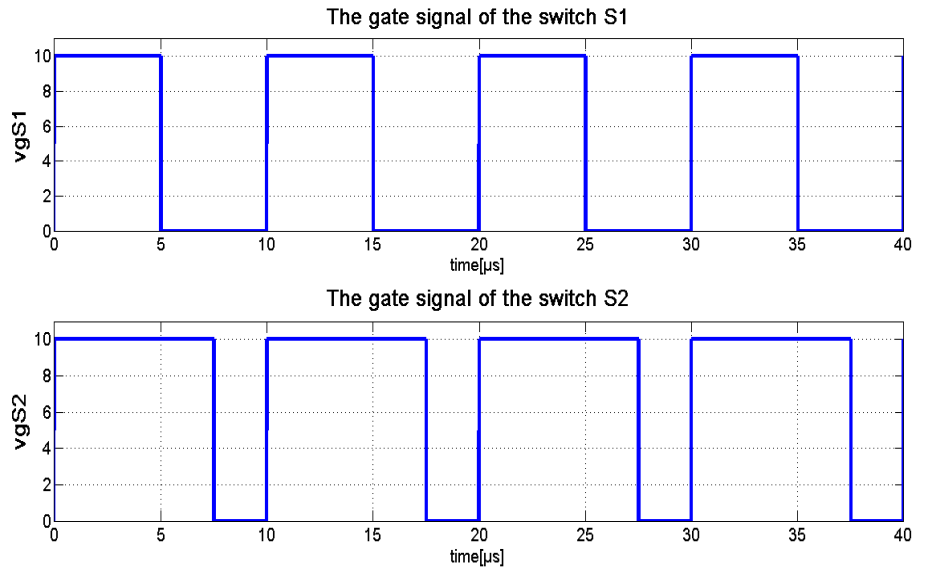

Figure 4.19. The control signals of HBLC when $d_1 \leq d_2$.

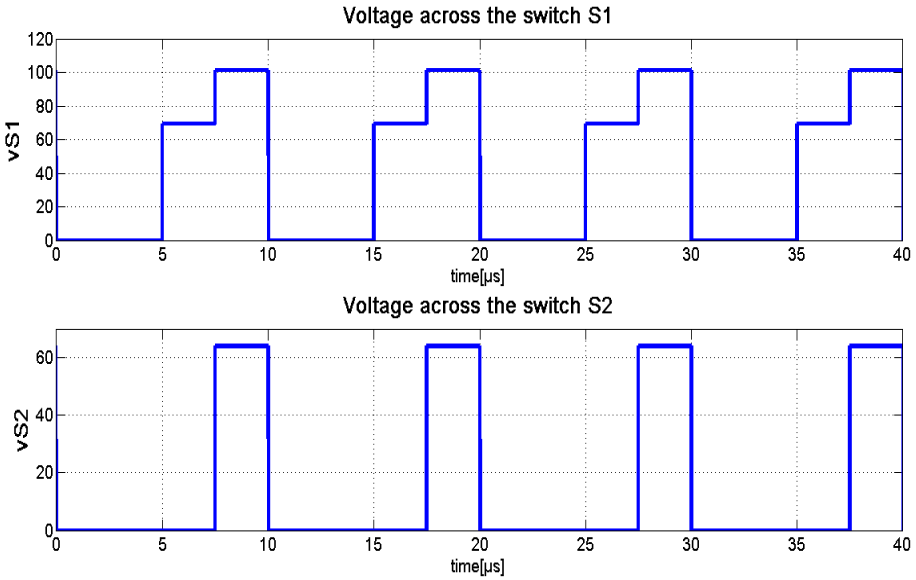

Figure 4.20. The voltage across the switches when $d_1 \leq d_2$.

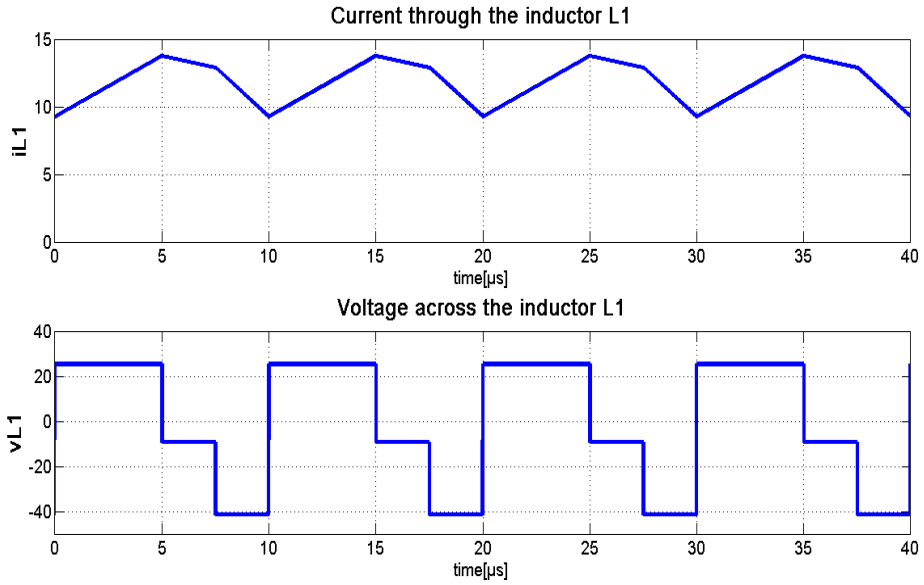

Figure 4.21. Inductor L_1 current and voltage when $d_1 \leq d_2$.

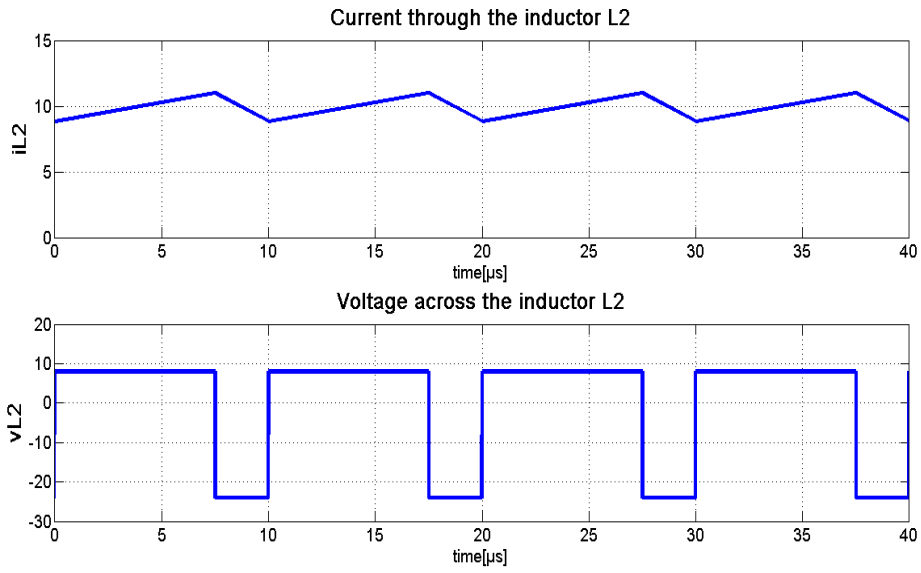

Figure 4.22. Inductor L_2 current and voltage when $d_1 \leq d_2$

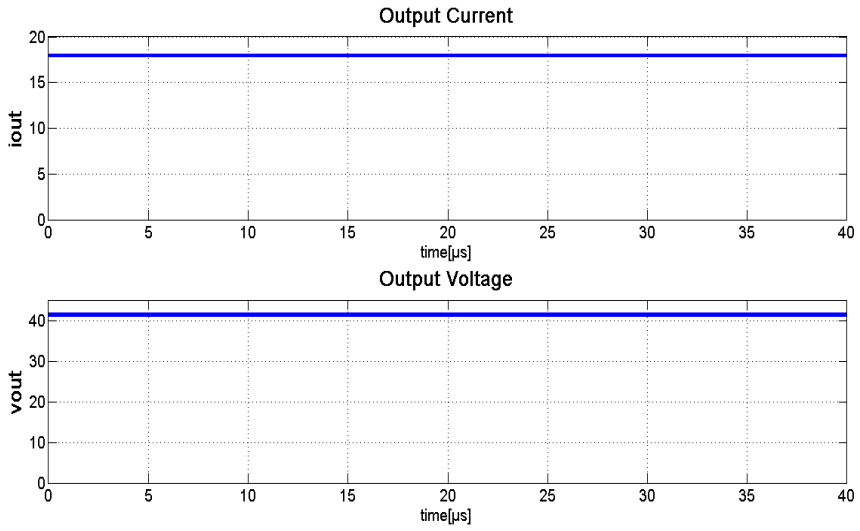

Figure 4.23. Output current and voltage when d_1=30% and d_2=50%.

In order to determinate the efficiency of HBLC, a simulation has been carried out in LTSpice. After a set of values have been obtained for the efficiency (in

different functionality points) an average value has been calculated. The efficiency has been determinate to be 94%. Figure 4.24 shows the circuit diagram used to find the efficiency.

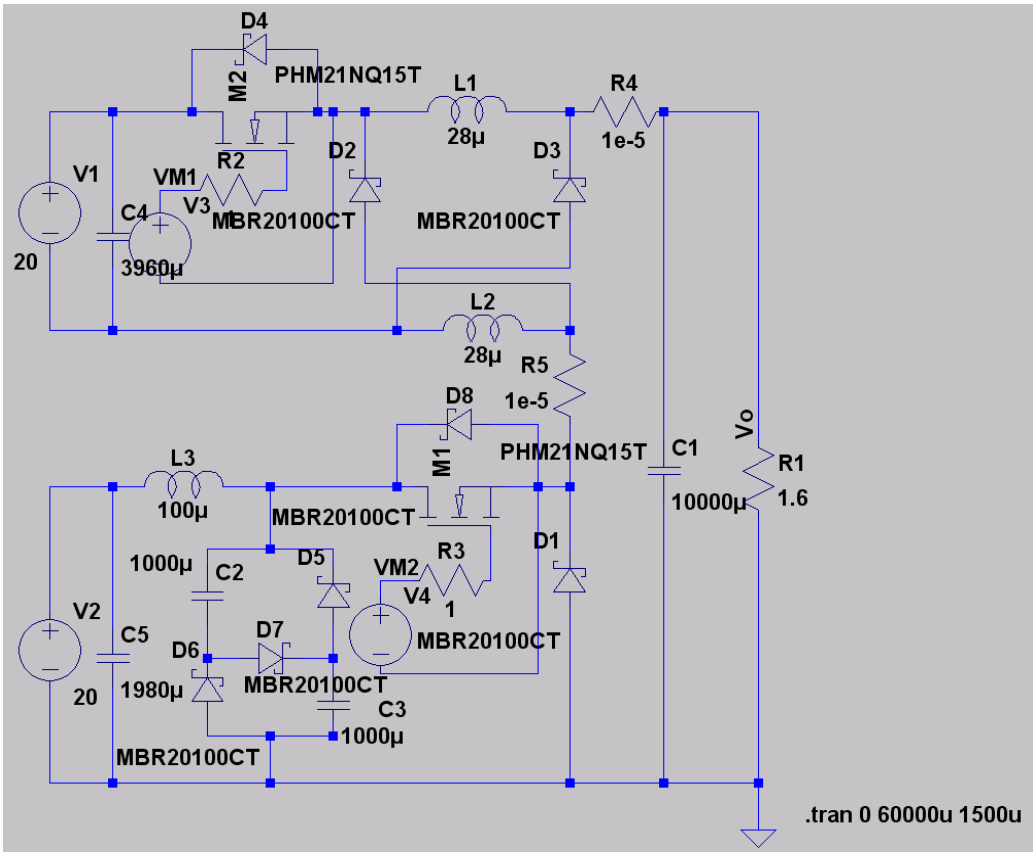

Figure 4.24. LTSpice circuit diagram for the HBLC.

4.6. Experimental results

In order to verify the simulation results presented above a prototype was built. The technical description of the laboratory prototype is presented in chapter 6 „Experimental Platform".

Two cases have been tested on the prototype: $d_1>d_2$ and $d_1 \leq d_2$.

The total current through the inductors L_1 and L_3 is the output current.

Figure 4.25 presents the inductors L_1 and L_2 waveforms when $d_1=70\%$, $d_2=25\%$, and $V_1=V_2=40V$.

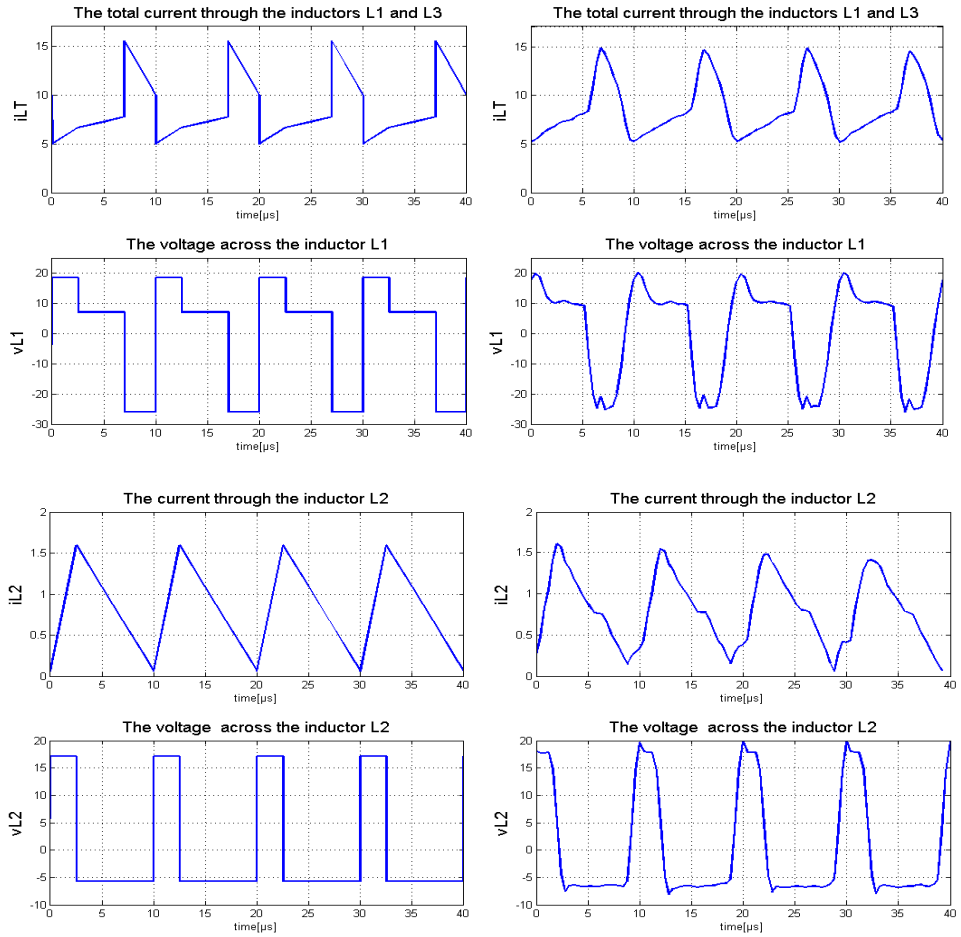

Figure 4.25. The inductors waveforms when d_1=70% and d_2=25%.

Figure 4.26 presents the inductors L_1 and L_2 waveforms obtained from simulations and experiments with d_1=25%, d_2=60%, V_1=60V and V_2=40V.

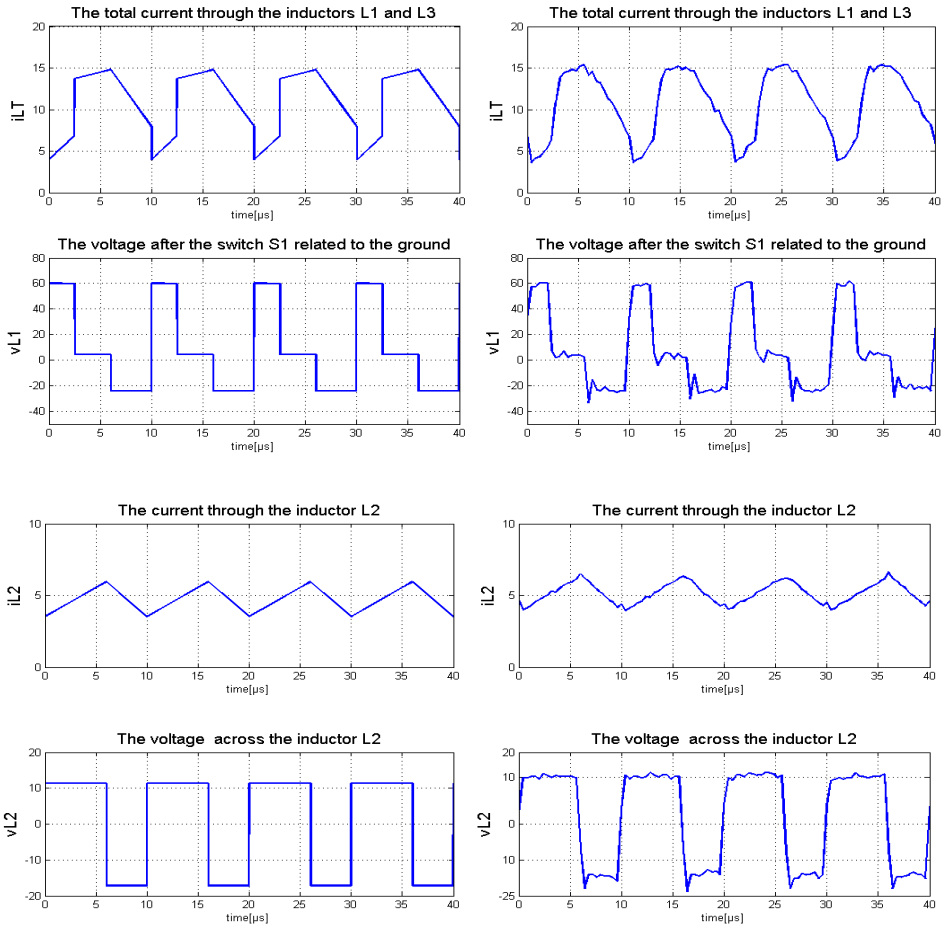

Figure 4.26. The inductors waveforms when d_1=25% and d_2=60%.

4.7. Conclusions

In this chapter a proposed dual input hybrid buck DC-DC converter structure was presented. HBLC can have a common ground for one input voltage and the converter output, which is a major advantage in most applications.

Operating modes, the corresponding converter circuit diagrams and the analytical description was presented. A comparison between HBLC and the dual input Buck converter, in terms of the voltage conversion ratio, was made.

In order to calculate the output inductances values, BCM was studied, analytically and using numerical methods, implemented in Mathematica. In this way the average limit value of the output inductor current was determinate.

Simulation results were made in PLECS, and the current and voltage waveforms for the key components were obtained. An efficiency study has been made using LTSpice.

A laboratory prototype was built and tested in order to validate the theory, and a good correspondence with the simulations was observed.

As a general conclusion related to the proposed dual input DC-DC converters, in table 4.4 is presented a synthetic comparison with reference to the voltage conversion ratio and number of power active and passive elements.

Table 4.4. Comparative evaluation of the proposed converters.

	Output voltage	No. of elements	No. of inductors
HBL	$V_0 = \frac{2d_1 - d_2}{2 - d_2} V_1 + \frac{d_2}{2 - d_2} V_2$ for $d_1 > d_2$ $V_0 = \frac{d_1}{2 - d_2} V_1 + \frac{d_2}{2 - d_2} V_2$ for $d_1 \le d_2$	7	2
HBC	$V_0 = d_1 V_1 + \frac{d_2}{2 - d_2} V_2$	11	3
HBLC	$V_0 = \frac{2d_1 - d_2}{(2 - d_1)(2 - d_2)} V_1 + \frac{d_2}{2 - d_2} V_2$ for $d_1 > d_2$ $V_0 = \frac{d_1}{(2 - d_1)(2 - d_2)} V_1 + \frac{d_2}{2 - d_2} V_2$ for $d_1 > d_2$	13	3
HBCL	$V_0 = \frac{d_1}{2 - d_1} V_1 + \frac{d_2}{(2 - d_1)(2 - d_2)} V_2$ for $d_1 > d_2$ $V_0 = \frac{d_1}{2 - d_1} V_1 + \frac{2d_2 - d_1}{(2 - d_1)(2 - d_2)} V_2$ for $d_1 > d_2$	13	3

References:

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CHAPTER 5
Dual Input, Small Power, PV and Wind Energy Conversion System

5.1. Introduction

The increasing demand on global electric energy requires the use of renewable energy sources. Renewable energies such as wind power and solar exist in abundance in nature. This is a promising way to solve the contradiction between the exhausting resources and the growing demands. In the past, renewable energy sources diffusion was limited by technological shortcomings and higher costs. In the last decades the efficiency and reliability of wind generators and PV arrays have been improved, while the costs have been lowered.

Wind power and PV array power, each by themselves, cannot continuously supply a system because they depend on the weather conditions. Fortunately, most of the time wind and PV power are complementary. Therefore a wind - PV hybrid generation system has a higher reliability for maintaining a continuous power delivery, by means of a storage element, especially when the system is off-grid [5.1-5.13].

Traditionally, hybrid systems tend to use two independent DC-DC converters to supply the electric energy demanded by the load, from the two input sources (PV and wind power) [5.14-5.17].

An alternative approach is to use multiple input DC-DC converters for mixing the energies [5.18-5.24].

The main objective of this chapter is to propose a mixed, small power, wind and PV system (WPVS), which transfers power from the two input sources to the load through the HBLC presented in the previous chapter.

The analyzed WPVS uses a variable speed wind turbine with a synchronous PM generator (SG) and a diode bridge rectifier (DBR) - as a first power source, and a PV array - as a second power source, connected to the HBLC inputs, as shown in figure 5.1. A dumping resistor (DR) is used for the dissipation of the wind turbine excess power. The load is assumed to be an AC load (ACL). Therefore, a voltage inverter is required, also for grid connection if available or needed. WPVS can work stand-alone or grid connected by means of a switch (RG) and a short-circuit fuse protection (F1).

The wind subsystem is the main power source of WPVS. The PV array subsystem starts operation when the wind power generation is not enough to satisfy the demanded power, in stand-alone regime.

The battery, connected directly to the HBLC output, is used to store supplementary energy or to ensure continuity in power supply.

The WPVS control is made through an energy management unit (EMCU), which maintains the power balance.

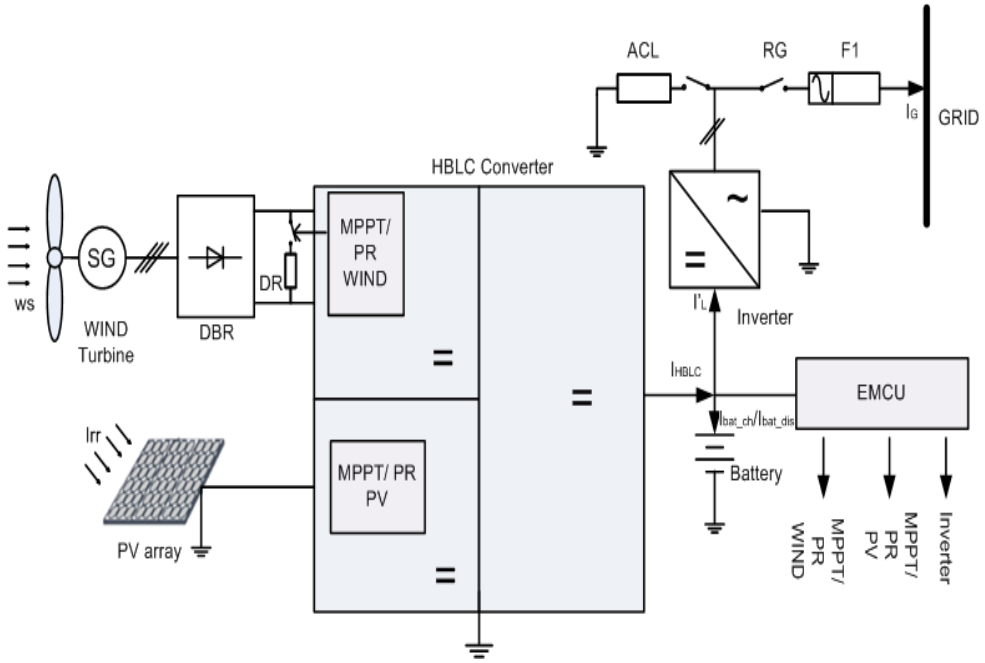

Figure 5.1. WPVS proposed topology.

5.2. PV and wind turbine system

5.2.1. PV panel

Solar cells are composed of various semiconductors materials that absorb light (solar irradiation) and convert it into electron-hole pairs and a semiconductor material with junction that separates photo-generated carries into electrons and electron holes. The double diode model (or double-exponential model) of a solar cell is presented in figure 5.2. The first diode is responsible for the diffusion current component. The second diode accounts for the losses due to the carrier recombination in the space charge region of the junction, and those to surface recombination. The R_p resistance models the leakage current across the junction. The series resistance R_S models the losses due to the internal resistance of the cell, as well as the losses at contacts and interconnections between cells and modules.

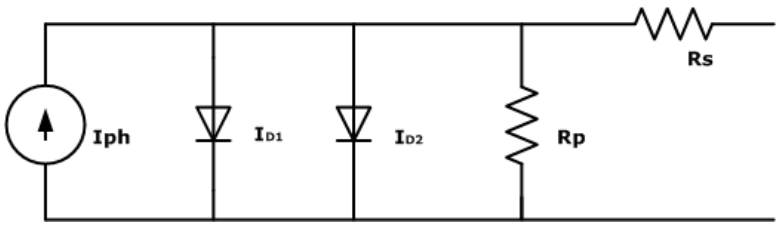

Figure 5.2. Equivalent circuit of a solar cell.

The output current I_{PV} is presented in the following equation and describes the entire current-voltage characteristics of a photovoltaic cell:

$$I_{PV} = I_{ph} - I_s(e^{(V+IR_s)/(NV_d)} - 1) - I_{s2}(e^{(V+IR_s)/(N_2V_d)} - 1) - (V + IR_s)/R_p \quad (5.1)$$

where:

- I_{ph} is the solar-induced current

$$I_{ph} = I_{ph0}\frac{I_{rr}}{I_{rr0}} \quad (5.2)$$

  - I_{rr} is the irradiation (light intensity) in W/m^2 falling on the cell;
  - I_{ph0} is the measured solar-generated current for the irradiation I_{rr0}.
- I_s is the saturation current of the first diode;
- I_{s2} is the saturation current of the second diode;
- V_t is the thermal voltage, k_BT/q, where:
  - k_B is the Boltzmann constant;
  - T is the device operating temperature parameter value;
  - q is the elementary charge on an electron.
- N is the quality factor (diode emission coefficient) of the first diode;
- N_2 is the quality factor (diode emission coefficient) of the second diode;
- V is the voltage across the solar cell electrical ports.

In order to obtain the appropriate voltage and output current for different applications, single solar cells are interconnected in series (for large voltage) or in parallel (for larger current) to form the photovoltaic module. Several of these modules can be connected to each other and form a panel.

A PV panel is characterized by the current-voltage (IV) curve given by the producer. The IV curve changes as the temperature or the irradiation varies. Figure 5.3. shows the dependency of the IV curve with the irradiation for the modeled PV panel.

A PV panel with 60 cells connected in series has been chosen for the simulation of the WPVS.

To get maximum power from the PV panel either the operating voltage or current should be controlled by a maximum point tracker (MPPT). Several methods have been developed in literature in order to determinate the MPPT:

- Short-current pulse based method [5.25];
- Incremental conductance method;
- Perturb and observe method [5.26-5.28];

- MPPT with ripple correlation control [5.29];
- Constant voltage method [5.30];
- Hill-climbing method combined with constant voltage.

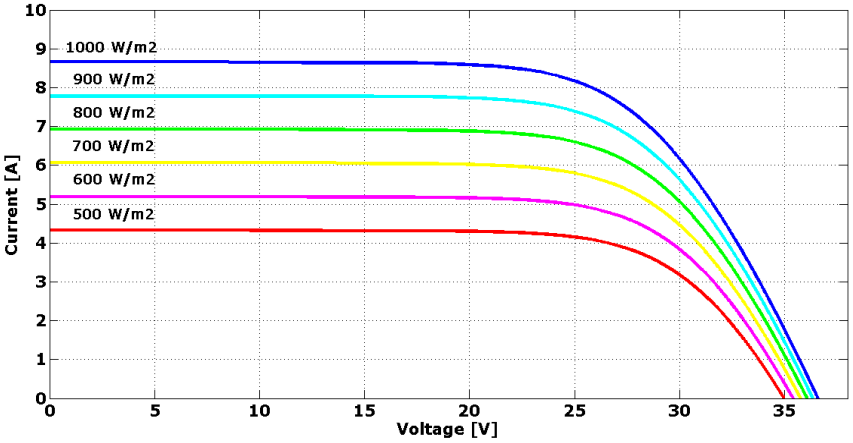

Figure 5.3. PV current-voltage curve dependency.

5.2.2. Wind Turbine

The wind turbines capture power from the wind by means of aerodynamic designed blades and convert it to rotating mechanical power.

The wind turbine mechanical power is given by the next equation:

$$P_m = C_p(\lambda)P_w \tag{5.3}$$

where $C_p(\lambda)$ is the power coefficient, which is a function of

$$\lambda = \frac{\omega_r R_t}{v_w} \tag{5.4}$$

Where ω_r is the rotating speed [rpm], R_t is the turbine blade radius [m] and v_w is the wind speed [m/s].

The wind power can be expressed by:

$$P_w = \frac{1}{2}\rho\pi R_t^2 v_w^3 \tag{5.5}$$

where ρ is the air density [kg/m^3].

The wind turbine has a maximum power point, too. In order to achieve this point several methods have been developed in the last decades:

- "kω^3" method [5.31];
- "Perturb and observe" method [5.32];
- Artificial intelligence [5.33-5.37].

5.2.3. Battery

The equivalent circuit which models the battery is represented in figure 5.4 [5.38-5.40].

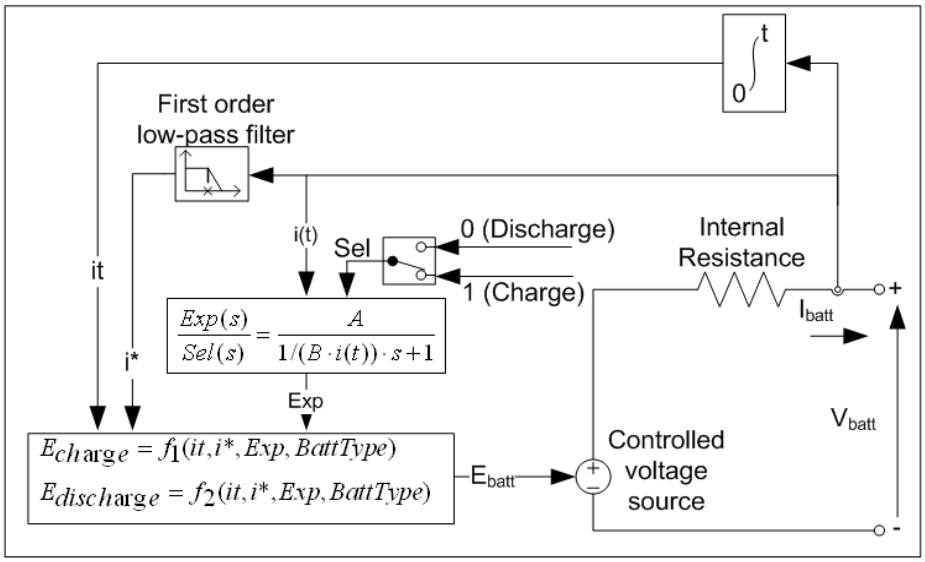

Figure 5.4. Battery modelation circuit.

The charge and discharge functions of the battery are presented in the following equations:

$$f_{dis} = E_0 - K\frac{Q}{Q-it}i^* - K\frac{Q}{Q-it}it + Laplace^{-1}(\frac{Exp(s)}{Sel(s)}0)\text{, for discharging (5.6.)}$$

$$f_{ch} = E_0 - K\frac{Q}{|it| + 0.1Q}i^* - K\frac{Q}{Q-it}it + Laplace^{-1}(\frac{Exp(s)}{Sel(s)}\frac{1}{s})\text{, for charging (5.7.)}$$

where E_{Batt} = Nonlinear voltage (V);
E_0 = Constant voltage (V);
Exp(s) = Exponential zone dynamics (V);
Sel(s) = Represents the battery mode. Sel(s) = 0 during battery discharge, Sel(s) = 1 during battery charging;
K = Polarization constant (Ah^{-1}) or Polarization resistance (Ohms);
i* = Low frequency current dynamics (A);
i = Battery current (A);
it = Extracted capacity (Ah);
Q = Maximum battery capacity (Ah);
A = Exponential voltage (V;)
B = Exponential capacity $(Ah)^{-1}$.

5.3. System operation strategy

The possibility of WPVS to satisfy the power demand depends on the atmospheric conditions. The battery bank state of charge (SOC), and the system status (grid connected or stand-alone), will define the control operation strategy. This is the EMCU role, which supervises the power flow of the whole system.

The proposed operation modes are dictated by the energy balance between the renewable sources, loads and storage elements.

The battery charging/discharging cycles must be made carefully, to extending its life cycle. The operation strategy takes in consideration SOC of the battery and provides the corresponding current references ($I_{max\ ch}$, $I_{max\ dis}$).

Both wind turbine and PV array subsystem (the input sources) can work at their maximum power (MPPT) or with a power regulation (PR). The power regulation control means that the subsystem can be inactive or working at a prescribed power.

Two cases will be described for the WPVS: grid connected and stand-alone.

5.3.1. Grid connected WPVS

In this case the following supposition has been made:

- the wind turbine and the PV array are working at the maximum power point;
- the load will be the main energy consumer;
- if the generated power is in excess, the battery bank will be charged (if is not fully charged) and the remained power is injected into the grid;
- if the generated power is not enough for the load, the battery bank supplies the difference, alone, or by means of the grid.

Figure 5.5. presents the flow chart of the grid connected WPVS [5.41-5.49]. The parameters used for the flow chart representation are:

- I_{HBLC}- the output current of HBLC;
- I'_{L}- the demanded current from the AC loads reflected to the DC bus side;
- I_{bat_ch}- the charging battery bank current;
- I_{bat_dis}- the discharging current of the battery;
- I_{max_ch}- the maximum charging current for the battery bank (according to SOC);
- I_{max_dis}- the maximum discharging current for the battery bank (according to SOC);
- I_{Gin}- the injected current into the grid;
- I_{Gout}- the input current from the grid.

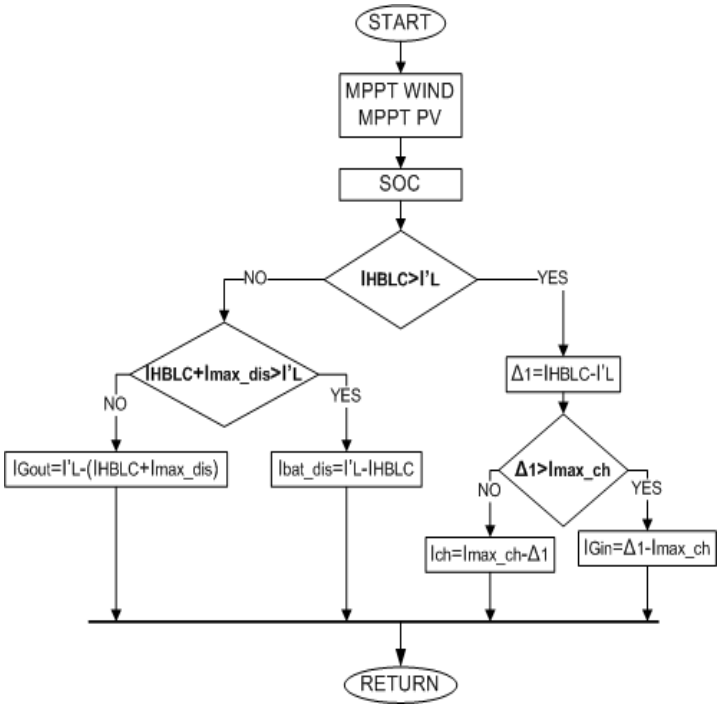

Figure 5.5. Flowchart for the grid connected WPVS.

The flow chart has four possible cases:

- the input sources give more power than needed. The remained power will be inject into the grid through I_{Gin};
- all generated power will be used by the AC loads and the battery bank (in charging mode);
- the input sources and the battery will supply the needed power by the AC loads;
- the input sources and the battery cannot generate enough power to ACL ($I_{HBLC}+ I_{max\_dis} < I'_L$). In this situation the system will take power from the grid through I_{Gout}.

5.3.2. Stand-alone WPVS

The following assumptions have been made for the stand-alone WPVS:

- the EMCU will try to get the maximum power from wind turbine which has the main role in energy generation;
- the PV array subsystem will play a complementary role;
- the stored energy in the battery bank will be used just in the case when the demanded power is higher than the input (PV and wind) power.

Figure 5.6. shows the operation strategy of the stand-alone WPVS [5.50-5.86]. The parameters used for the flow chart representation are the same as in previous subsection.

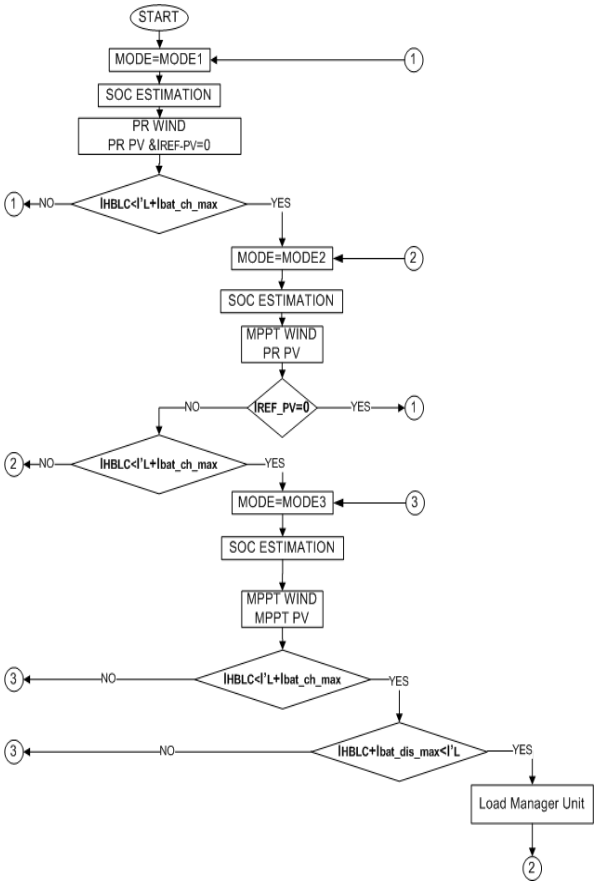

Figure 5.6. Flowchart for the stand-alone WPVS.

The flowchart has three sections, one for each operation mode presented bellow.

- operation mode 1: the wind turbine subsystem supplies all the demanded power, working under power regulation strategy (PR WIND). The PV array is inactive having zero reference current. The battery bank is storing energy. This operation mode is maintained as long as the wind turbine can provide (alone) all necessary power (to the load and to the battery);
- operation mode 2: the wind turbine subsystem works at maximum power point (MPPT WIND) and the PV array follows a power regulation strategy (PR PV). If the reference current of the PV array becomes zero, the wind turbine gives enough power to supply the load and to charge the battery to its maximum current, and WPVS reenters in mode 1. To pass in mode 3 the maximum HBLC output current must be lower than the total necessary current;
- operation mode 3: the wind turbine and the PV array work at maximum power point. The battery will ensure the power difference if necessary. In this case, if the maximum battery discharge current is exceeded, the load manager unit disconnects the load (or some loads). After this maneuver the system reenters mode 2.

5.4. Simulation results

In order to analyze the converter behavior a simulation of WPVS has been carried out in Matlab. The stand-alone WPVS consists of a variable speed wind turbine with a synchronous PM generator and a diode bridge rectifier - as a first power source, and a PV array - as a second power source, both connected at HBLC inputs.

Each input source of HBLC has its individual MPP control to get the maximum power, or can work in PR mode. The PR control means that the input sources can be inactive (if the reference current is zero) or work at a prescribed power. The HBLC output is connected to the battery and load (the inverter and AC loads were replaced by an equivalent DC resistive load).

The Matlab/Simulink model of WPVS is presented in figure 5.4.

5.4.1. Cosimulation, Matlab with PLECS

A first step in the HBLC integration into a hybrid system was the WPVS simulation using real models of the the converter elements. The WPVS has been simulated in Matlab/Simulink and the converter in PLECS, which is a blockset and can work under Matlab.

This simulation presents the most similar behaviour of the system to the real time conditions.

A simple mathematical relation was used to determine the maximum power point (P_{MPP}) of the wind turbine system, using information about its rotational speed ω_r [5.31]:

$$P_{MPP} = k_{opt}\omega_r^{\,3} \tag{5.8}$$

It has been known that optimum current for a photovoltaic panel is proportional to its short circuit current under various irradiation conditions.

The PV array is short-circuited for 100 μs at time intervals of 100 ms, and the short-circuit current is measured [5.87-5.92]. This method make use of the predetermined coefficient of 0.92 to obtain the maximum power point. This method has the advantage of simplicity in implementation.

From figure 5.7. it can be seen the IV curve for the modelled PV panel at 1000 W/m^2. For this irradiation the optimum current is 7.92A, corresponding to the point (MPP) where dP/dV=0.

Figure 5.8. presents the IV curve at 700 W/m^2. For this case the optimum current is 5.52A.

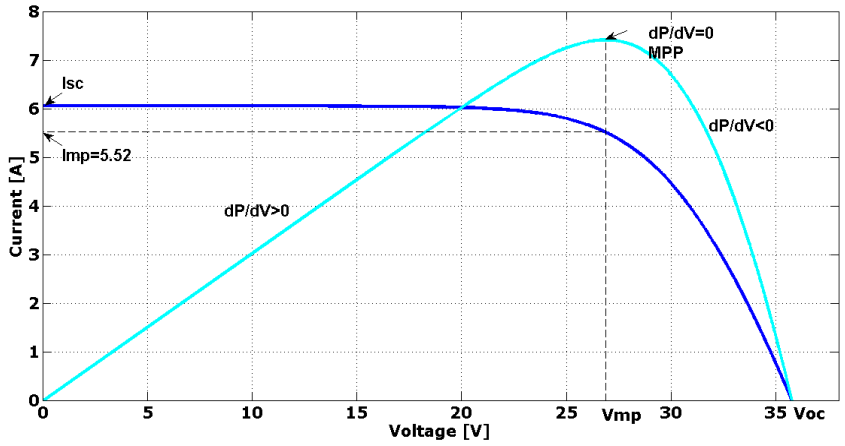

Figure 5.7. IV and PV curve for the simulated PV panel at 700 W/m^2.

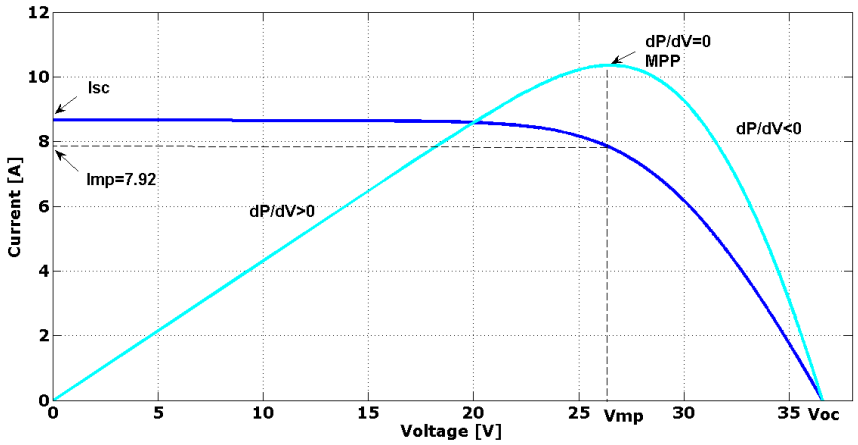

Figure 5.8. IV and PV curve for the simulated PV panel at 1000 W/m^2.

Figure 5.9. presents the system configuration used for the simulation of all operating modes.

The input sources parameters are: wind turbine nominal power P_{wind}=500W; PV panel nominal power P_{PV}=244W; PV open circuit voltage V_{oc}= 36.81V; PV short circuit current I_{sc}= 8.66A for a irradiation of 1000W/m^2; no. of PV cells is 60; battery nominal voltage 12V; battery capacity 110Ah.

The operating modes sequence, presented in the simulation results, is: mode 1, mode 2, mode 3, mode 2 and mode 1. For stabilization reasons, after a commutation WPVS remains in the new mode at least 30 ms.

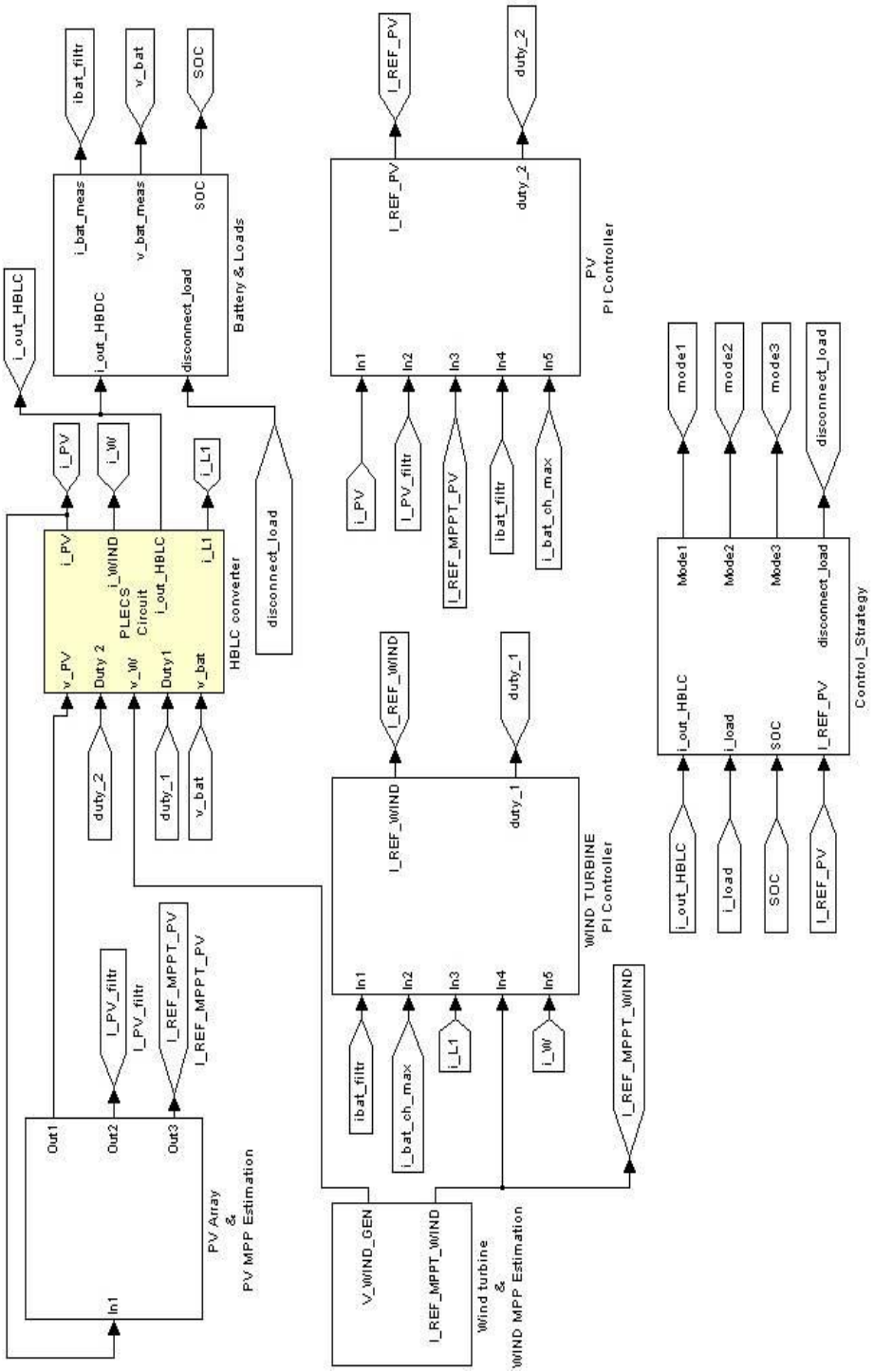

Figure 5.9. The WPVS block diagram

At the beginning WPVS operates in mode 1.

The condition to leave mode 1 and to enter mode 2 is satisfied at 0.02s, when the load current increases from 2A to 12A, as can be seen in figures 5.10-5.13. "load current waveform", but the system passes in mode 2 only at 0.03s after the delay is completed.

In mode 2 only the wind turbine system works at MPP and the PV system gives the supplementary power needed to charge the battery, at its maximum current (approximate 16.5A for SOC=50%). At 0.1s the load current is changed from 12A to 35A and the input sources don't have enough power to feed the load and to charge the battery, simultaneously. WPVS enters mode 3.

The wind turbine system is already in MPP from mode 2 and the PV system switches to MPPT mode. The output current of the PV panel rises.

Before reaching the reference value (5.57A), the MPP tracking algorithm, which runs once at 100ms, changes the MPP reference current at 8A (which corresponds to an irradiation of 1000W/m2), and the PV output current settles at this value.

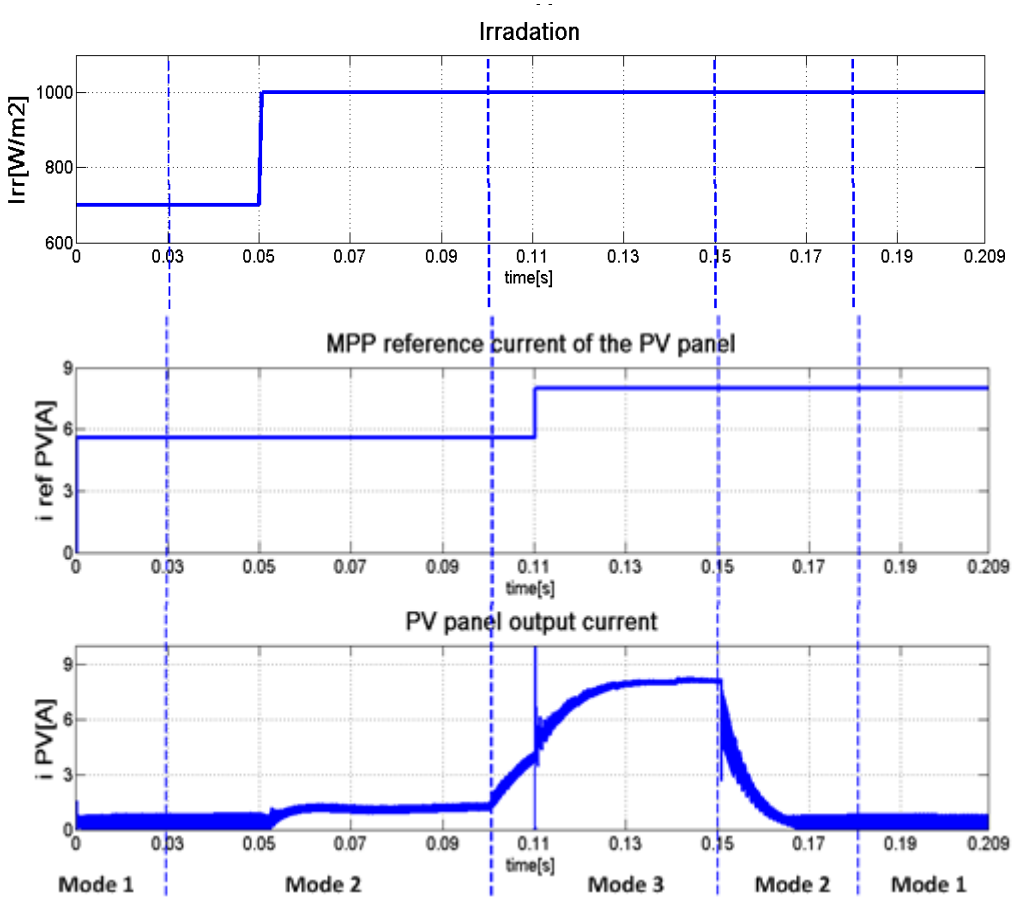

Figure 5.10. Irradation profile and the reference and measured PV current.

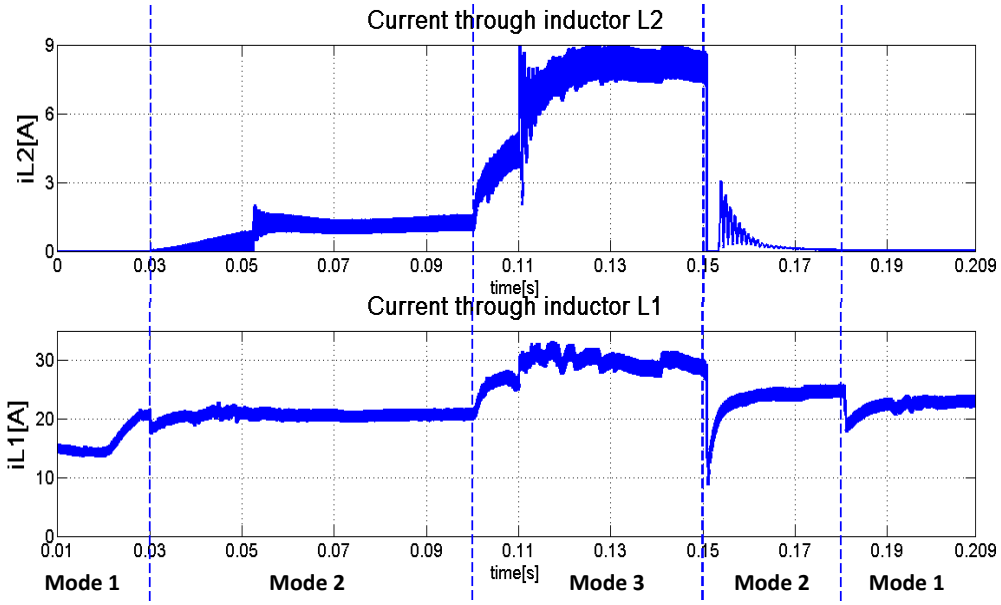

Figure 5.11. HBLC inductors currents.

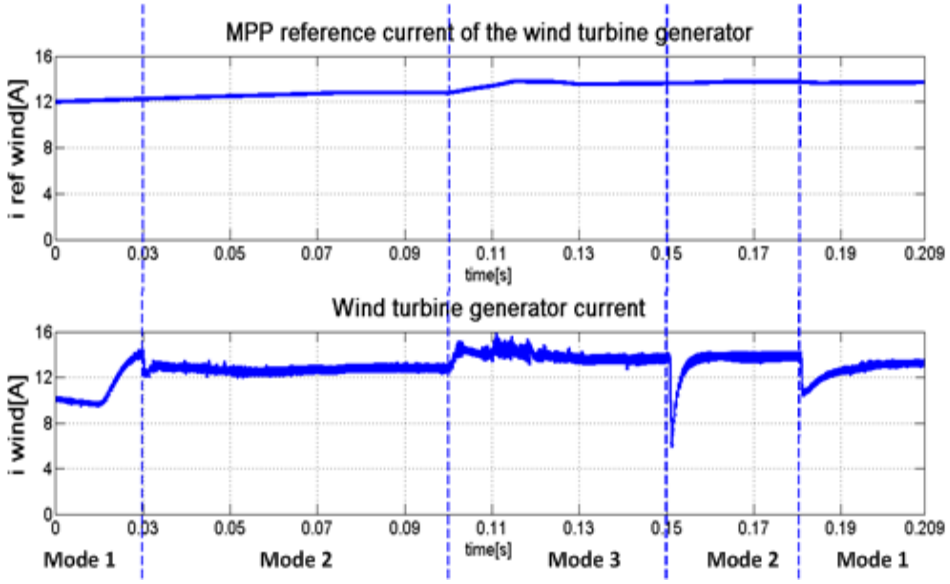

Figure 5.12. Prescribed and measured current for the wind turbine.

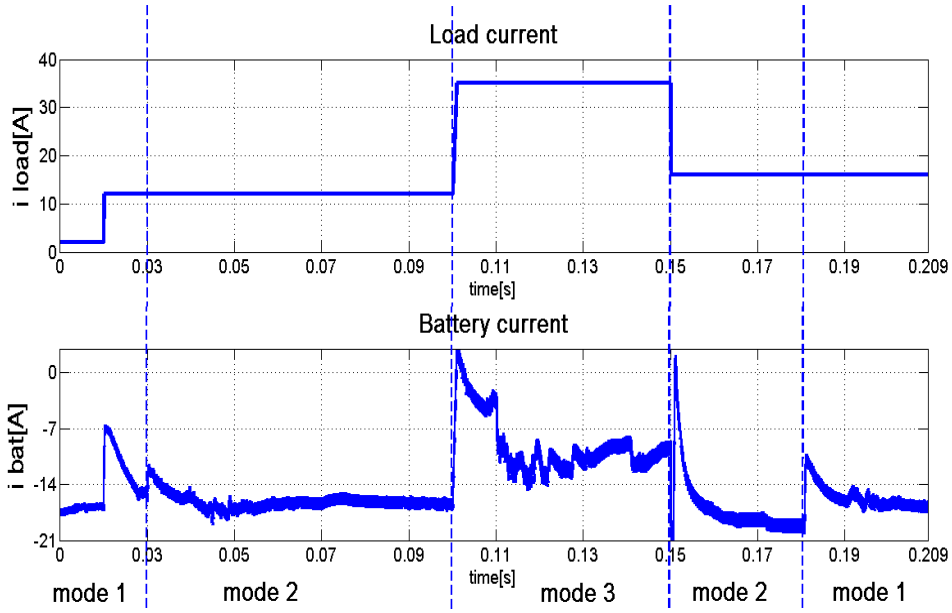

Figure 5.13. Load profile and the battery current.

At 0.15s the load current is reduced to 16A and WPVS enters in mode 2, but after the delay of 30ms the operation switches to mode 1 because the power given by the wind turbine is enough to supply the load and to charge the battery with the maximum charging current.

5.4.2. Matlab simulation without PLECS

Figure 5.14. presents the WPVS simulation setup developed in Matlab/ Simulink.

In order to catch the WPVS system behaviour in all three operating modes for a longer time the DC-DC converter (PLECS simulation) has been changed with the following equations:

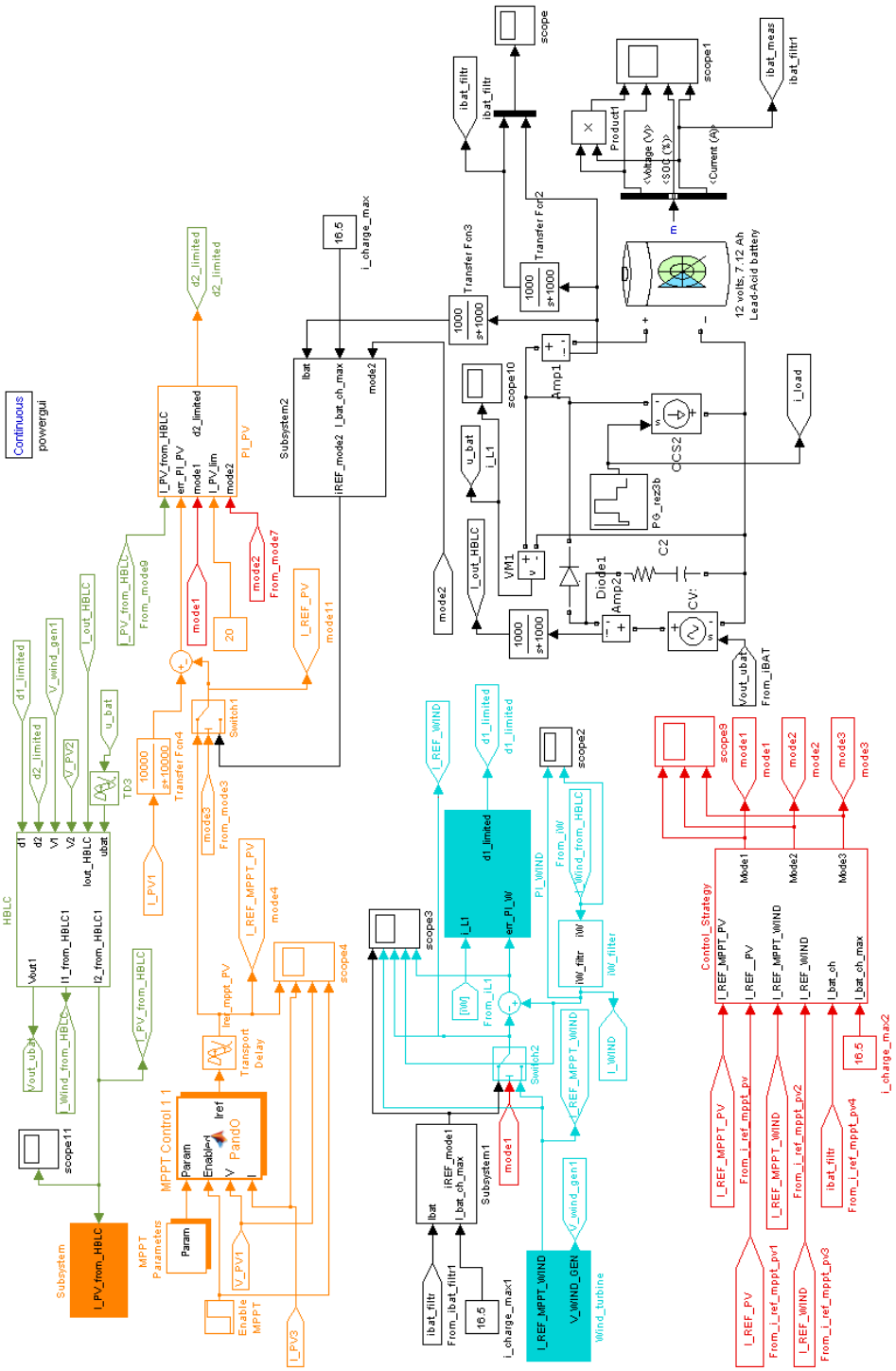

Figure 5.14. WPVS modelation in Matlab/Simulink

$$V_0 = \frac{d_1}{2-d_1}V_1 + \frac{d_2}{(2-d_1)(2-d_2)}V_2, \text{ for } d_1 \geq d_2 \quad (5.9.)$$

$$V_0 = \frac{d_1}{2-d_1}V_1 + \frac{2d_2-d_1}{(2-d_1)(2-d_2)}V_2, \text{ for } d_1 > d_2 \quad (5.10.)$$

$$I_{in1} = \frac{d_1}{2-d_1}I_{out} \quad (5.11.)$$

$$I_{in2} = \frac{d_2}{(2-d_1)(2-d_2)}, \text{ for } d_1 \geq d_2 \quad (5.12.)$$

$$I_{in2} = \frac{2d_2-d_1}{(2-d_1)(2-d_2)}, \text{ for } d_1 < d_2 \quad (5.13.)$$

The Matlab bloc diagram of the DC-DC converter is presented in figure 5.15. The converter prescribes two input currents: I_{in1} to the wind turbine source and I_{in2} to the PV panel source. The output voltage of the converter is sent to the battery subsystem, which prescribes the output current of the converter I_{out}.

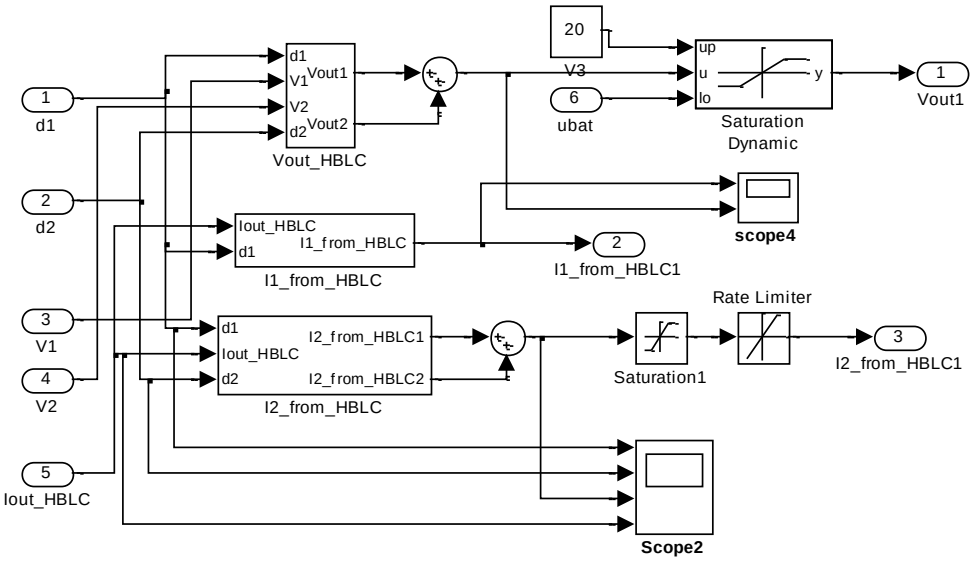

Figure 5.15. The bloc diagram of the HBLC converter.

The PV panel is modelled electrical and consists of sixty solar cells connected in series. The irradiation used for the simulation has a rump-up profile, starting from 700 W/m^2 and increasing to 1000 W/m^2.

For MPPT a perturb and observe algorithm was used. The flow chart of the algorithm is presented in figure 5.16.

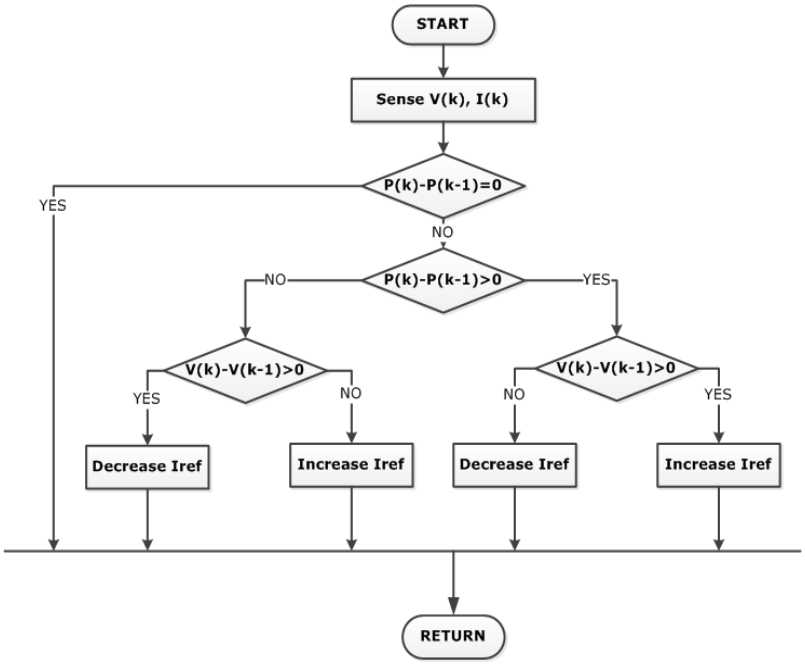

Figure 5.16. The flow chart for the perturb and observe algorithm.

The wind turbine is modelled and controlled exactly as in the previous simulation.

First has been studied the behavior of the system in operating mode 1, operating mode 2 and at the boundary between them. In figures 5.17 and 5.18 are presented the main simulation waveforms. In mode 1 the PV panel is inactive having the duty cycle d_2 limited to zero. In mode 2 the PV panel supplies the demanded power together with the wind turbine.

From figure 5.17 it can be seen that the wind turbine in mode 1 has two power regulation levels. The reference current is set first at 10A for 2s, and then at 11A for 3s.

It can be seen that the wind turbine current is following the reference current very accurate without ripples problems.

The PV panel irradiation is changed from 600W/m^2 in the first 5s to 1000W/m^2 in the last 5 s but that does not affects the PV panel functionality in these two modes.

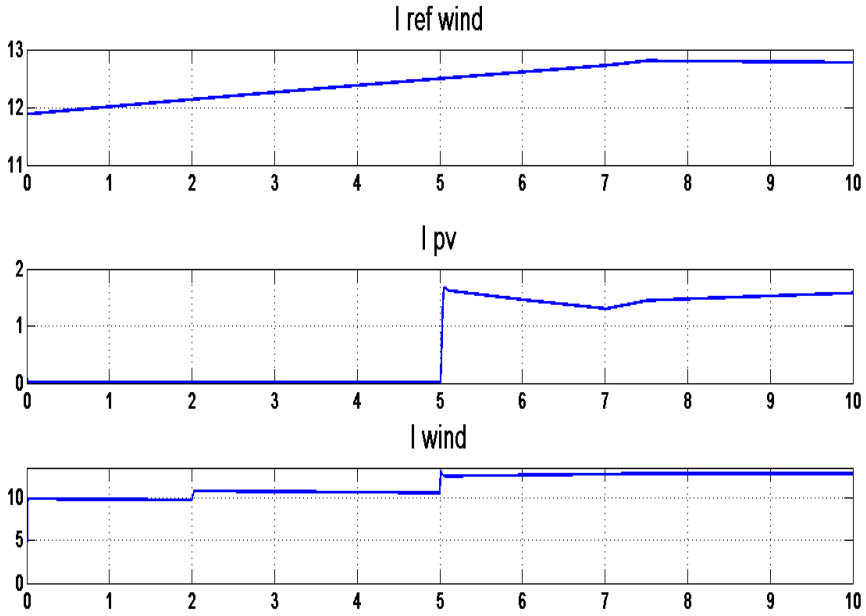

Figure 5.17. Input currents of the WPVS at the boundary between modes 1 and 2.

Figure 5.18. presents the load current which has three levels: 2A from 0s to 2s, 4A from 2s to 5s and 12A for the time range (5-10)s.

The battery current is 16.5A and the battery is charging in this two cases. At 5s which is the transition between the two operating modes the battery currents presents a ripple which is acceptable.

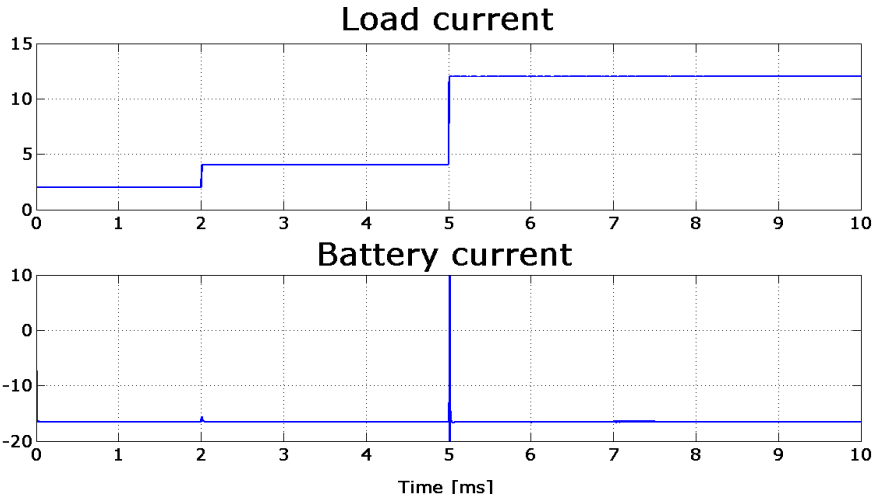

Figure 5.18. Output currents at the boundary between modes 1 and 2.

Figures 5.19. and 5.20. present the simulation results obtained at the boundary between mode 2 and mode 3. In mode 3 the PV panel works at maximum power point.

From 0s to 2s we can see WPVS working in mode 1 with the PV panel inactive and the wind turbine providing the needed power to the load. From 2s the PV panel has the current set around 1.5 A and working in power regulation. After 7s the PV panel works at MMPT and follows the reference current of 7.92A, corresponding to 1000W/m^2.

The wind turbine is set at MPP for the entire period of the two modes 2 and 3. It can be seen that the wind turbine current follows pretty well the reference current. Some negligible ripples are encounter at the transition points, at 2s and 7s.

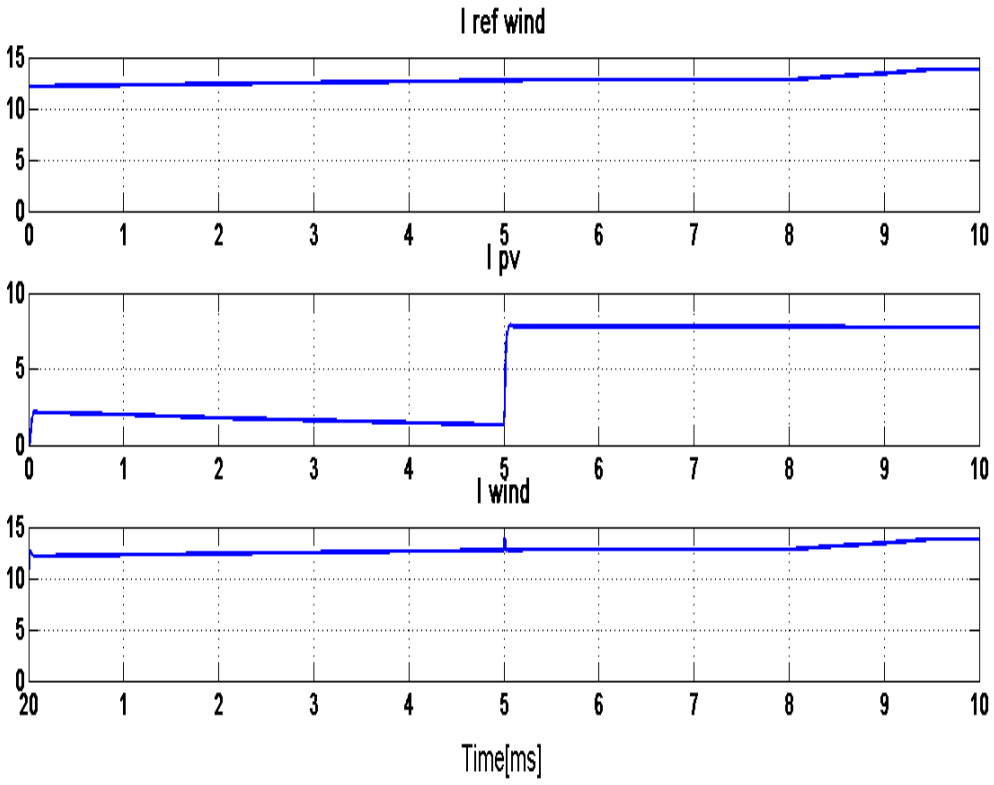

Figure 5.19. Input currents of the WPVS at the boundary between modes 2 and 3.

Figure 5.20. presents the load current of the WPVS and the battery current. The load current demands 12A for mode 2 and 35A for mode 3.

The battery current varies from 16.5A in mode 2 to 5A in mode 3 and is increasing in the last 2s of the mode 3. It has negligible ripples during the transition periods. For the entire period the battery is charging.

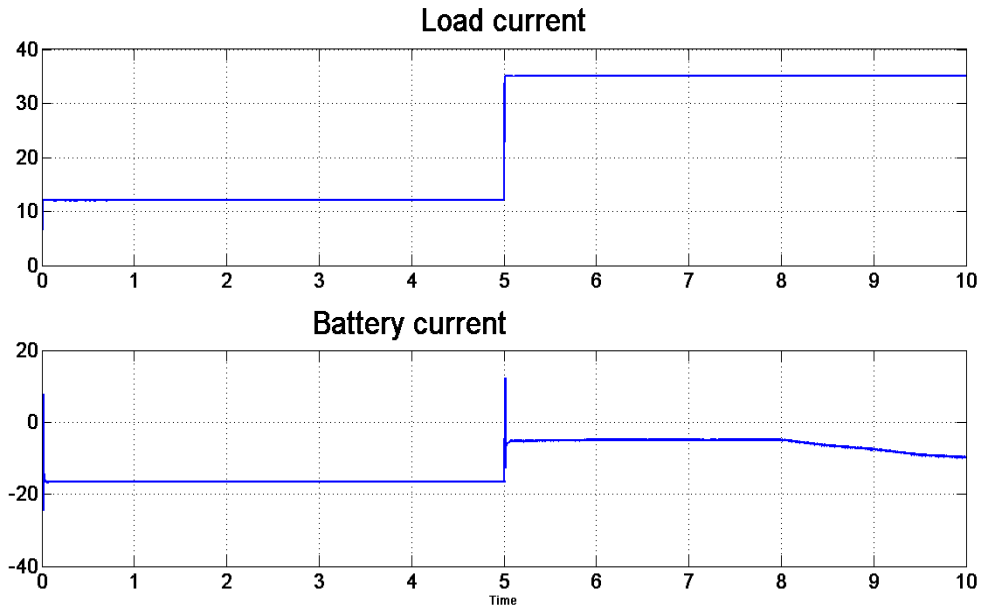

Figure 5.20. The output currents results at the boundary between modes 2 an 3.

The boundary between mode 3 and mode 2 has been simulated, too. The input and output currents are analyzed here and presented in figures 5.21 and 5.22.

In this case the PV panel starts working at MPP with a reference current of 5.52A from 2s to 3s, with a irradiation of 700 W/m^2. From 3s to 4s is the transition between the two irradiation level and the PV panel reference current is changed from 5.52A to 7.92A. At 4s the PV panel irradiation is increased at 1000 W/m^2. The PV panel current follows the prescribed current.

For the entire period the wind turbine follows the prescribed current and works at maximum power point tracking, as shown in figure 5.21.

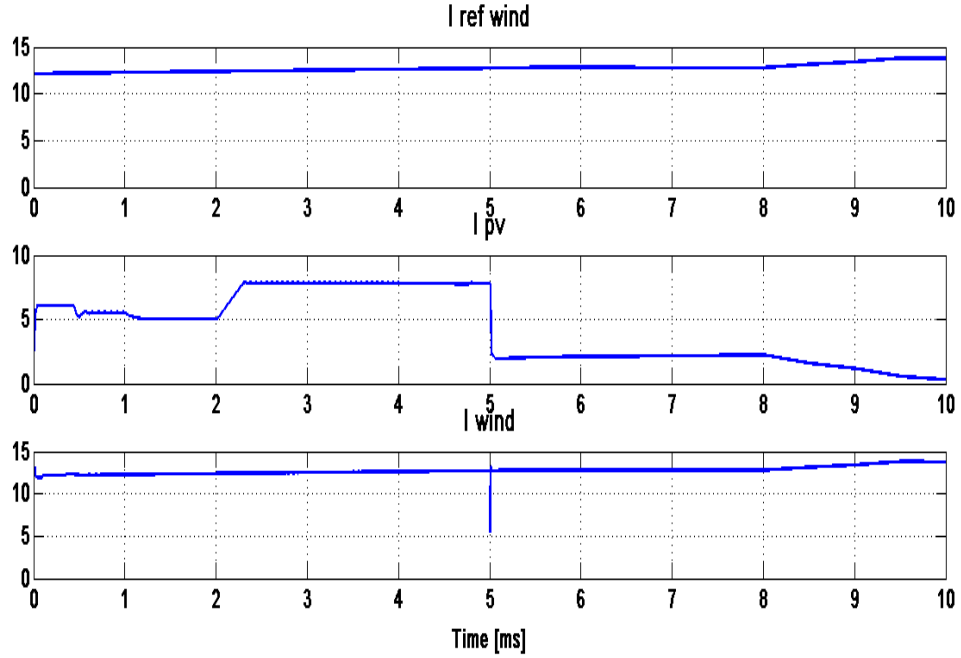

Figure 5.21. The input currents of the WPVS at the boundary between modes 3 and 2.

The load current is decreased from 35A in mode 3 to 14A in mode 2 as the figure 5.21 presents.

The battery current presented in figure 5.22 has a period of 0.4s in which the battery needs to be charged with a current of 10A. From 2.4s the battery current is around 0A and from 4s the battery currents stabilizes at 16.5A. A current ripple can be seen in this case, too.

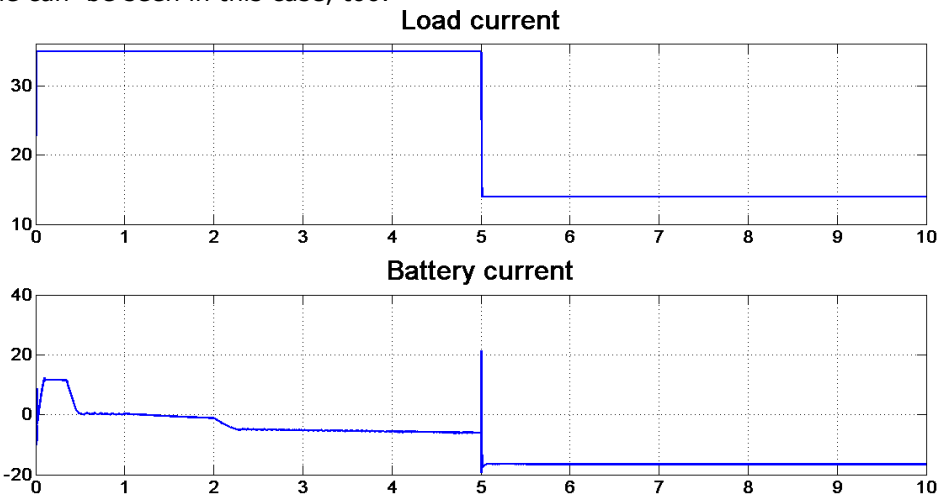

Figure 5.22. The simulation results for the output currents at the boundary between modes 3 and 2.

At the boundary between mode 2 and 1 the PV panel is passing from PR operation to being inactive. The irradiation is increased from 700 W/m^2 at 1000W/m^2.

In the power regulation mode the PV panel reference current is slowly decreasing from 3A to 2A, fig 5.23.

The wind turbine current is following the MPP reference current in mode 2 and then is working in PR with a prescribed current of 10.5A. The wind turbine current has negligible ripples at the transitions between the two different operating modes.

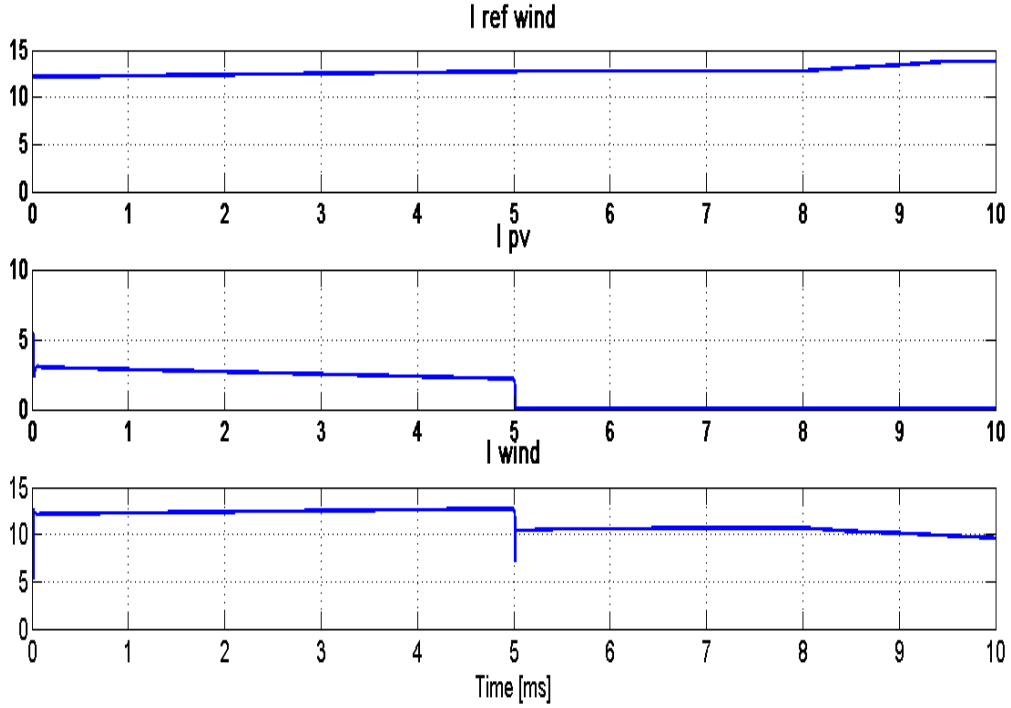

Figure 5.23. The input currents of the WPVS at the boundary between the modes 2 and 1.

The load current is decreased from 14A to 4A and makes possible the transition between mode 2 and mode 1, figure 5.24.

The battery current shown in figure 5.24 is stabile at 16.5A which is the maximum value. At the transition between the two modes some ripples can be seen.

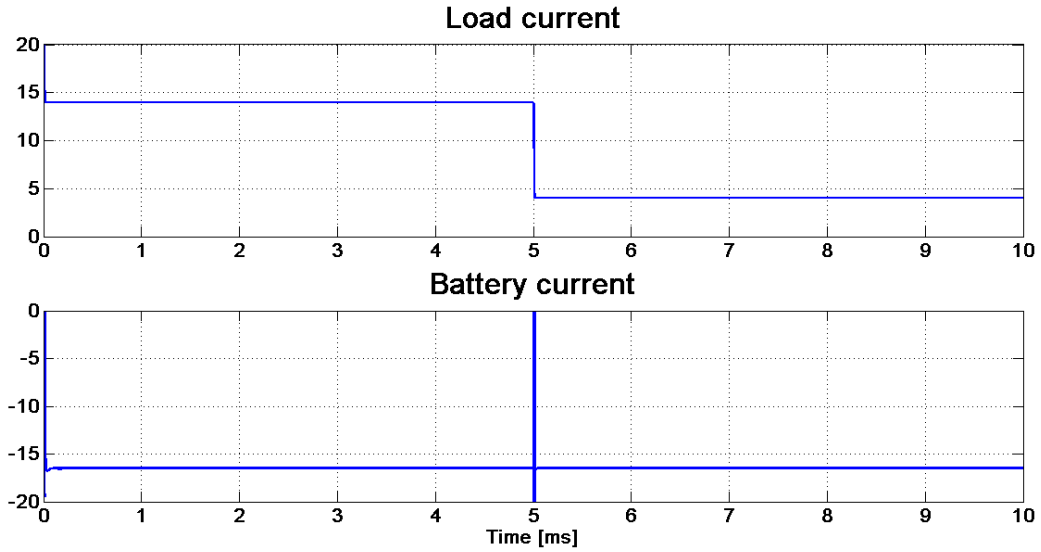

Figure 5.24. The simulation results for the output currents at the boundary between modes 2 and 1.

5.5. Experimental results

An experimental test bench was developed in order to obtain some preliminary results. It includes the HBLC prototype, a PV emulator, a DC power source (the wind energy system equivalent), a 12V/7Ah rechargeable battery, the resistive loads, and the corresponding voltage and current transducers.

The system is controlled using a dSPace platform.

The battery charging and discharging behaviour is observed and presented in this section.

Three operation modes are presented in the experimental results: in the first part of the experiment HBLC supplies from the two input sources the demanded power by the load and charges the battery. In the second part the input sources are not giving enough power to the load and the battery is discharging.

Figures 5.25 and 5.26 present the current and the voltage of emulated PV panel in the two different operation strategies. In the first section the PV panel works with MPPT and in the second part with PR. In the third section the PV is working with MPPT again.

Figure 5.27 presents the voltage of the wind turbine conversion system.

The battery current and voltage are presented in figures 5.28 and 5.29. It can be seen the battery charging and discharging characteristics in three operation modes. Some ripples can be observed at the boundary between charging and discharging regimes.

The load current is presented in figure 5.30. It can be seen that it has three levels corresponding to the system operation strategies.

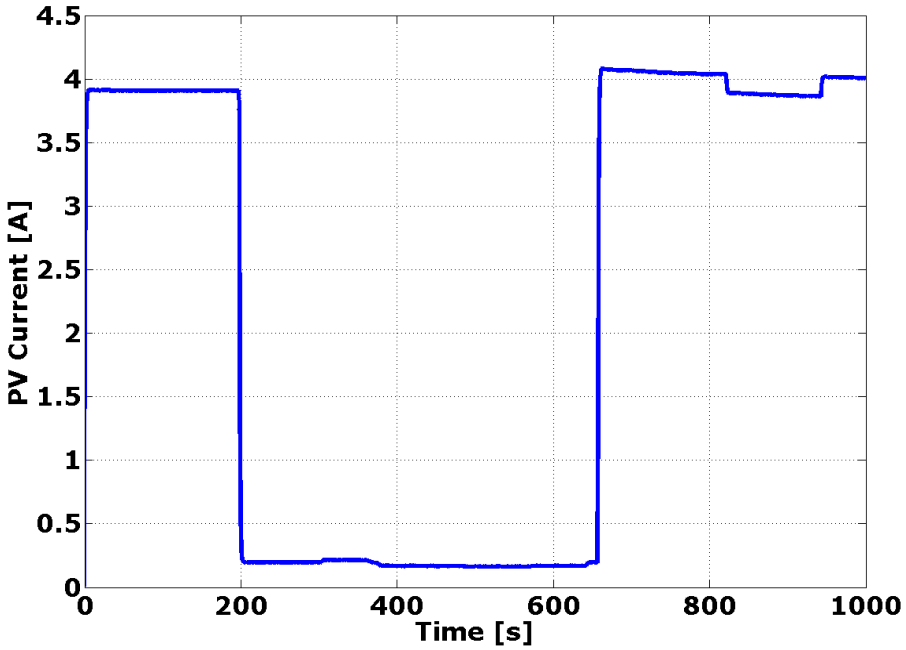

Figure 5.25. PV panel current obtained from experiment.

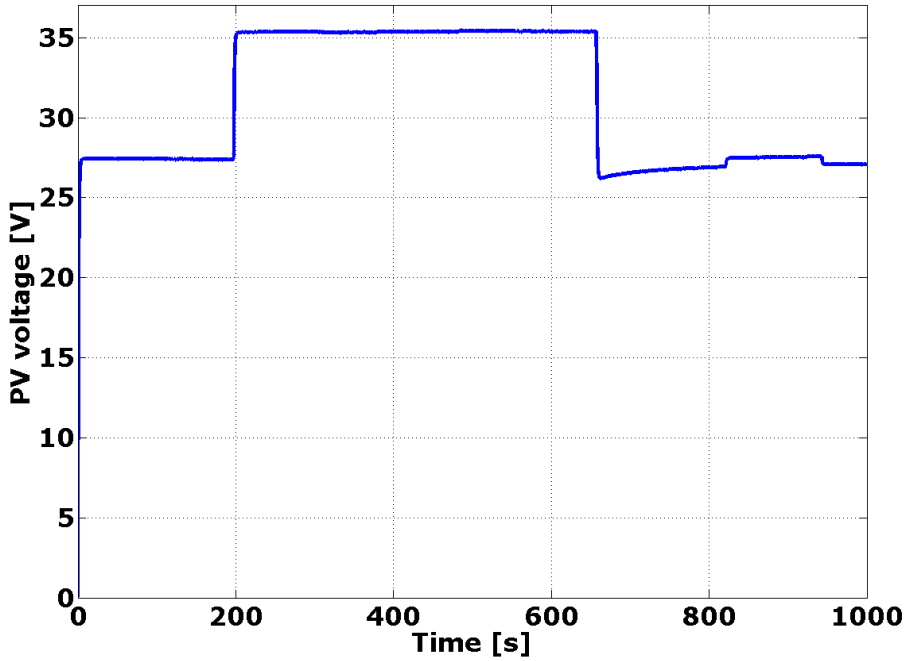

Figure 5.26. PV panel voltage.

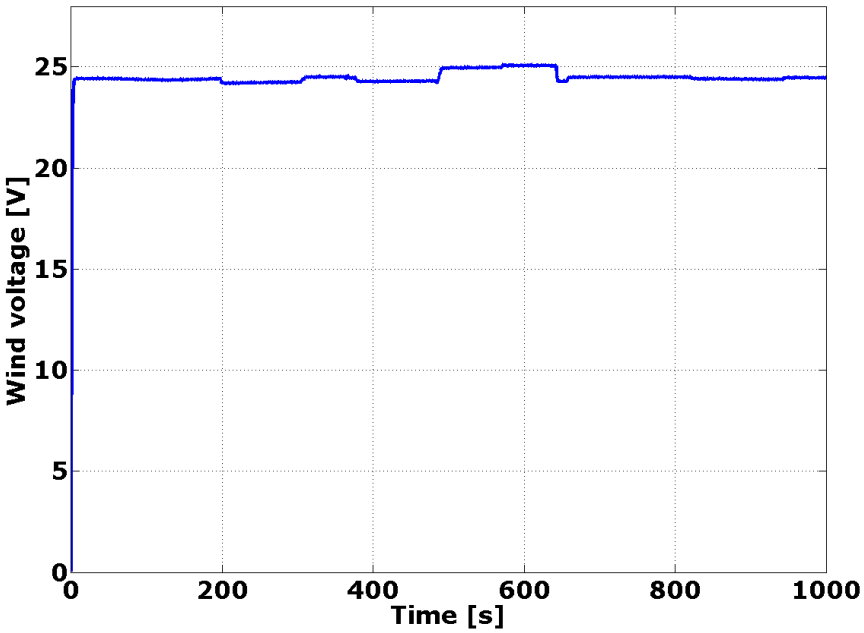

Figure 5.27. Wind turbine conversion system voltage.

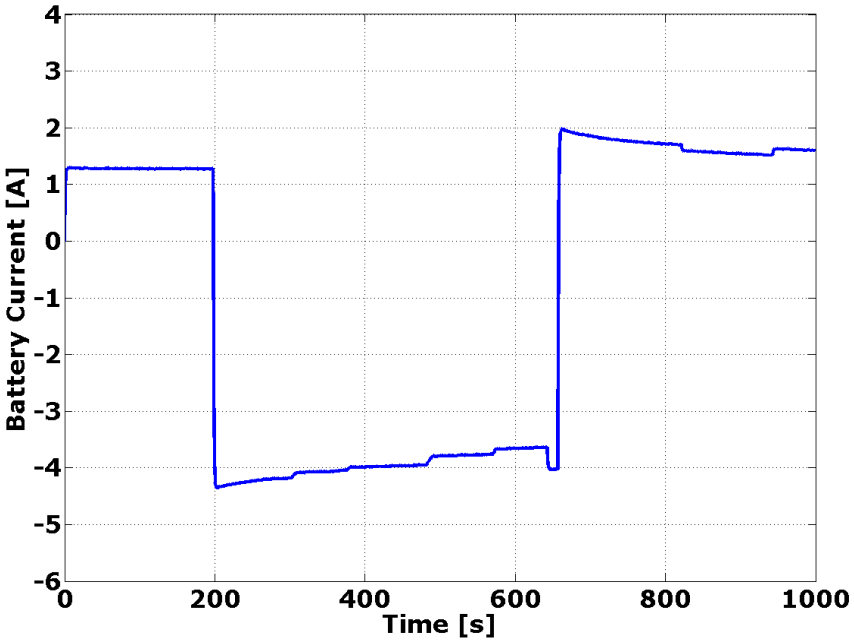

Figure 5.28. Battery current obtained from experiment.

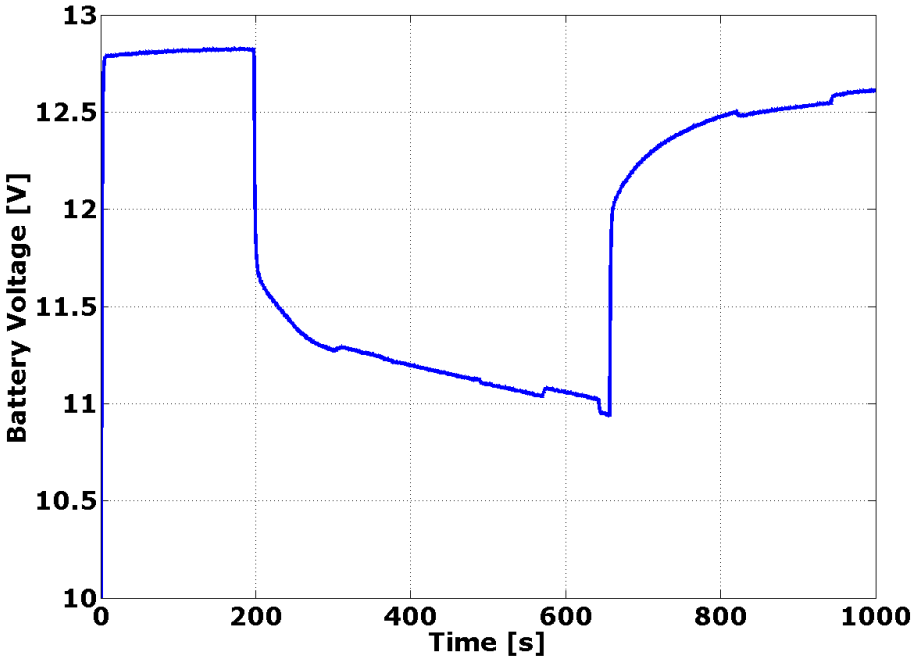

Figure 5.29. Battery voltage results.

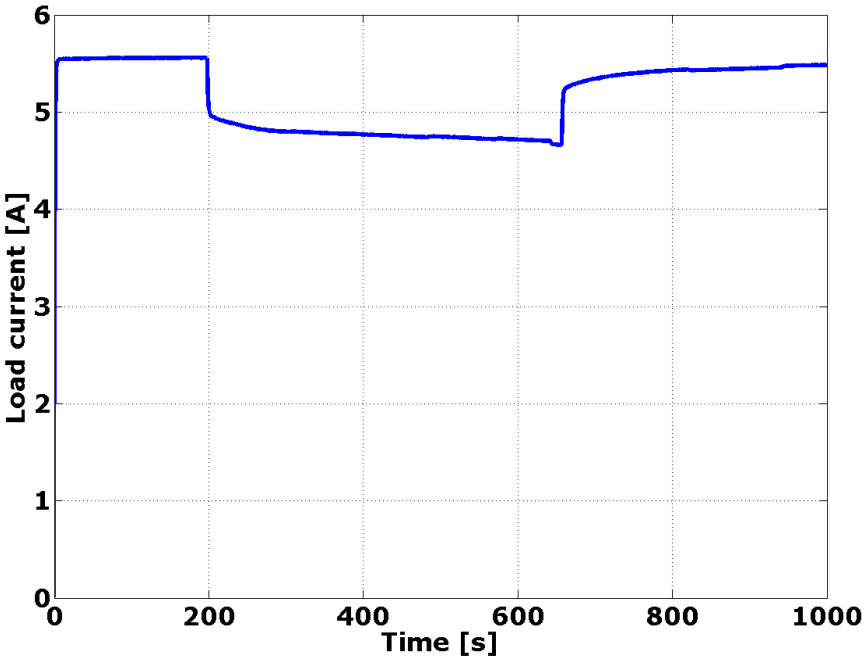

Figure 5.30. Load current profile.

5.6. Conclusions

The chapter presented and discussed a small power, mixed, wind turbine and PV array system in on-grid and off-grid regimes, which uses HBLC in order to transfer the energy from the two input sources to the load and the battery.

Two WPVS digital simulations have been carried out. A cosimulation between PLECS and Matlab/Simulink was chosen for a detailed analysis with the convertor elements. The cosimulation needs a very long run time.

A simulation where HBLC was replaced with the corresponded mathematical relations was performed in Matlab, without PLECS. This simulation has been prepared for the dSpace platform, in order to realize the set up control.

Two MPPT methods have been used to control the PV panel: the short current pulse based, and the perturb and observe tracking methods.

WPVS has three operating modes, which depends on the balance between the generated and the demanded power. Digital simulation results show that the system operation is stable in each operating mode, and the commutation between them is realized without any significant perturbation.

An experimental platform was also built, using PV and wind turbine system emulators, and some experimental results were presented. The control and data acquisition were made using a dSpace platform.

The experiments prove that the proposed HBLC is a viable solution for mixing renewable energy sources, and the proposed system completes the thesis content, adding a possible application for the proposed DC-DC hybrid structures.

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CHAPTHER 6
Experimental Platform

6.1. Dual input hybrid Buck converter prototypes

The experimental results for the proposed dual input hybrid Buck DC-DC converters have been obtained from two laboratory prototypes: first at 7.8 kHz and a second at 100 kHz.

The gate signals of the two power switches have been developed to be synchronized at turn on switch. The experiments have been made for a wide range of duty cycles.

6.1.1. The 7.8 kHz HBCL prototype

Figure 6.1 presents the circuit diagram of the prototype.

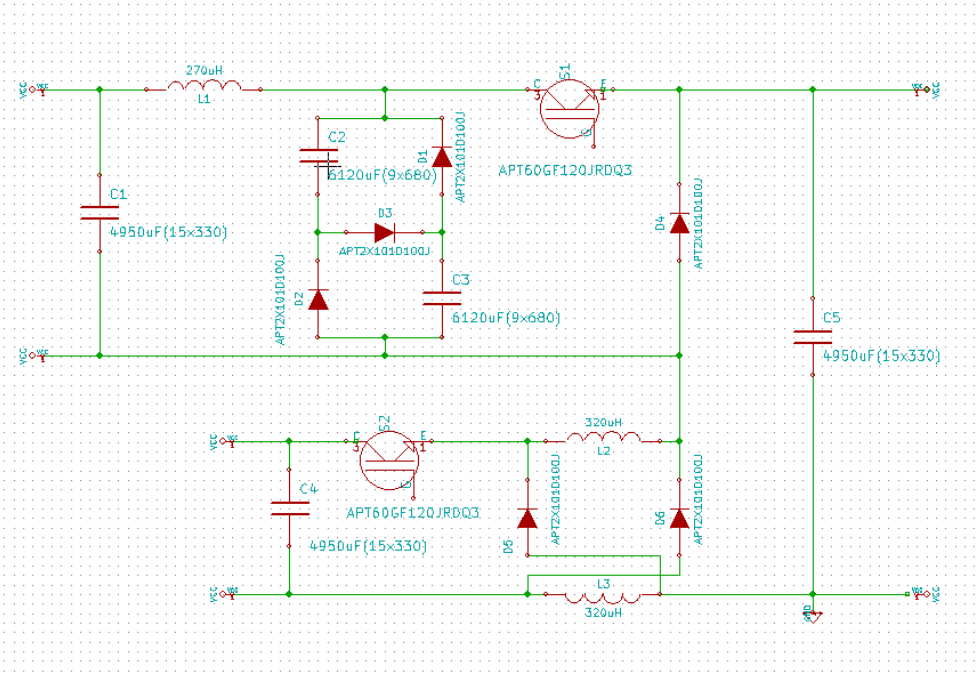


Figure 6.1 HBCL circuit diagram.

The prototype circuit parameters are:

Table 6.1. HBCL specifications

Parameter	Value
Input Voltage V_1	20-50V
Input Voltage V_2	20-50V
Inductor L_1	270μH
Inductors L_2=L_3	320μH
Capacitors C_1=C_2	6120μF
Capacitor C_3	4950μF

Thunderbolt IGBT APT60GT120JRDQ3 [1] was used for both switches and ultrafast soft recovery dual rectifier diode APT2X100D100J were chosen for the prototype development [2]. Technical specifications of the power elements are presented in the next table.

An optical isolated IGBT driver, HCPL-316J, controls the power transistors [3]. Figure 6.2. presents the circuit diagram of the power driver. The technical details of the IGBT driver are:

- 2.5 A maximum peak output current;
- Drive IGBTs up to I_C=150A, V_{CE}=1200V;
- Optically isolated, FAULT status feedback;
- SO-16 package;
- CMOS/ TTL compatible;
- 500ns max. switching speed.
- "soft" IGBT turn-off;
- Integrated fail-safe IGBT protection: desaturation (V_{CE}) detection and under Voltage lock-out protection (UVLO) with hysteresis;
- User configurable: inverting, noninverting, auto reset, auto-shutdown;
- Wide operating V_{CC} range: 15 to 30V
- -40 to +100 operating temperature range;
- 15kV/μs min. common mode rejection (CMR) at V_{CM}=1500V;
- Regulatory approvals: UL, CSA, IEC/EN/DIN EN 60747-5-2 (1230 V_{peak} working voltage).

Table 6.2. Power semiconductors specifications

	Parameter	Value
IGBT specifications	Collector-Emitter Voltage	1200V
	Continuous Collector Current	150A
	Collector Emitter On Voltage	3.2V
	Integrated Gate Resistor	2Ω
	Total Power Dissipation	830W
	Reverse Recovery Time	35ns
Diode specifications	Maximum D.C. Reverse Voltage	1000V
	Maximum Average Forward Current	95A
	Reverse Recovery Time	170ns

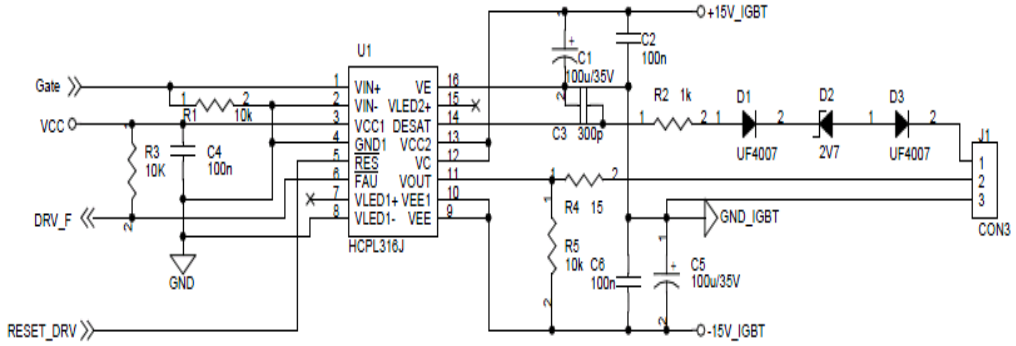


Figure 6.2. HCPL316J circuit diagram.

6.1.2. The 100kHz HBLC prototype

The prototype, build at 100 kHz switching frequency, is presented in figures 6.3 and 6.4. It can be seen the modularity of the construction: the hybrid Buck L side and the hybrid Buck C side, and the output capacitor bank, used to connect the two sides of the prototype.

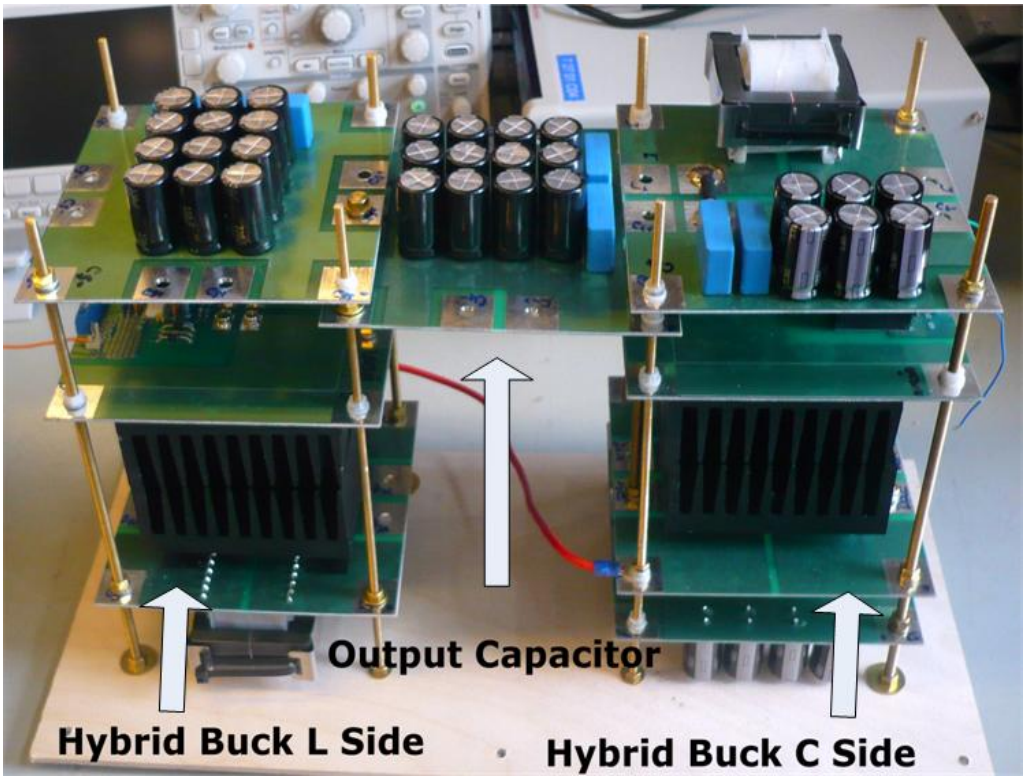


Figure 6.3. The 100kHz prototype.

For this prototype ACPL332J MOSFET driver was used [4]. The driver circuit diagram is presented in figure 6.3., and the technical details are given next:

- 2.5 A maximum peak output current;
- 2 A minimum peak output current
- 1.7 A Miller clamping;
- $I_{CC(max)}$<5mA maximum supply current;
- Open collector isolated fault feedback;
- Fault reset by next LED turn on (low to high) after fault mute period
- SO-16 package;
- CMOS/ TTL compatible;
- 250ns maximum propagation delay over temperature range;
- 100ns maximum pulse with distortion
- "soft" MOSFET turn-off;
- Integrated fail-safe MOSFET protection: desaturation (V_{CE}) detection and under Voltage lock-out protection (UVLO) with hysteresis;
- Wide operating V_{CC} range: 15 to 30V over temperature range
- -40 to +105 operating temperature range;
- 50kV/μs min. common mode rejection (CMR) at V_{CM}=1500V;
- Regulatory approvals: UL, CSA, IEC/EN/DIN EN 60747-5-2 (1230 V_{peak} working voltage).

The parameters of the HBLC power electronic devices are presented in table 6.3.

Table 6.3. Power semiconductors specifications

	Parameter	Value
MOSFET specifications	Drain-Source Voltage	200V
	Continuous Drain Current	120A
	Collector Emitter On Voltage	3.2V
	Drain-Source conduction Resistor	17mΩ
	Total Power Dissipation	600W
	Reverse Recovery Time	≤250ns
Diode specifications	Maximum D.C. Reverse Voltage	1000V
	Maximum Average Forward Current	60A
	Reverse Recovery Time	35ns

Figure 6.4 presents the circuit diagram of the prototype, and Figure 6.5 presents the schematic of power switch driver. Table 6.4. gives the other circuit parameters.

Table 6.4. HBLC specifications

Parameter	Value
Input Voltage V_1	20-60V
Input Voltage V_2	20-60V
Inductor L_1	28μH
Inductors L_2=L_3	28μH
Capacitors C_1=C_2	2640μF
Capacitor C_3	3960μF

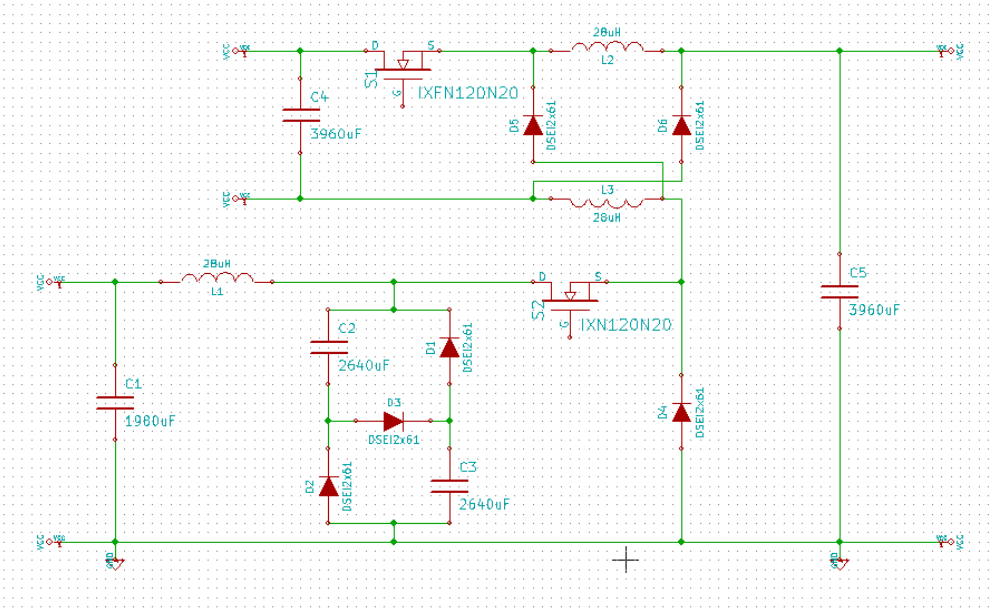


Figure 6.4. HBLC circuit diagram.

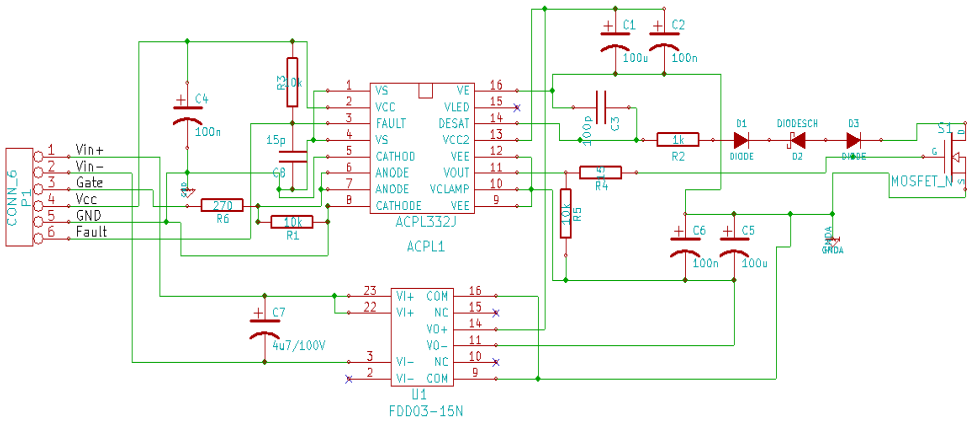


Figure 6.5. ACPL332J circuit diagram.

Figure 6.6-6.11 presents the circuit diagram of each PCBs, as configurable modules connection.

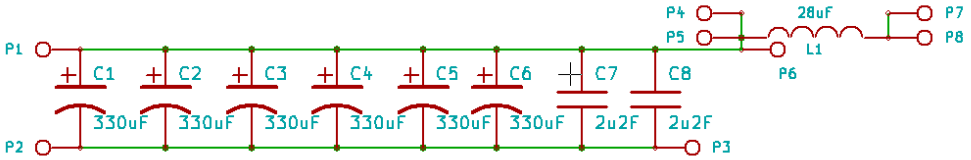


Figure 6.6. Capacitor C_1, inductor L_1 circuit diagram.

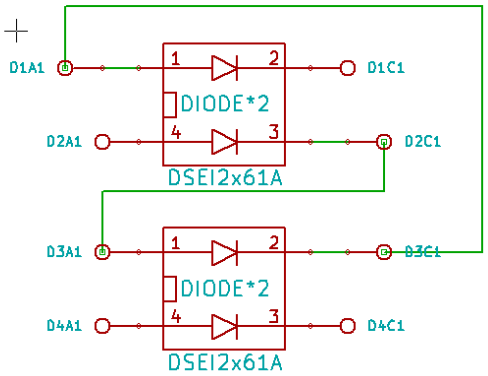


Figure 6.7. The diodes D_1, D_2, D_3 and D_4 circuit diagram.

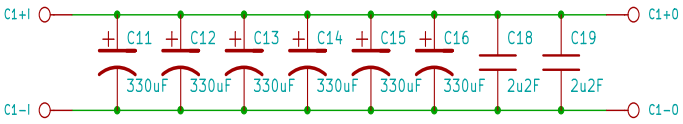


Figure 6.8. Capacitor C_4 circuit diagram.

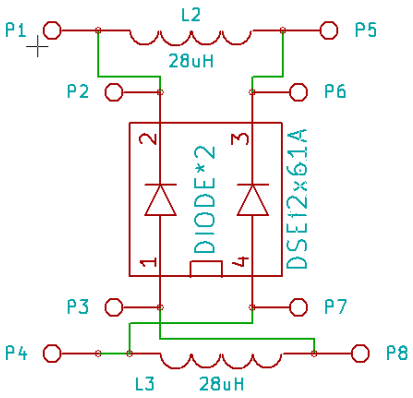


Figure 6.9. Diodes D_2 and D_3, inductors L_1 and L_3 circuit diagram.

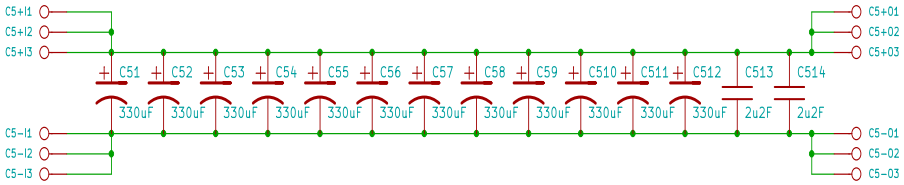


Figure 6.10. Capacitor C_5 circuit diagram.

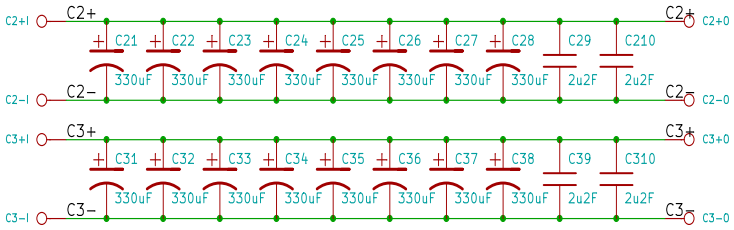


Figure 6.11. Capacitors C_2 and C_3 circuit diagram.

For the PWM gating signals, Texas Instruments TMS320F28335 Digital Signal Controller was used, figure 6.12, with:

- High-Performance Static CMOS Technology;
- High-Performance 32-Bit CPU ;
- 16-Bit or 32-Bit External Interface;

- On-Chip Memory;
- Clock and System Control;
- Up to 18 PWM Outputs.

An interface board has been used for PWM and for the converter feedback, signals, figure 6.12.

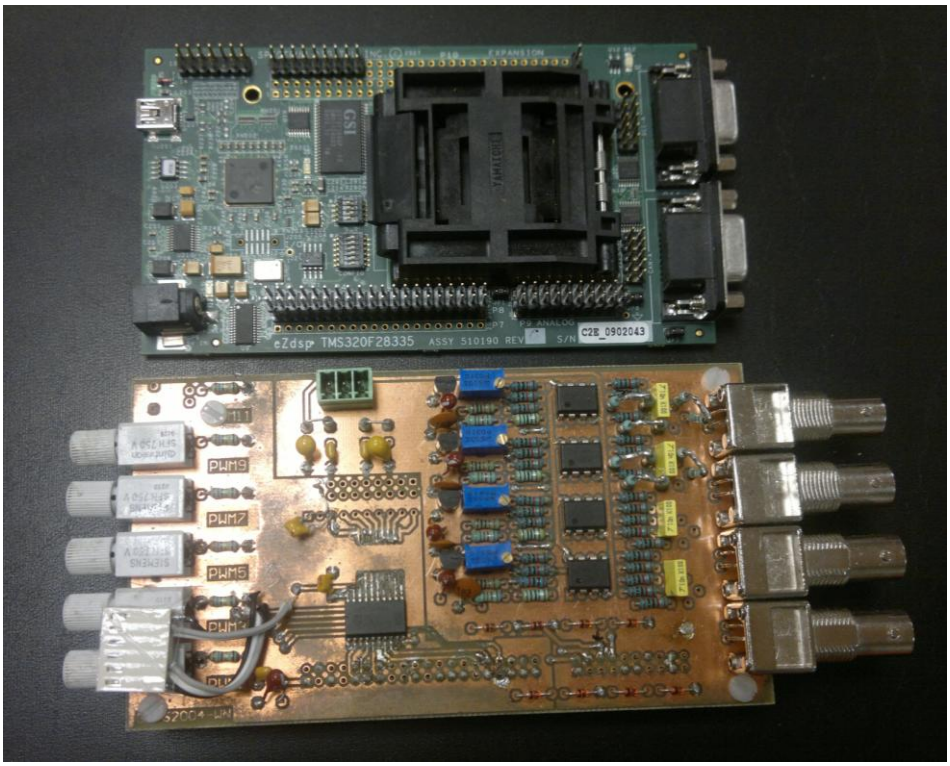


Figure 6.12. TMS320F28335 picture.

6.2. Wind and PV Mixed Energy System

Figure 6.13 presents the system configuration:

- A laboratory voltage source which keeps the place of the wind turbine;
- HBLC prototype;
- A current sensors board (4 current transducers LA 25-P);
- Zelio Isolated Analog Converters for the voltage signals acquisition;
- DS1103 control board;
- Regatron PV emulator;
- 12V/7Ah battery from Well ;
- 2.2Ω loads with max 10A;
- Three auxiliary laboratory voltage sources;
- Complementary tools (multimeters, oscilloscopes, etc.).

Figure 6.13. WPVS configuration.

6.2.1. DS1103

The dSpace DS1103 control board, figure 6.14, is designed to meet the requirements of modern rapid control prototyping.

Figure 6.14. DS1103 PPC Controller Board.

Technical description of the DS1103:

- ***Proccesor:*** IBM PowerPC 750GX, 933 MHz; Superscalar microprocessor; 3 integer units, 1 floating-point unit; 2 on-chip timer units; 32 KB instruction cache, 32 KB data cache; 1 MB, 4-way set-associative level-2 cache; Fast out-of-order instruction execution.
- ***Memory:*** 32 MB application SDRAM as program memory, cached; 96 MB communication SDRAM for data storage and data exchange with host.
- ***Interrupt Control Unit:*** Interrupts by host PC, CAN, slave DSP, serial interface, incremental encoders and 4 external inputs (user interrupts); PWM synchronous interrupt.

- ***Analog Input:*** 4 ADC units, 16-bit, multiplexed (4 channels each), sample & hold, 1 μs sampling time (for 1 channel); ±10V input voltage range; 83 dB signal-to-noise ratio; 4 channels, 16-bit, sample & hold, 800 ns sampling time; ±10V input voltage range; 83 dB signal-to-noise ratio.
- ***Analog Output:*** 8 channels, 16-bit, 5 μs settling time; ±10 V output voltage range.
- ***Incremental Encoder Interface:*** 6 channels digital input; 1 channel analog input with TC 3005H controller; Digital noise pulse filtering; Max. 1.65 MHz input frequency, i.e., fourfold pulse counts up to 6.6 MHz
- ***Digital I/O:*** 4-channel, 8-bit digital I/O port.
- ***Serial Interface:*** RS232 and RS422 transceiver support; Baud rate generator up to 1 Mbaud.
- ***CAN Interface:*** Infineon 80C164 microcontroller; ISO 11898 transceiver, max. 1 Mbaud; Clock frequency generator 10-20 MHz; 4 kWord of dual-port memory.
- ***Physical Characteristics:*** Power supply 5 V, 4 A / -12 V, 250 mA / 12 V, 750 mA; Operating temperature 0 to 50 °C (32 to 122 °F); Overtemperature sensor; Requires a full-size 16-bit ISA slot; I/O connection via 3 x 100 high-density connectors (ISA slots); Supports Plug & Play BIOS
- ***Slave DSP Subsystem:*** Texas Instruments' DSP TMS320F240, 20 MHz; 4 kWord of dual-port RAM; Supports symmetric/asymmetric PWM and space vector modulation; Three-phase PWM output plus 4 single PWM outputs; 4 capture inputs; 2 low-resolution ADC units for auxiliary purposes, sample & hold, 8 inputs each, 10-bit, 6.6 μs sampling time; 18-bit digital I/O (TTL)

Matlab/Simulink was design for the real time experimental test. Control Desk interface has been used for this scope (figure 6.15).

Figure 6.15. Control Desk interface.

6.2.2. PV emulator

For the PV panel emulator, Regatron Programmable High-Power DC Supplies was used. The product cod is TC.P.10.800.400.S. The parameters are:

- Line voltage 3 x 360 – 440 VAC
- Line frequency 48 – 62 Hz
- Mains connection type 3L+PE (no neutral)
- Input current 3 x 20 Arms
- Leakage current L to PE < 10 mA
- Output power range 0 – 10 kW
- Output voltage range 0 – 800 VDC
- Output current range 0 – 16 A
- Internal resistance range 0 – 1000 mΩ

The DC Power Supply can be programmed in order to have similar voltage/current characteristics as a real PV panel.

6.3. Conclusions

The experimental platform consists of:

- HBCL prototype, at 7.8kHz switching frequency, using IGBT transistors;
- HBLC prototype, at 100kHz switching frequency, using MOSFET transistors;
- A small-scale wind and PV mixed energy system, implemented with HBLC, DC power voltage sources for the input power generation, a rechargeable battery, resistive loads, and a dSpace control board;
- Additional electrical devices and tools.

All prototypes and the system were built with high performance components, in order to achieve good efficiency.

The circuit diagram and PCB conceptions and manufacture were made by the author, during the Ph.D. stage.

References:

[6.1] *APT150GT120JD*-http://www.microsemi.com/existing-parts/parts/47745#docs-specs
[6.2] *APT2X100D100J*-http://www.microsemi.com/existing-parts/parts/60108#docs-specs
[6.3] *HCPL316J*-http://www.avagotech.com/docs/AV02-0717EN
[6.4] *IXFN120N20*-http://ixdev.ixys.com/DataSheet/96538.pdf
[6.5] *DSEI2x61*-http://ixdev.ixys.com/DataSheet/96508.pdf
[6.6] *ACPL332J*-http://www.avagotech.com/docs/AV02-0120EN
[6.7] *Kicad*-http://www.kicad-pcb.org/display/KICAD/KiCad+EDA+Software+Suite
[6.8] *TMS320F28335*-http://www.ti.com/lit/ds/sprs439m/sprs439m.pdf
[6.9] *TC.P.10.800.400.S*-http://www.regatron.ch/download.php?file_id=214
[6.10] *dSpace*-http://www.dspace.com/en/pub/start.cfm

CHAPTHER 7
Conclusion and Contributions

7.1. Conclusions

The presents work is a research in the field of multi-input DC-DC converters. Based on the literature description of mixing technologies in this domain, four new topologies of dual input DC-DC converters have been proposed, studied analytically and simulated. Two of them was built as laboratory prototypes, and was tested in order to validate the theoretical aspects. An application with one of the proposed converter was implemented in a wind and PV mixed energy system.

The proposed converters have the following advantages:

- less power electronic components (they use some common components);
- reduced input current ripples for a part of them;
- the output voltage is reduced more times, for the same duty cycle, compared with the classical DC-DC converters;
- a relative good efficiency.

The proposed converters have been analytically studied, simulated (using PSim, LTSpice and PLECS), and partially experimented.

From the new topologies, HBLC has the advantage of a common ground between one input voltage source and the converter output. This topology is the main concern of the thesis.

A complete description of HBLC was made. The converter has an average efficiency of 94%, determined from simulation results. The converter has been studied in BCM in order to develop a design procedure.

The analytical procedure, having as objective the inductance values of the output filter in BCM was assisted by a numerical method (using Mathematica), and validated by simulations.

Small scale laboratory prototypes of HBCL and HBLC were built and tested. The experimental results were compared with simulations, and a good correspondence was obtained.

HBLC is suitable for renewable energy sources applications and a small mixed wind and PV energy system has been proposed, with the corresponding control algorithms, including the energy management.

The cosimulation between Matlab/Simulink and Plecs, using a complete model of HBLC, demonstrates that the system can achieve the proposed objectives.

In order to extend the simulation, in good conditions related to the computing time, HBLC was described in a simplified way, and the simulations were performed only with Matlab/Simulink.

The system was built using the HBLC prototype, an PV emulator, a variable voltage DC source (as a substitute for the wind produced energy), a small rechargeable battery, and resistive loads. The control was implemented with a dSpace board.

Preliminary experimental results validate the theoretical considerations and prove together that HBLC is a good solution for mixing renewable energy sources.

7.2. Contributions

The author contributions in this work can be summarized as follows:

- the review of the main multi-input DC-DC converters and systems, developed in the literature;
- four new dual-input DC-DC converter topologies based on hybrid and classical structures have been proposed;
- the analytical study, validated by simulations, of the proposed converters, made in PSim, LTSpice, and PLECS;
- the design procedure, regarding the output inductive elements for HBLC, based on BCM equations, solved in Mathematica;
- HBLC integration into a wind turbine and PV mixing energy system;
- the control strategy proposed for the system, studied with digital simulations (cosimulations Matlab/Simulik-PLECS, and only with Matlab/Simulink);
- the laboratory prototypes (HBCL at 7.8kHz, and HBLC at 100kHz) built in order to validate the theoretical results;
- the small scale wind and PV mixing energy system and the corresponding control, using dSpace board;
- the preliminary experimental results obtained with the proposed wind turbine and PV mixing energy system;

7.3. Future work

The thesis leaves open the following research direction:

- A more complex design procedure for all converters elements;
- Experimental validation of the converters efficiencies;
- Full experimental validation for the wind and PV mixing energy system;
- The implementation of control strategies, both for converters and systems in an industrial hardware;
- The extension of the proposed converters applications in other industries (e.g. automotive).

Appendix

A1. TMS320F28335 Digital Signal Controller Program

```
// TI File $Revision: /main/8 $
// Checkin $Date: April 21, 2008   15:41:53 $
//###########################################################
#########################
//
// FILE:    Example_2833xEPwmUpDownAQ.c
//
// TITLE:   Action Qualifier Module - Using up/down count
//
// ASSUMPTIONS:
//
//    This program requires the DSP2833x header files.
//
//    Monitor ePWM1-ePWM3 pins on an oscilloscope as described
//    below.
//
//      EPWM1A is on GPIO0
//      EPWM1B is on GPIO1
//
//      EPWM2A is on GPIO2
//      EPWM2B is on GPIO3
//
//      EPWM3A is on GPIO4
//      EPWM3B is on GPIO5
//
//    As supplied, this project is configured for "boot to SARAM"
//    operation.  The 2833x Boot Mode table is shown below.
//    For information on configuring the boot mode of an eZdsp,
//    please refer to the documentation included with the eZdsp,
//
//      $Boot_Table:
//
//        GPIO87   GPIO86     GPIO85   GPIO84
//         XA15     XA14       XA13     XA12
//          PU       PU         PU       PU
//       ==========================================
//          1        1          1        1    Jump to Flash
//          1        1          1        0    SCI-A boot
//          1        1          0        1    SPI-A boot
//          1        1          0        0    I2C-A boot
//          1        0          1        1    eCAN-A boot
//          1        0          1        0    McBSP-A boot
//          1        0          0        1    Jump to XINTF x16
//          1        0          0        0    Jump to XINTF x32
```

```
//         0      1      1      1    Jump to OTP
//         0      1      1      0    Parallel GPIO I/O boot
//         0      1      0      1    Parallel XINTF boot
//         0      1      0      0    Jump to SARAM       <- "boot to SARAM"
//         0      0      1      1    Branch to check boot mode
//         0      0      1      0    Boot to flash, bypass ADC cal
//         0      0      0      1    Boot to SARAM, bypass ADC cal
//         0      0      0      0    Boot to SCI-A, bypass ADC cal
//                                  Boot_Table_End$
//
// DESCRIPTION:
//
//    This example configures ePWM1, ePWM2, ePWM3 to produce an
//    waveform with independant modulation on EPWMxA and
//    EPWMxB.
//
//    The compare values CMPA and CMPB are modified within the ePWM's ISR
//
//    The TB counter is in up/down count mode for this example.
//
//    View the EPWM1A/B, EPWM2A/B and EPWM3A/B waveforms
//    via an oscilloscope
//
//
//###########################################################################
// $TI Release: DSP2833x/DSP2823x C/C++ Header Files V1.31 $
// $Release Date: August 4, 2009 $
//###########################################################################


#include "DSP28x_Project.h"     // Device Headerfile and Examples Include File


// Prototype statements for functions found within this file.
void InitEPwm1(void);
void InitEPwm2(void);

void main(void)
{
  int i = 0;

// Step 1. Initialize System Control:
// PLL, WatchDog, enable Peripheral Clocks
// This example function is found in the DSP2833x_SysCtrl.c file.
  InitSysCtrl();

// Step 2. Initalize GPIO:
// This example function is found in the DSP2833x_Gpio.c file and
// illustrates how to set the GPIO to it's default state.
```

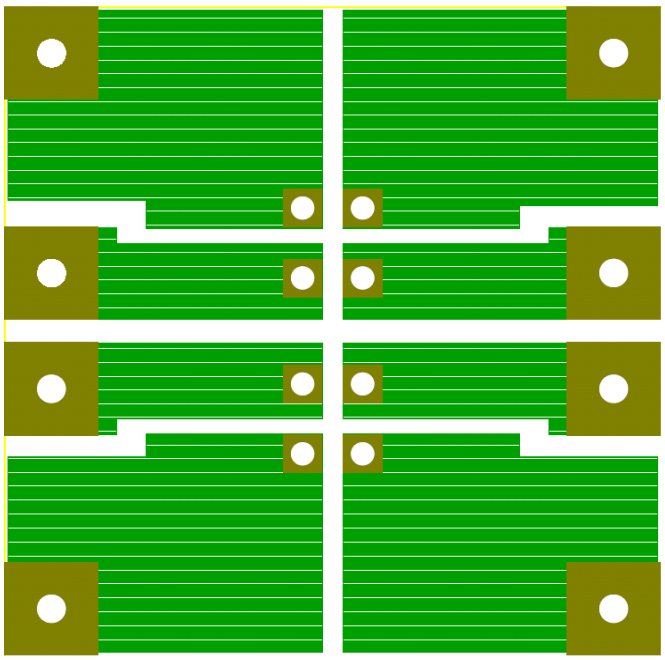
```
// InitGpio();  // Skipped for this example

// For this case just init GPIO pins for ePWM1, ePWM2, ePWM3
// These functions are in the DSP2833x_EPwm.c file
   InitEPwm1Gpio();
   InitEPwm2Gpio();


// Disable CPU interrupts and clear all CPU interrupt flags:
   IER = 0x0000;
   IFR = 0x0000;

// Step 4. Initialize all the Device Peripherals:
// This function is found in DSP2833x_InitPeripherals.c
// InitPeripherals();  // Not required for this example

// For this example, only initialize the ePWM

   EALLOW;
   SysCtrlRegs.PCLKCR0.bit.TBCLKSYNC = 0;
   EDIS;

   InitEPwm1();
   InitEPwm2();

   EALLOW;
   SysCtrlRegs.PCLKCR0.bit.TBCLKSYNC = 1;
   EDIS;

// Step 5. User specific code, enable interrupts:

// Enable CPU INT3 which is connected to EPWM1-3 INT:
   IER |= M_INT3;

// Enable EPWM INTn in the PIE: Group 3 interrupt 1-3
   PieCtrlRegs.PIEIER3.bit.INTx1 = 1;
   PieCtrlRegs.PIEIER3.bit.INTx2 = 1;
   PieCtrlRegs.PIEIER3.bit.INTx3 = 1;

// Enable global Interrupts and higher priority real-time debug events:
   EINT;   // Enable Global interrupt INTM
   ERTM;   // Enable Global realtime interrupt DBGM

// Step 6. IDLE loop. Just sit and loop forever (optional):
   for(;;)
   {
      i = i +1;
      asm("        NOP");
   }

}
```

```
void InitEPwm1()
{

        EPwm1Regs.TBPRD = 1500; // Period = 601 TBCLK counts
        EPwm1Regs.CMPA.half.CMPA = 600; // Compare A = 1050 TBCLK counts
        EPwm1Regs.CMPB = 200; // Compare B = 200 TBCLK counts
        EPwm1Regs.TBPHS.all = 0; // Set Phase register to zero
        EPwm1Regs.TBCTR = 0; // clear TB counter
        EPwm1Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP;
        EPwm1Regs.TBCTL.bit.PHSEN = TB_DISABLE; // Phase loading disabled
        EPwm1Regs.TBCTL.bit.PRDLD = TB_SHADOW;
        EPwm1Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_DISABLE;
        EPwm1Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1; // TBCLK = SYSCLK
        EPwm1Regs.TBCTL.bit.CLKDIV = TB_DIV1;
        EPwm1Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
        EPwm1Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
        EPwm1Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO; // load on CTR =
Zero
        EPwm1Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO; // load on CTR =
Zero
        EPwm1Regs.AQCTLA.bit.ZRO = AQ_SET;
        EPwm1Regs.AQCTLA.bit.CAU = AQ_CLEAR;
        EPwm1Regs.AQCTLB.bit.ZRO = AQ_SET;
        EPwm1Regs.AQCTLB.bit.CBU = AQ_CLEAR;

   EPwm1Regs.ETSEL.bit.INTSEL = ET_CTR_ZERO;     // Select INT on Zero event
   EPwm1Regs.ETSEL.bit.INTEN = 1;               // Enable INT
   EPwm1Regs.ETPS.bit.INTPRD = ET_3RD;          // Generate INT on 3rd event
}


void InitEPwm2()
{
        EPwm2Regs.TBPRD = 1500; // Period = 601 TBCLK counts
        EPwm2Regs.CMPA.half.CMPA = 900; // Compare A = 750 TBCLK counts
        EPwm2Regs.CMPB = 200; // Compare B = 200 TBCLK counts
        EPwm2Regs.TBPHS.all = 0; // Set Phase register to zero
        EPwm2Regs.TBCTR = 0; // clear TB counter
        EPwm2Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP;
        EPwm2Regs.TBCTL.bit.PHSEN = TB_ENABLE; // Phase loading disabled
        EPwm2Regs.TBCTL.bit.PRDLD = TB_SHADOW;
        EPwm2Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_DISABLE;
        EPwm2Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1; // TBCLK = SYSCLK
        EPwm2Regs.TBCTL.bit.CLKDIV = TB_DIV1;
        EPwm2Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
        EPwm2Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
        EPwm2Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO; // load on CTR =
Zero
        EPwm2Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO; // load on CTR =
```

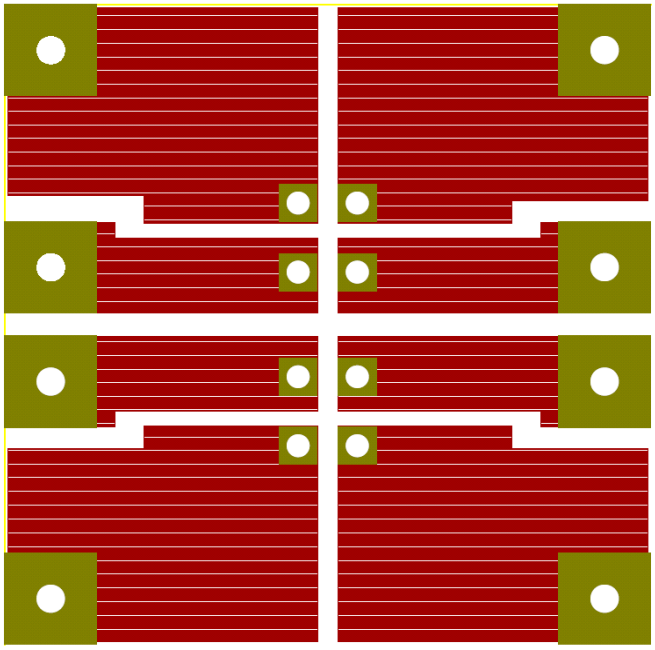
```
Zero
        EPwm2Regs.AQCTLA.bit.ZRO = AQ_SET;
        EPwm2Regs.AQCTLA.bit.CAU = AQ_CLEAR;
        EPwm2Regs.AQCTLB.bit.ZRO = AQ_SET;
        EPwm2Regs.AQCTLB.bit.CBU = AQ_CLEAR;

   EPwm2Regs.ETSEL.bit.INTSEL = ET_CTR_ZERO;      // Select INT on Zero event
   EPwm2Regs.ETSEL.bit.INTEN = 1;                 // Enable INT
   EPwm2Regs.ETPS.bit.INTPRD = ET_3RD;            // Generate INT on 3rd event
}
```

A2.HBLC PCB's

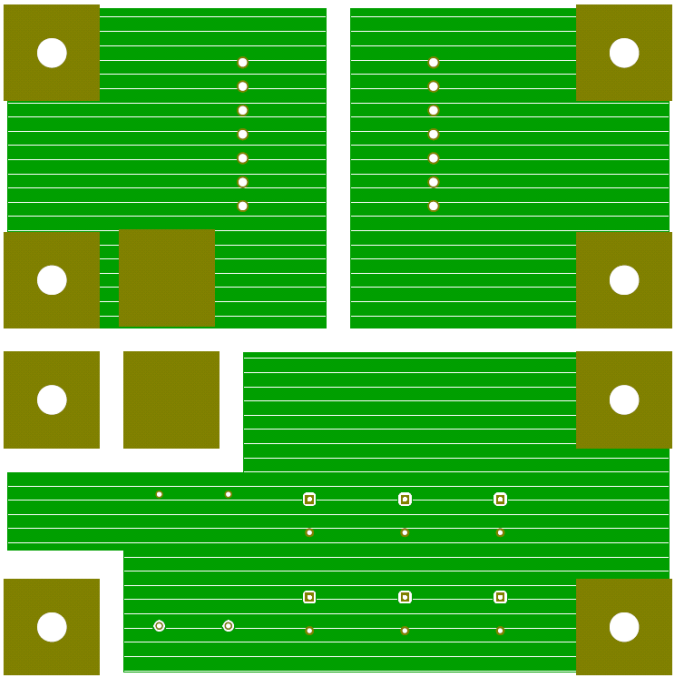
Diodes D_1. D_2 D_3 and D_4 PCB-front side



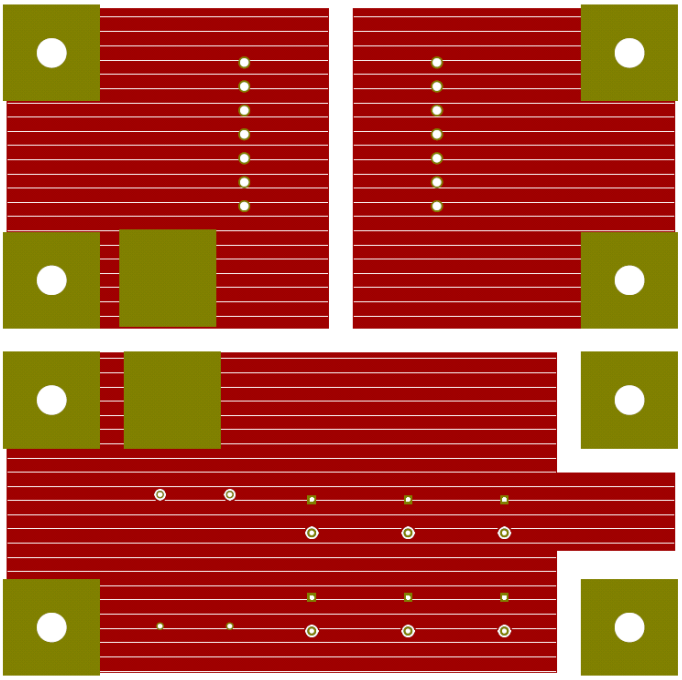
Diodes D_1. D_2 D_3 and D_4 PCB-back side



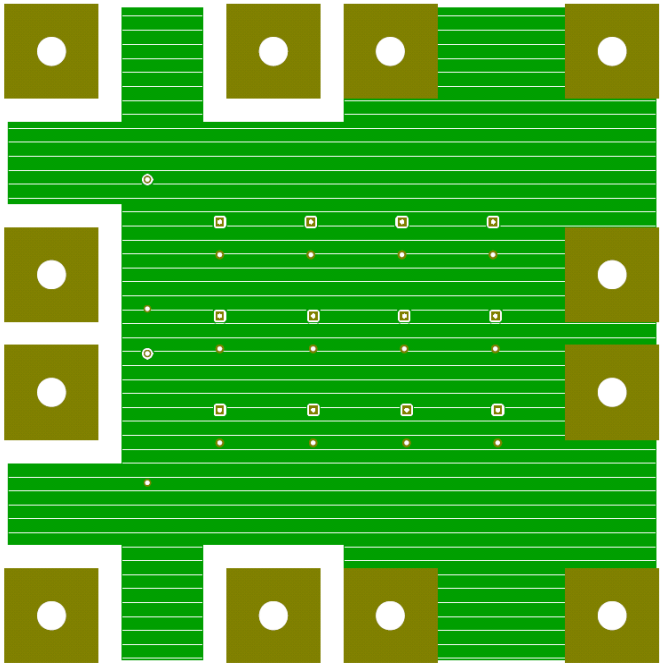
Inductor L_1 and capacitor C_1 PCB-front side



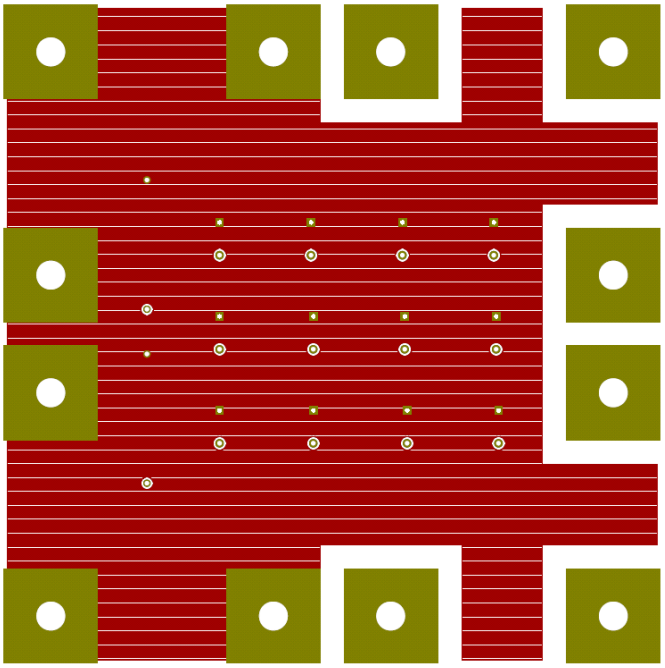
Inductor L_1 and capacitor C_1 PCB-back side



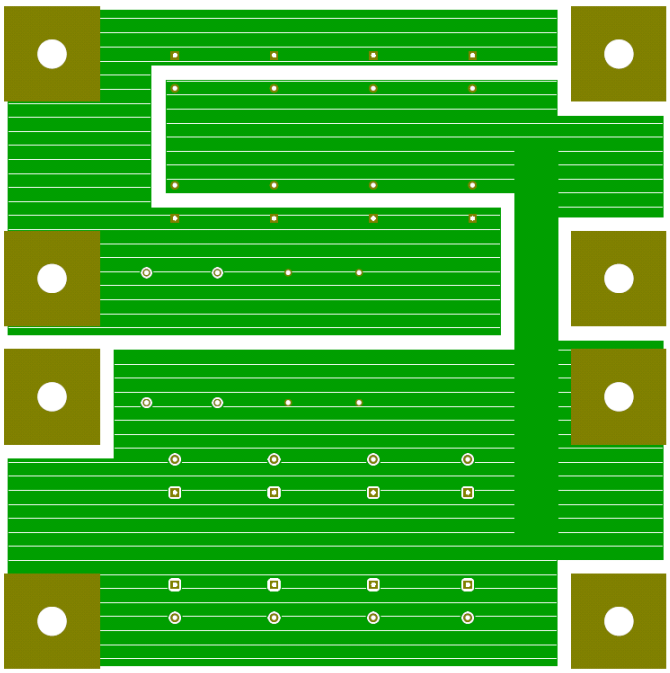
Capacitor C_4 PCB-front side



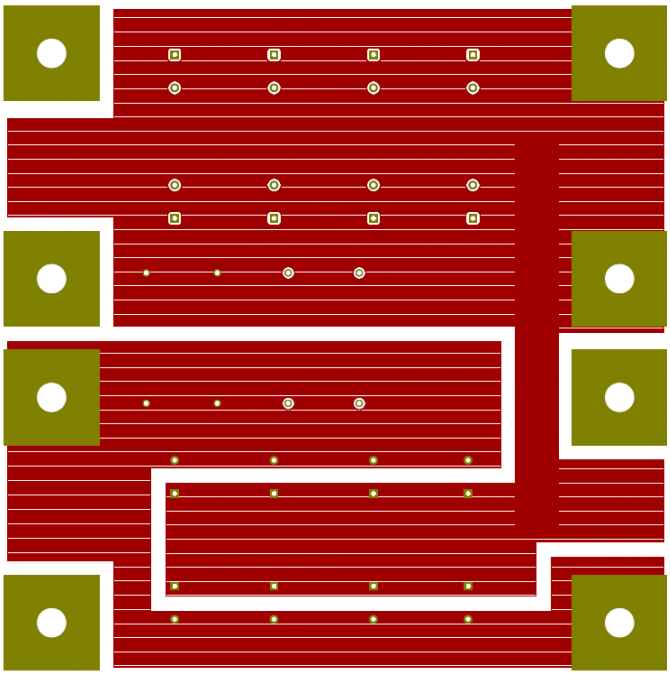
Capacitor C_4 PCB-back side



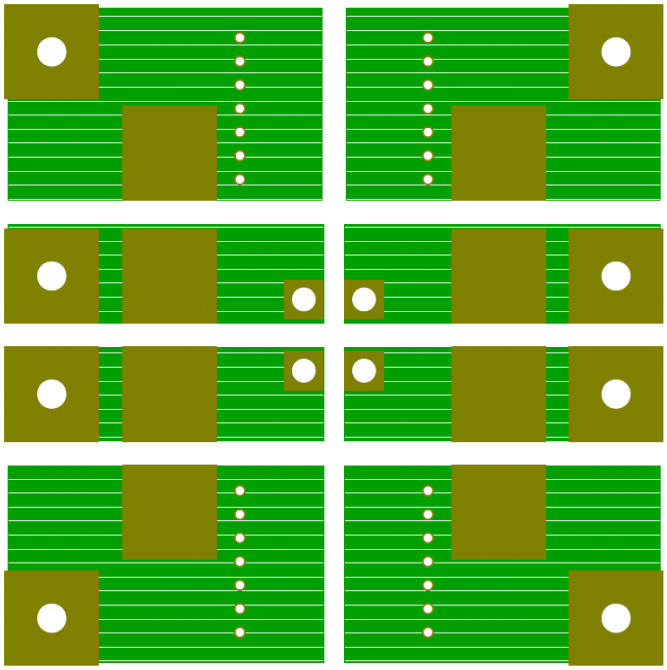
Capacitors C_2 and C_3 PCB-front side



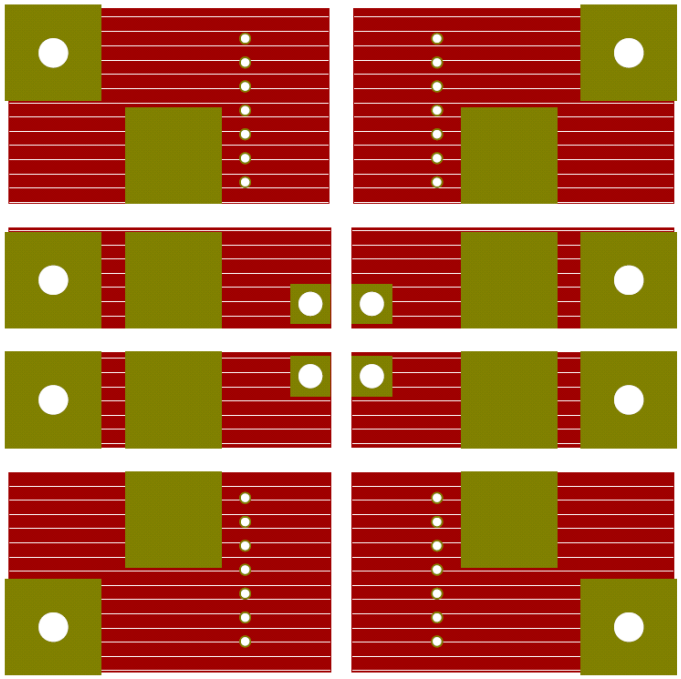
Capacitors C_2 and C_3 PCB-front side



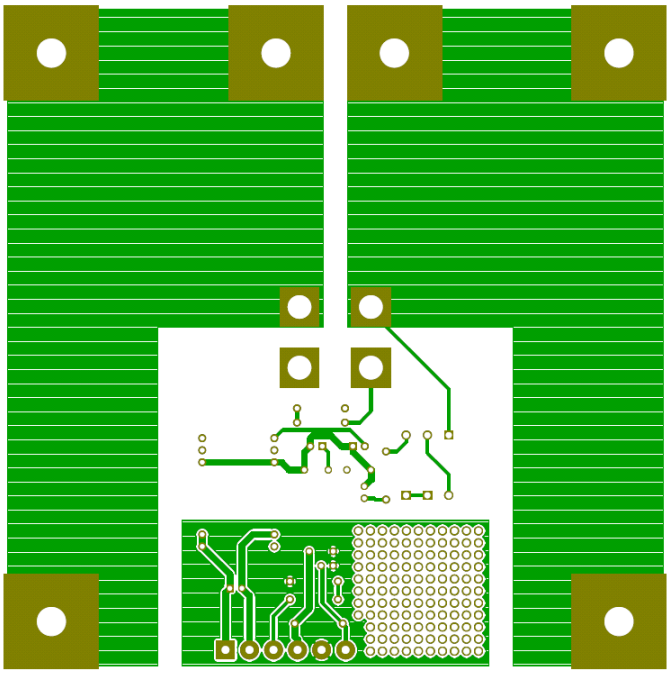
Inductors L_2 and L_3 with the diode D_5 and D_6 PCB- back side



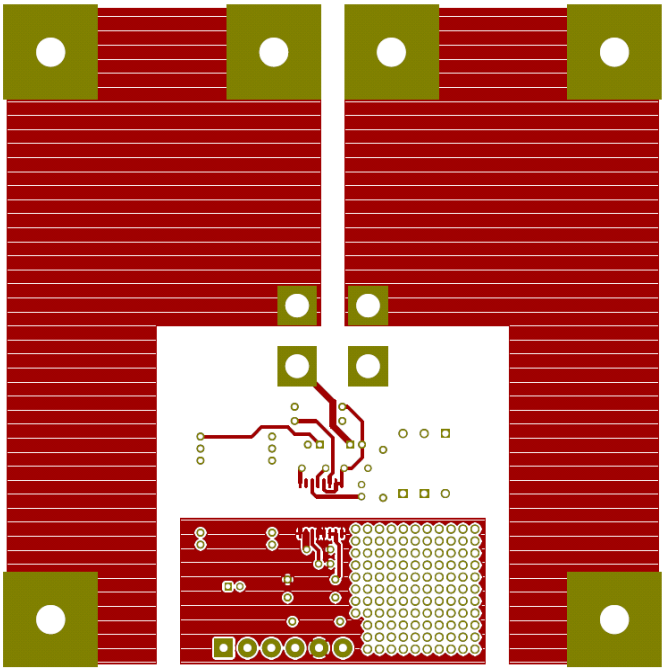
Inductors L_2 and L_3 with the diode D_5 and D_6 PCB- back side



HCPL 316J circuit PCB-front side



HCPL 316J circuit PCB-front side



A3. Wolfram Mathemathica obtained function from the interpolation

F2Gr9[k_,x_,y_]=If[k<1,0.0005987348677853262` +0.1028727971990411` k-0.06689495214778732` $k^2$+0.0810486275364256` k^3+0.04680911195580413` $k^4$-0.0038566951667272343` k^5+0.00039559890801383555` $k^6$+0.0005713100759059349` k^7-0.01886014738283569` $k^8$-0.00004752509724103651 5` k^9+0.956271240920538` x-0.2530384086447573` k x+0.06407468258201698` $k^2$ x+0.03480766151388609` k^3 x-0.04886333529053044` $k^4$ x-0.06164286960770681` k^5 x-0.021527958822582013` $k^6$ x-0.036980322821406224` k^7 x-0.014537103693744337` $k^8$ x-0.5909135264621191` x^2+0.04831063696135399` k $x^2$+0.05157236766042776` k^2 x^2-0.05850167333764194` $k^3$ $x^2$-0.11850858517305533` k^4 x^2-0.004076478626492871` $k^5$ $x^2$+0.009530170388101928` k^6 x^2+0.042365288336162626` $k^7$ $x^2$-0.14224300535782997` x^3+0.017960339517867734` k $x^3$+0.03145637237714819` k^2 x^3-0.18166239903770404` $k^3$ $x^3$+0.052661893531005276` k^4 x^3+0.18874412721270817` $k^5$ $x^3$+0.04827891767269702` k^6 x^3-0.06660787964811607` $x^4$+0.06134549720974037` k x^4-0.19470085357899602` $k^2$ $x^4$+0.024270810800792943` k^3 x^4+0.48489637148263004` $k^4$ $x^4$-0.049910424076776795` k^5 x^4-0.14793912699842648` $x^5$-0.3662502296587102` k x^5-0.03714563856556598` $k^2$ $x^5$+0.552073533420129` k^3 x^5-0.2235137692499982` $k^4$ $x^5$+0.2562447499578666` x^6-0.24911419808663507` k $x^6$+0.17231285289673728` k^2 x^6-0.3399589192824124` $k^3$ $x^6$+0.5902137318864149` x^7-0.7431138619454711` k $x^7$+0.34588511964790086` k^2 x^7+0.9342690977356539` $x^8$+1.3959317940662472` k x^8-0.7297937357607707` $x^9$-0.007081365663840207` y+0.35315050588953384` k y-0.02662767049426263` k^2 y+0.040211681932973656` $k^3$ y+0.01359358622328708` k^4 y-0.012197410631967952` $k^5$ y+0.01968680470495002` k^6 y+0.00925212170815408` $k^7$ y+0.042807697014856635` k^8 y+0.23913193360042995` x y-0.041579467126730885` k x y-0.0009733383568625828` $k^2$ x y+0.0006017773360575071` k^3 x y-0.07248101119880697` $k^4$ x y-0.021557183167563346` k^5 x y-0.0004567779533600886` $k^6$ x y-0.01215842426708462` k^7 x y+0.009591435107607866` $x^2$ y-0.06785859977250225` k x^2 y+0.06666238085069126` $k^2$ $x^2$ y-0.08827267387819486` k^3 x^2 y-0.04150223749196938` $k^4$ $x^2$ y+0.0668329775559222` k^5 x^2 y-0.08633238841960929` $k^6$ $x^2$ y-0.18236945488404377` x^3 y+0.0797460219103094` k $x^3$ y+0.030990762008880533` k^2 x^3 y-0.06858817666114504` $k^3$ $x^3$ y+0.20817367360635503` k^4 x^3 y-0.1578052951208555` $k^5$ $x^3$ y+0.09395500224074518` x^4 y-0.018409565562579246` k $x^4$ y+0.027144591100835818` k^2 x^4 y+0.20344866638175538` $k^3$ $x^4$ y-0.1793379721493875` k^4 x^4 y-0.13728446562326607` $x^5$ y-0.05499731609568734` k x^5 y+0.03184840213765069` $k^2$ $x^5$ y-0.2500464449409707` k^3 x^5 y+0.08998611736004135` $x^6$ y-0.5161604992975305` k x^6 y-0.2653197881701096` $k^2$ $x^6$ y-0.2958445319543663` x^7 y-0.6808323198356234` k $x^7$ y+1.4493846340943213` x^8 y+0.026527865482926773`

y^2+0.36242451960468214` k $y^2$-0.07410680707039545` k^2 y^2+0.00013502897033250291` $k^3$ $y^2$-0.017460136382933936` k^4 y^2+0.010081418926677799` $k^5$ $y^2$+0.04835364405056379` k^6 y^2+0.00952248159882704` $k^7$ $y^2$-0.178499561803295` x y^2-0.048504931550417754` k x $y^2$-0.02294533067883933` k^2 x y^2-0.026026460702622944` $k^3$ x $y^2$-0.04987518925789724` k^4 x y^2+0.040331151172782076` $k^5$ x $y^2$-0.0762834587398834` k^6 x y^2+0.29079819153231706` $x^2$ $y^2$-0.09731693725080358` k x^2 y^2+0.11784795824675469` $k^2$ $x^2$ $y^2$-0.05004807817357492` k^3 x^2 y^2+0.07256755736301257` $k^4$ $x^2$ $y^2$-0.12526685584688516` k^5 x^2 y^2-0.08452715094893981` $x^3$ $y^2$+0.1289179637865053` k x^3 y^2+0.19171842753605092` $k^2$ $x^3$ $y^2$+0.05559107772920493` k^3 x^3 y^2-0.09522933171404464` $k^4$ $x^3$ $y^2$+0.04631069805883153` x^4 y^2+0.22903840925929006` k $x^4$ $y^2$+0.13782697596080304` k^2 x^4 y^2-0.14642755142991934` $k^3$ $x^4$ $y^2$-0.27270074142260764` x^5 y^2-0.03384104580325704` k $x^5$ $y^2$-0.34416134095974055` k^2 x^5 y^2-0.5579690048387931` $x^6$ $y^2$-1.256496723069291` k x^6 y^2+0.5075452021332016` $x^7$ $y^2$-0.021839732380798338` y^3+0.20759375561500137` k $y^3$-0.14498738382784299` k^2 y^3-0.03490406496406031` $k^3$ $y^3$-0.02673877770363487` k^4 y^3+0.06862908893140017` $k^5$ $y^3$+0.024219966565947004` k^6 y^3-0.2995734122304685` x $y^3$-0.1423460009045694` k x y^3+0.0175260976676401` $k^2$ x $y^3$-0.02336912691399905` k^3 x y^3+0.020759835600892087` $k^4$ x $y^3$-0.02309402481498532` k^5 x y^3+0.4020234030044196` $x^2$ $y^3$-0.044578744983027024` k x^2 y^3+0.2763946842959673` $k^2$ $x^2$ $y^3$+0.01507819510706` k^3 x^2 y^3-0.013212306701132775` $k^4$ $x^2$ $y^3$-0.061862370206416016` x^3 y^3+0.3985500493806691` k $x^3$ $y^3$+0.3269932616654801` k^2 x^3 y^3-0.060140195913177256` $k^3$ $x^3$ $y^3$-0.14120040441208798` x^4 y^3+0.4516779347806012` k $x^4$ $y^3$-0.14894217925842765` k^2 x^4 y^3-0.6159677703889566` $x^5$ $y^3$-0.9382807118185348` k x^5 y^3-0.316163124679241` $x^6$ $y^3$-0.04226554298724363` y^4-0.05573823438683184` k $y^4$-0.18089356726266886` k^2 y^4-0.06123802016271528` $k^3$ $y^4$+0.001874621882793548` k^4 y^4+0.09755609070500369` $k^5$ $y^4$-0.26545637947493606` x y^4-0.21129805561192042` k x $y^4$+0.15683649949927791` k^2 x y^4-0.010899494281856294` $k^3$ x $y^4$+0.039829218736154026` k^4 x y^4+0.36471018501987634` $x^2$ $y^4$+0.2227445713827828` k x^2 y^4+0.43577506361672674` $k^2$ $x^2$ $y^4$-0.017278840259008263` k^3 x^2 y^4-0.14964922842817505` $x^3$ $y^4$+0.7647448955387661` k x^3 y^4+0.11591151216586455` $k^2$ $x^3$ $y^4$-0.35141988903112203` x^4 y^4-0.283851756107892` k $x^4$ $y^4$-0.6688710531240675` x^5 y^4+0.00042313523833366985` $y^5$-0.34193534830989186` k y^5-0.13447911083650463` $k^2$ $y^5$-0.10313616086654502` k^3 y^5+0.04340019293885504` $k^4$ $y^5$-0.2265569093076094` x y^5-0.09542924453813727` k x $y^5$+0.3148590226430207` k^2 x y^5-0.05343296715019712` $k^3$ x $y^5$+0.22591273587688782` x^2 y^5+0.6695249021341709` k $x^2$ $y^5$+0.28083082615763155` k^2 x^2 y^5-0.18161878503141116` $x^3$ $y^5$+0.313768910509128` k x^3 y^5-0.4884299696322048` $x^4$ $y^5$+0.04569274798521071` y^6-0.5017394119015656` k $y^6$-0.06108506895450165` k^2 y^6-0.21526235060395107` $k^3$ $y^6$-0.2360097418514805` x y^6+0.24988484737858055` k x

y^6+0.18332937430043467` k^2 x y^6+0.1984185729807357` x^2 y^6+0.5064676609751235` k x^2 y^6-0.18201091005264577` x^3 y^6+0.05535751910106305` y^7-0.43658617722887966` k y^7-0.25165094647588826` k^2 y^7-0.11693888509614418` x y^7+0.20999054618996385` k x y^7+0.30380177906867867` x^2 y^7+0.1825699284873344` y^8-0.5778957856790755` k y^8+0.2205738500317406` x y^8+0.6011353041391524` y^9,0.19320525474592745` +0.04226342136296775` k+0.0003674528518334953` k^2-0.00011020800252471557` k^3+0.000010910779640134225` k^4-2.5464224120672276`*^-6 k^5+8.780996628582285`*^-8 k^6+9.286002242722569`*^-9 k^7-4.918044400622312`*^-10 k^8+7.210393160012694`*^-12 k^9+0.1922290592755779` x+0.08987235677901649` k x+0.0003903555795447464` k^2 x-0.0006754483324038546` k^3 x+0.0000781516188876153` k^4 x+7.559943951787981`*^-6 k^5 x+1.307989102532761`*^-6 k^6 x-1.255031660396142`*^-7 k^7 x+3.5737759223380207`*^-9 k^8 x+0.049108715244281995` x^2+0.14041229049251294` k x^2+0.0005271449574824299` k^2 x^2-0.0029042442231907344` k^3 x^2+0.0000840972415312244` k^4 x^2+0.0000256011627229606` k^5 x^2+3.1554418875296276`*^-6 k^6 x^2+4.927703768145286`*^-7 k^7 x^2-0.155957361203677` x^3+0.12205831556828421` k x^3-0.0016961911060752008` k^2 x^3-0.007509542400944465` k^3 x^3-0.0001835654282064147` k^4 x^3+7.805010353512363`*^-6 k^5 x^3-0.00010960917837058126 3` k^6 x^3-0.16584494097706728` x^4-0.01944368465590635` k x^4-0.02507359525697483` k^2 x^4-0.01152584433617546` k^3 x^4+0.00021949480511066895` k^4 x^4+0.00002536634013509993` k^5 x^4+0.21018331748520977` x^5-0.14228108211355586` k x^5-0.0813954279784934` k^2 x^5-0.010792334559083926` k^3 x^5+0.006389986519607627` k^4 x^5+0.7332852842235443` x^6-0.04296768097108389` k x^6-0.02959296567392342` k^2 x^6+0.009704895589919032` k^3 x^6+0.7827298710106542` x^7-0.12493044659468527` k x^7-0.0684957162704208` k^2 x^7+0.2896391875390099` x^8-0.43144886844699015` k x^8-0.13598412611856295` x^9+0.1607811559886411` y+0.09117348038664187` k y+0.00449869417816175` k^2 y-0.00040253282728945275` k^3 y+6.043898408587048`*^-6 k^4 y-8.641053091001079`*^-6 k^5 y-6.754616352298883`*^-7 k^6 y+3.5525872972265434`*^-8 k^7 y-1.8945864055369285`*^-9 k^8 y+0.031207669772202348` x y+0.1283491118336628` k x y+0.009791605363948764` k^2 x y-0.0013674771206122144` k^3 x y+0.00003963310831118872` k^4 x y+4.951067807853607`*^-6 k^5 x y-1.2684079918323844`*^-6 k^6 x y-1.0443969987434074`*^-6 k^7 x y-0.12802139586721084` x^2 y+0.09009519073800061` k x^2 y+0.012113998760811266` k^2 x^2 y-0.0030426377377175805` k^3 x^2 y-0.00003158472160974245 4` k^4 x^2 y+0.00002328902078574988 8` k^5 x^2 y-7.365715997115424`*^-6 k^6 x^2 y-0.12716650868066512` x^3 y-0.04401009175264472` k x^3 y-0.011755976751610065` k^2 x^3 y-0.0037020473019934` k^3 x^3 y+0.000415300284557114` k^4 x^3 y+0.00011163838381165045` k^5 x^3 y+0.09553734699607759` x^4 y-0.11101438206295881` k x^4 y-0.06128362936389124` k^2 x^4 y-0.0042896122403304785` k^3 x^4 y+0.003125852395556562 5` k^4 x^4 y+0.22940653764640836` x^5 y+0.029191942826604995` k x^5 y+0.03311773956750183` k^2 x^5

y+0.01645026197536017` $k^3$ $x^5$ y-0.19657114706353104` x^6 y-0.07920148299579079` k $x^6$ y+0.04380711854531722` k^2 x^6 y-0.821375860955634` $x^7$ y-0.3287108938570701` k x^7 y-0.5254322559191793` $x^8$ y+0.014628909517669625` y^2+0.10980465745064644` k $y^2$+0.0161583714925713` k^2 y^2-0.000024439355050119914` $k^3$ $y^2$-9.12954330040786`*^-6 k^4 y^2-0.00001634568242529455` $k^5$ $y^2$-6.197626281256074`*^-7 k^6 y^2+6.364406829011337`*^-7 $k^7$ $y^2$-0.1028044381619623` x y^2+0.053920391306837574` k x $y^2$+0.019476189933810683` k^2 x y^2+0.0006642276453600627` $k^3$ x $y^2$+0.00008118861391421381` k^4 x y^2+5.297223006820647`*^-6 $k^5$ x $y^2$+3.352829919663853`*^-6 k^6 x y^2-0.08605627670014872` $x^2$ $y^2$-0.07186991167957023` k x^2 y^2-0.00904495955090174` $k^2$ $x^2$ $y^2$+0.002241424168458456` k^3 x^2 y^2+0.0006054843836458449` $k^4$ $x^2$ $y^2$+0.00008940420502380596` k^5 x^2 y^2+0.052380643295825105` $x^3$ $y^2$-0.09896964763157667` k x^3 y^2-0.05760471471101063` $k^2$ $x^3$ $y^2$-0.0007713325014127353` k^3 x^3 y^2+0.0005863540336705571` $k^4$ $x^3$ $y^2$+0.006342208508162638` x^4 y^2+0.055174507991476364` k $x^4$ $y^2$+0.05771430230489271` k^2 x^4 y^2+0.017932589022480332` $k^3$ $x^4$ $y^2$-0.5107248556898396` x^5 y^2-0.067238191089761` k $x^5$ $y^2$+0.07133022855906006` k^2 x^5 y^2-0.8516190157811692` $x^6$ $y^2$-0.16299227672148864` k x^6 y^2+0.1012020582286409` $x^7$ $y^2$-0.07719207732348826` y^3+0.01871158532409379` k $y^3$+0.0217875453380413` k^2 y^3+0.0036266776460969203` $k^3$ $y^3$+0.00017764109654231942` k^4 y^3-0.00003396336063162027` $k^5$ $y^3$+0.000010976524682723495` k^6 y^3-0.04172822887228245` x $y^3$-0.09585003845148549` k x y^3-0.013336707292462769` $k^2$ x $y^3$+0.006361649282500934` k^3 x y^3+0.0007947059733579368` $k^4$ x $y^3$+3.4219786943191396`*^-6 k^5 x y^3+0.05706569173579776` $x^2$ $y^3$-0.09283672481286447` k x^2 y^3-0.0626005459510694` $k^2$ $x^2$ $y^3$-0.0000658401297283018` k^3 x^2 y^3-0.0014466447155897923` $k^4$ $x^2$ $y^3$-0.04509706621310848` x^3 y^3+0.06147506526195746` k $x^3$ $y^3$+0.06213913695635782` k^2 x^3 y^3+0.015029904953927411` $k^3$ $x^3$ $y^3$-0.4747768718209163` x^4 y^3-0.059405435592892214` k $x^4$ $y^3$+0.05751512758832853` k^2 x^4 y^3-0.4646849139812501` $x^5$ $y^3$+0.038885736010231826` k x^5 y^3+0.7221466194569306` $x^6$ $y^3$+0.002871734196502631` y^4-0.11248171110900058` k $y^4$-0.02162778086457655` k^2 y^4+0.008792992028211537` $k^3$ $y^4$+0.0009723989354471046` k^4 y^4-0.00011446038260722575` $k^5$ $y^4$+0.08733200829235586` x y^4-0.08608825896254406` k x $y^4$-0.07058928096187791` k^2 x y^4-0.0017349722314795285` $k^3$ x $y^4$-0.0031569743390006326` k^4 x y^4-0.01068226107111786` $x^2$ $y^4$+0.06071977206878216` k x^2 y^4+0.058398948567406274` $k^2$ $x^2$ $y^4$+0.009005019342216166` k^3 x^2 y^4-0.3038559864545226` $x^3$ $y^4$-0.05018803951866211` k x^3 y^4+0.030079553479826947` $k^2$ $x^3$ $y^4$-0.054769958630147525` x^4 y^4+0.2248463700592014` k $x^4$ $y^4$+0.899635504404007` x^5 y^4+0.12422865769352573` $y^5$-0.07674944015187074` k y^5-0.07767048216954332` $k^2$ $y^5$-0.0052081145063702155` k^3 y^5-0.0046906226022605585` $k^4$ $y^5$+0.04969051914971514` x y^5+0.05680681114649006` k x $y^5$+0.05416249459046148` k^2 x y^5+0.0012742824557324115` $k^3$ x $y^5$-0.13174787936887555` x^2 y^5-0.04724501911351984` k $x^2$ $y^5$+0.0052600444001465975` k^2 x^2

y^5+0.18946496117429149` $x^3$ $y^5$+0.3351571563445298` k x^3 y^5+0.5998760414628614` $x^4$ $y^5$+0.0971437852161788` y^6+0.048315680666574094` k $y^6$+0.053485199208211924` k^2 y^6-0.006839037354978664` $k^3$ $y^6$-0.026742307491441995` x y^6-0.06463590505979416` k x $y^6$-0.008594804496836769` k^2 x y^6+0.2243796215139973` $x^2$ $y^6$+0.31927643222184543` k x^2 y^6+0.03287398802288416` $x^3$ $y^6$-0.007570776549535853` y^7-0.11681025316947706` k $y^7$-0.008982238948650884` k^2 y^7+0.10332836374167705` x $y^7$+0.13786969344709873` k x y^7-0.4574574439678334` $x^2$ $y^7$-0.06427655278343761` y^8-0.23040447916222917` k $y^8$-0.4904359787181786` x y^8+0.2949667644867255` y^9];

AUTHOR'S PAPERS RELATED TO THE THESIS

1. O. Cornea, N. Muntean, M. Gavriş, "Interleaved 3 Phase DC/DC Converter for Automotive Applications", *IEEE 12th International Conference on Optimization of Electrical and Electronic Equipment (OPTIM 2010)*, Moeciu,Brasov, Romania, vol.10, Mai 2010, pp. 377-382—ISI Proceedings, Scopus.
2. M. Gavriş, O. Cornea, N. Muntean, "Multiple Input DC-DC Topologies in Renewable Sytems- A General Review", *IEEE 3th International Symposium on Exploitation of Renewable Energy Sources (EXPRES 2011)*, Subotica, Serbia, vol.1, Martie 2011, pp. 123-128— IEEE Xplore, Scopus.
3. N. Muntean, M. Gavriş, O. Cornea, "Dual Inpu Hybrid DC-DC Converters", *IEEE International Conference on computar as a tool joint with CONFTELE 2011 (EUROCON 2011)*, Lisabona, Portugalia, Aprilie 2011, pp. 150-154--IEEE Xplore, Scopus.
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6. N. Muntean, M. Gavriş, O. Cornea, "Dual Input, Small Power, PV and Wind Energy Conversion System", *IEEE 13th International Conference on Optimization of Electrical and Electronic Equipment (OPTIM 2012)*, Moeciu, Brasov, Romania, Mai 2012, pp. 169-174— IEEE Xplore, Scopus.
7. O. Cornea, N. Muntean, R. Teodorescu, M. Gavriş, "Dual Input Hybrid Buck LC Converter for mixed wind and PV renewable energy system", *IEEE ECCE EUROPE 15th International Power Electronics and Motion Control Conference and Exposition (EPE-PEMC 2012)*, Novi Sad, Serbia, September 2012, pp. 1-6.- IEEE Xplore.

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Curriculum Vitae

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