High Power Voltage Multiplier (VM) PFC Converter with Inherent ZCS Characteristics and High Step-Up Gain for Enhanced Low-Line Efficiency

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***Abstract*—In this paper, a Voltage Multiplier (VM) converter configuration has been designed for high Power PFC application, ensuring reduced losses and high system efficiency.The conventional PFC system is improved with adding VM circuit configuration that enhances the static gain features with moderate duty ratio (D), and hence, the reverse recovery (RR) issue is resolved. The VM section inherently adds two main specific features of clamping behavior and ZCS phenomenon to the PFC system. An experimental prototype of $2\ kW$, $600\ V$ VM PFC converter configuration is designed and its effectiveness is validated under low line input of $100\ V$, operating at a high duty ratio, $D = 0.67$. The Real-Time Interface (RTI) feature of dSPACE1104 and MATLAB/Simulink are used to give the control signal for the verification of the system. Always, less than half of the output voltage ($300\ V$) appears across the switches of the converter, hence, voltage stress of the switch is minimized. Also, ZCS phenomenon is evident during switching commutations due to the snubber circuit behavior of the resonant tank, included in the proposed PFC converter. Hence, the overall system efficiency is improved. Furthermore, higher system efficiency is maintained for different rating which has been tested in this research work.**

I. Introduction

The rapid growth of Power Supply Units (PSUs) in industrial and commercial power distribution system demands high efficiency with the high quality of power in many aspects [1], [2]. Also, high power and high voltage AC-DC system is required for many applications [3]. However, it is hard to achieve high output voltage and high efficiency simultaneously at low AC input [4], [5], [6].

The boost Power Factor Correction (PFC) converter is most popular due to its superior performance. It controls the shape of input current to obtain high quality power [7], [8], [9], [10]. Generally, the input side injected harmonics, input power factor (pf), output voltage ripple, efficiency, size of the converter/filter etc. are considered as the fundamental performance index for power quality improvement while designing PFC converter [3]. However, the converter should essentially operate at high switching frequency for achieving high power density and small converter size [11]. However, this high switching operation results in higher switching losses and hence, converter efficiency is reduced. Furthermore, the high duty cycle operation of Voltage-Doubler (VD) or Voltage-Multiplier (VM) converter gives rise to reverse recovery problem, which in turn limits the voltage gain and efficiency of the converter system [12], [13], [14]. The implementation of proper soft-switching concept helps to attain desired high efficiency [13], [15], [16]. Also, the high output voltage could be obtained with modification in conventional converter configuration which helps to attain high static gain even at moderate duty ratio. These ideas motivated for integrating these two concepts to design a high static voltage-gain Boost Voltage Multiplier (VM) PFC circuit which is having inherent soft switching feature.

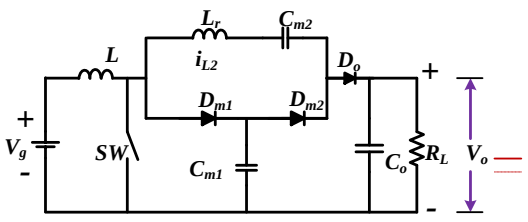

Fig. 1. Circuit configuration of high step-up Voltage Multiplier (VM)

In recent years, several novel high step-up PFC converter configurations have been developed for high voltage and power applications. Whereas, the reverse recovery issue during switching of devices isn't being considered to limit the switch losses. On the contrary, in many other research articles, several passive snubber circuits for implementation of suitable soft switching concept have been developed. But, the usability of such converters for high power and voltage applications aren't being discussed. Furthermore, the recently developed novel high step-up converters and multiplier converters [17], [18], [19], [20], [21], [22], [23], [24], [25], [26] are tried for PFC applications. Also, these aren't suitable for heavy loading as they give large input current ripple and higher conduction losses [27]. Furthermore, researchers are interested in designing high static voltage gain multiplier circuit which not only has the enhanced performance in high voltage and power application but also has inherent features to alleviate the reverse recovery losses. The popular CockcroftWalton (CW) Voltage Multiplier (VM) is improved to resolve certain practical limitations [28]. However, it suffers due to the non-ideal characteristics poor output voltage regulation with high output

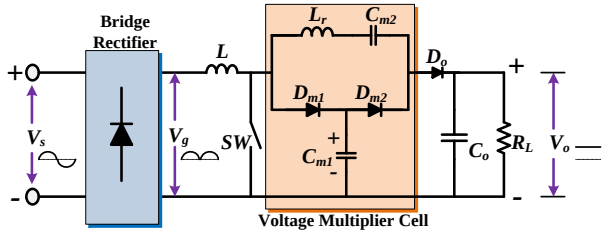

Fig. 2. Circuit configuration of VM PFC Converter system

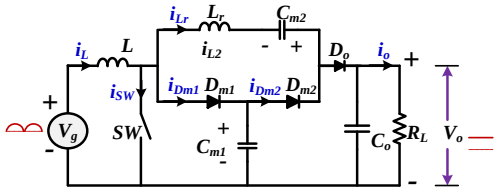

Fig. 3. Simplified equivalent circuit configuration of VM PFC converter

ripple at heavy loading conditions [28]. In [29], compromising circuit complexity, high power and high voltage PFC converter is designed with enhanced ZCS technique. Again, the VM having presented in [30] has inherent ZCS technique and is performing satisfactorily, but this has't been tried for PFC application. This idea motivated to implement the VM circuit configuration, (reported in [17], [25]) presented in Fig. 1 for designing high power PFC system which ensures limited losses and high system efficiency.

In this paper, the VM circuit configuration (reported in [17], [25]) presented in Fig. 1 has been designing for high power PFC system which ensures reduced losses and high system efficiency. The proposed PFC system includes a voltage multiplier (VM) unit embedded in the conventional PFC configuration to enhance the static gain features with moderate duty ratio (D), and hence, the reverse recovery issue is resolved. The VM section inherently adds two main specific features of clamping behavior and ZCS phenomenon to the PFC system. To examine the usability of the proposed system, an experimental prototype of 2 kW, 600 V VM PFC converter configuration is designed and validated under low line input of 100 V, operating at a high duty ratio, $D = 0.67$. The Real-Time Interface (RTI) feature of dSPACE1104 and MATLAB/Simulink are used to give the open loop control signal for the verification of the system.

II. Proposed VM PFC Converter

The proposed VM PFC Converter is presented in Fig. 2. The conventional boost converter is appended with a VM cell without losing its inherent property as pf corrector in PFC system. The VM cell composes a multiplier diode pair (D_{m1}, D_{m2}), multiplier capacitor pair (C_{m1}, C_{m2}) and a resonant inductor (L_r). The boost inductor, switch, output diode and the output capacitor are denoted as L, SW, D_o and C_o respectively.

The simplified VM PFC system is presented in Fig. 3. The inclusion of resonant inductor, L_r is to obtain ZCS turn-on behavior and, hence, the negative effects of reverse recovery current of all diodes is minimised. Thus, the current transitions in all components happen in a resonant way with low $\frac{di}{dt}$. The multiplier capacitor, C_{m1} operates as clamping capacitor and eliminates the switching over voltage. Both the multiplier capacitors work in such a manner that half of the energy consumed by the load is transferred through them and the second half is transferred directly.

A. Characteristics of VM PFC Converter

The main characteristics of the VM converter are as follows;

1) The input current is naturally continuous while the converter includes only one inductor for energy storage.
2) The VM also operates as a regenerative clamping circuit, reducing problems with layout and the EMI generation.
3) Due to the clamp circuit behavior, large output voltage gain is achieved without high duty ratio compared to the conventional PFC converter.
4) The clamped circuit is used to minimize the voltage stress across switches. Every switching device blocks a similar voltage. Consequently, low voltage rating and low on-state resistance ($R_{DS(ON)}$) switching devices can be used which leads to minimization of the cost.
5) The VM operates with inherent ZCS turn-on feature and hence, minimizes the effects of the reverse recovery current of all diodes with the inclusion of a small inductance, L_r.

B. Operation of VM PFC Converter

In this paper, continuous conduction mode (CCM) operation of proposed converter have been considered. For the simplicity in operational analysis, certain initial assumptions have been considered as:

- The switch, SW is considered in OFF state.
- The multiplier capacitor, C_{m1} is initially fully charged with a voltage, $V_{Cm1} = \frac{V_o}{2}$.
- The system is operating with high static gain, i.e. ($Q > 5$, where, $Q = \frac{V_o}{V_g} = \frac{2}{1-D}$. Therefore, $V_g < V_{Cm1}$, where, V_g is the boost multiplier input voltage.
- Hence, D_{m1} and D_{m2} are in blocking state to attain ZCS commutation.
- The resonant inductor current, i_{Lr} is equal to input inductor current, i_L. i.e. $i_L = i_{Lr} = i_o$.
- The energy of the input inductor is transferred to the load, R_L through the diode, D_o.

The CCM operation of the proposed converter is analyzed by five switching stages, as illustrated in Fig. 4. The Stage I, Stage II and Stage III describe the ON state of the switch, SW whereas, Stage IV and Stage V describe the OFF state. The ideal currents and voltages of each switching state are displayed in Fig. 5.

1) Stage I [T_0, T_1]: The Fig. 4(a) describes the operation of proposed converter in switching State I [T_0, T_1]. Also, the direction of circuit current with voltage polarity is presented. The ideal current and voltage waveforms of the circuit during the state, [T_0, T_1] are displayed in Fig. 5.

This state starts at $t = T_0$ and ends at $t = T_1$. At T_0, the switch, SW is turned with ZCS commutation. The inductor, L

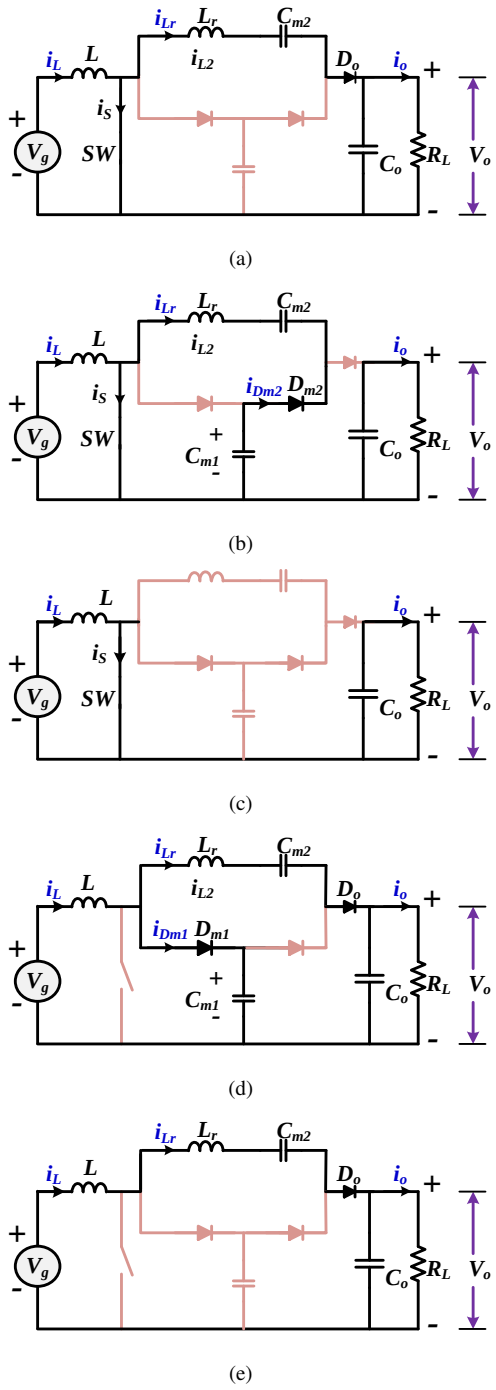

Fig. 4. Circuit diagram: (a) Stage I [T_o to T_1], (b) Stage II [T_1 to T_2], (c) Stage III [T_2 to T_3], (d) Stage IV [T_3 to T_4], and (e) Stage V [T_4 to T_5]

starts charging linearly whereas, the resonant inductor current, i_{Lr} and output diode current, i_{Do} are reduced linearly to zero at $t = T_1$. Thus, the output diode, D_o becomes OFF, and its reverse recovery current is also minimised.

The capacitor, C_{m1} is initially charged with $\frac{V_o}{2}$ i.e.

$$V_{Cm1} = \frac{V_o}{2} \tag{1}$$

Therefore, applying KVL to the circuit, Fig. 4(a);

$$V_{Dm1} = \frac{V_o}{2} \tag{2}$$

$$V_{Dm2} = -\frac{V_o}{2} \tag{3}$$

2) Stage II [T_1, T_2]: This switching state starts when the resonant current becomes zero at $t = T_1$ and ends at $t = T_2$ as the operational circuit is shown in Figure 4(b). The ideal currents and voltages of the VM PFC circuit during this switching state, [T_1, T_2] are shown in Fig. 5.

The switch, SW remains in ON state and the inductor, L is in progress to stores energy. Whereas, the output diode, D_o is blocked at $t = T_1$ (end of $StageI$) and the multiplier diode, D_{m2} starts conducting. The capacitor, C_{m1} transfers energy to the capacitor, C_{m2} in a resonant manner. At $t = T_2$, the diode D_{m2} is blocked with low $\frac{di}{dt}$, when the energy between both the multiplier capacitors C_{m1} and C_{m2} are balanced.

Applying KVL to the circuit, Fig. 4(b);

$$v_{Dm1} = v_{Cm2} \tag{4}$$

3) Stage III [T_2, T_3]: The Fig. 4(c) describes the State III operating condition. The figure indicates the direction of circuit current with voltage polarity. Further, the ideal currents and voltages of the PFC circuit for this switching state [T_2, T_3] are presented in Fig. 5.

The proposed converter goes into this stage during $t = [T_2, T_3]$. When both the multiplier capacitors are reached to balanced energy state, then this stage starts. The multiplier section completely isolates both input section and output section, since it behaves as dead-circuit during this period. The input inductor is still in charging state and hence, the increasing current flows through the switch only. The output capacitor supplies to the load during this period.

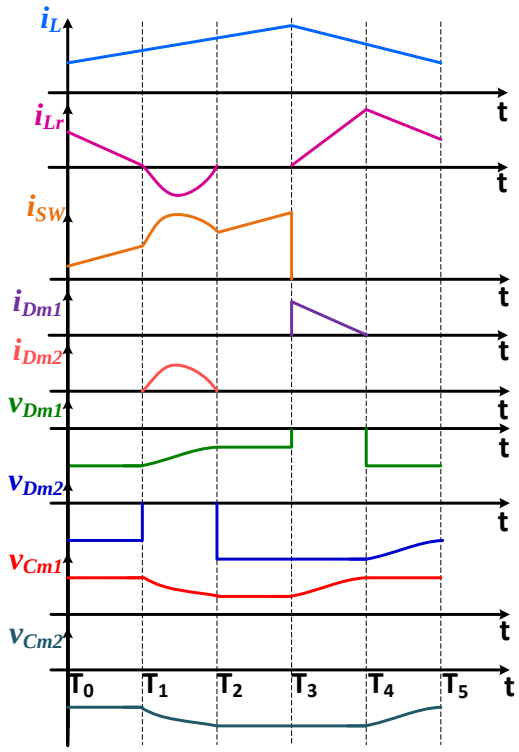

Fig. 5. Switching state voltages and current of the VM PFC converter

The capacitors C_{m1} and C_{m2} are at the same energy level. Therefore, applying KVL to the circuit, Fig. 4(c);

$$v_{Dm1} = -v_{Cm1} \tag{5}$$

And,

$$v_{Dm2} = v_{Cm2} \tag{6}$$

4) Stage IV [T_3, T_4]: At the end of $StageIII$. i.e. at $t = T_3$, the switch, SW turns OFF. At the same time, the diode, D_{m1} starts conduction, since the capacitor, C_{m1} is completely discharged in previous stage. During this stage, the stored energy of inductor, L is transferred to the capacitor, C_{m1} through diode, D_{m1} until $i_{Dm1} = 0$ at $t = T_3$.

The Fig. 4(d) describes the operation of the proposed converter in State IV. The direction of circuit current with voltage polarity is also presented. Also, the ideal currents and voltages of the VM PFC converter during the operating state, [T_3, T_4] are displayed in Fig. 5.

Applying KVL to the circuit, Fig. 4(d);

$$v_{SW} = v_{Cm1} \tag{7}$$

And,

$$v_{Dm2} = v_o - v_{Cm1} \tag{8}$$

The resonant inductor current, i_{Lr} rises from zero and charges the output capacitor, C_o through diode, D until $i_{Lr} = i_L$ at $t = T_3$.

5) Stage V [T_4, T_5]: The switch, SW remains in OFF state as before. At $t = T_4$, the diode, D_{m1} is blocked with low $\frac{di}{dt}$, minimising the diode reverse recovery current. During this stage, both the inductors L and L_r are in series i.e. $i_{Lr} = i_L$ and the inductor, L remains in discharging state. The stored energy is transferred to the load, R_L through diode D_o.

This stage is nothing but the initial assumption state of the proposed converter for operational analysis. After this stage, the circuit further enters the $StageI$ and continues the CCM operation.

The Fig. 4(e) describes the switching State V of the proposed converter. The direction of the circuit current with voltage polarity is also presented in the figure. The ideal currents and voltages during the state, are shown in Fig. 5 [T_4, T_5].

Applying KVL to the circuit, Fig. 4(e)

$$v_{Dm1} = -(v_{SW} + v_{Cm1}) \tag{9}$$

And,

$$v_{Dm2} = v_{Cm1} - v_o \tag{10}$$

$$v_{SW} = -(v_{Dm1} + v_{Cm1}) \tag{11}$$

III. Experimental Result Analysis

A 2 kW, 600 V output hardware prototype of proposed VM PFC Converter is designed in our laboratory. The block diagram presented in Fig. 7 describes about the Real-time implementation (RTI) of the proposed system. The experimental set-up is presented in Fig. 6 The set-up includes mainly a VM PFC power circuit and switch driving circuit. The power

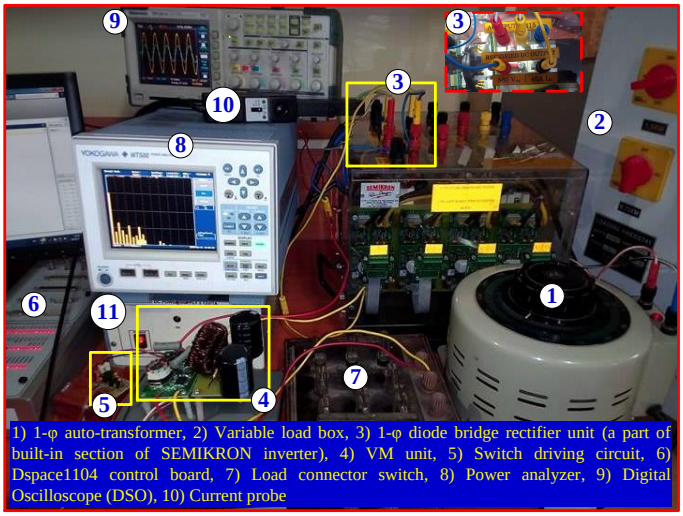

Fig. 6. Experimental Set-Up of proposed VM PFC system

circuit incorporates a $1-\phi$ auto-transformer, $1-\phi$ diode bridge rectifier followed by the proposed VM unit and DC dynamic load. The $1-\phi$ rectifier unit is a part of built-in rectifier section of SEMIKRON inverter, which is discussed briefly in Appendix A. The proposed VM PFC converter system, operating in open loop control is modeled in the MATLAB/Simulink and downloaded to the dSPACE, which delivers the required regulating signals to the driver section. The switching driver circuit receives the analog switching signal from dSPACE1104 board and is used to drive the switch. In addition, to process the control algorithm on VM PFC prototype, the RTI feature is enabled. The essential driving pulse is generated by the master bit I/O. For the designing of the prototype, ferrite core type inductor and plain polyester type capacitor are used. The components, used for the experimental designing of proposed PFC converter are enlisted in TABLE I.

A. Design Consideration of VM PFC Converter

The design consideration of proposed VM PFC converter includes;

Selection of Duty Ratio (D): For the proposed VM configuration, the relationship between rectified input voltage, output voltage, duty ratio (D) and voltage gain is given by:

TABLE I
Experimental Design Parameters of VM PFC Converter

System Parameters	Specification	Rating
Boost Inductor (L)	Ferrite Core Type	0.83 mH
Output Capacitor (C_0)	Electrolytic type	680 μF
Resonant Inductor (L_r)	Ferrite Core Type	37 μH
Multiplier Capacitor (C_{m1}, C_{m2})	Ceramic Type	45 μF
Multiplier Switch (SW)	MOSFET:FCP20N60	20 A, 600 V
Multiplier Diodes (D_{m1}, D_{m2}), Output Diode (D_0)	VS-20ETF06FPPBF	20 A, 600 V
Load	Resistive Load Box	Maximum Load upto 5 kW
Switching Frequency (f_{SW})		40 kHz
Duty Ratio (D)		0.67

$$Q = \frac{V_o}{V_g} = \frac{2}{1-D} \tag{12}$$

From the Equation (12), the value of D can be selected depending on the desired voltage gain (Q) ratio.

Selection of Switch Voltage Rating: The voltage across multiplier capacitors decide the voltage rating of the switching devices which includes FET switch (SW) and circuit diodes. Thus, the maximum rating of voltage for these devices can be selected as:

$$V_{SW} = V_{Dm1} = V_{Dm2} = V_{Do} = V_{Cm2} = \frac{V_g}{1-D} \tag{13}$$

Selection of Front End Inductor: The allowable ripple content of the input inductor current mainly decides its minimum inductance value and is expressed as:

$$L = \frac{V_g D}{\triangle I_L f_{SW}} \tag{14}$$

Selection of VM Capacitors: The rating selection of VM capacitors is decided by the VM capacitor voltage, the maximum output power (P_o) and the switching frequency (f_{SW}). The energy stored in the multiplier capacitor governs the maximum output power ($P_{o_{max}}$). Thus, the value of the VM capacitors is given by:

$$C_{m1} \geq \frac{P_{o_{max}}}{V_{Cm1}^2 f} \tag{15}$$

Selection of Resonant Inductor (L_r): The commutation losses across the switches can be reduced with the help of resonant inductor (L_r). It limits the rate of change of current which can be expressed as:

$$\frac{di}{dt} = \frac{V_o - V_{Cm2}}{L_r} \tag{16}$$

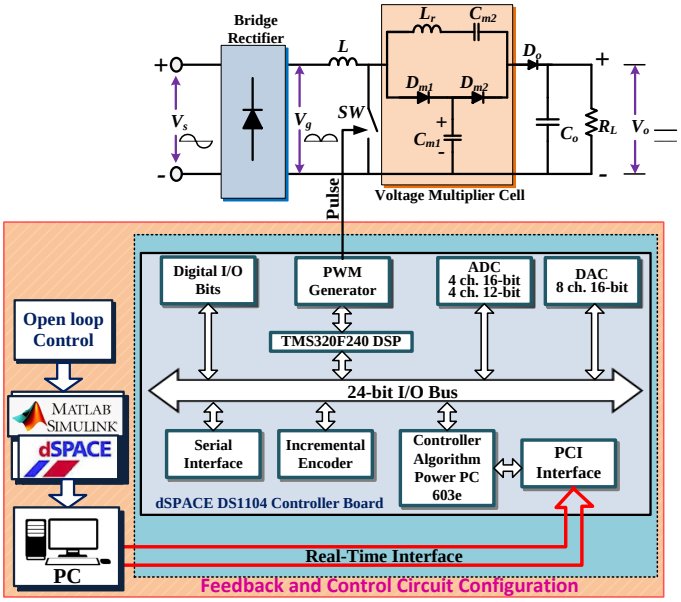

Fig. 7. Block diagram representation of Real-time implementation of VM PFC converter system

B. Comparative Analysis of Theoretical Losses and Efficiency

Switch conduction loss: The RMS value of switch current $I_{SW_{rms}}$ mainly decides the switch conduction loss and can be expressed as (neglecting the current ripple):

$$I_{SW_{rms}} = \frac{P_g}{V_g}\sqrt{D} \tag{17}$$

Hence, the power loss during switch conduction is given by:

$$P_{SW(cond)} = I_{SW_{rms}}^2 R_{DS_{on}} \tag{18}$$

For high power application, the RMS value of switch current (I_{SW}) comparatively very high in Boost PFC converter than the the proposed VM PFC converter.

Switch Commutation Loss: The operation of such systems is greatly effected by the commutation loss across the controlled switching device. The current flowing through the switch during commutation is a combination of current flowing through the switch and the reverse recovery current of diode. The commutation loss is expressed as:

$$P_{SW(off)} = (\frac{1}{2} V_s I_s T_{off}) f_{SW} \tag{19}$$

The traditional Boost PFC system suffers due to large reverse recovery current. However, the commutation loss for the proposed system is negligible, as the reverse recovery current is limited due to its inherent ZCS mode of operation.

Diode Conduction Loss: The diode average current decides its conduction loss which is equivalent to the output current for the proposed system. For high power rating with low output voltage, the output current rises to a high value. This causes an increase in diode conduction loss which in turn affects the system efficiency.

The conduction loss of boost diode is expressed as:

$$P_D = \frac{P_o}{V_o} V_f \tag{20}$$

where, V_f is forward blocking voltage of the diode. The conduction loss of multiplier (three) diodes is expressed as:

$$P_D = 3\frac{P_o}{V_o} V_f \tag{21}$$

The forward blocking voltage in For high power, high voltage (say ($600 V_{DC}$)) system is comparatively larger than the equal rating of proposed PFC converter system. Thus, the diode conduction loss is noticeably reduced and maintaining high system efficiency in proposed system.

Theoretical Efficiency:

Hence, based on the losses calculated, the system efficiency of the PFC converter system is estimated:

$$\eta = \frac{P_o}{P_o + P_{SW(cond)} + P_{SW(off)} + P_D + P_{Lin}} \tag{22}$$

The efficiency of the proposed VM PFC converter is higher than the boost PFC system as the theoretical losses in the proposed converter is comparatively quit low.

C. Result Analysis

In this paper, the proposed system has been examined for its inherent ZCS phenomenon and static gain response at low input level. The ZCS characteristic is validated with voltage-current characteristics of the switching devices and the multiplier capacitors. The static gain of the proposed system is compared with the conventional PFC configuration with respect to duty cycle at different loads. Also, the efficiency and $\%THD$ with respect to load for both conventional and proposed converter have been discussed.

1) Switch Voltage and Current Characteristics: The voltage across the switch and current flowing through it during turning ON and OFF instants are as shown in Fig. 8(a). In case of a conventional boost PFC converter, the voltage across the switch during OFF condition is same as the output voltage. Whereas, for the proposed configuration switch voltage is reduced to below 50% of the output voltage as evident from the waveform. Thus, the switching loss is also reduced to a great extent comparatively. Also, due to the snubber circuit behavior of the resonant tank, ZCS phenomenon is evident during switching commutations. Hence, conduction loss is also minimized, enhancing the overall system efficiency. The reduction in commutation loss of the switch is also supported by low di/dt factor in RR current of diodes.

2) Diode Voltage and Current Characteristics: The voltage across the diodes and current flowing through them during turning ON and OFF instants are as shown in Fig. 8(c) , Fig. 8(d) and Fig. 8(b) All the diodes of the proposed configuration have a small RR area of current with very low di/dt. The RR portion of Diode, D_{m1} occurs during the OFF state of the switch. Hence, it doesn'tt quite affect the commutation loss of the switch, SW. However, negligibly small RR zones with low di/dt of multiplier diode, D_{m2} and output diode, D_o coincide with the ON state of the switch, SW. Thus, the switch is quite unaffected due to the RR current of these diodes. Hence, the switch commutation loss is significantly reduced. Also, as evident from the waveforms, the diode voltages are always observed below fifty percentage (50%) of the output voltage. This is highly advantageous in terms of low power loss, voltage stress reduction and selecting diodes with low rating.

3) VM Static Gain Analysis: The input current and output voltage of the proposed VM PFC converter is displayed in Fig. 9. The system is operating at a low line supply of $100\ V$ and duty cycle $D = 0.67$. It is evident from the waveforms that nearly $600\ V$ (double of conventional output) is obtained at the output terminals. The input current (I_s) is in phase with the line voltage and sinusoidal in shape. Also, its $\%THD$ content with spectrum analysis of the VD PFC systems is presented in Fig. 10.

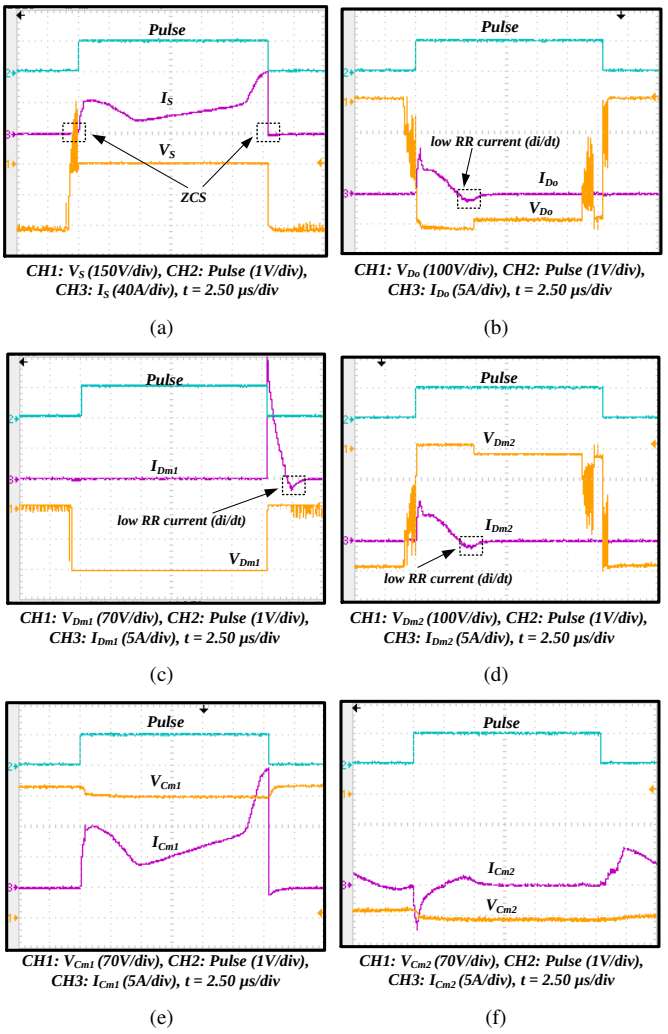

Fig. 8. Voltage and Current Characteristics of proposed system: (a) Converter Switch, S (b) Multiplier Diode, D_{m1} (c) Multiplier Diode, D_{m2} (d) Output Diode, D_0 (e) Multiplier Capacitor, C_{m1} (f) Multiplier Capacitor, C_{m2}

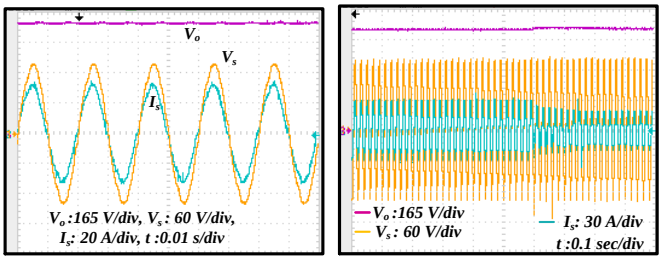

Fig. 9. Input Voltage, Input Current and Output Voltage Waveforms of Proposed VM PFC system: (a) Steady loading condition, (b) Load variation condition

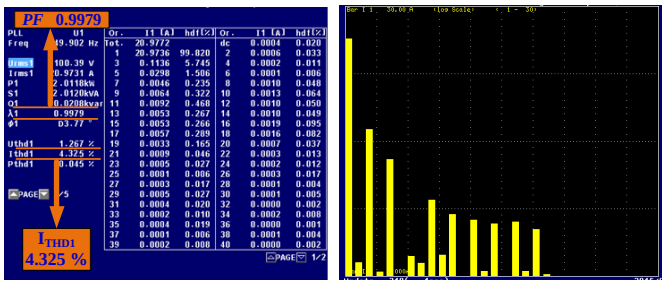

Fig. 10. Power analyser results of Proposed VM PFC system, illustrating: (a) power consumption, input power factor and %THD, (b) harmonics spectrum

TABLE II
COMPARATIVE PERFORMANCE ANALYSIS BASED ON LOAD VARIATION

S.N.	Load (W)	Conventional PFC System			VM PFC System		
		Efficiency (%)	THD (%)	pf	Efficiency (%)	THD (%)	pf
1	400	97.31	3.06	0.996	97.92	4.14	0.986
2	600	97.01	3.94	0.998	97.52	4.22	0.988
3	800	96.41	4.11	0.989	97.73	3.96	0.99
4	1000	96.02	4.26	0.987	97.81	3.80	0.992
5	1200	95.00	4.35	0.987	97.54	3.91	0.996
6	1400	94.42	4.49	0.983	97.81	3.88	0.997
7	1600	93.94	5.33	0.982	97.91	3.01	0.998
8	1800	93.13	5.73	0.983	98.26	3.16	0.998
9	2000	93.10	6.16	0.981	98.30	3.16	0.999
10	2200	92.31	6.56	0.982	98.22	3.22	0.997
11	2400	92.11	6.72	0.981	98.26	3.04	0.998
12	2600	92.17	6.82	0.980	98.29	3.15	0.999
13	2800	92.19	7.01	0.980	98.29	3.11	0.997

TABLE III
COMPARATIVE PERFORMANCE ANALYSIS BASED ON INPUT VARIATION

S.N.	Input RMS Voltage (V)	Conventional PFC System		VM PFC System	
		Efficiency (%)	pf	Efficiency (%)	pf
1	80	90.13	0.983	97.02	0.992
2	100	91.91	0.989	97.23	0.996
3	120	93.14	0.992	98.14	0.997
4	140	94.32	0.996	98.05	0.998
5	160	96.11	0.990	98.17	0.999
6	180	96.14	0.998	98.17	0.998
7	200	96.17	0.999	98.25	0.998
8	220	96.19	0.998	98.26	0.999
9	240	96.23	0.997	98.29	0.998

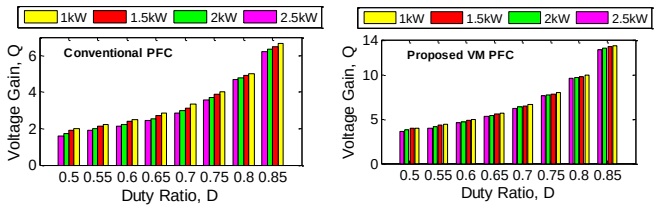

Fig. 11. Voltage Gain vs Duty Ratio for different Load Ratings: (a) Conventional system (b) Proposed VM PFC system

The performance of the proposed converter has been tested under load variation, and the relevant result waveforms are displayed in Fig. 9(b). The presented waveforms are captured for a load decrement of 50%. The output voltage is regulated, and the input voltage is sinusoidal, as presented in the figure.

In this research work, the proposed PFC system is tested under various operating conditions to validate its performance and compared with that of a conventional system of equal rating. A comparative analysis on the efficiency,%THD and pf of proposed system with the conventional system for various load conditions are presented in Table II. The efficiency of both conventional and proposed PFC systems is nearly equal at a lower level of loading. However, the efficiency of the conventional system decreases linearly with the increase of load. On the contrary, the system efficiency of the proposed system is comparatively very high at heavy loading conditions. Furthermore, the input current %THD for conventional system exceeds the IEC 61000-2-2 standard, while operating under heavy loading condition. Whereas, the input current %THD level of the proposed PFC system is under the standard limit irrespective of load rating.

Furthermore, the Table **??** describes the behavior of efficiency with respect to changes in input voltage. Although, the system efficiency increases for both the systems with an increase in supply voltage, but the VM PFC converter efficiency is comparatively very high at any input level.

The variation in static voltage gain (Q) with respect to duty ratio (D) at individual load ratings for both the systems are described in Fig. 11. For the performance analysis, a constant supply voltage of 100 V is given to both the systems. The value of D is varied within a range of $D = (0.5\ to\ 0.85)$ for each value of load (P) i.e. $P = (1\ kW, 2\ kW, 3\ kW\ and\ 4\ kW)$. The static voltage gain of proposed VM PFC system is nearly double to that of the conventional system for each D value under each specified load.

IV. CONCLUSION

A high power VM PFC converter with inherent ZCS feature and high static gain is proposed in this paper to obtain enhanced efficiency at low line input. The system is validated with an experimental prototype of 2 kW, 600 V rating, operating at a high duty ratio, $D = 0.67$. The performance of the proposed system is tested at low line input of 100 V. It is observed that always less than half of the output voltage (300 V) appears across the switches, hence, voltage stress of the switch is minimized. Furthermore, the switch conduction loss and diode commutation loss are minimized, and hence, the overall system efficiency is improved. The proposed PFC system includes a voltage multiplier (VM) unit embedded in conventional PFC configuration to enhance the static gain features with moderate duty ratio (D), and hence, the reverse recovery issue is resolved. The VM section inherently adds two main specific features of clamping behaviour and ZCS phenomenon to the PFC system. For both the steady state and transient loading condition unity pf and regulated output voltage are evident. The performance of the proposed converter in term of efficiency, pf, %THD under different input voltage and load is examined and compared with that of the conventional system. The system efficiency of the proposed system is maintained high for different load ratings with a slight variation of around 1%. Whereas, the efficiency variation increases upto 6% for the conventional system. Also, with respect to different line voltages, the system efficiency is maintained high and steady for the proposed system. For the proposed system, the input current %THD is maintained within the standard limit, even at higher load ratings. However, with the conventional system, it increases gradually above the limit at higher ratings. The voltage gain for the proposed system is also observed to be almost double as compared to the conventional system for different load ratings. Moreover, the presented experimental results infer that the proposed VM PFC converter offers enhanced low-line-efficiency and is a better choice for high power with high voltage applications.

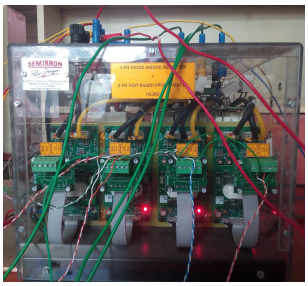

Fig. A1. SEMIKRON built power electronics teaching kit

APPENDIX

A. 1-ϕ DIODE BRIDGE RECTIFIER (A BUILT-IN SECTION OF SEMIKRON POWER ELECTRONICS TEACHING KIT)

A pictorial view of the SEMIKRON power electronics teaching kit is presented in Figure A1. It consists of an isolated $3-\phi$ diode bridge rectifier and $3-\phi$ inverter section. The rectifier section can be used both for $1-\phi$ and $3-\phi$ AC-DC conversion system, as per the requirement. The specification of the rectifier section is presented in Table A1.

TABLE A1
SPECIFICATION OF THE SEMIKRON BUILT $1-\phi$ DIODE BRIDGE RECTIFIER

Input AC voltage (V_s)	415 $Volt$
Output DC voltage (V_o)	600 $Volt$
Input AC current (I_s)	30 Amp
Fundamental frequency	50 Hz
Diode bridge module	SKD 160/18 (1 Nos)

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