165W Current fed push pull converter

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***Abstract*— The aim of this project is to implement the proposed DC-DC isolated converter on a half brick sized Printed circuit broad (PCB), this is achieved with the help of planar inductor and planar transformer. Current fed Push-pull converter consists of a pre-regulated buck converter stage where the wide range of input is regulated. The inductor of the buck stage acts as current source to the push-pull converter stage, this is an advantage as buck stage is used, the selection of transformer is easy for wide range of input voltages. Buck's output which is pre-regulated is fed as push-pull's input, here the buck stage switches operate at 300 kHz and push pull stage switches operate at half frequency of the buck stage i.e., 50 percent of duty cycle. Here, the switching losses are reduced in push-pull stage. The output is low voltage and high current, for this synchronous rectification is used in Schottky diode, hence, high efficiency is achieved. The proposed converter is hardware implemented to verify the design results.**

Keywords—Half brick sized PCB, Current fed push-pull converter, Push-pull converter stage, Pre-regulated buck converter stage.

I. Introduction

Current-fed converters are like voltage-fed converters in many ways. In current-fed the voltage source is replaced by current source and the parallel dc-link capacitor is removed series inductor is placed, similarly forward blocking devices by symmetric blocking devices. These converters are preferred in medium-to high-power applications (hundreds of kilowatts to megawatts). Some examples for high-power applications are ship propulsion, high-voltage and HVDC systems. Current fed converters are higher reliability and easy recoverability from short-circuit faults these are the advantages. [1]

Push-pull converter is majorly used switching supply belonging to the family of forward converters. There are many circuit configurations within the push-pull converter sub-family itself. These circuits vary only in the mode in which the transformer primary is driven. These consist the conventional two-transistor, one-transformer push-pull two-transistor, two-transformer push-pull converter, half-bridge converter and full-bridge converter. [2]

Buck fed converters feeding current cancel the need of capacitor at the output of the buck. This also avoids output inductors and flux imbalance, limitation of inrush current, reduced losses in MOSFETs and diodes acting as some of the advantages of current fed converters. There are two types-namely buck voltage fed and buck current fed converters which can be used to supply push pull converter. Voltage controller and current controller is used by average current mode control in a converter. This is to achieve control over variations in input voltage, input current and load. [3]

Buck and push-pull converters which are cascaded is used in several applications like high level DC voltage equipments such as medical and industrial X-Rays, carbon dioxide laser-based systems and travelling wave tube (TWT) in satellites. Electronic ballast that is used in compact fluorescent lamps and light emitting diodes also use current fed push pull topology. [4]

A 165W current fed push pull converter which can be powered by DC source is proposed in this work. Closed loop hardware implementation of the proposed converter is carried out along with design in Mathcad and simulation in LT spice. Current Fed Push-Pull Converter (CTM12619D1160-R&D) is used to deliver 165W power for various power applications in space and defense fields. The converter is implemented on half brick sized PCB. This paper provides all the electrical performance for wide input voltage range from 17V to 40V. Here, even if the input range is wide the pre-regulated buck stage aides in applying a stable input to push-pull stage. Ambient and ESS test's (Thermal cycling test, high temperature test and low temperature test) are performed and results are tabulated.

II. Specifications of the Converter

Table 1. Specifications of the converter

Input voltage	17V-40V(DC)
Output voltage	3.3V
Output current	50A
Maximum output power	165W
Efficiency	85% at 50% load
	81% at Full load
Line regulation	± (0.1-0.3) %
Load regulation	± (0.1-0.3) %
PCB Size	60mm × 58mm × 4.8mm

III. Operation and Design

Buck converter which has buck regulation stage cascaded by a push-pull isolation stage which also provides voltage reduction in transformer forms a current fed push-pull converter. The buck part is synchronous, both the upper and lower MOSFETS are N-channel, LM5101 drives these. Signals to this driver is given by LM5041, this LM5041 drives the push-pull part directly.

Push-pull takes input directly from inductor current of the buck stage. The buck inductor needs a current path, so the push-pull duty cycles overlap slightly. Proper flux balance in the transformer is provided by giving one cycle of buck regulator for each of the push and pull switching events.

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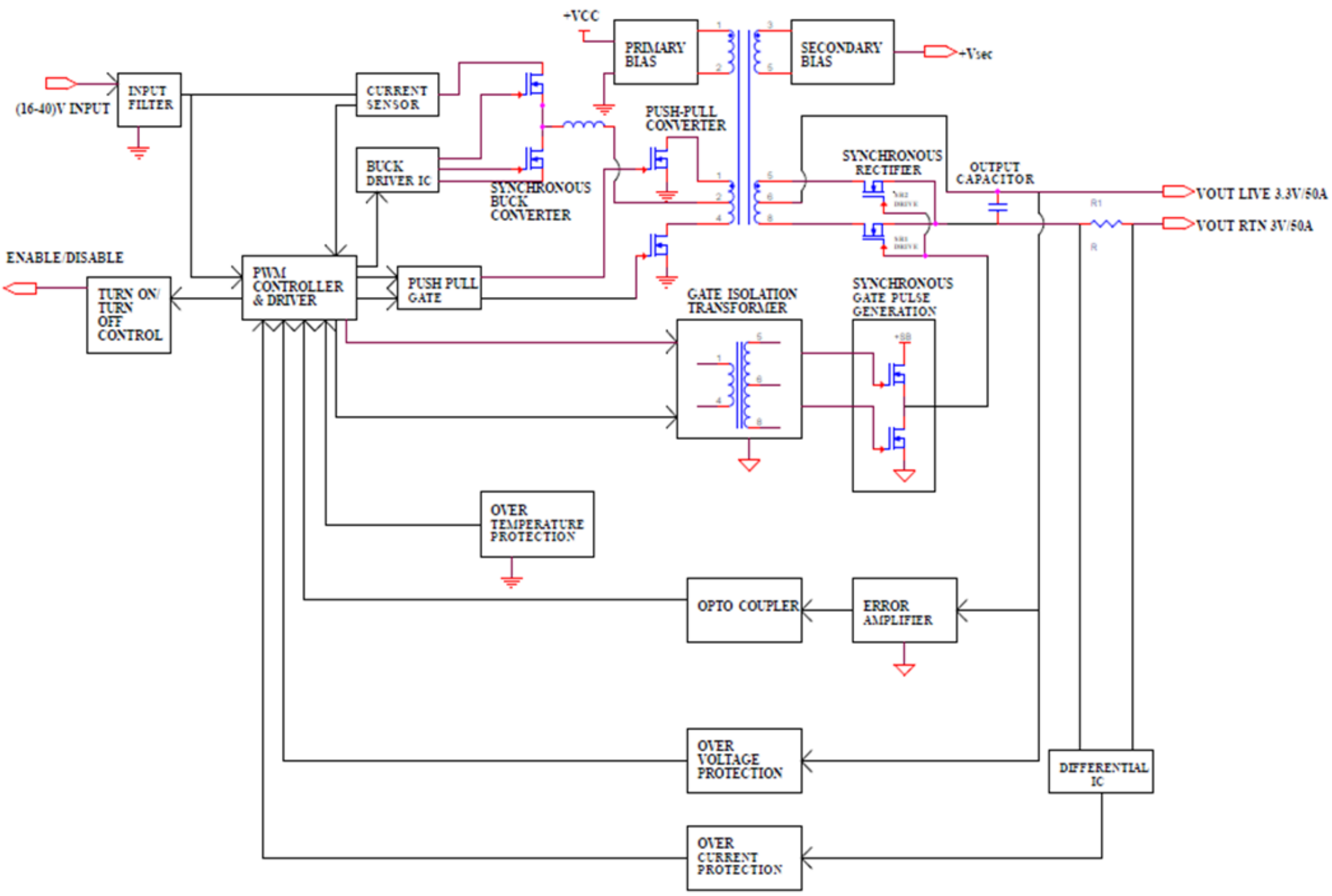

Figure 1: Block Diagram of proposed converter

If transformer operated when both the primary windings are active during the short overlapping time will not cause a problem to either transformer or current source. The impedance at V_{CT} node falls towards zero and the magnetomotive force of transformer breaks down when both windings are active. During this period, the inductor source current divides evenly between both the primary windings. As Switching losses need both voltage and current to be present some of the losses are avoided in the current fed push-pull topology.

The output stage makes use of synchronous rectification to avoid using a large percentage of the 3.3 V output by the forward voltage drop of a Schottky rectifier. From output a feedback is taken and processed by reference and amplifier and it is coupled back to the LM5041 controller via opto-coupler. Block diagram of the proposed converter is shown in Figure 1

A. *Abbreviations:*

V_{ds}	: Drain to source voltage
R_{ds}	: Drain to source resistance
L_{min}	: Minimum synchronous Buck inductance
$V_{in\text{-}max}$	: Maximum input voltage
BV_{out1}	: Nominal buck output voltage
BD_{min}	: Minimum buck duty cycle
ΔbI	: Input buck current ripple (20%)
BI_{out1}	: Buck output current
$Buck\_F_{SW}$	: Buck switching frequency
ApM	: Required inductor area product
PLE_{max}	: Maximum energy handled by inductor
IB_m	: Inductor maximum flux density
IK_w	: Inductor window utilization factor
IK_c	: Inductor crest factor
IJ	: Inductor current density
TApM	: Required transformer area product
PD_{min}	: Minimum push-pull duty cycle
TK_w	: Transformer window utilization factor
TJ	: Transformer current density
TB_m	: Transformer maximum flux density
PFreq	: Push-pull frequency
V_{ct}	: Transformer center-tap voltage
TI_{prms}	: Max rms current of transformer primary
PV_{out1}	: Push-pull output voltage
TI_{srms}	: Max Secondary rms current
V_{out}	: Output voltage
N	: Number of transformer's turns
V_{spike}	: Voltage spike caused by leak inductance
V_{in}	: Input voltage
R_{set}	: External resistor to set the overlap time
D	: Duty cycle
I_{out}	: Output Current

B. *MOSFET selection and design for buck stage*

The buck stage is synchronous, both the upper and lower MOSFETS are N-channel both the MOSFETS are driven by LM5101 which in-turn acquires signals by LM5041.

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The MOSFET selected for the upper part is BSZ096N10LS5ATMA1 with V_{ds}=100V, R_{ds}= 9.7mΩ, 40A.

The MOSFET selected for the Lower part is BSZ018NE2LSIXT with V_{ds}=25V, R_{ds}= 1.5mΩ, 40A.

Some of the key features considered while selecting these MOSFETS are voltage, current and temperature rating, switching frequency, Lower R_{ds}.

C. GATE driver

Gate drivers are chosen based on following:

- Source and sink capabilities.
- output current
- dv/dt considerations.
- Layout and ground considerations
- Size of bypass capacitor

D. Inductor design

Inductor acts as current source to the push pull stage.

- Synchronous buck minimum inductance Given by

$$L_{min} = \frac{(V_{in-max} - BV_{out1})BD_{min}}{\Delta bI * BI_{out1} * Buck\_F_{SW}} \quad (1)$$

- Required inductor area Ap (Area product m^4) Given by

$$A_pM = \frac{2PLE_{max}}{IB_m * IK_W * IK_C * IJ * 10^4} \quad (2)$$

E. MOSFET selection and design for push-pull stage

The stress across MOSFETs in push-pull stage is given by

$$Voltage\ Stress = (V_{out} * N * 2) + V_{spike} \quad (3)$$

In this converter push-pull MOSFET stress depends only on V_{out}, and not on the V_{in} for the input range 16-40V

The MOSFET selected for the push-pull stage is BSZ096N10LS5ATMA1 with V_{ds}=100V, R_{ds}= 9.7mΩ, 40A.

F. Push-pull transformer

Push-pull converter operates in two quadrants of BH curve moving back and forth as each primary is activated, this allows the maximum power capability of a push-pull transformer to be twice that of a forward transformer.

Required transformer area Ap (Area product m^4) Given by

$$TA_pM = \frac{1 - PD_{min}}{TK_W * TJ * 10^4 * TB_m * PFreq} * \left(V_{ct} * TI_{prms} + PV_{out1} * TI_{srms}\right) \quad (4)$$

G. MOSFET selection for synchronous rectification stage

- The voltage stress across MOSFETs in synchronous rectification stage is given by

$$Voltage\ Stress = (V_{out} * 2) + V_{spike} \quad (5)$$

In this converter push-pull MOSFET stress depends only on V_{out}, and not on the V_{in} for the input range 16-40V.

- The current stress through MOSFETs in synchronous rectification stage is given by

$$Current\ Stress = \frac{I_{out}}{2} \quad (6)$$

- The MOSFET selected for the synchronous rectification stage is BSZ018NE2LSIXT with V_{ds}=25V, R_{ds}= 1.5mΩ, 40A

H. Overlap time

Push-pull receives input from inductor current of buck, this inductor current needs a path, because of which the push-pull duty cycles overlap slightly, but this slight overlap does not cause any problem in transformer or current source even if the transformer is operating when both the primary windings are active.

The overlap time is given by.

$$Overlap\ Time(ns) = (3.66 * R_{set}) + 7 \quad (7)$$

Overall transfer function of buck and push-pull converters combined is given by Buck stage transfer function:

$$V_{ct} = V_{in} * D \quad (8)$$

Push-pull stage transfer function:

$$V_{out} = \frac{V_{ct}}{N} \quad (9)$$

Overall transfer function from (8) and (9):

$$V_{out} = \frac{V_{in} * D}{N} \quad (10)$$

IV. Experimental Results and Waveforms

The PCB top view is shown in the figure below, it consists of the converter, DC voltage source, regulated DC source for DC fan, Digital Signal Oscilloscope (DSO), Electronic load, Digital Multimeter (DMM). The input voltage is varied from 17-40V at minimum, nominal and maximum load conditions and efficiency, ripple voltages, line and load regulations are all tabulated as shown in the tables below.

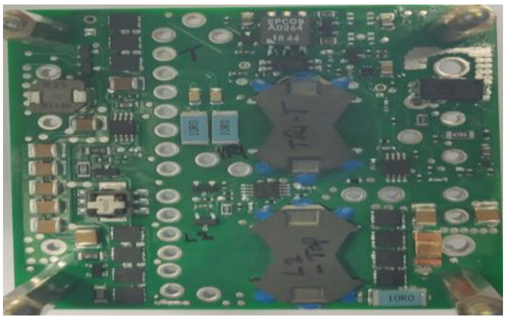

Figure 2: Printed Circuit Board

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A. *Efficiency*

The efficiency is calculated at minimum, nominal and maximum input voltages varying from 17- 40V at full load, these are tabulated in Table 2 and Table 3.

TABLE 2. INPUT POWER AT MIN, MAX AND NOMINAL LOAD

Input voltage V_{in} (V)	Input current I_{in} (A)	Input power P_{in} (W)
17	11.73	199.41
28	7.27	203.67
40	5.15	206.01

TABLE 3. OUTPUT POWER AND EFFICIENCY AT MIN, MAX AND NOMINAL LOAD.

Output voltage V_{out} (V)	Output current I_{in} (A)	Output Power P_{out} (W)	Efficiency η (%)
3.32	50	166.25	83.37
3.32	50	166.2	81.60
3.32	50	166.3	80.72

B. *Ripple voltage*

Ripple voltage is calculated for minimum, nominal and maximum input voltages varying from 17-40V at 10%, 50 % and full load, this is tabulated in Table 4.

TABLE 4. RIPPLE VOLTAGE AT MIN, MAX AND NOMINAL LOAD

Input Voltage V_{in} (V)	Ripple voltage $\Delta V_{pk\text{-}pk}$ (mV)		
	10% Load	50% Load	100% Load
17	21.6	23.2	58.0
28	42.4	41.6	64.0
40	30.4	43.2	64.0

C. *Line and load regulations*

Line and load regulations are calculated for minimum, nominal and maximum input voltages varying from 17-40V at 10%, 50 % and full load, this is tabulated in Table 5.

$$Line\ regulation = \frac{V_{out}\ (at\ V_{in-min}) - V_{out}\ (at\ V_{in-max})}{V_{out}\ (at\ V_{in-nom})} * 100 \quad (11)$$

$$Load\ regulation = \frac{V_{out}\ (at\ 10\%\ load) - V_{out}\ (at\ 100\%\ load)}{V_{out}\ (at\ 50\%\ load)} * 100 \quad (12)$$

TABLE 5. LINE AND LOAD REGULATION AT MIN, MAX AND NOMINAL LOAD

Input Voltage V_{in} (V)	Load condition			Load regulation (%)
	10% Load	50% Load	100% Load	
17	3.32	3.32	3.32	-0.03
28	3.32	3.32	3.32	-0.03
40	3.32	3.32	3.32	-0.06
Line regulation (%)	0.00	-0.03	-0.03	

D. *Experimental waveforms*

Buck converter switching mode for Vin: 40V and Load 50A is shown in Figure 3.

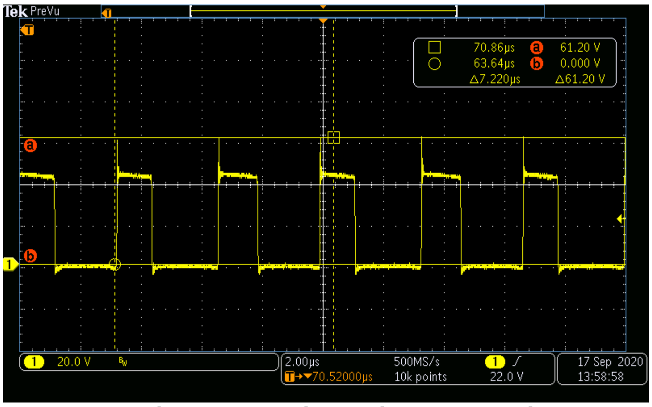

Figure 3: Buck converter switching mode at Vin-max and Iout-max

Push-pull V_{DS} for 40V and 50A is shown in Figure 4 and Figure 5

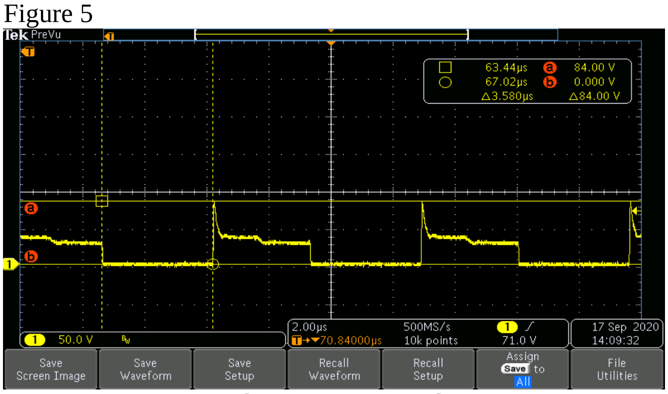

Figure 4: Push VDS at Vin-max and Iout-max

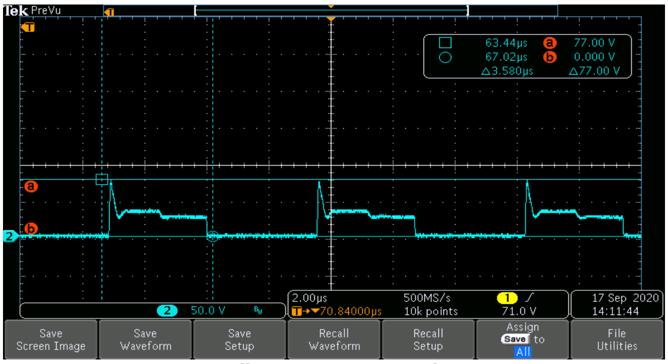

Figure 5: Pull VDS at Vin-max and Iout-max

Synchronous rectifier top and bottom V_{DS} for 40V and 50A is shown in Figure 6 and Figure 7

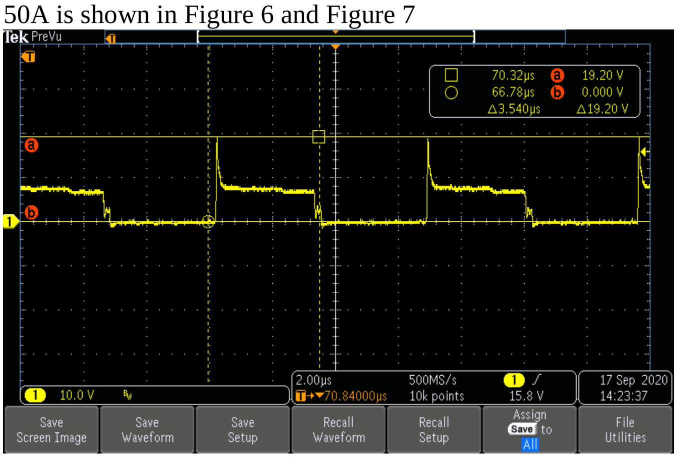

Figure 6: Synchronous Rectifier top VDS at Vin-max and Iout-max

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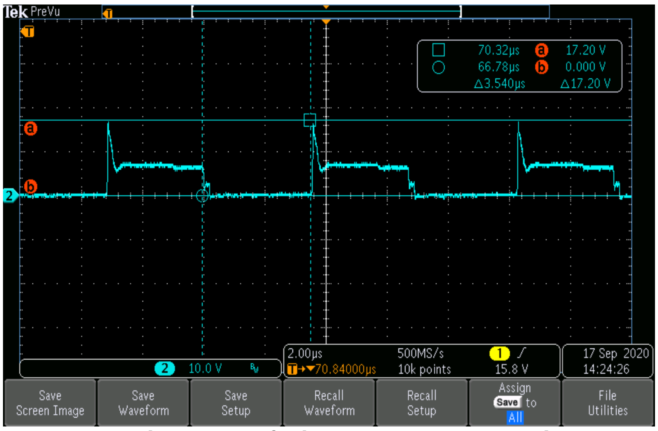

Figure 7: Synchronous Rectifier bottom VDS at Vin-max and Iout-max

Ripple voltage 28V and 50A is shown in Figure 8

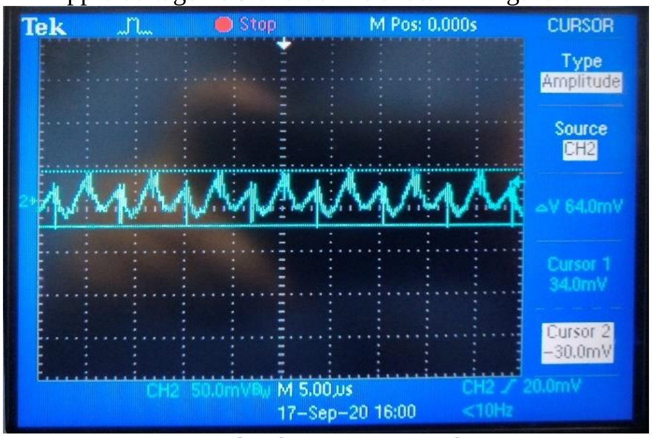

Figure 8: Ripple voltage at Vin-nom and Iout-max

V. Conclusion

The hardware of current fed push-pull converter is implemented on half brick sized PCB. Input voltage is pre-regulated by using buck converter, low output voltage and high output current is achieved with the help of synchronous rectification. Efficiency is calculated for minimum, nominal and maximum input voltages and is seen to be high for all. Ripple voltages, line regulation and load regulation are also realized by experimental results

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References

[1] L. Umanand, Power Electronics: Essentials & Applications, Wiley, 2009.

[2] V. J. Thottuvelil, T. G. Wilson and H. A. Owen, "Analysis and design of a push-pull current-fed Converter," in *1981 IEEE Power Electronics Specialists Conference*, Boulder, Colorado, USA, USA, 1981.

[3] N. O. S. Richard Redl, "Push-pull current-fed multiple-output dc/dc power converter with only one inductor and with 0 to 100% switch duty ratio," in *1980 IEEE Power Electronics Specialists Conference*, Atlanta, Georgia, USA, USA, 1980.

[4] R. Redl and N. O. Sokal, "Push-pull current-fed multiple-output regulated wide-input-range DC/DC power converter with only one inductor and with 0 to 100% switch duty ratio: operation at duty ratio below 50%," in *1981 IEEE Power Electronics Specialists Conference*, Boulder, Colorado, USA., 1981.

[5] A. I. Pressman, Switching Power Supply Design, McGrw-Hill, 1991.

[6] T. M. U. W. P. R. Ned Mohan, Power Electronics: Converters, Applications, and Design, John Wiley & Sons, 2003.

[7] A. K. Maini, Handbook of Defence Electronics and Optronics: Fundamental, Technologies and Systems, John Wiley & Sons Ltd, 2018.

[8] M. I. Krishna Gopinathan, "Pre-regulated Push Pull Converter for Hybrid," in *IEEE International Conference on Technological Advancements in Power & Energy*, Bengaluru, India, 2015.

[9] D. W. Hart, Power Electronics, McGraw-Hill, 2010.

[10] L. Flores, A. Soto, P. Alou, O. Garcia and J. Cobos, "Current fed push-pull topology with self driven synchronous rectification applied to low voltage," in *9th IEEE International Power Electronics Congress, 2004. CIEP 2004*, Celaya, Gto., Mexico, Mexico, 2004.

[11] N. M. S. B. D. Maiti, "Design Procedure of a Push Pull Current-Fed DC-DC Converter," in *Proceedings of National Powe Electronics Conference*, Roorkee, India, 2010.

[12] B. K. Bose, Modern Power Electronics and AC Drives, Prentice Hall PTR, 2002.

[13] B. M. M. Ananda, "Pre-regulated Current fed Push Pull Converter for Hybrid energy Systems," in *International Conference on Computation of Power, Energy Information and Communication (ICCPEIC)*, Karnataka, India, 2016.

[14] H. F. A.-C. Z.-C. S. C.-F. P.-P. C. f. M.-C. Applications, "High Frequency Active-Clamped Zero-Current Switching Current-Fed Push-Pull Converter for Micro-Converter Applications," in IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, 2020.

[15] S. Tandon and A. K. Rathore, "Partial Series LC Resonance-Pulse Assisted Zero Current Switching Current-Fed Push-Pull Converter," in IEEE Industry Applications Society Annual Meeting, Detroit, MI, USA, 2020.

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