DESIGN AND ANALYSIS OF NEW LOGICAL LOW POWER FULL ADDER WITH LOW POWER TECHNIQUES

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Abstract: *In this work, a logical 1-bit full adder design employing complementary metal–oxide–semiconductor (CMOS) logic is described. The schematic plan was implemented using Microwind 9.1 version. In this full adder, numbers of transistors are reduced by logicism. Consequently average power and layout area also reduced. The proposed full adder is compared with hybrid full adder utilizing CMOS logic and transmission gate logic. The simulation results of proposed circuit for 1.2-V supply at cmos 0.12µm technology, the average power consumption is 9.079 µW and layout area 213.8µm^2 both performance parameters are reduced when compared to hybrid full adder. Hybrid full adder has 14.005 µW power consumption and 299.4 µm^2 layout area. Further reducing power the proposed full adder was implemented along with some low power techniques and their results are tabulated.*

Keywords: *Logical design, Power gating, LECTOR, ULLC, LPSR, low power.*

1. Introduction

Enhanced usage of the portable devices which is operated by batteries, like mobile phones, personal digital assistants (PDAs), and laptop necessitate VLSI [2]. Full adders, substantiating for all the aforenamed circuit applications as a main functional block [3], this persist researchers to focus on this domain over the years. Lots of logic styles [4] are present but each experiencing its own vantage and weakness. To implement 1-bit full adder cells many logics are studied and investigated. The designs, presented as yet are classified into two assorts: 1) static and 2) dynamic. Typically Static full adders are more authentic, uncomplicated with low power prerequisite but unremarkably the demand of layout area is larger compared to dynamic similitude. The hybrid logic styles [1] provide anticipating processing performance, most them are affected by poor driving capability effect. This effect is overcome by using suitably designed buffers otherwise drastic degrade in their performance during cascaded mode of operation [3]. The main objective of this paper is to improve the power by reducing transistor count. The circuit was implemented using Microwind 9.1. The average power consumption (9.079 μW) of the proposed circuit was reduced compared with hybrid full adder. Layout size Width: 27.0µm (450 lambda), Height: 7.9µm (132 lambda), Surf: 213.8µm2 (0.0 mm2).

2. Related Work

Robustness against voltage scaling and transistor sizing are the merits of standard complementary (CMOS) style- based adders (with 28 transistors) [4]; while the high input capacitance and requirement of buffers are the bottlenecks of this logic style. Mirror adder is another complementary type smart design [5] with intimately same utilization power and transistor count but inside the adder the maximum carry propagation path/delay is comparatively smaller than that of the standard CMOS full adder [6]. On the other hand, good voltage swing restoration is offered by CPL employing 32 transistors [7]. Nevertheless, for low-power applications CPL is not a right choice. Since its high switching activity of intermediate nodes (increased switching power), high transistor count, static inverters, and overloading of its inputs are tuned into bottlenecks of this approach. However, the other retreats of CPL like slow-speed and high-power consumption remain an area of pertain for the researchers. The voltage degradation was successfully addressed in TGA, which uses only 20 transistors for full adder implementation [8], [9].

2.1. Hybrid Logic

Afterwards, research workers concentrated on

the hybrid logic approach which tapped the characteristics of different logic styles in order to amend the overall performance. Vesterbacka [11] proposed a 14-transistor full adder applying more than one logic style for their execution set up. Likewise, Zhang *et al* proposed the hybrid pass logic with static CMOS output drive full adder (HPSC) [12]. In that HPSC circuit, XNOR, and XOR functions were rendered by pass transistor logic module simultaneously by using only six transistors, and utilized in CMOS module to obtain full outputs swing of the full adder results increase in transistor count and decrease in speed. While promising performance were provided by the hybrid logic styles, majority of these hybrid logic adders affected by poor driving capability issue.

Bhattacharyya reported a Hybrid 1- bit Full Adder employing both complementary metal–oxide–semiconductor (CMOS) logic and transmission gate logic (TGL) [1]. In existing full adder, 6T for *XNOR* + 2T for *XOR*, 4T for sum and 4T for carry out totally 16 transistors are used. For *XNOR* and carry out, CMOS logic is used. For output sum, transmission gate logic is applied shown in Fig 1. Hybrid full adder has 14.005μW power consumption and 299.4 μm^2 layout area. In this hybrid full adder, logic is used for carry out, the same logic is used in proposed logical adder but implementation is different. But proposed full adder is simulated in Microwind 9.1 version, for the comparison the existing hybrid full adder is simulated in Microwind 9.1 also.

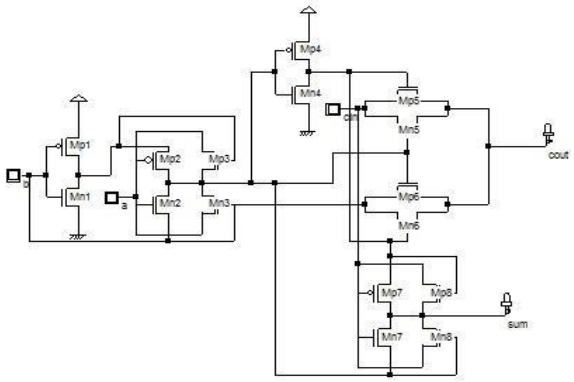


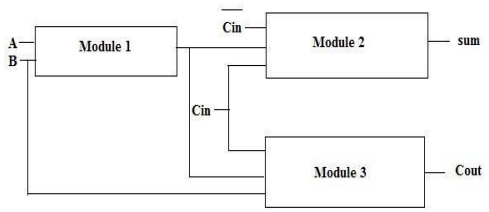
Fig 1: Detail circuit diagram of existing full adder.

2.2. Motivation

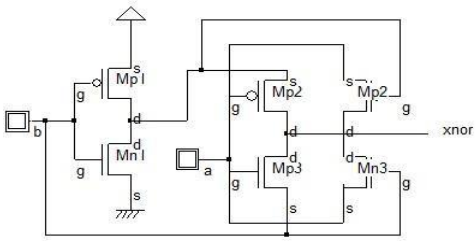
Early days gates such as *XOR*, *AND* and *OR* gates are used to implement full adders. Each gate require 6 transistors to implement totally 30 transistors are used. Due to large number of transistors the full adder requires high power consumption, larger area and also comparatively low speed. For that reason the researchers go for transistor implementation full adder without gate usage. For past 20 years there are many different full adders are arrived. Standard static complementary metal–oxide– semiconductor (CMOS), dynamic CMOS logic, complementary pass-transistor logic (CPL), and transmission gate full adder (TGA) are the most important logic design styles in the conventional domain [8],[21]. The other adder designs use more than one logic style, known as hybrid-logic design style, for their implementation. These designs exploit the features of different logic styles to improve the overall performance of the full adder.

3. Design Contrive of the Proposed Full Adder

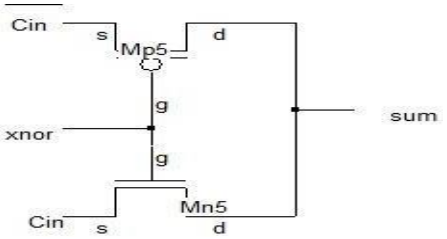
The proposed full adder circuit is represented by three blocks as shown in Fig. 2(a). Module 1 is XNOR module its output act as a select line for other two modules and module 2 generates the sum signal (SUM) and module 3 generates the output carry signal (*C*out*)*. Each module is designed separately such that the entire adder circuit is optimized in terms of power, delay, and area. These modules are discussed below in detail.



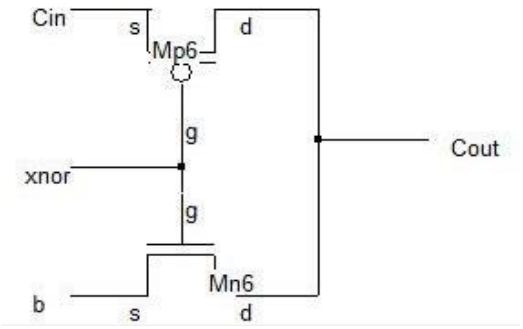
(a)



(b)



(c)



(d)

Fig. 2 (a) Schematic structure of proposed full adder. (b) XNOR module. (c) Sum generation module. (d) Carry generation module.

3.1. XNOR Module

In the proposed full adder circuit, XNOR module is responsible for most of the power consumption of the entire adder circuit. Therefore, this module is designed to minimize the power to the best possible extend with avoiding the voltage degradation possibility. Fig. 2(b) shows the modified XNOR circuit where the power consumption is reduced significantly by deliberate use of weak inverter (channel width of transistors being small) formed by transistors Mp1 and Mn1 [Fig. 2(b)]. Full swing of the levels of output signals is guaranteed by level restoring transistors Mp3 and Mn3 [Fig. 2(b)]. Various XOR/XNOR topologies have already been reported [8] and [13]–[15]. The XOR/XNOR uses four transistors but at the cost of low logic swing. To the contrary, the XOR/XNOR reported uses six transistors to get better logic swing compared with that of 4 T XOR/XNOR. In this paper also, the XNOR module employed 6 T, but having different transistor arrangement than previous 6 T XOR/XNOR [8]. The modified XNOR presented in this paper offers low- power and high-speed (with acceptable logic swing) compared with previous 6 T XOR/XNOR.

3.2. Sum Generation Module

In the proposed circuit, the output sum signal is implemented by the transistors Mp5, Mn5, as shown in Fig. 2(c). For this module Cin and inverse of Cin are the input. According to the XNOR output the sum be either Cin or inverse of Cin, so the output of XNOR act as a select line for sum generation. Only two transistors are required for this module.

3.3. Carry generation module

In this module, B and Cin are the inputs. The carry out is generated using two transistors such as Mp6, Mn6 as shown in Fig. 2(d). The output carry be input B or input Cin according to XNOR select line.

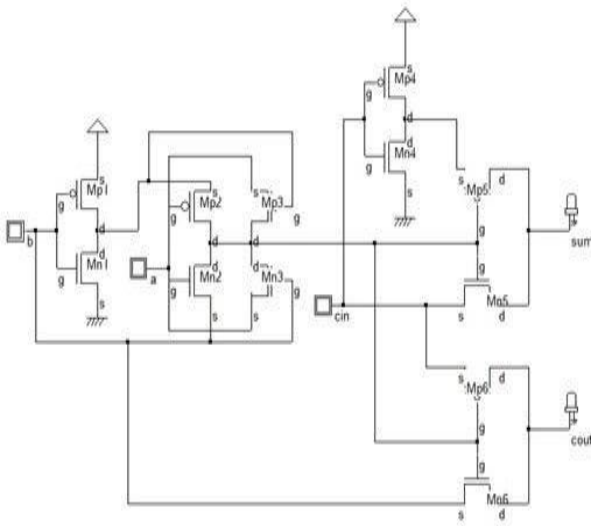


Fig. 3: Detail circuit diagram of proposed Full adder.

4. Operation of the Proposed Full Adder

Analyzing the truth table of a full adder, the condition for sum and Cout generation has been deducted as follows:

If, A=B, then sum =Cin; else, sum = ~ Cin. If, A=B, then Cout = B; else, Cout = Cin.

Fig. 3 shows the detail diagram of the proposed full adder. The select line is implemented by XNOR module. In which, the inverter comprised of transistors Mp1 and Mn1 generate B‟, which is effectively used to design the controlled inverter using the transistor pair Mp2 and Mn2. Output of this controlled inverter is basically the XNOR of A and B. But it has some voltage degradation problem, which has been removed using two pass transistors Mp3 and Mn3. The parity between inputs A and B is checked by A xnor *B* function. Because of this function A xnor B act as a select line for both sum and carry out generation. If they are same, then sum is same as Cin and *C*out is same as B, which is implemented using the CMOS logic realized by transistors Mn5 and Mn6.Otherwise, the input carry signal (*C*in*)* is reflected as *C*out and inverse of C_{in} is reflected as sum which is implemented by another CMOS logic consisting of transistors Mp5 and Mp6.

4.1 Operation of Module 1 (XNOR)

In which, the inverter comprised of

transistors Mp1 and Mn1 generate B‟, which is effectively used to design the controlled inverter using the transistor pair Mp2 and Mn2 shown in Fig.2(b). Output of this controlled inverter is basically the *XNOR* of A and B. But it has some voltage degradation problem, which has been removed using two pass transistors Mp3 and Mn3. The parity between inputs A and B is checked by A *XNOR B* function.

4.2 Operation of Module 2 (sum generation)

Fig.2(c) shown if the inputs A and B are same, then *XNOR* output will be logic "1‟, the *XNOR* output is connected to gate terminal of nmos Mn5 and pmos Mp5, so it turn ON the transistor Mn5, the input Cin is given to the source terminal of nmos the active nmos pull down the Cin to the drain terminal which is output sum, results the output sum is same as Cin. Otherwise the inputs A and B are different, the *XNOR* output will be logic „0‟, it turns ON the pmos Mp5. In which, inverse of Cin is given to the source terminal so the pmos pull up the inverse of Cin to the drain terminal as output sum. Consequently the sum will be either Cin or inverse of Cin according the inputs A and B.

4.3 Operation of Module 3 (Cout generation)

In the Fig.2 (d) two transistors are connected back to back that is both gate terminals are connected. The inputs A and B are same, then *XNOR* output will be logic
„1‟, the *XNOR* output is connected to gate terminal of nmos Mn6 and pmos Mp6, so it turn ON the transistor Mn6, the input B is given to the source terminal of nmos the active nmos pull down the B to the drain terminal which is output Cout, results the output Cout is same as B. Otherwise the inputs A and B are different, the *XNOR* output will be logic „0‟, it turns ON the pmos Mp6. In which, the input Cin is given to the source terminal so the pmos pull up the Cin to the drain terminal as output Cout. Consequently the Cout will be either input Cin or input B according the inputs A and B.

5. Implementation of Low Power Techniques

The proposed full adder is implemented with some low power techniques and results are obtained and tabulated for comparison.

5.1. NORMAL SLEEP

Traditionally sub threshold leakage current is controlled by NMOS sleep transistor introducing in the pull down path and PMOS sleep transistor in the pull up path of a CMOS circuit. In sleep transistor technique [16], an NMOS sleep transistor is connected in the pull down path and PMOS transistor is connected in the pull-up path.

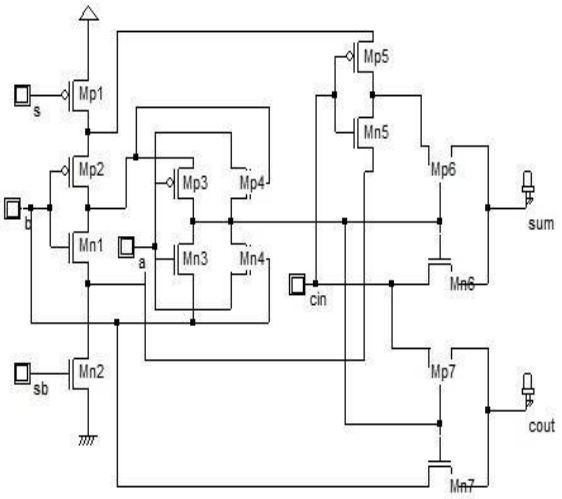


Fig. 4 Proposed full adder with normal sleep.

During normal operation the sleep signal S is at logic 0 voltage level and complementary sleep signal Sb is at logic 1 voltage level. The circuit composed of transistors Mp2 and Mn1 functions as a traditional inverter. During normal operation the transistors Mp1 and Mn2 are also on and hence the node VG is at ground potential and node VP is at VDD. Thus the inverted output is obtained from the inverter. When inverter has ideal in stand-by or sleep mode the signal S is at logic 1 and signal Sb is at logic 0. This makes the two transistors Mp1 and Mn2 into cut-off state. Thus the node VG is at a virtual ground potential and node VP is at a virtual power potential. Thus the inverter enters in to sleep mode. Due to the cut off transistors Mp1 and Mn2 the potential VG increases; the potential VP drops. The source to body potential of transistor M1 increases and causes rise in threshold voltage of transistor Mp2. Thus sub threshold current of transistor Mp2 reduces. This sleep method is applied to proposed circuit shown in Fig 4 and their output are observed and tabulated below.

5.2. POWER GATING

In the Fig 5, the proposed full adder is implemented with power gating technique. In which, two complementary transistors are connected to pull down transistor of XNOR structure and cmos inverter. For this power gating structure nmos Mn2 and pmos Mp2 are connected cascaded [20]. This structure will be present between both XNOR inverter and cmos inverter nmos and the Gnd. For power gating structure gate of the pmos is connected to Gnd and S input is given to the nmos Mn2. Logic 1 is set to the S input for normal operation. This technique provides low leakage and state retention at large total power consumption.

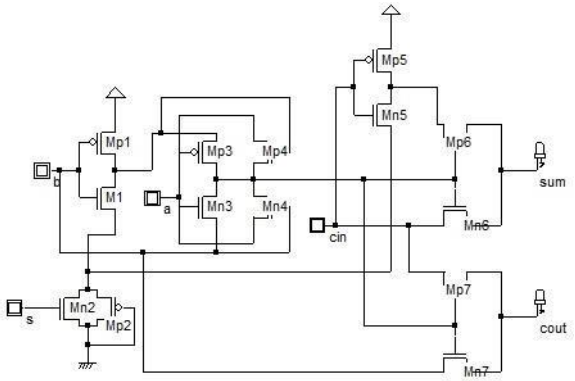


Fig 5: Proposed full adder with power gating technique.

5.3. LECTOR TECHNIQUE

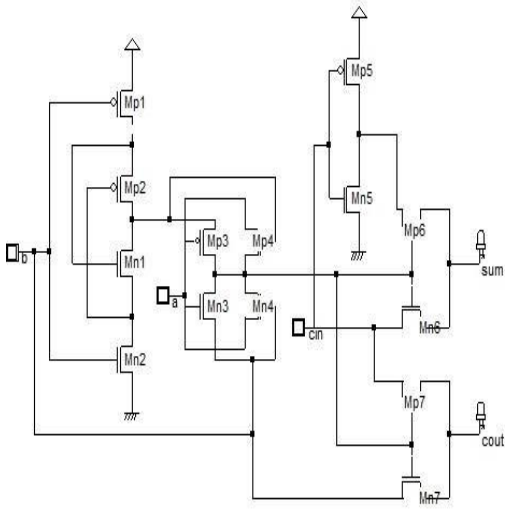


Fig 6: proposed full adder with LECTOR technique.

The topology of a LECTOR CMOS gate with proposed full adder is shown in Figure 6. Two LCTs (Mp2 and Mn1) are introduced between nodes Mp1 and Mn2. The gate terminal of each LCT is controlled by the source of the other, therefore they termed as self-controlled stacked transistors [19]. As LCTs are self-controlled, no need of external circuit; thereby the limitation with the sleep transistor technique has been overcome. Increase in resistance of the path from Vdd to Gnd by the introduction of LCTs, thus reducing the leakage current.

5.4. NOVAL TECHNIQUE

In sleep transistor technique, pull-up and/or pull-down or both networks are cut off from supply voltage or ground using sleep transistors. This approach offers very good reduction in leakage power but introduce the state information loses during sleep mode. To retain the state of the circuit, Sleepy Keeper method introduces additional keeper transistors to the sleep transistor technique. This circuit methodology has resulted in large dynamic power dissipation. Power gating method provides state retention with large associated power consumption. The novel techniques are used to reduce leakage power in inverters with ultra-low leak operation and state retention. Two novel low leak circuit techniques for logic gates are.

1. An ultra-low leakage power reduction (ULLC) technique with lowest leakage power.

2. State retention low leakage technique (LPSR)

In Fig 7 the proposed full adder with ULLC technique is shown. This model is just a vice versa of normal sleep transistor set up. In which pull down transistor nmos is connected to XNOR pmos and pull up transistor is connected to XNOR nmos transistor. The two pull up Mp2 and pull down transistor Mn2 have the inputs S=1 and Sb=0 respectively. This ULLC is used for only XNOR module. For normal operation both transistors will be ON state and normal cmos inverter is present between these two ULLC transistors. This provides very low power consumption [2] but slightly low output swing.
To overcome this, use LPSR technique. In the proposed full adder LPSR is used in both invertors in the proposed circuit. Similarly ULLC also can be used for both inverters it will produce very low power consumption but its output swing will be

comparatively worst. This LPSR technique will be vice versa of power gating technique. Use pmos instead of nmos and nmos instead of pmos in LPSR technique compared to power gating. This mode provides full output swing at cost of little high power [2] when compared to all the techniques.

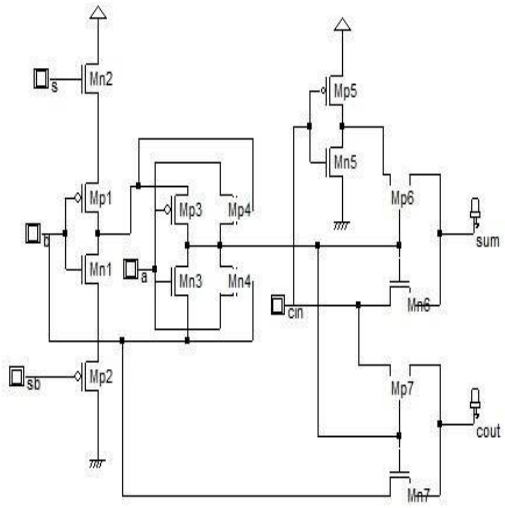


Fig 7: Proposed full adder with ULLC technique.

From Fig 7 MP2 and Mn2 forms the LPSR model and this is connected to both the inverters in the circuit. Mp2 is directly connected to Gnd because it provides logic 0 to pmos which turn ON the pull up transistor. For nmos Mn2 Sb =1 input is given to it and this will turn ON the nmos transistor. For normal operation both transistor in LPSR model will be in ON state. This will provides full output swing.

6 Performance Analysis of the Proposed Full Adder And Simulation Results

The simulation of the proposed full was carried out using CMOS 0.12µm technology Microwind 9.1. The simulation results are compared with hybrid full adder in terms of power and area. The existing hybrid full adder was carried out in Cadence Virtuoso software, for the comparison the existing full adder is simulate also in Microwind 9.1.From the simulation results, the performance parameters power and area are compared and the proposed system has reduced area and power than hybrid full adder. Along with this, a comparison of proposed full adder with some low power techniques also observed and tabulated. In this comparison, power consumption, layout area and output swing status are the parameters. According this the following full adder may be used for the users convenient. This report provides some new and clear perspective to the designers of VLSI products.

Table 1 Comparison between proposed and existing full adder.

Design	Average power (μW)	Layout area (µm^2)	Transistor count	Improved power in %	Improved area in %
Hybrid FA	14.005	299.4	16	35.17	28.59
Logical FA	9.079	213.8	12		

Table 2 Comparison between proposed full adder (PFA) with some low power techniques.

S.No	Model	Power Consumption (µm)	Layout Area (µm^2)	Transistor Count	Output Swing Status	Reduction in Power (%)	Effect in Area (%)
1.	Proposed FA with Normal sleep	4.469	308.2	14	Full o/p swing.	68.08	2.9 (Increased)
2.	PFA with Power gating.	7.542	278.1	14	Full o/p swing.	46.14	7.1 (Decreased)
3.	Normal sleep only for XNOR.	6.901	308.2	14	Full o/p swing.	50.72	2.9 (Increased)
4.	PFA with LPSR model	7.347	278.1	14	Full o/p swing.	47.54	7.1 (Decreased)
5.	PFA with ULLC only for XNOR.	2.409	308.2	14	Close Full o/p swing.	82.73	2.9 (Increased)
6.	PFA with LECTOR method.	4.949	308.2	14	Close Full o/p swing.	64.66	2.9 (Increased)
7.	PFA with ULLC model.	0.605	323.2	14	Low o/p swing.	95.68	7.9 (Increased)

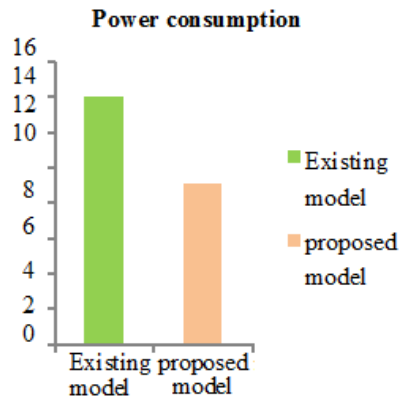


Fig 8: Power Consumption %

7. Conclusion

The simulation was carried out using Microwind 9.1 and compared with hybrid 1- bit full adder. The simulation results established that the proposed adder offered improved power and area compared with the earlier reports. The proposed full adder offered 35.17% improvement with respect to the recent existing design in terms of power and 28.59% improvement in layout area. To reduce power some low power techniques are used. The simulation will be carried for the proposed full adder with some low power techniques and their results are tabulated. In which, some model has obtained very high power improvement such as 95.68% and some model has increased layout area like 7.9%. This work will give the new perspective to the designers. Future work will be tried to reduce area and also make a view about delay parameter.

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