A New Zero Voltage Switching Three Level Bidirectional Converter

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Abstract: *In this paper a new bidirectional three level converter with soft switching operation and high efficiency is proposed. In the proposed converter by means of using two resonant LC elements soft switching operation for all the semiconductor elements are obtained. Also three level structure of the proposed converter caused lower voltage stress for all of the switches. Soft switching conditions is provided without auxiliary switch, which implementation of control circuit is simple. To justify the analysis, a prototype converter is designed, simulated and finally practically implemented. Simulation and experimental results have shown that the proposed converter operates under zero voltage switching condition and with these results the proposed converter has achieved the efficiency of 98%.*

Key words: *Bidirectional DC-DC converter, zero voltage switching (ZVS), zero current switching (ZCS), pulse width modulation (PWM), three level converter.*

1. Introduction

The bi-directional DC-DC converters with high DC voltage links have many uses in battery charging systems, renewable energy systems, uninterruptible power supplies and hybrid vehicles [1]-[3], and today the use of these converters is increased. Between different converters, the bi-directional buck -boost converter is more widely considered because of its simple structure, high efficiency and low price [3]-[6]. Three-level structure is used to reduce voltage stress on the switches, which the voltage of the switch is reduced by half the output voltage, therefore, the converter can be implemented by using lower voltage switches. However, due to the hard switching operation, the switch losses in the multi-level converters are high and by increasing switching frequency, switching losses increases and the converter efficiency decreases.

To reduce the volume and weight of the converter it is necessary to increase the switching frequency, so it is necessary to use auxiliary circuits to reduce the switch losses by providing soft switching conditions. One method for achieving soft switching conditions is to use an auxiliary switch with the creation of a resonance in an inductor and a capacitor in order to provide the zero current switching conditions [7]-[10]. However because of resonant conditions in the circuit, voltage and current stress in these converters are high. In [10]-[13] the converters have been introduced with the Active- Clamp auxiliary circuit, which by using one or more auxiliary switch soft switching conditions is provided. Although the main and auxiliary switches operate under zero voltage switching conditions and switching losses is decreased, but voltage stress on the switch is increased.

In this paper a new bidirectional three level converter is proposed. In the proposed converter, a three-level method has been used to reduce voltage stress of the switches. Also, to establish the soft switching condition in the proposed converter, two similar LC resonances are used for each pair of switches, this method does not require the addition of auxiliary switch, therefore, control circuit of the proposed converter is not complicated, also the proposed converter can be implemented in proper volume and weight. In section 2 the proposed converter is introduced and operation of the converter is described. In section 3 design procedure of the proposed converter is illustrated. To verify theoretical analysis, simulation and experimental results of the proposed converter are presented in section 4. Finally in section 5 conclusion of this paper is presented.

2. Circuit Description and Operation

The proposed converter is shown in Fig 1. The low voltage (V_L) side is on the left and high voltage (V_H) side is on the right. S_1, S_2, S_3 and S_4 are converter switch, C_d, C_{O1} and C_{O2} are capacitors in low voltage and high voltage sides. Two similar LC circuits consist of L_{r1}, C_{r1} and L_{r2}, C_{r2} have been used to eliminate the power loss of the switches. The switches operate at constant frequency. This converter operates at four intervals in both buck and boost modes. For simplicity of circuit analysis, the following assumption have be considered.

- L_B is large enough, therefore at one operation cycle its current considered to be fixed.
- C_{O1}, C_{O2} and C_d is large enough, therefore at one operation cycle their voltage considered to be fixed.
- All switches are ideal.

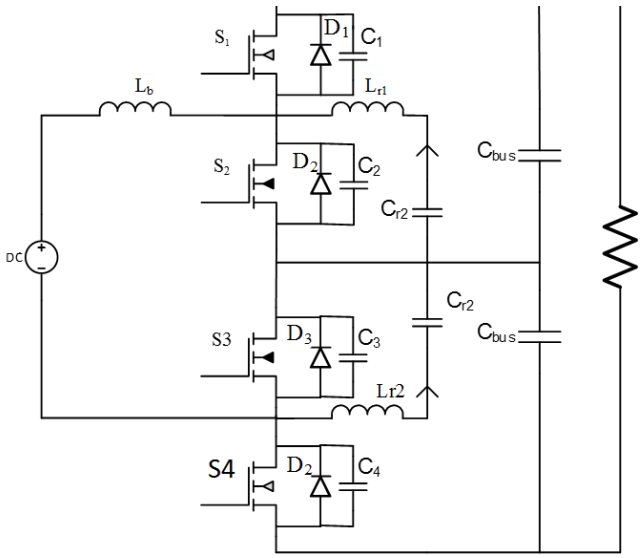

Fig. 1. Proposed soft-switching bidirectional converter

For simplicity of circuit analysis, the following assumptions have be considered.

- The capacitors in the input and output of bidirectional converter are large enough, therefore the input and output voltage is considered to be fixed.
- All semiconductor devices are ideal.

2.1. The boost mode of operation

When power transferred from V_L to V_H the proposed converter operates as boost converter. In this mode S_2 and S3 are main switch and duty cycle (D) is ratio between turning on S_3 to switching period. The key waveform of boost operation with D>0.5 and D<0.5 is shown in Fig2.

Mode 1: In this mode, the input inductor is charged by the input voltage and the resonance occurs between C_{r1} and L_{r1}.

S_2 is turned off under zero voltage due to snubber capacitor (C_r) and the L_{r1} current and the L_b current starts charging C_2 and discharging C_1. At the end of this mode, C_2 is charged to the output voltage and C_1 is fully discharged.

Equations in this situation are obtained.

$$-V_L + L_b \frac{di_{LB}}{dt} = 0 \quad (1)$$

$$-V_{cr1} + L_{r1} \frac{di_{Lr1}}{dt} = 0 \quad (2)$$

$$-C_{r1} \frac{dV_{Cr1}}{dt} = i_{Lr1} \quad (3)$$

$$-V_{cr2} + L_{r2} \frac{di_{Lr2}}{dt} = 0 \quad (4)$$

$$-C_{r1} \frac{dV_{Cr2}}{dt} = i_{Lr2} \quad (5)$$

Mode 2: In this mode, C_1 is completely discharged and C_2 is charged. The body diode S_1 is conducts and S_1 can be turns on under ZVS. In this state, the L_r current is reversed and the current from the diode transferred to the S_1. This mode ends when S_1 turns off.

$$-V_H + L_b \frac{di_{LB}}{dt} - V_L = 0 \quad (6)$$

$$-V_{cr1} + L_{r1} \frac{di_{Lr1}}{dt} + V_{o1} = 0 \quad (7)$$

$$-C_{r1} \frac{dV_{Cr1}}{dt} = i_{Lr1} \quad (8)$$

$$-V_{cr2} + L_{r2} \frac{di_{Lr2}}{dt} + V_{o2} = 0 \quad (9)$$

$$-C_{r2} \frac{dV_{Cr2}}{dt} = i_{Lr2} \quad (10)$$

Mode 3: This mode starts with the turning off S_1. The L_{r1} current charge C_1 and discharges C_2. The diode of the body S_2 conducts, and S_2 can be turn on under ZVS.

Circuit equations in this mode are given below, which writing volt-sec balance and ignored resonance modes

$$V_{o2} + L_b \frac{dI_{Lb}}{dt} - V_L = 0 \quad (11)$$

$$V_{o1} + L_b \frac{dI_{Lb}}{dt} - V_L = 0 \quad (12)$$

$$(V_L - \frac{V_H}{2})D + (V_L - V_H)(\frac{1}{2} - D) = 0 \quad (13)$$

$$\frac{V_H}{V_L} = \frac{1}{1-D} \quad (14)$$

$$\frac{V_H}{V_L} = \frac{1}{1-D} \quad (15)$$

The equivalent of these modes are shown in Fig 3.

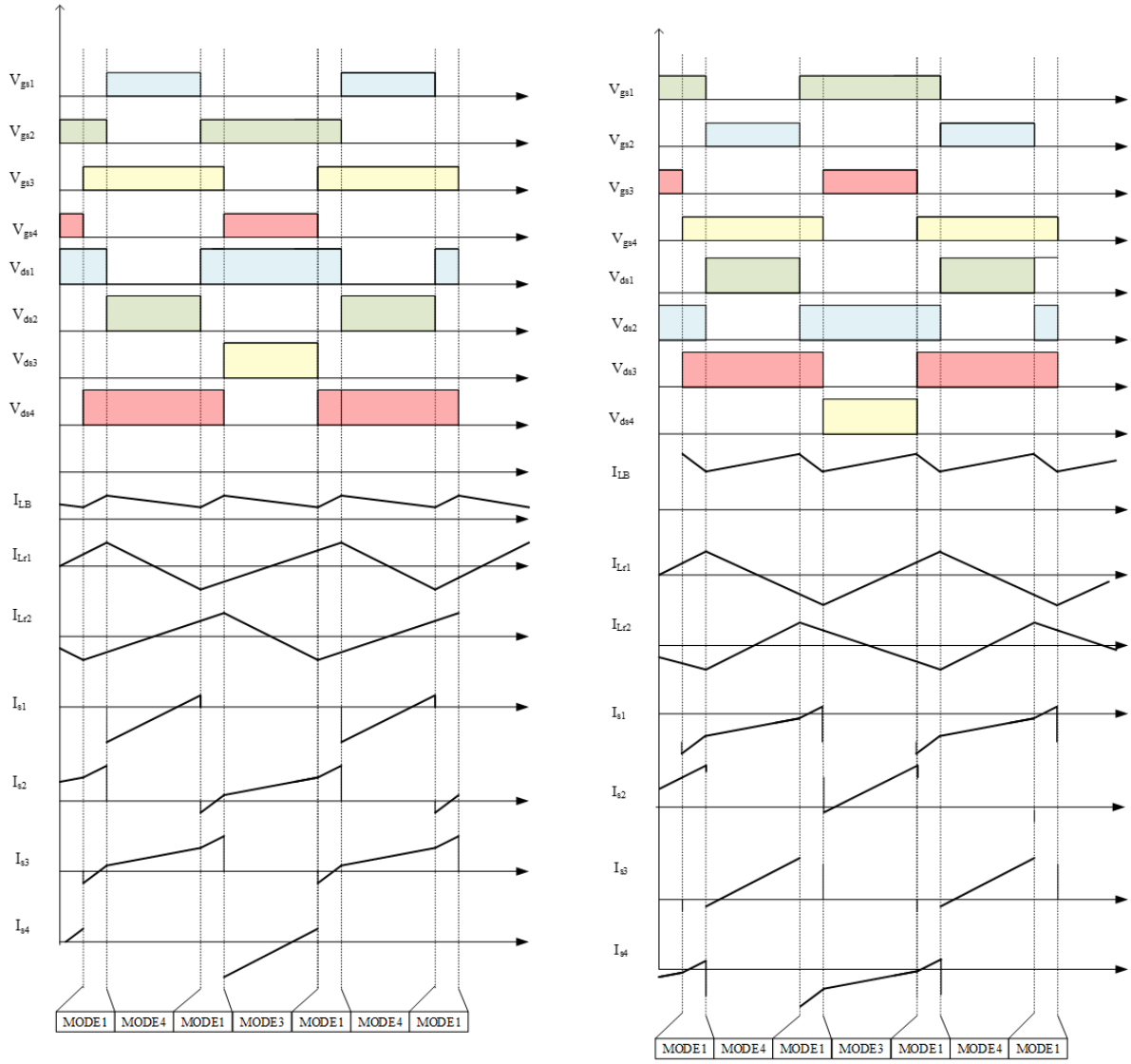

Fig. 2. The key waveform of the proposed converter in boost operation with D>0.5 (a) and D<0.5 (b).

2.2 The buck mode of operation

When power transferred from V_H to V_L the proposed converter operates as buck converter. In this mode S_1 and S_4 are main switch and duty cycle (D) is ratio between turning on S_1 to switching period. The key waveform of buck operation with D>0.5 and D<0.5 are shown in Fig 4.

Mode 1: In this mode, the output inductor is discharged by the output voltage and the resonance occurs between C_{r1} and L_{r1}. At the end of this mode, S_2 is turned off under zero voltage, and the difference between L_{r1} current and L_b current starts charging C_2 and discharging C_1. C_2 is charged to the output voltage (V_L) and the C_1 is completely discharged.

$$V_H - L_b \frac{di_{LB}}{dt} - V_L = 0 \tag{16}$$

$$-V_{cr1} + L_{r1} \frac{di_{Lr1}}{dt} + V_{o1} = 0 \tag{17}$$

$$-C_{r1} \frac{dV_{Cr1}}{dt} = i_{Lr1} \tag{18}$$

$$-V_{cr2} - L_{r2} \frac{di_{Lr1}}{dt} + V_{o2} = 0 \tag{19}$$

$$-C_{r2} \frac{dV_{Cr2}}{dt} = i_{Lr2} \tag{20}$$

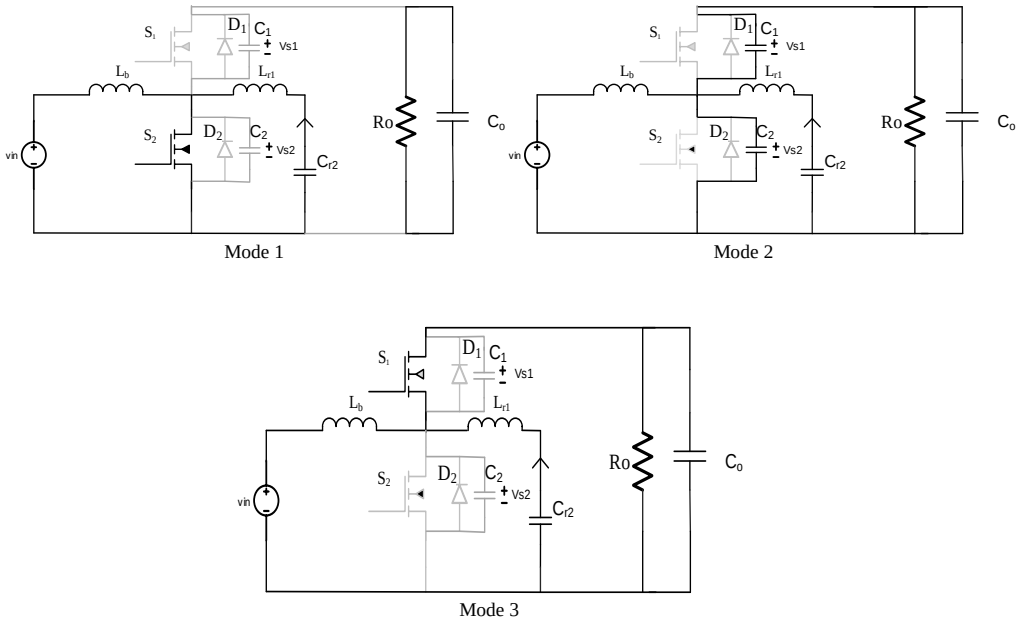

Fig. 3. The equivalent circuits of the proposed converter in boost operation

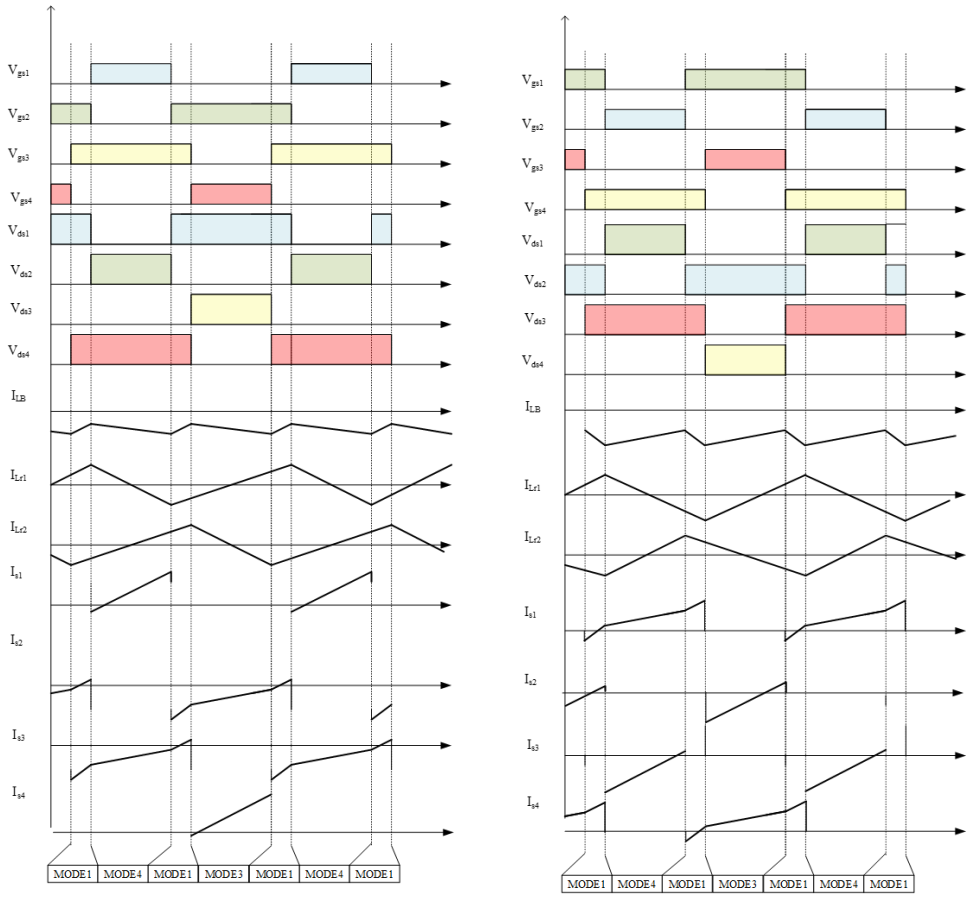

Fig. 4. The key waveform of the proposed converter in buck operation with D>0.5 (a) and D<0.5 (b).

Mode 2: In this mode, S_2 is turned off and the body diode of S_1 conducts, and S_1 can be turned on under ZVS. By changing the direction of the L_{r1} current the

current is transmitted from the body diode of S_1 to S_1, and the power transmitted from input to the output.

The equations in this mode is presented below.

$$-V_L + L_b \frac{di_{LB}}{dt} = 0 \quad (21)$$

$$-V_{cr1} + L_{r1} \frac{di_{Lr1}}{dt} = 0 \quad (22)$$

$$-C_{r1} \frac{dV_{Cr1}}{dt} = i_{Lr1} \quad (23)$$

$$-V_{cr2} + L_{r2} \frac{di_{Lr2}}{dt} = 0 \quad (24)$$

$$-C_{r2} \frac{dV_{Cr2}}{dt} = i_{Lr2} \quad (25)$$

Mode 3: By turning off S_1, this mode begins and as a result, the L_{r1} current starts charging C_1 and discharging C_2, and when the body diode of S_2 turns on, the ZVS condition is provided for S_2. Finally the current from the body diode of S_2 is transferred to S_2.

$$V_{o1} - L_b \frac{dI_{Lb}}{dt} - V_L = 0 \quad (26)$$

$$V_{o2} - L_b \frac{dI_{Lb}}{dt} - V_L = 0 \quad (27)$$

$$(V_L - \frac{V_H}{2})D + (V_L)(\frac{1}{2} - D) = 0 \quad (28)$$

$$\frac{V_L}{V_H} = D \quad (29)$$

The equivalent of these modes in buck mode are shown in Fig 5.

3. Zero voltage conditions

This switching transition period corresponds to the switching time from mode1 to mode 3 in the boost operation. C_1 and C_2 are the parasitic capacitances of S_1 and S_2, respectively. C_1 has been charged to V_{o1} as i_{Lb} and i_{Lr1} flows through S_2.

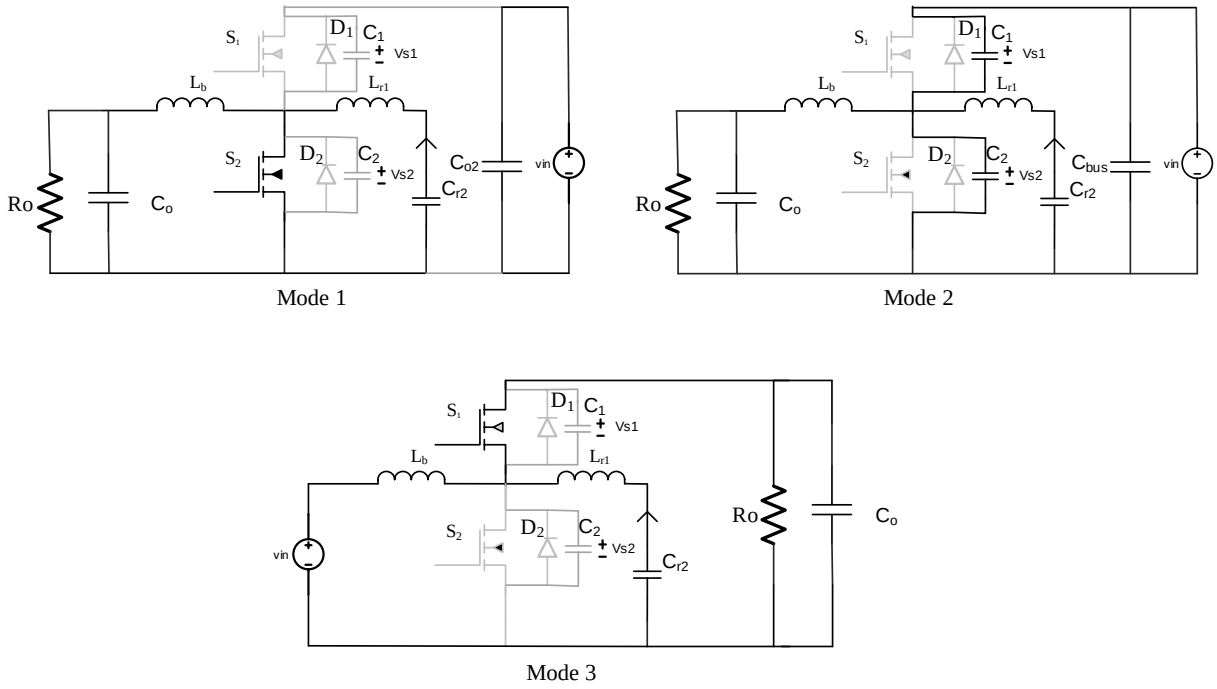

Fig .5. The equivalent circuits of the proposed converter in buck operation

i_{Lb} and i_{Lr1} are divided to the capacitances, and cause to charging C_2 and discharging C_1. C_1 is completely discharged by the inductor current, which reversely flows through S_1. The switch voltage V_{S1}, before S_1 is turned on, becomes zero. S_1 can be turned on at zero-voltage when a control signal is applied to S_1. C_2 has been charged to V_{o1} as i_{Lb} and i_{Lr1} passes through S_1. The switching transition for other power switches is similar to the switching transition for S_1. As described in (21), the zero-voltage switching condition for power switches in one switching leg can be expressed as

$$-V_{cr1} + I_{r1} \frac{di_{Lr1}}{dt} = 0 \quad (30)$$

$$\frac{\Delta I_{Lr1}}{2} = \frac{\Delta I_{Lr2}}{2} > \left| I_{Lb,ave} \right| + \frac{\Delta I_{Lb}}{2} \quad (31)$$

Where ΔiL_{r1} and ΔiL_{r2} are the current ripples of L_{r1} and L_{r2}, respectively. $|i_{Lb},avg|$ is the total value of the average inductor current i_{Lb},avg. By the assumption that $L_{r1} = L_{r2} = L_r$, the following relation can be obtained as

$$\frac{V_L T_{on}}{2L_r} > \frac{P_d}{V_L} + \frac{V_L T_{on}}{2L_b} \quad (32)$$

Where P_d is the evaluate power of the proposed converter. By simplifying (27), the inductance of L_r can be decided as

$$L_r < \frac{L_b V_L^2 T_{on}}{2V_L^2 T_{on}} = L_b \quad (33)$$

In the event that, L_r is lower than L_b, power switches in the proposed converter operate under the zero-voltage switching condition irrespective of the voltage conversion ratio. The proposed converter can achieve the zero-voltage switching even for the high voltage conversion ratio and light load condition.

4. Simulation and Experimental Results of Proposed Converter

4.1 Simulation result

To verify the theoretical analysis, the proposed converter is simulated and results of this simulation are shown in Fig 6 and Fig 7. This simulation is done with PSPICE software and designed value of parameter in the converter is shown in table 1.

Table 1. Parameters of simulation

parameter	value
V_L	50V
V_H	150V
P	100W
Dead time	2μs
Switching frequency	100kHz
All switch	IRFP260
L_B	600μH
L_r	200μH
C_r	2μF
C_{O1},C_{O2}	100μF

As can be seen from Fig 6 and Fig 7. The current of the switches is negative when switches turns on, so ZVS condition for all switches is provided. Also when the switches are turned off, due to the parasitic capacitor of the switches, the voltage of the switches goes up slowly, so the switches will be turns off under ZVS.

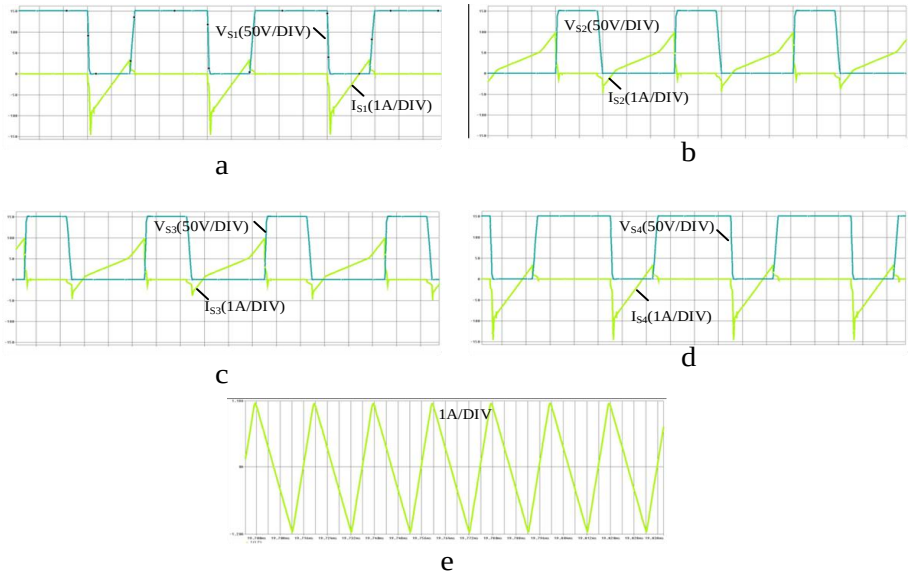

Fig. 6. Simulation results of the proposed converter in boost operation. a) voltage and current of S_1 b) voltage and current of S_2 c) voltage and current of S_3 d) voltage and current of S_4 e) current of L_r. (with 4μs/div horizontal scale).

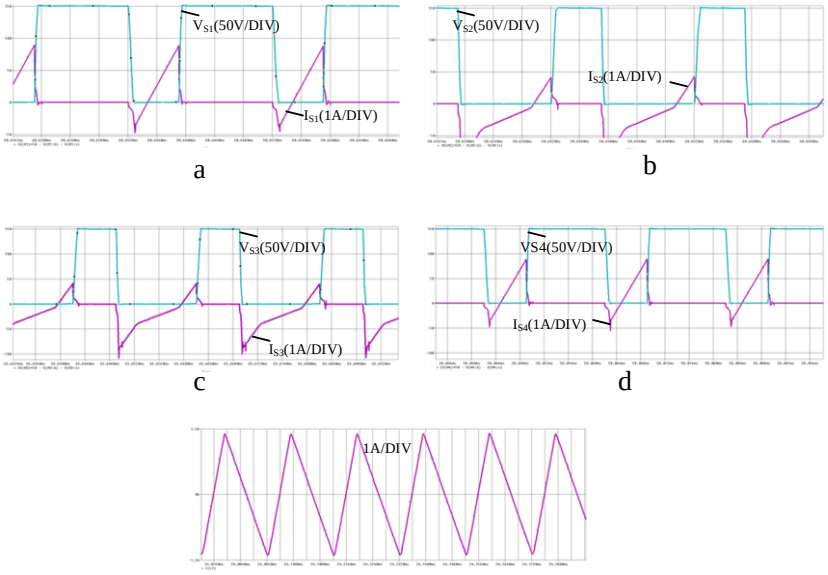

Fig. 7. Simulation results of the proposed converter in boost operation. a) voltage and current of S_1 b) voltage and current of S_2 c) voltage and current of S_3 d) voltage and current of S_4 e) current of L_r. (with 4μs/div horizontal scale).

4.2 Experimental results

To validity of theoretical analysis and simulation results an experimental circuit in accordance with the designed values of Table 1 is implemented, which is shown in Fig 8. The measured waveforms are presented in Fig 9 and Fig 10 for boost and buck operation, respectively.

As is clear from these figures, similar to the simulation results, ZVS conditions are observed for all switches.

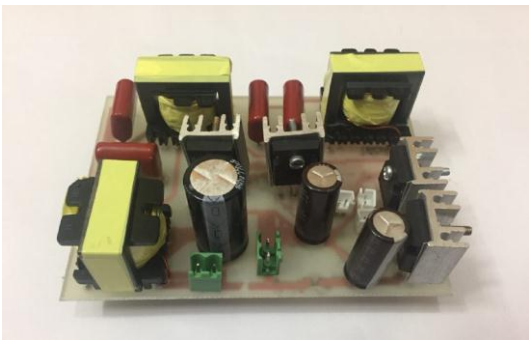

Fig. 8. The experimental prototype of circuit

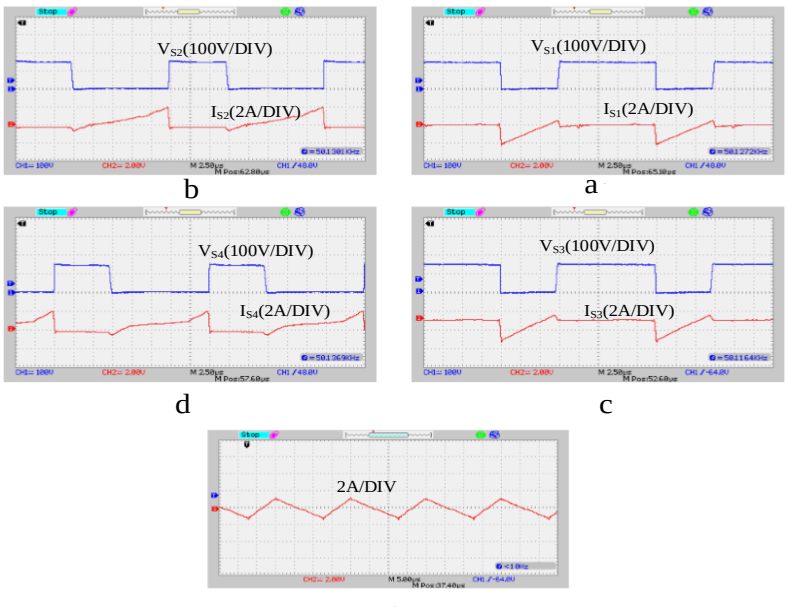

Fig. 10. Experimental results of the proposed converter in boost operation. a) voltage and current of S_1 b) voltage and current of S_2 c) voltage and current of S_3 d) voltage and current of S_4 e) current of L_B. (with 2.5μs/div horizontal scale).

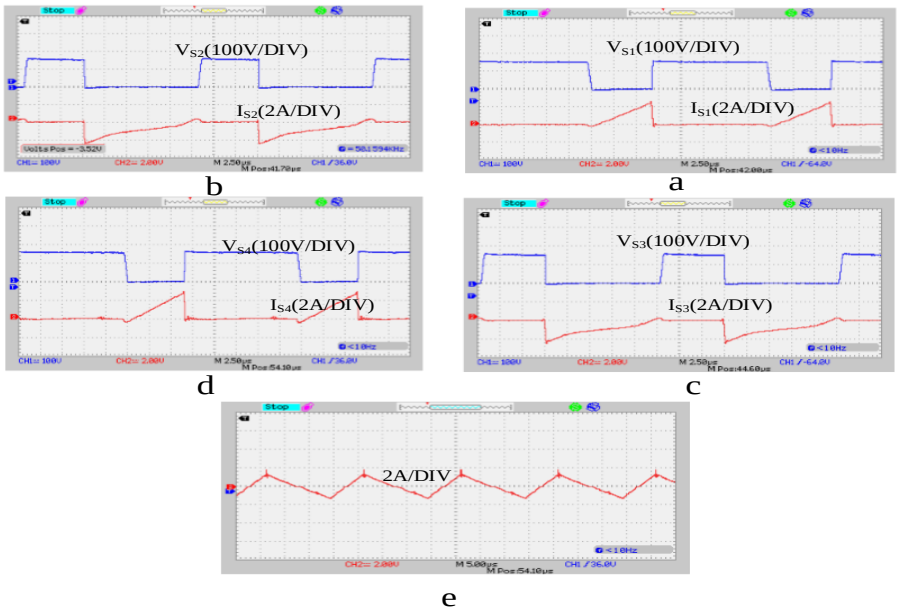

Fig. 11. Experimental results of the proposed converter in buck operation. a) voltage and current of S_1 b) voltage and current of S_2 c) voltage and current of S_3 d) voltage and current of S_4 e) current of L_B. (with 2.5µs/div horizontal scale).

Fig 12 shows the efficiency of the proposed converter in buck and boost operation, which increase in efficiency is evident in these results.

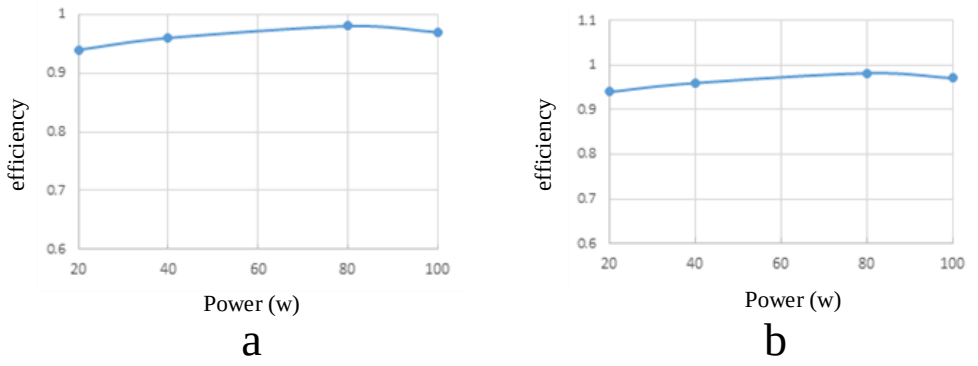

Fig. 12. Efficiency of the proposed converter in (a) buck and (b) boost operation.

5. Conclusion

In this paper a new bidirectional three level converter is proposed. In the proposed converter, a three-level method has been used to reduce the voltage stress of the switches, and the use of this method has caused the voltage of the switch to be lower than the high voltage side. Also, to establish the soft switching condition in the proposed converter, the LC circuit is used for each pair of switches, with this method in the converter, the auxiliary switch is not used, and the complexity of the control circuit of the converter does not increase and the converter can be implemented in proper volume and weight. The voltage stress of the switches in proposed converter reduces in comparison with active clamp method. The measured waveforms verify the ZVS conditions for all switches.

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