

HARMONIC ANALYSIS OF A NOVEL MULTILEVEL INVERTER WITH REDUCED SWITCHES USING GENETIC ALGORITHM

¹Maheshwari N.I, ²Chandrasekaran M

¹Lecturer (Senior Grade), EEE, Thiagarajar Polytechnic College, Salem, TN, India

²Principal, Government College of Engineering, Burgur, TN, India

¹mahesweritp16@gmail.com

Abstract-In recent years the Multilevel Inverter (MLI) has become familiar in Industrial applications. Specifically MLI is used for medium voltage and high power applications. In this paper, a MLI has been suggested with minimal number of semiconductor switches and a suitable switching technique is used to minimize the lower order harmonics. Among the various Pulse Width Modulation(PWM) techniques, Selective Harmonic Elimination Pulse Width Modulation (SHEPWM) is used in this paper. The solutions for the SHEPWM based nonlinear equations are solved meta-heuristic Genetic Algorithm (GA). The optimal values of the switching angles for a given modulation index is found. These result increases the degree of freedom. The seven level MLI is chosen, as the case study for implementation. The results are analyzed for the Total Harmonic Distortion (THD). This circuit can be extended for any levels. The result of simulation is compared with experimental values.

Keywords- Pulse width modulation, Selective Harmonics elimination, Meta heuristic genetic algorithm

INTRODUCTION

The electrical energy has become important commodity, in recent days. The conventional energy sources are depleting in nature as well as it causes pollution and hazardous to the environment. Hence, renewable energy sources like PV solar cells, wind and fuel cells etc. are preferred to produce the essential electrical energy. Amongst the available renewable sources the solar energy is preferred since it is easily available and our country being a tropical country the solar energy exists for more than 300 days.

The power from solar being direct current it needs to be converted into alternating current to be readily used. For medium and high voltage power application multilevel inverters are preferred since single semi-conductor switch is difficult to withstand high voltage and power [1]. The attractive features of MLI like the output voltage generated has low distortion and dv/dt rating, smaller common mode voltage which reduces the stress in the motor bearings and the ability to operate at lower switching frequency are effectively utilized. The solar panels may be suitably connected in series or in parallel according to the requirement of voltage and power. The multilevel inverters reduce the distortions caused by the harmonics present in

the output voltage when compared with the conventional inverters. However, the Total Harmonic Distortions (THD) should be within the permissible range of IEEE standards. As per the IEEE 519-1992 standards, the THD must be less than 5% and the individual harmonics less than 3%. The prominent types of multilevel inverters are: flying capacitor inverter, cascaded H bridge inverter and neutral diode inverter [2]-[5]. Amongst the various types of inverters, H bridge inverter is mostly preferred since less number of semiconductor components are used which reduces the bulkiness, switching losses, cost and improves the efficiency. The multilevel inverters find its applications in distributed generating stations, in high voltage direct current (HVDC) transmission, AC/DC electric drives and flexible AC transmission (FACTS)[6]

A. Conventional Topology

In the conventional MLI, three dc voltage sources with three H-bridge units are used. Each bridge consisting of four switches and altogether, twelve switches in total is used in the conventional seven level MLI which is represented in Figure 1. The expression to specify the m levels of output voltage, $m=(n+2)/2$ where, n is the total number of switches used. The output of each bridge gives three levels $+V_{dc}$, 0, $-V_{dc}$ [7]. The three Bridges are cascaded in such a fashion to produce stepped seven level staircase waveforms.

The various levels of voltages depend on the angle of switching the power electronic devices. Based on the switching angle stepped output voltage is obtained in MLI. While turning on the devices, the correct switching angle is considered since it is directly connected with the generation of harmonics. Hence, the optimum switching angle is chosen to reduce the harmonics and to get the output voltage with perfect sinusoidal waveform.

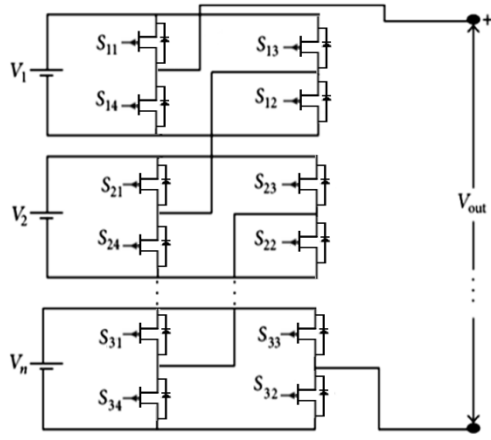


Fig.1 Conventional cascaded seven level MLI

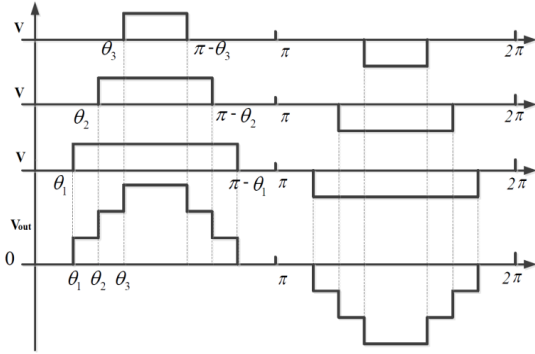


Fig.2 Staircase output waveform of seven level MLI

B. Mathematical model:

According to the Fourier series, the output voltage of a periodical function of a MLI is given as:

$$V(\omega t) = a_0 + \sum_{n=1}^{\infty} (a_n \cos(n\omega t) + b_n \sin(n\omega t)) \quad (1)$$

Due to quarter wave symmetry, only odd function exists. Hence, $a_0 = a_n = 0$ for all n .

Let $\omega t = \theta$, the constant b_n is given in equation

$$b_n = \begin{cases} \frac{4}{\pi} \int_0^{\pi} \sin(n\theta) d\theta & \text{for odd } n \\ 0 & \text{for even } n \end{cases} \quad (2)$$

$V(\omega t)$ can be expressed as,

$$V(\omega t) = \sum_{n=odd}^{\infty} b_n \sin(n\omega t) \quad (3)$$

b_n is determined in equations from (4) to (6)

$$b_n = \frac{4}{\pi} \int_{\theta_1}^{\frac{\pi}{2}} V(\theta) \sin(n\theta) d\theta \quad (4)$$

$$b_n = \frac{4}{\pi} \left(\int_{\theta_1}^{\frac{\pi}{2}-\theta_1} \frac{V_{dc}}{3} \sin(n\theta) d\theta + \int_{\theta_2}^{\frac{\pi}{2}-\theta_2} \frac{V_{dc}}{3} \sin(n\theta) d\theta + \int_{\theta_3}^{\frac{\pi}{2}-\theta_3} \frac{V_{dc}}{3} \sin(n\theta) d\theta \right) \quad (5)$$

$$b_n = \left(\frac{V_{dc}}{3} \right) \frac{4}{n\pi} [\cos(n\theta_1) + \cos(n\theta_2) + \cos(n\theta_3)] \quad (6)$$

By substituting the equation 6 and equation 3 by get the periodic function $V(\omega t)$. The periodic function $V(\omega t)$ is expressed as

$$V(\omega t) = \frac{4}{n\pi} \sum_{n=1,3,5}^{\infty} [\cos(n\theta_1) + \cos(n\theta_2) + \cos(n\theta_3)] \sin(n\theta) \quad (7)$$

Due to quarter wave symmetry along X axis the even harmonics contents are not appear. The required switching angles θ_1, θ_2 and θ_3 are calculated, with the constraint function $0 < \theta_1 < \theta_2 < \theta_3 < (\pi/2)$. With suitable determination of switching angles θ_1, θ_2 and θ_3 , the value of $V(\theta) = V_1 \sin(\theta)$ can be achieved. This consists of the desired fundamental voltage V_1 and the unwanted lower order harmonics. In this the desired fundamental output voltage has to be controlled. And, amongst the harmonics the prominent are fifth and seventh, should be eliminated. Hence, the resulting equations are reduced as follows:

$$\left(\frac{4V_{dc}}{3\pi} \right) [\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3)] = b_1 = V_1 \quad (8)$$

$$\left(\frac{4V_{dc}}{15\pi} \right) [\cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3)] = b_5 = 0 \quad (9)$$

$$\left(\frac{4V_{dc}}{21\pi} \right) [\cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3)] = b_7 = 0 \quad (10)$$

In case of balanced, wye connected, three phase system, the third harmonic isn't been considered since the triplen harmonics are naturally invalidated in the line to line voltages. Expecting an adjusted three stage framework bring down request third harmonic isn't considered. In view of this, the triplen harmonic isn't considered for disposal in the stage framework. The most extreme essential voltage ($V_{1max} = 4V_{dc}/3\pi$) is accomplished when all the exchanging edges are equivalent to zero.

The value of m_a is expressed as,

$$m_a = \frac{\pi V_1}{4sV_{dc}} \quad (11)$$

where, 's' is the number of dc sources which is also equal to the number of switching angles.

By substituting the parameter of m_a in equation number 8 to equation number 10 to get Non_linear transcendental value. The mathematical function of Non_linear transcendental is expressed as

$$[\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3)] = 3m_a \quad (12)$$

$$[\cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3)] = 0 \quad (13)$$

$$[\cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3)] = 0 \quad (14)$$

For the proposed MLI the suitable switching angles are obtained, using Selected Harmonic Eliminations (SHE) to eliminate or to reduce the lower order harmonics. To obtain the arithmetic results, for non-linear transcendental equations which contain the trigonometric terms the following methods are followed. For the given equations, there may be one solution, many solutions or no solution for the range of modulation indices. The methods adopted are:

- a. In Newton-Raphson iterative method, where initial guess is required [6].
 - When the initial guess is right choice quick converging take place.
 - If the guess is not correct one then the solution will get deviated from the correct solution.

Also, when the number of levels is increased it increases the computational burden and time consumption is increased for converging.

- b. In Mathematics theory of resultant, the non-linear equations is converted into polynomial equations. The possible solutions are obtained.
 - upto six switching angles, for equal sources
 - upto three switching angles, for unequal sources

Using Functions Solve in Matlab software all the solutions are observed for the modulation index range from 0.485 to 1.07[15]. Then solved for cosine function, from these values the $\theta_{1,2}$ and θ_3 suitable for seven level MLI are obtained [10]

- c. Intelligent algorithms like Genetic Algorithm or Particle Swarm Optimization is used for optimizing the trigonometric angles of harmonics, hence the THD can be reduced.

I. PROPOSED MODEL

The proposed topology of seven level MLI consists of three dc sources and six switches [17]. In this topology, at any given time only two switches conduct. Among six switches, two switches S_2 and S_4 are used for negative and positive polarity respectively. The rest of the four switches are used to generate the $+V_{dc}$, $+2V_{dc}$, $+3V_{dc}$, $0V$, $-V_{dc}$, $-2V_{dc}$ and $-3V_{dc}$ of desired seven level waveforms.

The expression used to find the number of switches for a multilevel inverter is, $m_p = 2 * n - 5$ where, ' m_p ' specifies the

number of levels and 'n' is the number of semiconductor switches. $m_p = 1 + 2 * s$ where, 's' denotes the dc sources required

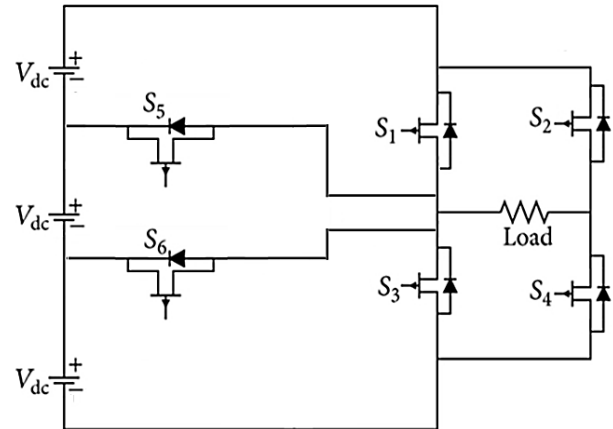


Fig. 3. Configuration of Proposed Seven Level Inverter using Six Switches

C. Modulation Techniques:

There are number of switching or modulation techniques [7] to turn on and off the semiconductor devices of MLI. The main aim is to remove or reduce lower order harmonics and hence, to reduce the THD.

Modulation methods are developed for multilevel inverters based on Pulse Width Modulation (PWM). In PWM the width of the Pulses decides ON and OFF control of switching devices. They are classified into Sinusoidal PWM, Selective Harmonic Elimination PWM, Space-Vector PWM. The performance of multilevel inverter is related with switching strategy. Selective Harmonic Elimination using Pulse Width Modulation (SHEPWM) is a famous strategy used to reduce or eliminate the unwanted lower order harmonics [8, 9].

The aim of SHEPWM in this MLI is to eliminate or reduce fifth and seventh harmonics and hence, to minimize the Total Harmonic Distortion (THD) with desired magnitude of fundamental component.

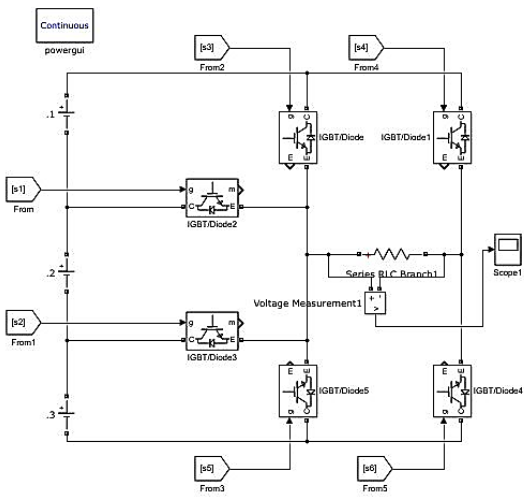


Fig. 4 Simulation model using Matlab/ Simulink

Among the number of modulation techniques carrier based PWM technique is preferred to generate the gate driving signals. One sinusoidal, modulating signal with 50 Hz and m-1 triangular, carrier signal of 1550Hz are compared. If the sinusoidal is greater than the triangular signal, PWM output is high which triggers the semi conductor device. Otherwise PWM output is low turns off the respective active device. Based on phase shifting they are classified as Phase Disposition, phase opposition disposition and alternate phase opposition disposition. Phase disposition PWM (PDPWM) is preferred as it reduces the harmonics compared with others.[19]

The switching sequence is given in Table I

TABLE I SWITCHING SEQUENCE

Sl. No.	The status of various switches		Output Voltage Generated
	Switches to be turned ON	Switches to be turned OFF	
1	S1, S4	S2, S3, S5, S6	$3V_{dc}$
2	S4, S5	S1, S2, S3, S6	$2V_{dc}$
3	S4, S6	S1, S2, S3, S5	V_{dc}
4	-	S1, S2, S3, S4, S5, S6	0
5	S2, S5	S1, S3, S4, S6	$-V_{dc}$
6	S2, S6	S1, S3, S4, S5	$-2V_{dc}$
7	S2, S3	S1, S4, S5, S6	$-3V_{dc}$

The switching pulses are generated using carrier based PWM technique as shown in the fig. 5

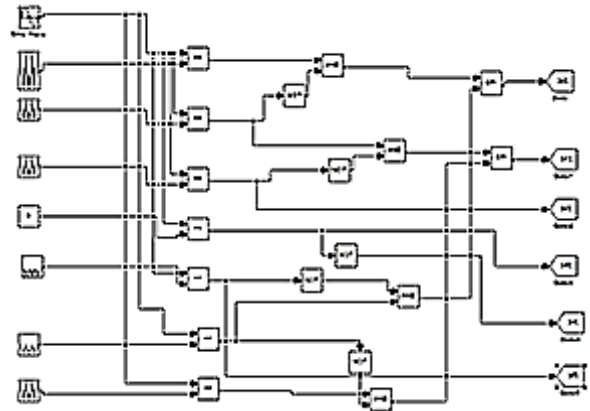


Fig. 5. Generation of switching pulses using carrier based PWM

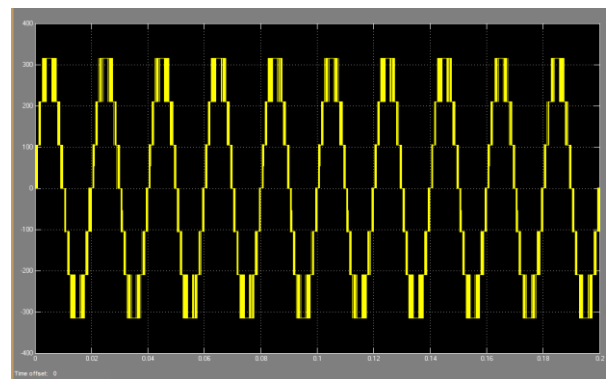


Fig. 6 Simulation result of phase output voltage

II. GENETIC ALGORITHM

Genetic Algorithm (GA) is derivative free stochastic optimization method based on the concepts of natural selection and evolution process. John Holland proposed and investigated the GA from the University of Michigan in the year 1975. They represent an intelligent exploitation of a random search to solve optimization problem. The Fourier series transform the output voltage of MLI, results into non-linear transcendental equations where in few regions more than one solutions and in some other regions no solutions are obtained[13,14]. Hence to this problem a optimisatic Genetic algorithm a part of evolutionary programme is suggested.

In this seven level multilevel inverter, the switching angles required for semiconductor switches are selected such that the lower order fifth and seventh order harmonics are eliminated or reduced while the desired fundamental component is achieved.

The objective function of the output voltage is to optimize the switching angles such that, to reduce the total harmonic distortion (THD) with the desired fundamental component.

Objective function, $THD = \frac{\sqrt{\sum_{n=5,7}(V_n^2)}}{V_1}$,

Constraint function is $0 < \theta_i < \pi / 2$,

Where, θ_i is the switching angles of the semiconductor devices. In case of seven level MLI, three switching angles are required. i.e.

$0 < \theta_1 < \theta_2 < \theta_3 < \pi / 2$

Fitness value, check $THD < 1$

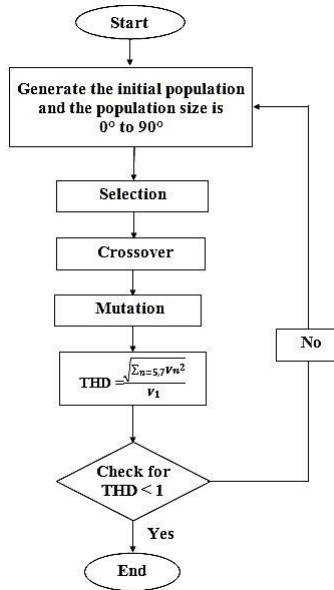


Fig.7 Flow chart of Genetic algorithm

Step1 Generate the required number of population and select the individuals randomly. The selected individuals are called parents and these individuals contribute to the population at the next generation.

Step 2 Apply the GA operator, crossover rules to combine two parents to form the children for the next generation.

Step 3 Apply the mutation rules a, i.e., apply the random changes to individual parents.

Step 4 Evaluate the $THD = \frac{\sqrt{\sum_{n=5,7}(V_n^2)}}{V_1}$, and check it whether it is minimum with the existing THD value.

Step 5 Repeat the steps from step 1to step 4 until stopping criterion $THD < 1$ is met.

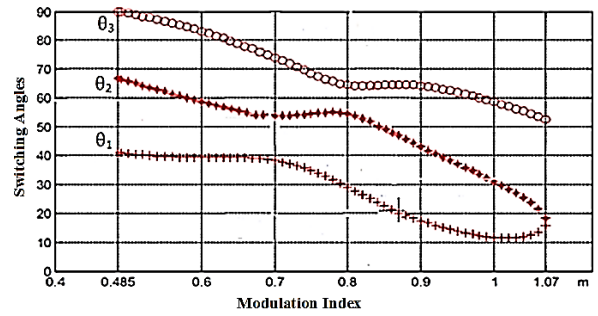


Fig. 8 Switching angles Vs modulation index m_a of seven level inverters

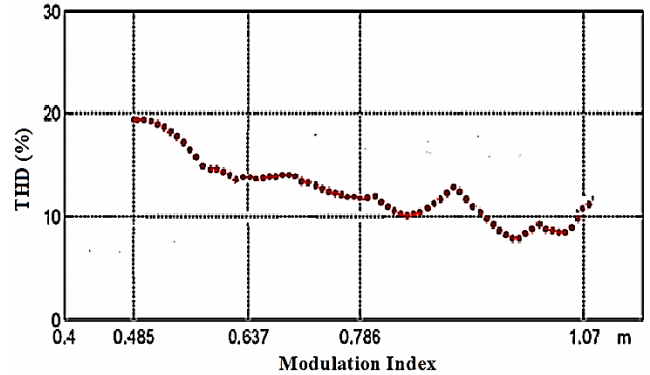


Fig. 9% THD Vs modulation index m_a of seven level inverters

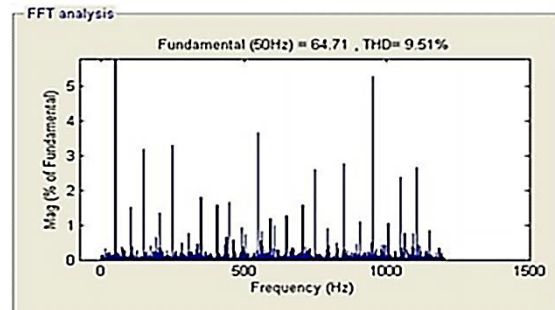


Fig. 10 % THD Vs Harmonic order of simulation

III. EXPERIMENTAL MODEL

Figure 11 shows an experimental setup of the hardware proto model. IGBTs are used as semiconductor switches. The renewable energy sources PV panel as input source, yield voltage will differ because of temperature, light and different elements. In photovoltaic frameworks, the working dc voltages of standard PV modules go from 12 to 48V. Hence, the different voltages arrive at the inverter stages will cause unregulated fundamental with a higher magnitude of low order harmonics. Figure 12 and 13 shows the phase output voltage and the THD measured in the power analyser for the modulation index of 0.863. The %THD is found to be 10.84 experimentally.

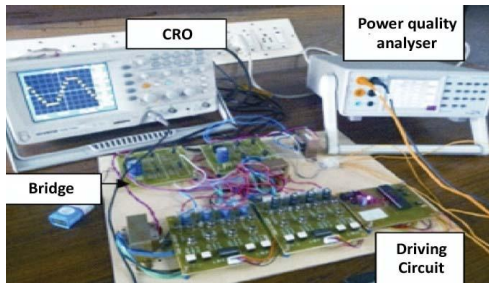


Fig.11 Hardware Proto model

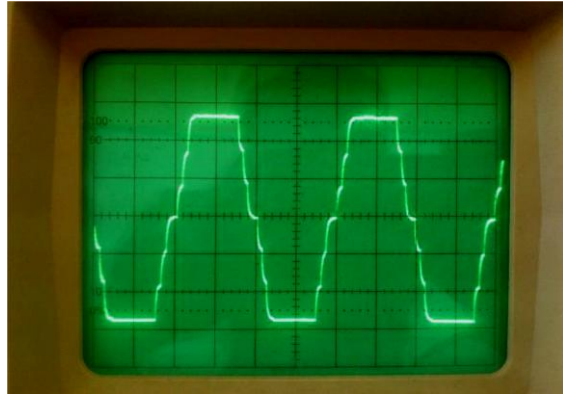


Fig.12. Experimental results of Output Voltage

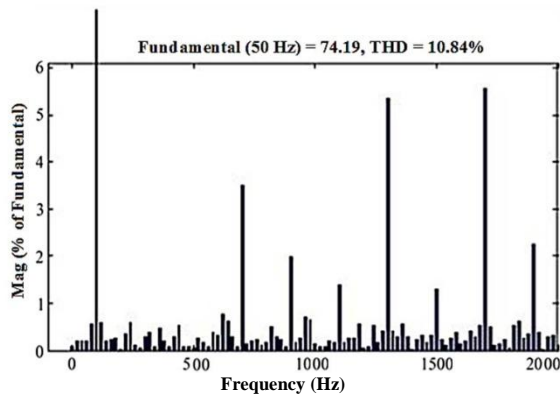


Fig. 13 FFT Analysis for seven level inverter proto model

TABLE II GENERAL COMPARISON OF POWER COMPONENT REQUIREMENTS AMONG MULTILEVEL INVERTER TOPOLOGIES

Topology	Diode clamped	Capacitor clamped	Cascaded
Power semiconductor switches	$2(m-1)$	$2(m-1)$	$2(m-1)$
Clamping diodes	$(m-1)(m-2)$	0	0
DC bus capacitor	$(m-1)$	$(m-1)$	$(m-1)/2$
Balancing capacitor	0	$(m-1)(m-2)/2$	0
Voltage balancing	Average	High	Very small

TABLE III COMPARISON OF COMPONENTS FOR SEVEN LEVEL MLI TOPOLOGIES

Topology	Power	Clamping	DC bus	Balancing
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	semi-conduct or switches	diode	capacitor	capacitor
Diode clamped	12	30	6	0
Capacitor clamped	12	0	6	15
Cascaded	12	0	3	0
With reduced number of switches	6	0	0	0

From the table III it is observed that, the proposed topology requires reduced number of power semiconductor switches and nil number of diodes and capacitors.

TABLE IV PARAMETERS OF THE PROPOSED INVERTER

Parameters	Typical Value
DC voltage to Inverter	23.2 X 4 nos.
Power frequency	50 Hz
Carrier frequency	1550Hz
Load resistance	100 Ohms

TABLE V COMPARISON OF %THD

Intelligent Algorithm	THD (%)
GA	12.98
PSO	12.25
GA with reduced switches (Simulation)	9.51
GA with reduced switches (proto model)	10.84

IV. CONCLUSION

For a given multilevel inverter, seven level is considered for analysis and comparison. In the conventional seven level cascaded multilevel inverter 12 switches are used. Whereas in this proposed topology reduced number of switches i.e. six number of switches are used with three dc sources. Using SHEPWM the non-linear transcendental equations are obtained to minimize the low order harmonics. Solving the non-linear using function solve predicts the range of modulation index is from 0.48 to 1.07. Using carrier based PWM technique reduced multilevel inverter circuit is simulated and %THD is 9.51

The THD values using various optimization techniques are compared. Among the various values PSO reduces the THD whereas the GA has better convergences. The multilevel inverter with reduced switches is experimentally synthesized and the % THD using GA is 10.84% where the lower order harmonics are minimized. By reducing the higher order harmonics, this system can very well maintain the %THD, less than 5% as per IEEE 519-1992. The reduction can be

achieved using suitable filter of smaller size and hence the cost of the system is reduced. The %THD of simulation results are compared with experimental proto model.

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