PV panel sourced multi level inverter with novel approach

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Abstract-In recent years, inverters are used in wide applications to have efficient current during power losses. The battery of the inverter stores the voltage of the current and emits current during power losses. Nowadays, solar energy is preferred for storing the voltage sources of the battery. But due to many unfavorable conditions, the battery provides insufficient voltage for the inverter. To overcome the issue, we proposed A single-phase nine-level inverter is implemented which fed with a photovoltaic system. A pulse-width-modulated (PWM) regulation strategy is handled to generate the PWM signals for the inverter. Typically, Maximum Power Point Tracking (MPPT) is permitted in this multilevel inverter to extract extremely high power from the sun at daytime. An adaptive MPPT procedure is deployed with a standard trouble and sense way for the PV system. The proposed work with a reduced number of switches converts DC to AC which is capable of producing nine levels of output-voltage levels from the dc supply voltage. The Pulse Width Modulation (PWM) signals are generated to the inverter by using PID and Fuzzy Controllers, and the total harmonic distortion (THD) results are compared. The voltage control of Single-Phase Induction Motor for better performance is discussed and implemented in MATLAB / SIMULINK. The Simulation circuit is analyzed, and results are discussed for the proposed method which has better accuracy in contrast with the traditional methods.

1. Introduction

In general, the inverters are used for the conversion of DC power to AC power at the terminal voltage. It is because DC power can be stored while AC power cannot be able to store. However, DC power cannot be transported to very long distance whereas AC power is transported. Therefore to store the power, we store it in DC power, and for transporting to the variousapplication, we have to convert it into AC power. The inverteris used for this conversion purpose which greatly hashigh power quality, lower order harmonics, lower switching losses, and better electromagneticinterference,and frequency. But it faces with many drawbacks such as less efficiency, high cost, and high switching losses. Hence multi-level inverter is introduced which produce staircase waveform and have constrained harmonic level. It has three types namely, diode clamped, flying capacitor inverter and cascaded multilevel inverter. The work provides the output with lower order harmonics. The low distortion based input current is fed in the inverter and also CM voltages are extremely reduced by means of classical method. It have the capability of working at a very low switching frequency.

In general, a series connected series connected single full bridge inverter is built in cascaded multiple inverter whereas individual possess their own isolated dc bus. The sinusoidal waveform voltage is the output of the multilevel inverter which drawn with the help of numerous separate dc sources that received by means of some sources such as solar cells, fuel cells, batteries, ultra capacitors, etc. Auspiciously, some sources such as transformer, clamping diodes or flying capacitors are not required in this inverter. Five dissimilar voltage outputs +2 V_{dc}, + V_{dc}, 0 ,–2 V_{dc} and –V_{dc} are generated by each level can generate by connecting the dc sources to the ac output side via dissimilar combinations of the four switches. As a consequence, the output voltage of an M-level inverter is simply defined as the sum of each individual inverter outputs. The active devices of every H-Bridge switches only at the threshold frequency, and a quasi- square waveform is produced by every H-bridge using phase-shifting about its positive and negative phase legs switching timings. The phase shift of half cycle or 180˚ is achieved by each switching device anyway of the pulse width of the quasi-square wave and therefore this switching method fallouts in equalizing the current stress in each active device. This kind of inverter topology is appropriate for high voltage and high

power inversion since the ability of synthesize waveforms with low switching frequency as well as better harmonic spectrum.

The proposed work used cascaded H-bridge topology because of its simplicity and other advantages. Some of the noble features of the inverter are suitable to high-voltage, high-power applications than the conservative inverters. The inverter changes every device only once per line cycle and through increasing the number of levels it produces a multistep staircase voltage waveform which imminent on a pure sinusoidal output voltage. Its structure comprised of a cascade connection with several single-phase, full-bridge Inverter units and every bridge is suckled with individual DC source. Hence the inverter needs neither voltage balance circuits nor voltage matching of the switching devices.

In general, "switched mode" is handled by the power electronic converters where the switches in the converter are in either on or off states. Excluding the transition from conducting to non-conducting, the process in the linear region suffers with loss of efficiency as well as an agonizing rise in switch power dissipation. Hence the switches replace among these two states in order to switch the flow of power in the converter. When the inductors and capacitors at the input and output nodes of the converter average or filter the switched signal, the switch get altered. Therefore, the switched component is decreased and also the expected dc or low frequency ac component is reserved which is known as Pulse Width Modulation, since the desired average value is controlled by modulating the width of the pulses.

In case of an alternative application, the pulse number may be low is in converters that described as amplifiers and upper output threshold frequency may be relatively high. In these cases, these low pulse numbers residence the largest difficulties on effective modulation in order to lessen the alteration as possible. The state of the art of multilevel inverters have acknowledged more attention for their ability on high-power and medium voltage operation and because of other advantages such as high power quality, lower order harmonics, lower switching losses, and better electromagnetic interference. With a number of dc voltage sources as the input and with a suitable procedure of the power-semiconductor-based devices, a stepped voltage waveform is produced by the inverter. The structure of the proposed cascaded multi-level inverter comprised of diode clamped multilevel inverter, flying capacitor multilevel inverter and cascaded multilevel inverter. The inverter constructed with several single-phase H-bridge inverters which are further differentiated as symmetric and asymmetric groups which built on the magnitude of dc voltage sources. In case of symmetric, all H-bridges have identical dc voltage sources whereas in asymmetric, it is alternate. As we discussed above, the multi-level inverter generate output voltage waveform having better harmonic profile and lower total harmonic distortion (THD).

Various methods and approaches are proposed to resolve the issue for achieving a desired output by increase the number of levels without a substantial upsurge in the number of circuit's components. To increase the number of levels, multilevel DC connection including a single-phase full-bridge inverter has also been proposed as an alternative way while the amount of DC sources can be abridged and the topologies use huge capacitor banks which make them repellent. Since the three-level structure of the diode-clamped inverter is not cost effective, it is widely used in every industrial application. A single-phase inverter is used for domestic or low-power a application which has power range less than a kW. The output voltage waveform in the harmonic reduction is either deprived of growing switching frequency or lessening the inverter power output is a significant advantage of multilevel inverters.

Nowadays, the traditional approach dc power distribution system (DC PDS) is incapable to meet the demands of more conversion stages, low efficiency and poor transient response where the upcoming electronic devices such as computer, telecom, electric vehicle, and other similar areas require the power supply with low voltage and high current. Hence, an alternative strategy named High frequency ac power distribution system (HFAC PDS) is introduced which has advantages like fewer conversion stages, higher efficiency, faster response, high power density, distributed heat profile and potential aimed at connector-less power transfer. But this method has

shortcoming about the huge requirement of insulated gate bipolar transistors (IGBTs) as well as huge bidirectional power switches. To overcome this drawback, an asymmetric topology has been existed that face the draw backs such as increase in the number of IGBTs in bidirectional power switches result as cost effective. In some other topology, three algorithms have been offered that shrink the number of required power switches however increase the variety of dc voltage sources.

In order to evaluate the magnitudes of dc voltage sources for the conventional cascaded multilevel inverter, several algorithms have been presented. The major advantage of this topology is to produce a substantial number output voltage levels with low number of dc voltage sources and power switches then its short comings is the high variety in the magnitude of dc voltage sources. Alternatively we proposed cascaded multilevel inverter which has huge advantages such amplified number of output voltage levels, shrink the number of power switches, driver circuits, and also cost of the inverter. In this proposed topology, the unidirectional power switches are used and a new algorithm is introduced to control the magnitude of the dc voltage sources. Moreover, the proposed topology is compared with other topologies from different points of view such as the number of IGBTs, number of dc voltage sources, the variety of the values of the dc voltage sources, and the value of the blocking voltages per switch.

In traditional MLIs, it consists of neutral-point-clamped (NPC) inverter, flying-capacitor (FC) inverter and cascade H-Bridge (CHB) inverter. Here, the NPC utilize diode and FC inverters capacitors in order to clamp the voltage levels whereas more levels can be acquired by means of increasing the number of power devices. The circuit configurations and controls of these inverters is complex with the increasing number of voltage levels. On the other hand, the CHB inverter upsurges the output voltage levels and shortens the modulation through the combination of H-bridge cells. Yet, the number of power devices and input dc sources multiplies in case where the outputting more voltage levels. Several simplified topologies have been proposed in recently years to overcome the shortcomings of the traditional ones. However, they have the common disadvantage that symmetric or asymmetric dc inputs are needed. A single phase grid-connected inverter was proposed. However, the limited five output levels will lead to more output harmonics. A seven-level PWM inverter was proposed, where three capacitors are connected in series and then paralleled with the dc source to achieve redundant ±1/3 V_{dc} and ±2/3 V_{dc} voltage levels. Though, the capacitors voltages are in unbalancing conditions, the control complexity get increasing. Temporarily, both topologies and the multicarrier modulation method are assumed to decline the THD of the staircase outputs. A grid-connected converter topology was proposed are comprised with a single voltage source, a flying capacitor and eight switches. It can output nine levels exactly when the HF modulation strategy keeps the capacitor voltage at a desired level such as 1/3Vdc, which is indeed difficult to be realized without any auxiliary charging circuit, and the literature merely presents the experimental results from a seven-level prototype. High Frequency (HF) modulation has restricted the proposed topology for only low frequency (LF) occasions. Based on switched-capacitor (SC) techniques, a series of step-up multilevel topologies was presented. However, the power switches in the backend H-bridges tolerate the abruptly cumulative voltage levels from the SC frontends, and particularly high voltage stress has restricted their applicability to low input occasions only.

2. Literature survey

Owing to outstanding merits, High frequency alternating current (HFAC) has previously been applied in many power distribution systems [1]. The regulation of the flow of current for high frequency resonant inverter which constructed in parallel connection is more intricate than the low frequency complement. Approaches from topology, modulation, and control perspectives have already been proposed; though, most of them are problematic to bring about the synchronization of magnitude and phase in high frequency circumstance concurrently. The amalgamated PSM in steady state eliminates the modulation coupling between magnitude and phase completely. Therefore, the controllers of magnitude and phase can be independently proficient without any interactions. The scale of unified PSM is determined by zero voltage switching and total harmonic distortion of the resonant inverter. A multilevel inverter that has

been theorized to constraint the component count, especially for maximum number of output levels [2]. It also embraces floating input dc sources consecutively connected in opposite polarities with each other via power switches. Every input dc level seems in the stepped load voltage separately or in preservative combinations with other input levels. This work requires reduced number of power switches as compared to classical topologies.

A new single-phase cascaded multilevel inverter consist of a series connection of the proposed basic unit and only positive levels at the output is possible [3]. In order to achieve also negative outputs, H-bridge is included to the proposed inverter which is known as developed cascaded multilevel inverter. The space for installation and cost of the inverter are controlled. The comparison of the conventional cascaded multilevel inverters with the proposed cascaded topology results with these topographies. Besides, the ability of the proposed inverter to generate all voltage levels (even and odd) is reconfirmed by using the experimental results of a 15-level inverter. Alternatively, a new general cascaded multilevel inverter using developed H-bridges is proposed [4]. The proposed topology requires a small amount of dc voltage sources and power switches.it consists of lower blocking voltage on switches, which results in decreased complexity and total cost of the inverter. These abilities obtained within comparing the proposed topology with the conventional topologies from aforementioned points of view. Moreover, a new algorithm to determine the magnitude of dc voltage sources is proposed. The performance and functional accuracy of the proposed topology using the new algorithm in generating all voltage levels for a 31-level inverter are confirmed by simulation and experimental results.

A new cascaded multilevel inverter is proposed which run with two different algorithms to determine the magnitude of the dc voltage sources are presented [5].To generate maximum numbers of output voltage levels by using a constant number of power switches and/or dc voltage sources, several optimum structures of the inverter are obtained. In comparison with the conservative cascaded multilevel inverters, the presented inverter is able to generate a high number of output voltage levels by using a lower number of power electronic devices such as power switches, driver circuits, power diodes, and dc voltage sources. Conventionally, a new topology for asymmetrical cascaded multilevel inverter consists of series connection of several basic units [6]. Reduction of number of power switches, driver circuits, IGBTs and dc voltage sources are some advantages of the proposed topology in comparison with the conventional cascaded multilevel inverters. As a consequence, to produce whole output voltage levels, a new algorithm to control the magnitudes of dc voltage sources is presented.

In low-power renewable systems [7], a single-phase grid-connected converter is implemented. An appraisal of modern topologies and a theoretical power loss comparison with the proposed solution is realized. The converter architecture is based on a full-bridge topology with two additional power switches and two diodes linked to the midpoint of the dc link. The two added levels are acquired by the discharge of the two capacitors of the dc link, the balancing of the midpoint voltage is obtained with a specific pulse width modulation (PWM) strategy. An operative circuit configuration of a multilevel inverter which increase the number of output voltage levels with a reduced number of circuit components is illustrated in [8]. This seven-level pulse width-modulation inverter comprises a single dc voltage source with a series of capacitors, diodes, active switches for developing output voltage levels, and an H-bridge cell. Subsequently, computer-aided simulations and experiments are carried out to verify the validity of the approach. The work introduces a modified switching strategy to solve the capacitor voltage unbalancing that occurs in series-connected capacitors.

In the work of [9], the paper presents a single-phase transformer less grid-connected photovoltaic converter based on two cascaded full bridges with different dc-link voltages. The converter develops up to nine voltage levels with a single dc bus, since one of the full bridges is supplied by a flying capacitor. The multilevel output reduces harmonic distortion and electromagnetic interference. A suitable switching strategy is employed to regulate the flying-capacitor voltage, improve the efficiency (most devices switch at the grid frequency), and minimize the common-mode leakage current with the help of a novel dedicated circuit (transient circuit). The increase of transmission

frequency reveals more merits than low- or medium-frequency distribution among different kinds of power applications. High-frequency inverter serves as source side in high-frequency ac (HFAC) power distribution system (PDS) [10]. Though, it is difficult to acquire a high-frequency inverter with both simple circuit topology and straightforward modulation strategy. A novel switched-capacitor-based cascaded multilevel inverter is detailed in this paper, and it is built by a switched-capacitor frontend and H-Bridge backend. Through the conversion of series and parallel connections, the switched-capacitor frontend increases the number of voltage levels. The output harmonics and the component counter can be significantly reduced by the increasing number of voltage levels.

3. Proposed method

3.1. Block Diagram

A solar cell is usually consisting of a P-N junction semiconductor which generates currents with the help of photovoltaic effect. The construction of Photo Voltaic (PV) arrays are done by connecting numerous solar cells in series and in parallel. A PV cell is usually a diode of a large-area forward bias and the input voltage is suckled by a photo voltage. Due to minimum voltage than the single-phase voltage to drive the Induction Motor in the PV arrays, dc–dc boost converter was required which is a power electronic circuit gives the output voltage better than the input voltage. The application of the boost converter is to increase the input voltage of the inverter interjected among the PV array and Nine-Level Inverter. The block diagrams of the single-phase PV fed nine-level inverter which drive an induction motor are exposed in Fig. 4.2.

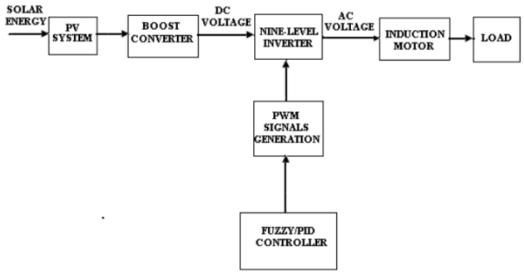

Figure 1. Block Diagram of the Overall System

In general, the single pulse width modulation control possesses a single pulse per half cycle whereas the output voltage (rms) is improved by alteration of pulse width. In the inverter, in contrast with the rectangular control signal of amplitude V_c along with triangular carrier signal V_{car}, the gating signals are produced. Filters is mainly used to drive the loads in inverter which convert the inverter output (i.e., square wave) into pure sinusoidal wave. The principle of Induction is the electro-magnetic field is induced into the rotor when rotating magnetic field of stator cuts the stationary rotor. The application of a PID controller/fuzzy controller is to control speed, temperature, flow, pressure and other process variables. A nine-level inverter topology for medium-voltage Induction motor is usually drive with open-end stator winding.

3.2. Multilevel Inverter Topology

A single phase nine-inverter includes a single-phase conventional H-bridge inverter, three bidirectional switches, and a capacitor voltage divider which formed by the capacitors C_1, C_2, C_3 and C_4, as depicted in Figure 2. The H-bridge topology of the proposed work has substantial expedient over other topologies such as less power switch, power diodes, and a smaller amount of capacitor for inverters of the similar number of levels. In this work, Photovoltaic (PV) arrays were connected with the inverter with the help of a dc–dc boost converter. Then, the output power produced by the inverter is delivered to induction Motor.

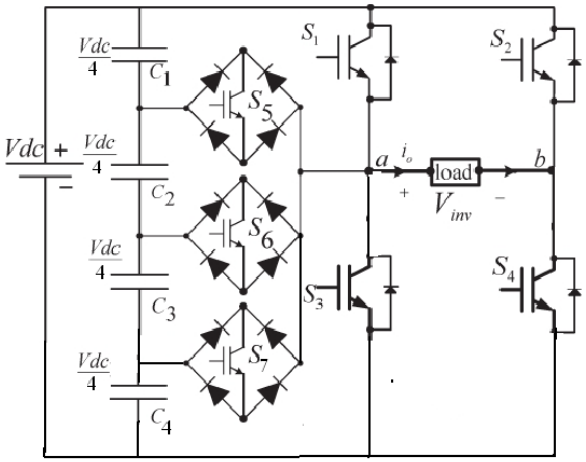

Figure 2. Single-Phase Nine-Level Inverter

The single-phase nine-level inverter is implemented using the seven-level inverter as shown in Figure 2. Due to the PV arrays had a voltage that

was lower than the single-phase voltage; the dc–dc boost converter was needed. High dc bus voltages are obligatory in order to safeguard that flow of power from the PV arrays to the single-phase induction motor. To acquire pure sine-wave, LC-filter is molded and it is also used to drive a single-phase induction motor. Proper switching of the inverter generate nine output-voltage-levels (V_{dc}, $3V_{dc}$ /4, V_{dc}/2, V_{dc} /4, 0,,– V_{dc} /4, $-V_{dc}$/2, -$3V_{dc}$/4, -V_{dc}) from the dc supply voltage. The proposed inverter's operation can be classified into nine switching states. The vital nine levels of output voltage were made as follows.

Maximum positive output (V_{dc}): *S1* is ON, where the load positive terminals linked to V_{dc}, and *S4* is ON, when the load negative terminal is connected to ground. All other controlled switches are OFF; the voltage applied to the load terminals is V_{dc}.

Three-fourth positive output (3 V_{dc} /4):In this level, the bidirectional switch *S5* is ON, when the load positive terminal is connected and *S4* is ON, which link the load negative terminal with ground. Other controlled switches are OFF where 3 V_{dc} /4 voltage fed to the load terminals.

Half of the positive output (V_{dc}/2). Meanwhile, the bidirectional switch *S6* is ON, linking with the load positive terminal, and *S4* is ON, which connect the load negative terminal with ground. All other controlled switches are OFF; the voltage applied to the load terminals is V_{dc} /2.

One-fourth of the positive output (V_{dc} /4): The bidirectional switch *S7* is ON, connecting the load positive terminal, and *S4* is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is V_{dc}/4.

Zero output: This level can be produced by two switching combinations; switches *S3* and *S4* are ON, or *S1* and*S2* are ON, and all other controlled switches are OFF; terminal *ab* is a short circuit, and the voltage applied to the load terminals is zero.

One-fourth negative output ($-V_{dc}$ /4):At this level, the bidirectional switch *S5* is ON where the load positive terminal is linked and *S2* is ON, the load negative terminal is linked to V_{dc} whereas the other controlled switches are OFF; $-V_{dc}$/4 voltage is given to the load terminals.

Half of the negative output ($-V_{dc}$/2): The bidirectional switch *S6* is ON, connecting the load positive terminal, and *S2* is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the applied voltage to the load terminals is $-V_{dc}$/2.

Three-fourth negative output ($-3V_{dc}$/4): The bidirectional switch *S7* is ON which connect the load positive terminal, and *S2* is ON that linked the load negative terminal to ground. The other controlled switches are OFF; here, the applied voltage to the load terminals is $-3\ V_{dc}$/4.

Maximum negative output ($-V_{dc}$): In this level, the switch *S2* is ON, relating the load negative terminal to V_{dc}, and *S3* is ON, the load positive terminal is connected to ground whereas the other controlled switches are OFF; the applied voltage to the load terminals is $-V_{dc}$.

Table 1 describes the combinations of switches producing nine output-voltage levels (V_{dc}, $3V_{dc}$ /4, V_{dc}/2, V_{dc} /4, 0,,– V_{dc} /4, $-V_{dc}$/2, -$3V_{dc}$/4, -V_{dc}).

Table 1. Output Voltage According to the Switches On Off Condition

V_0	S_1	S_2	S_3	S_4	S_5	S_6	S_7
V_{dc}	on	off	off	on	off	off	off
$3V_{dc}/4$	off	off	off	on	on	off	off
$V_{dc}/2$	off	off	off	on	off	on	off
$V_{dc}/4$	off	off	off	on	off	off	on
0	on	on	off	off	off	off	off
$-V_{dc}/4$	off	on	off	off	on	off	off
$-V_{dc}/2$	off	on	off	off	off	on	off
$-3V_{dc}/4$	off	on	off	off	off	off	on
$-V_{dc}$	off	on	on	off	off	off	off

3.3. MPPT Control of the System

In PV system, the recurrent nature of their energy source is an intrinsic drawback of PV system. Though the solar energy is extant all over the day time, the levels of solar irradiation differ with sun intensity and unpredictable shadows cast by clouds, birds, trees, etc. It results with the incompetent result for renewable system. The transfer power of system is enhanced by using maximum power point tracking (MPPT) algorithms.

A solar cell is comprised of a P-N junction semiconductor that produces currents via the photovoltaic effect. PV arrays are constructed by placing numerous solar cells connected in series and in parallel. A PV cell is a diode of a large-area forward bias with a photo voltage and the equivalent circuit is shown. The current voltage characteristic of a solar cell is derived in as follows.--

$$I = I_{ph} - I_D \tag{1}$$

$$I = I_{ph} - I_0 exp\left[\frac{q(V+R_s i)}{AK_B T} - 1\right] - \frac{V+R_s i}{R_{sh}} \tag{2}$$

Where I_{ph} = photo current, I_D = diode current, I_0= saturation current, A = ideality factor, q = electronic charge $1.6x10^{-19}$, kB = Boltzmann's gas constant (1.38x10-23), T = cell temperature, R_s = series resistance, R_{sh} = shunt resistance, I = cell current, V = cell voltage.

The shunt resistance (R_{sh}) is usually very high whereas the series resistance (R_s) is very trivial. Consequently, to simplify the solar cell model, both the resistances are ignored.

$$I = I_{ph} - I_0\left[exp\left(\frac{qV}{kT}\right) - 1\right] \tag{3}$$

The maximum power from the array can be drawn by adjusting the output current (or voltage) of the PV array. Due to the similarities of the shape of the wind and PV array power curves, a similar maximum power point tracking scheme known the standard perturb and observe method is often applied to these energy sources to extract maximum power.

PV system detects method for the consistent agitates. This affect the operating system and find the output. When the perturbation has a positive change results in the output power, the control algorithm will linger with preceding perturbation. Contrariwise, if output power detects a negative change, then the control algorithm will reverse the direction of the preceding perturbation step. If the power change in is seems to be close to zero (within a specified range) then no changes is acquired to the system operating point meanwhile it resembles to the maximum power point (the peak of the power curves).

3.4. DC-DC Boost Converter Model

The dc–dc boost converter is modeled to initiate the Induction Motor since the PV system arrays possess lesser voltage than the single-phase voltage. Boost converter is usually a power electronic circuit that delivers the output voltage superior than the input voltage. The converter comprised of components such as dc input voltage source *Vs*, boost inductor *L*, controlled switch *S*, diode *D*, filter capacitor *C*, and load resistance *R*.

By Faraday's law for the boost inductor,

$$V_s\, DT = (V_0 - V_s)/(1 - D)T \tag{4}$$

from which the dc voltage transfer function turns out to be

$$M_v = \frac{V_0}{V_s} = \frac{1}{1-D} \tag{5}$$

Consequently, the desired greater output is achieved by this convertor than the input voltage .The boost converter works in the CCM for L >Lb where

$$L_b = \frac{(1-D)^2 DR}{2f} \tag{6}$$

Where *d* represents the duty ratio of dc to dc converter. In general, a duty ratio is termed as the ratio of turn on time to that of total time. The boost converter enhances the voltage from PV array to the required value formerly nurturing to the Nine-Level Inverter system. LC-filter is used as a second order filter and it has better filtering ability than L-filter. This humble design of the configuration is easy to design and to works without any difficulties.

3.5. Modeling of LC-Filter

In filter designing, initially the best filter which comforts the structure and the operation process has to be determined. Then the designed impedance (R_d)is evaluated from the lowest voltage (V_{min}) divided by the highest current (I_{max}). Finally, the inductor (L) and the capacitor (C) values are equated from the previous step by following equation. The design impedance (R_d) is determined by,

$$R_d = \frac{V_{min}}{I_{max}} \quad (7)$$

The inductance (L) and the capacitance (C) values of the filter can be calculated by

$$L = \frac{Rd}{2\pi f} \quad (8)$$

$$C = \frac{1}{2\pi f Rd} \quad (9)$$

3.6. Control system

The control system of the proposed work consists of MPPT algorithm, a dc-bus voltage controller, reference-current generation, and a current controller. Maximization of the energy transmitted from the PV arrays to the grid, and in the presence of grid voltage harmonics, generation of a sinusoidal current with minimum harmonic distortion are the major work done by the control system.

The proposed inverter used the perturb-and-observe (P&O) algorithm owing to its simple structure and prerequisite of small measured parameters intended for its wide usage in MPPT. The algorithm periodically perturbs (i.e., increment or decrement) the array terminal voltage and compares the PV output power with prior perturbation cycle. If the power was seem to be increasing gradually, the perturbation would continue in the same direction in the subsequent cycle; else, the direction would be overturned. Thus the array terminal voltage is perturbed by every MPPT cycle; when the MPP is reached, the P&O algorithm will oscillate around it.

In this work, the P&O algorithm was applied in the dc–dc boost converter. The duty-cycle function is the output of the MPPT. For instance, the dc-link voltage V_{dc} was meticulous in the dc–ac seven level PWM inverter, then the variation of the duty cycle deviates the voltage at the output of the PV panels. A PID controller was employed to preserve the output voltage of the dc–dc boost converter (V_{dc}) constant by linking V_{dc} and V_{dcref} and suckling the error into the PID controller that subsequently tries to decrease the error. As follows, the V_{dc} can be preserved at a constant value and at more than $\sqrt{2}$ of V_{grid} to inject power into the grid.

The frequency and phase of the PV inverter must equal in order to distribute energy to the grid; therefore, a grid synchronization method is needed. The sine lookup table produce reference current must be brought into phase with the grid voltage (V_{grid}). In this case, the grid period and phase must be noticed. The proposed inverter delivers an analog zero-crossing detection circuit on any one of its input ports where the grid voltage is to be connected. The zero-crossing circuit generates an in-phase square-wave output that fed into the digital I/O port on eZdsp board TMS320F2812.

In many applications, PI algorithm was considered as the feedback current controller. The current introduced the grid called as grid current I_{grid}, was identified and fed back to a comparator which compared it with the reference current $I_{gridref}$. $I_{gridref}$ is the result of the MPPT algorithm. The inaccuracy from the contrast procedure of I_{grid} and $I_{gridref}$ was fed into the PI controller. The output of the PI controller is represented by V_{ref}, drives over an anti -windup process afore being associated with the triangular wave in order to deliver the switching signals for S_1–S_6. Finally, V_{ref} converts into V_{ref1}; V_{ref2} and V_{ref3}which can be derived from V_{ref1} by means of shifting the offset value corresponding to the generosity of the triangular wave.

4. Results and discussions

The performance of the multilevel inverter corroborated by designing with the source modeling in MATLAB /Simulink, and the experimental waveforms are acquired. Moreover, the performance of the inverter is deliberated under steady state condition and validated with the models to their efficiency conditions.

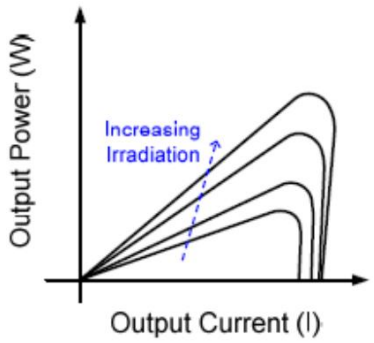

Figure 3. PV cell power characteristics

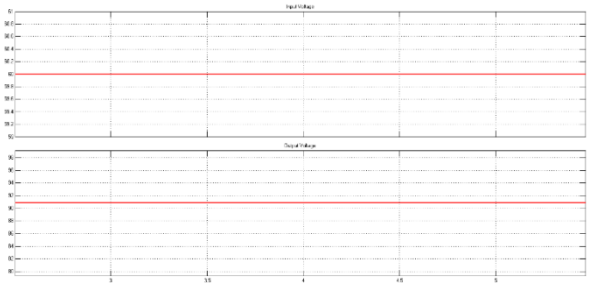

Figure 4. the Input and the Output RMS voltage of the nine level inverter.

Where the Y axis as Voltage and the X-axis as Time.

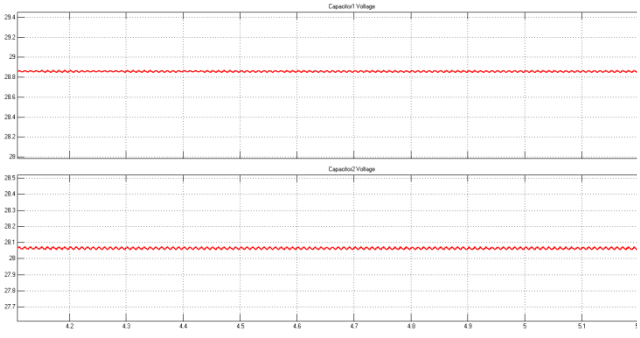

Figure 5. simulation results of the two capacitors voltages.

From the Figure 5, it is clear that both capacitorspossess similar variations in alternate voltages.

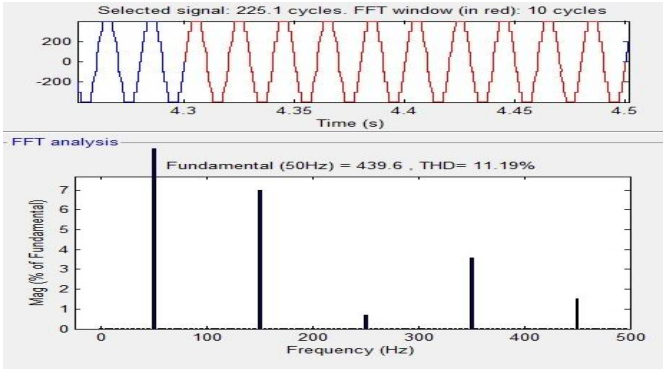

Figure 6. Total harmonic distortion of nine level output voltage.

The Total Harmonic Distortion of the output voltage is 11.9%.

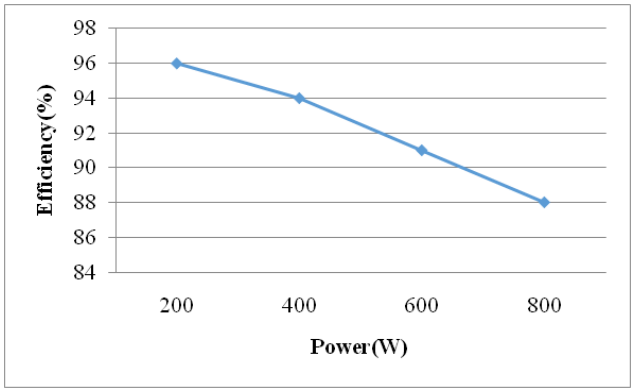

Figure 7. Power Vs. efficiency waveform

As a consequence, the performance of the nine-level inverter has greatly enhanced by lessening switch count which includes a single-phase conventional H-bridge inverter, three bi-directional switches, and a capacitor voltage divider molded by C1, C2, C3,and C4. The proposed H-bridge topology is significantly advantageous over other traditional approaches having less power switch, power diodes, and less capacitor for inverters of the similar number levels.

Table 2. Existing Vs. Proposed Comparison

	Existing	Proposed
Number of switches	9	7
Level	9	9

Efficiency	94%	98%
THD	11.9%	11.19%

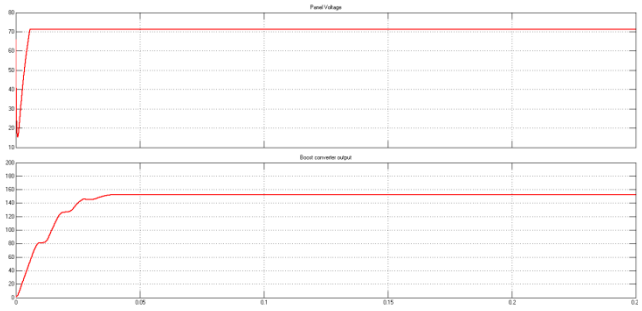

Figure 8. Panel voltage and boost converter output voltage

The voltage produced by the panel is about 70 V whichimprovedupto150V.

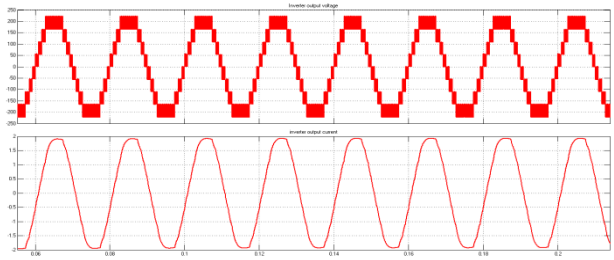

Figure 9. nine level inverter output voltage and current

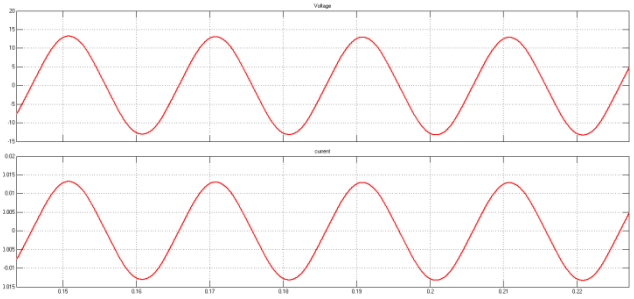

Figure 10. Filtered voltage and current

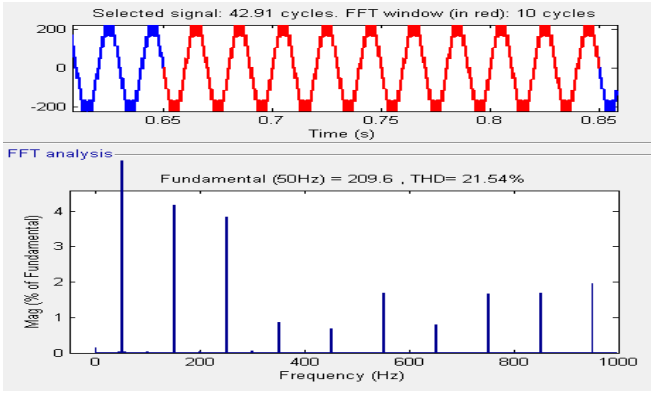

Figure 11. Total Harmonic Distortion with RL load

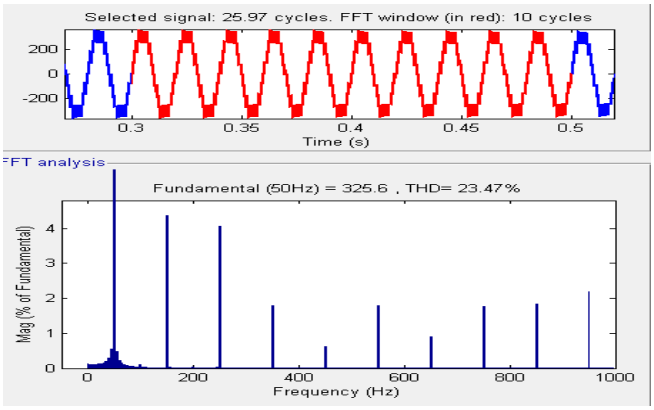

Figure 12. Total Harmonic Distortion with motor load

5. Conclusion

Any number of levels develops the basic topologies at the output where the 31-level, 127-level, and general topologies which are consequently obtainable. Moreover, a new algorithm is designed to define the magnitude of the dc voltage sources. The proposed general topology was compared with the different kinds of illustrated topologies in literature from various points of view. The comparison of results deliberatesthat the proposed work needs a trivial amount of IGBTs, power diodes, driver circuits, and dc voltage sources. Likewise, the magnitude of the blocking voltage of the switches is inferior to that of conventional methods. The nine-level inverter has a maximumnumber of selection of dc voltage sources in contrast with other topologies. The accuracy of the performance estimated over the MATLAB simulation.

6. Future scope

In general, the inverter requires a constant dc voltage to preserve the output voltage level of the inverter. The proposed work deals with procurement the binary, trinary and the modular multilevel inverters, with a solar interface and yields a high output voltage levels which are not satisfactory in all inverters. Therefore a study of the voltage regulation is obligatory. Furthermore, the terminal voltage of the solar panel is expected to be altering best owing to the solar irradiance. As a consequence, generating a constant voltage out of the solar and extraction of the maximum power output from the solar is described as the extension of this work.

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