ANALYSIS OF STANDBY LEAKAGE POWER REDUCTION BY V BODY CONTROL SYSTEM FOR CORE DEVICES

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Abstract*: In current technology of Very large scale Integration (VLSI) has many advancement and support high performance computing, core devices and consumer electronics. The introduced new VLSI technology reduces size of transistor, results in powerful and compact wireless devices. The Control of leakage power consumption is a major difficulty one which faced in technology of CMOS circuit design and implementation, especially in handheld devices like cellular phones and PDA's. Miniaturized electronics have the leakage current in the active and standby mode due to sub threshold leakage that causes the high power dissipation. There are several works have been carried out to achieve low power consumption in CMOS VLSI circuits. In order to resolve this problem, proposed research work introduced a V_{body} control system based on the Sleepy Lector concept to reduce standby leakage power of CMOS that generates an optimal reverse body-bias voltage from leakage monitoring circuit. In addition to, V_{body} control system that comprises of several clocking algorithms and techniques like Clock Gating (CG), Energy Recovery Clock (ERC), and Clock enable Sleepy Lector and Clock boosting Sleepy Lector. Sleepy Lector reduces leakage current by introducing sleep transistors and leakage controlled transistor (LCT). Energy recovery circuit controls current flow by setting low voltage drop across the device. Clock gating offers reduction of clock power. The proposed optimal V_{body} control systems are implemented and simulated in HSPICE using 32nm N-MOSFET technology. The results are evaluated using ISCAS85 benchmark circuits for two different operating temperatures 25°C and 100°C. The results obtained with these implementations are compared to analyze for better performance. The maximum reduction in leakage power consumption of the proposed methods CESL, CGSL, CBSL and ERCSL from the existing work, are 92.33%, 99.41%, 99.70% and 99.93% respectively.*

Keywords: *Standby leakage power, Sleepy Lector, V_{body} control system, Power consumption, Core Devices, Electronics devices*

I. INTRODUCTION

Advanced technologies such as remote sensing areas, military, surveillance, bio-medical field and portable devices that are requires low power consuming circuits. Therefore, low-power design of VLSI design is necessary for current and future wireless communication devices. The marketing and usage of mobile hand-held devices are ever increasing all over the world today. Since battery life time is backbone of such devices. The portable mobile communication devices like notebook computers, hearing aids, personal communication devices (like mobiles, PDA's and pocket Pc's) which require less power requirements. Unfortunately, degrading of speed of designed circuits increases the level of power consumption. And also thermal issues are another problematic one in electronic system design, which affects system performance, density, reliability, power consumption and cost. Generally, the overall life time of a VLSI system evaluated as how much amount of power will be consumed by it. In the evolution of integrated circuits the size of the transistor is reduced by introducing novel technologies. In VLSI circuits, the speed and component density per chip increase with the reduction of supply voltage to reduce power consumption. The Modeling and CMOS transistor structure which mainly depends on Leakage power. It also CMOS behavior that depends on oxide thickness, channel length doping level and profile. These will further suppress the different kinds of leakage current such as gate oxide tunneling, sub-threshold leakage and reverse bias junction.

Conventionally, the expression for power (P) estimation1 is given by following equation as

$$\mathbf{P} = \frac{\mathbf{1}}{\mathbf{t}} \int \mathbf{i}\, \mathbf{dt} \quad \text{---------- (1)}$$

Where P= Amount of leakage power in watts, t= Time, i= Amount of leakage current

Standby leakage power is a crucial factor that desires the circuit performance, especially in nanometer regime technology. Leakage power in standby mode is high compared to active mode. The power dissipation of CMOS technology can be divided into three components,

- Static Power Dissipation (S.P.D)
- Dynamic Power Dissipation (D.P.D)
- Short Circuit Power Dissipation (Sc.P.D)

Thus the total power dissipation (P.D) is given by

$$\mathbf{P.D = S.P.D + D.P.D + Sc.P.D} \quad \text{----- (2)}$$

i. Static Power Dissipation (S.P.D)

When the circuit is undergoes in idle mode owing to different kind of leakage current that will flow from either source to drain or gate to substrate is called Static power consumption (S.P.D). This will degrades the battery life-time, additional cooling arrangements and packaging cost. The major contribution for static power dissipation is reverse bias between the diffusion region and substrate of the CMOS transistor. S.P.D is normally expressed as a product of leakage current and supply voltage.

ii. Dynamic Power Dissipation (D.P.D)

Another one is Dynamic power dissipation which is caused due to charging and discharging of capacitances at the output side. It can be reduced by reducing load capacitor or rail voltage (V_{dd}).

iii. Short Circuit Power Dissipation (Sc.P.D)

And third one is the Short circuit power dissipation is mainly due to to the conducting path between rail voltage (V_{dd}) and ground.

The above three major leakage current are the main sources of power consumption during CMOS circuit design and implementation. This will incorporates that as increasing knowledge of CMOS technology, total power consumption is degraded. With the technology improvement, the sub-threshold leakage, gate-oxide tunneling and reverse bias junction mainly affect power dissipation. Scaling of gate oxide thickness increases gate oxide tunneling current and increases sub-threshold current by disturbing threshold voltage [1-3]. The FIGURE 1 and FIGURE 2 show how leakage and dynamic power dissipation increases with the reduction of size of the components and gate length.

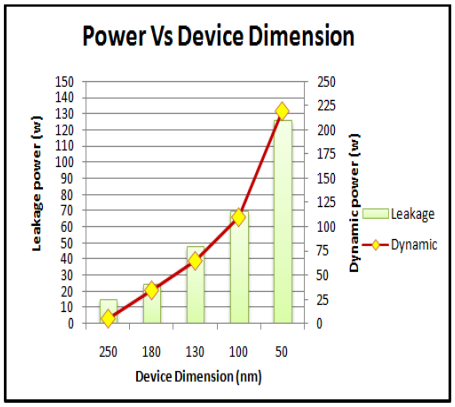


FIGURE1. Power Vs Component size (nm)

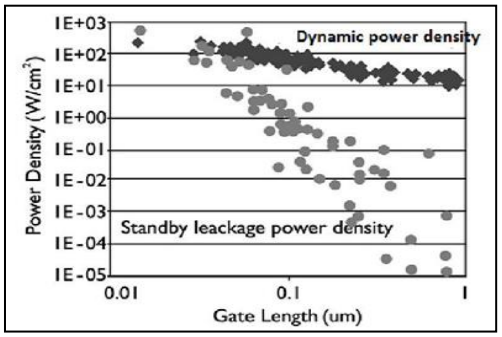


FIGURE2.Power density Vs Gate length (µm)

Now, discuss proposed sleep lector concept in detail. In sleep mode approach, a PMOS transistor is inserted between pull up network and V_{dd} and an NMOS transistor is inserted between pull down network and ground. It reduces leakage current by restricting the supply voltage to flow from V_{dd} to ground [5]. In Lector approach, two leakage controlled transistors (PMOS and NMOS) are inserted between pull up and pull down network. In this connection, the gate of one transistor is controlled by the source of another transistor, to reduce leakage current by increasing

path resistance between supply and ground [6]. If sleep transistor disable or cut from the power supply source which from main circuit and result will degrades leakage current efficiently, but output logic is not obtained properly and desired. With additionally, extra hardware must be required for sleep signal enable, this will increasing area needed for the circuit implementation. In lector approach, main idea is the value of path resistance from ground to supply is increasing which leads to reduction of leakage current in the circuit. However, it works properly in standby mode, but partial output will be obtained only.

Another technology to reduce power dissipation is employing energy recovery circuits which control the current through components with low voltage drop and salvages the stored energy of the capacitor by utilizing AC supply voltage [7, 8]. Energy recovery clocking is an operative method for achieving low power as the major fraction of total power in a highly synchronous system is dissipated on the clock network [9]. In energy recovery clocking system, the clock recovers energy from clock network
capacitances to supply voltage. In energy recovery clocking small amount of energy is lost on flip-flops due to non-adiabatic switching. To reduce the flip-flop power in idle mode, clock gating can be applied to the energy recovery clock. This can be done by masking the local clock signals through masking logic gates (NAND/NOR) [10]. However the clock gating cannot work for energy recovery clocking as masking logic gates removes energy recovery from remaining capacitances in downstream fan-out.

The main objective of this paper is to reduce the standby leakage power of CMOS. An optimal reverse body bias voltage is generated using Sleepy Lector. In addition, the clock power is reduced by employing various clocking circuits like clock enable, clock boosting, energy recovery, clock gating. Thus by employing four different clocking circuits we have designed four configurations for optimal V_{body} control system. They are

- CESL (Clock Enable Sleepy Lector),
- CGSL (Clock gating Sleepy Lector),
- CBSL (Clock Boosting Sleepy Lector) and
- ERCSL (Energy Recovery Clock Sleepy Lector).

Hence, the proposed V_{body} control system can effectively improves leakage power reduction in wireless hand-held devices and also provides longer battery life time. The works related to leakage reduction are discussed in chapter 2. In chapter 3 the theory of reverse body bias is explained. Chapter 4 discusses about the existing work of leakage reduction. In chapter 5, the proposed work is explained and the experimental evaluations are described in chapter 6.

II. RELATED WORKS

The adaptive Reverse Body Biasing method can be used to reduce leakage current **[11-14]**. Still, substantial adjustment must be made in circuit. In those works, all components of leakage current and minimum supply voltage are not taken into account. Hence it is not suitable for VLSI systems. Kim et al identified that both optimal power supply voltage and optimal body bias voltage can be used to reduce leakage power. However they need many circuit overhead. So they proposed a novel technique to reduce standby leakage power for VLSI systems by utilizing body bias voltage only. Here all components of leakage current are considered at the cost hardware components. **Yong et al [15]** proposed novel approach to reduce hardware components by optimizing body bias voltage with reduced efficiency in standby current reduction. In **[16]**, Delay and Power monitoring schemes for reducing power dissipation is proposed. It can be achieved through dynamic control of supply voltage and threshold voltage in active mode and standby mode. In active mode any one of the supply voltage and threshold voltage is controlled based on the results obtained from delay monitoring. Selection of any one voltage is to evade oscillation problems between them, if any. Power monitoring is used to identify optimum body bias by comparing sub threshold current to substrate current. In standby mode the power monitoring accuracy can be enhanced by considering the effects of reducing supply voltage and gate oxide leakage

current. This work found out optimum body bias conditions with an error of less than 20% with respect to actual minimum leakage current on standby mode.

Johnson et al [17] proposed stack insertion technique to reduce leakage reduction. A leakage control transistor is introduced in series with gates having large amount of sub-threshold leakage in non-critical paths. In standby mode, it is switched off. This stacking effect reduces leakage current using single-threshold voltage. High values can be given for threshold voltage, in some transistors in non-critical path, in order to diminish leakage current. Further, desired performance can be attained by using low threshold voltages for transistors in critical path. Thus reduction of power consumption and high performance are attained concurrently **[18]**, **[19]**. Another novel technique for body biasing has been introduced by **kuroda et al** based on Variable threshold CMOS **[20]**. The body bias is controlled by employing a self-substrate bias circuit. Thus various threshold voltages are obtained. The applied voltage for body bias in active mode is almost equal to zero. However greater reverse body bias voltage is applied in standby mode to increase the value of threshold voltage and to the leakage current. It has been implemented in a two dimensional discrete cosine transformer core processor. **Keshavari et al** gave an account on effectiveness of reverse body biasing. They stated that reverse body biasing reduces leakage of

VLSI circuits by three orders of scale in a 0.35 μm technology. However recent studies described that the efficiency of reverse body bias technique reduces with technology scale **[21]**. Dynamic threshold SRAM configuration can be employed to decrease leakage power in memory architectures. Mizuno stated that body biasing can reduce sub-threshold voltage without losing data stability **[22]**. **Jeon et al [23]** had proposed a new optimal reverse body biasing approach that is applied in CMOS circuits in both standby and sleep mode, obtaining a low leakage currents. This can be achieved by applying optimal reverse body bias at substrate terminal which increases threshold value of the transistors. The optimal reverse bias voltage is selected which accomplished by comparing sub-threshold and band to band currents concurrently. Moreover the deviations in temperature and supply voltage are compensated by using an additional feedback loop.

III. PROBLEM STATEMENT AND DEFINITION

As growing global marketing, battery powered portable devices and electronic systems demands circuit design with low power reduction. Large leakage power consumption has been considered as a major challenging task for Electrical and electronics circuit designers. With the technology advancement increases, results in nanometer regime, device density has been also increased. For Internet of things (IOT) application, it is also needed a low power consumed electronic devices. Along with static and dynamic power consumption, standby leakage power consumption is also a key issue during circuit design and implementation. Although, as increasing the number of devices in circuit will increases the system power utilization. Hence, this research paper considers reduction of standby leakage current in electrical and electronic devices. This proposed research work carried out to design a V_{body} control system based on the Sleepy Lector concept to reduce standby leakage power of CMOS. V_{body} control system generates an optimal reverse body-bias voltage from leakage monitoring circuit. Here many approaches for clocking are used, such as Clock Gating (CG), Energy Recovery Clock (ERC), Clock enable Sleepy Lector and Clock boosting Sleepy Lector. The results obtained with these implementations are compared to analyze for better performance.

IV. STANDBY LEAKAGE CURRENT IN REVERSE BODY BIASING

Total leakage current of n-MOSFET in off-state is given as the summation of various leakage currents such as Sub-threshold leakage current (I_{STH}), band-to-band tunneling leakage current (I_{BBT}), gate to drain induced leakage current (I_{GID}), bulk oxide tunneling leakage current in gate terminal (I_{GB}), oxide tunneling leakage current in drain (I_{DG}). I_{BBT} and I_{GID} have two components such as reverse bias between drain to bulk and source to bulk p-n junction leakage currents. Hence, it is expressed as,

$$I_{BTBT} = I_{BBTDB} + I_{BTBTSB}$$ ---------- **(3)** And

$$I_{GID} = I_{GIDDB} + I_{GIDSB}$$ ---------- **(4)**

Then, Total leakage current (I_L) is given by

$$I_L = I_{STH} + I_{BBT} + I_{GID} + I_{GB} + I_{DG}$$ -- **(5)**

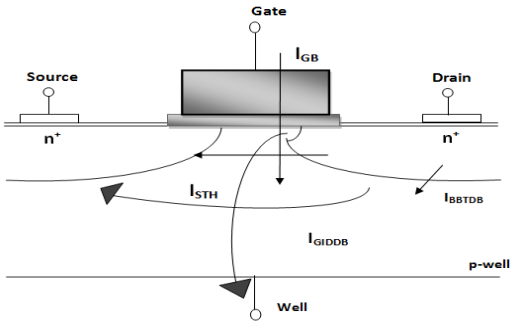


FIGURE3. Standby leakage current of MOSFET

The above FIGURE 3 shows standby leakage current of MOSFET and its operating principle is discussed below in detail. The MOSFET is said to be in off-state when it is working below the threshold voltage, (gate-to-source voltage, (V_{GS}=0). Still a small amount of current passes through the device in off-state which causes significant power dissipation in the device. So it is very essential to select the value for sub-threshold leakage current (I_{STH}). I_{STH} is the weak reverse conduction current and controlled by the diffusion current passing across drain and source when V_{GS} is less than V_{th} **[36]**. The electric field intensity across the depletion region becomes high due to the raise of I_{BBT} caused by heavy doping of Source/drain and substrate region. If this electric field becomes greater than 106 V/cm, the voltage drop across the junction is greater than the silicon band-gap and hence the enormous amount of I_{BBT} passes across substrate junctions **[4]**.

Standby power can be reduced by applying reverse body bias to NMOS and PMOS transistors. The value of optimal reverse body bias does not differ with the chip's logic state. The total standby leakage power is modified to have two components by applying reverse body bias voltage (V_{body}). They are leakage current (I_{dd}) in supply voltage (V_{dd}) pin and leakage currents I_{BP} and I_{BN} passing through NMOS and PMOS body pins correspondingly. The Total standby leakage power (P_{SL}) is given by

$$\mathbf{P_{SL} = V_{dd}\, I_{dd} + \left(V_{dd} + V_{body}\right)I_{BP} + V\_body I_{BN}}$$ ---------- **(6)**

Thus, by applying Reverse body bias voltage, the threshold voltage is increased to reduce sub-threshold leakage current in MOSFET. The Following FIGURE 4 clearly shows the result impact of changes of body bias voltage and supply voltage leakage power in NMOS transistor (32-nm) CMOS technology.

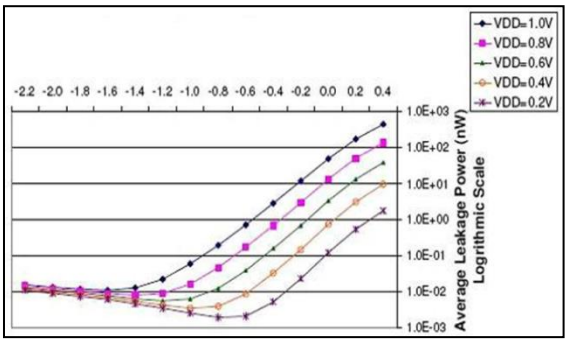


FIGURE4. Result of body bias and supply voltage on NMOS transistor of 32-nm CMOS technology [4]

When the body bias voltage is in the range of -0.8 V to -2.2 V the leakage power increases with increased I_{BBT}. As gate current lightly affects power, an optimal reverse body bias voltage value can exist to have the marginal standby leakage power in a device for each unique supply voltage. Therefore, optimal body bias voltage can be estimated by relationship between I_{STH} and I_{BBT}. The marginal leakage power with respect to optimal V_{body} can be calculated by

$$\frac{\partial PSL}{\partial V_{body}} = 0$$ ---------- **(7)**

There is another factor to adversely affect leakage even at optimal V_{body}, which is gate current. So the supply voltage must be reduced to lessen the gate current, which in turn reduces the value of optimal V_{body} **[4]**.

V. EXISTING V_{body} CONTROL SYSTEM

The band-to-band tunneling current, I_{BBT} increases leakage power when RBB is very large. To overcome this issue, in paper **[23]**, the authors introduced a V_{body} control system to adjust and maintain the optimum body bias voltage with the varying operating states that used to keep balanced

sub-threshold leakage current with BTBT leakage. By adjusting the body bias in RBB direction, results increases threshold voltage and reduces sub-threshold leakage current. The tuning of body voltage is proceed until determining the optimum body bias value, to avoid extreme reverse body bias. The block diagram shown in FIGURE 5 has leakage monitoring circuit, current comparator and charge pump. The optimum body bias voltage is computed by the current comparator circuit. The current mode circuit is employed in this work to manipulate the active signals present in the current domain. This circuit has better sensitivity, high speed and requires less power. Due to the analog circuits in the scheme, the control circuits are not needed. The leakage monitoring circuit which, splits up the total leakage current into sub-threshold leakage current I_{STH} and BTBT leakage current I_{BBT}. The separated leakage components are passed to the current comparator which creates a pulse width according to the magnitude of the leakage components. The current comparator is designed using the current mirrors. The charge pump is either discharging or charging its output capacitor which depends on signals received from current comparator and its self bias voltage level. This circuit gives the optimal body bias voltage to fit the sub-threshold leakage with $I_{BBT.}$ This work mainly focused on minimization of N-MOSFET leakage current by using an N-well P-type substrate technique. The value of body biasing voltage in this work varies from -0.9V to 0V. This sign can be inverted before V_{body} is fed to the substrate.

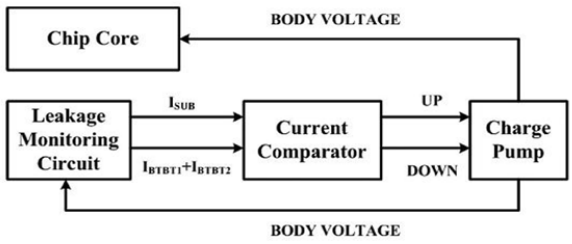


FIGURE5. Existing optimal V_{body} control system [23]

This existing optimal V_{body} control system was implemented and simulated in HSPICE using 32nm technology. The simulation results are evaluated by an effective technique called ISCAS85 benchmark circuits, in addition to results are undergoes at different operating temperature from 25ºC to 100ºC. The experimental evaluations illustrated that the leakage power is reduced about 1491 times. The power consumption of the scheme is very small which is equal to 41µW, with the supply voltage being same as the core power supply. This implementation also proved that the leakage power is very less sensitive for the changes in temperature. Thus the Optimal V_{body} control system can reduce standby power in large with less hardware overhead and minimal power overhead.

V. PROPOSED V_{body} CONTROL SYSTEM

As the leakage monitoring of the existing optimal V_{body} control system has many transistors, we proposed a modified optimal V_{body} control system by employing Sleepy Lector concept for leakage monitoring. The clock pulse for the transistors of Sleepy Lector circuit is generated by using four different clocking schemes, namely clock gating, Energy recovery clock, clock enable, clock boosting. The purpose of implementing various clocking scheme is to reduce the power consumption. The aim of these clock generating circuits is to reduce power consumption in MOSFETs. The block diagram of V_{body} control system using CESL, CGSL, CBSL, and ERCSL are given in following figures. The theory behind the various techniques implemented in the proposed work is described in the subsequent sections.

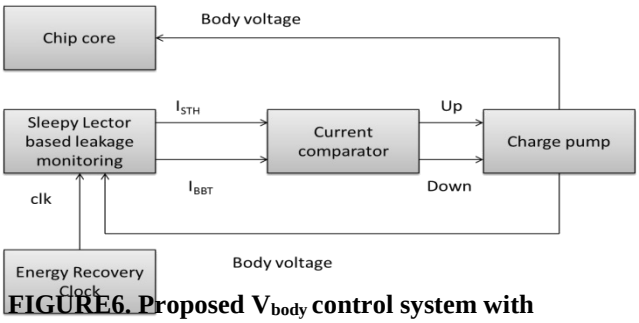


FIGURE6. Proposed V_{body} control system with CESL

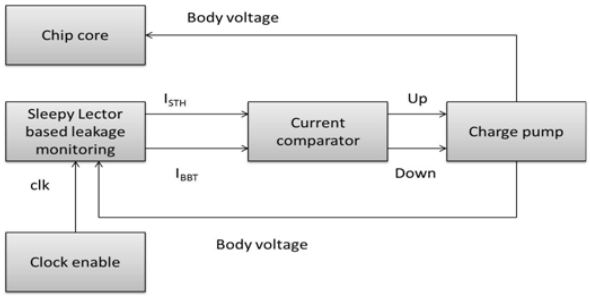


FIGURE7. Proposed V_{body} control system with CGSL

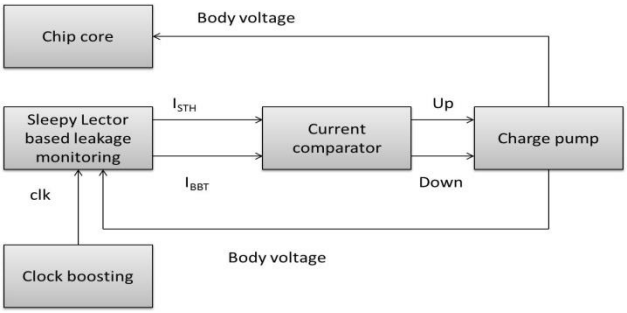


FIGURE8. Proposed V_{body} control system with CBSL

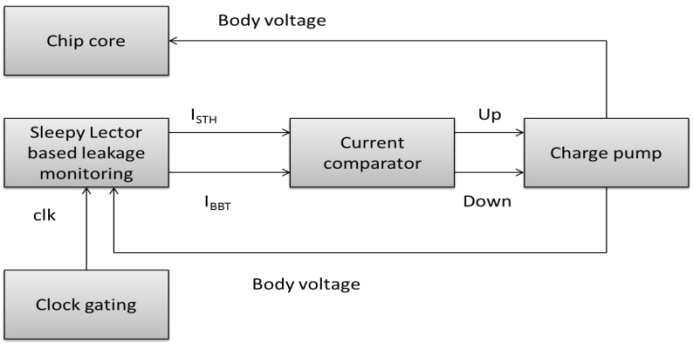
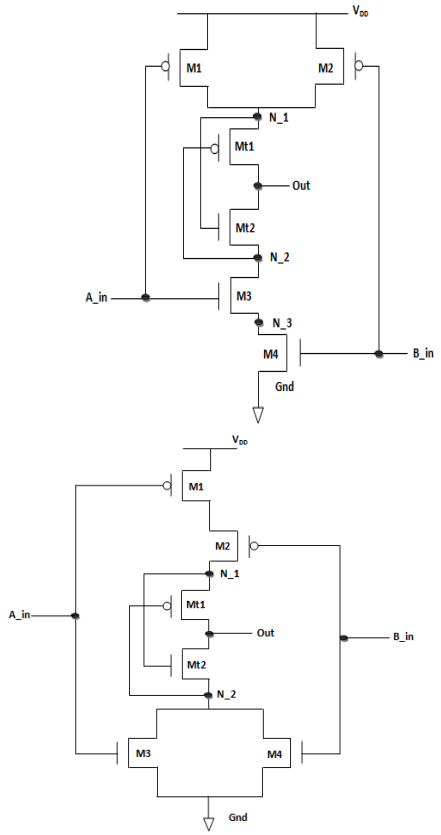


FIGURE9. Proposed V_{body} control system with ERC circuit for clock pulse generation

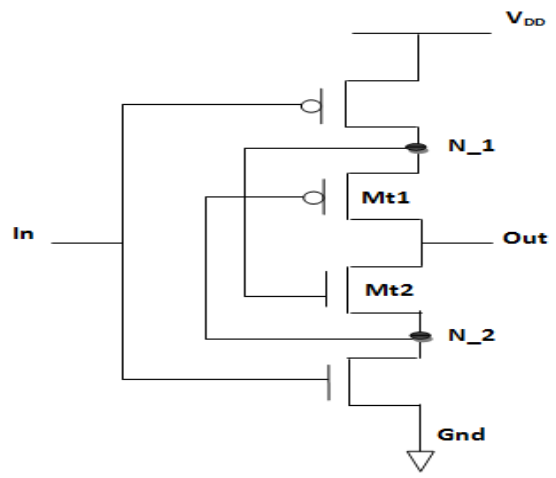
SLEEPY LECTOR

Lector concept

In LECTOR circuit, two Leakage control transistors (LCT) are inserted between pull-up and pull-down circuit of the logic gate in such a way that the gate of one LCT is governed by the source of other. It confirms that at least one LCT works in its near cutoff region. The basic notion of the LECTOR approach is that a state with many transistor OFF in V_{dd} to ground path has less leakage than the state with only one transistor OFF in V_{dd} to ground path **[40]**, **[41]**. FIGURE 10 illustrates the application of LECTOR concept in CMOS NAND, NOR, NOT gates. In a CMOS NAND gate, the Lector concept is introduced to understand the concept. Two LCTs Mt1 (PMOS) and Mt2 are inserted between nodes N_1 and N_2 of pull-down and pull-up circuit of NAND gate as shown in FIGURE 10.a. The drain nodes of two LCTs connect with each other to create the output node of the NAND gate. Correspondingly the source nodes are connected to N_1 and N_2. The voltage potential at nodes N_1 and N_2 controls the switching of LCTs Mt2 and Mt1 respectively. The resistance of V_{dd} to ground path and propagation delay increase due to the insertion of LCTs. Hence the transistors are designed with suitable size to make propagation delay equal to the standard value in order to reduce the above mentioned effect. As the operation of LCT gates is improved by utilizing many transistors, the number of transistor of path is increased. However it causes incorrect logic switching.



a) LECTOR based NAND gate
b) LECTOR based NOR gate



(c) LECTOR based NOT gate
FIGURE10. LECTOR Concept [40]

Sleepy Lector

Another new architecture is proposed in **[42]**, named as Sleepy Lector approach. It is the combination of both Sleep and Lector approaches. In this work, apart from LCTs (Mt1 and Mt2) two additional transistors are employed. In Sleepy Lector, a PMOS transistor, ST1 is inserted above pull-up network and NMOS transistor, ST2 is inserted below pull down network. LCTs are placed between pull-up and pull-down network as in Lector approach. Here at least one LCT is near cut-off region forever. So the path from V_{dd} to ground is made to have low resistance. Thus the leakage current is reduced. The stacking effect obtained by two transistors causes more reduction in leakage current. In active mode one sleep transistor becomes on and decreases the resistance of path from V_{dd} to ground to improve the performance. While in sleep mode both sleep transistors become off and increases the resistance of path from V_{dd} to ground. Thus the leakage current is reduced in an effective manner by combining the Sleep mode and Lector concept. Hence we have incorporated the Sleepy Lector circuit in our proposed work to achieve much reduced power consumption. The following FIGURE 11 shows the proposed Sleepy Lector concept is shown in below.

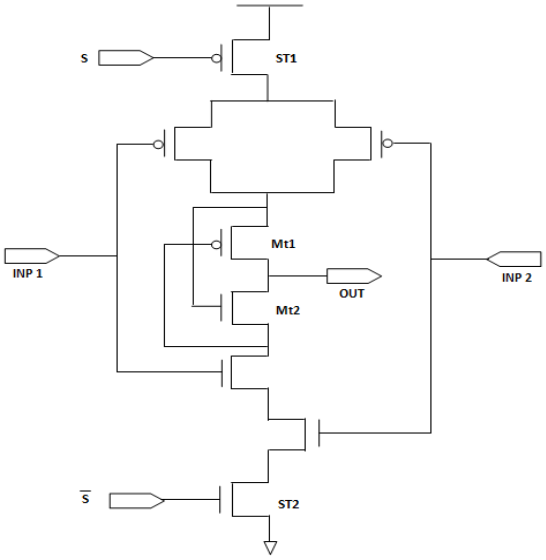


FIGURE11. Sleepy Lector Concept [42]

Clock Gating (CG)

In Field Programmable Gate Array (FPGA), the clock signals are disseminated through a programmable clock tree. The device is divided into various clock regions to provide the distribution of limited number of clock signals into each region. Clock load placement controls clock wire usage. Clock load must be placed in such a way that the clock capacitance is reduced to reduce dynamic power. In **[43]**, Wilton et al introduced clock-aware placement technique which has less number of regions traversed by clock signals and less number of resources in regions. Then placement techniques for reducing clock spine usage have been distributed by Actel and Xilinx for their corresponding designs **[44]**, **[45]**.

Stratix-III and Virtex-5 FPGAs contain clock enable pins on flip-flops of logic blocks. But these pins do not reduce switching activity on clock signal and power saving is not achieved on clock network **[47]**, **[48]**. In addition, FPGAs give gating at the top-level of the clock tree. Xilinx Virtex-6 FPGA has clock gating capability on a regional basis **[49]** and also proposes that gating has the ability to save the power of clock tree up to 30-80% **[50]**.

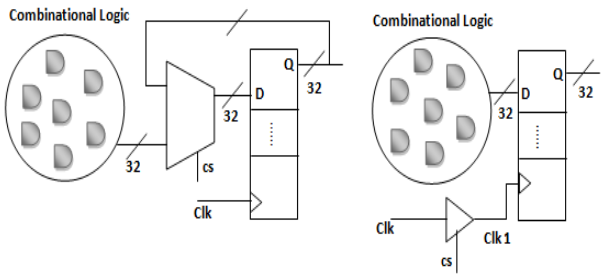


FIGURE12. Clock Gating [46]

Energy Recovery Clock (ERC)

Energy Recovery Clock (ERC) can be used to diminish power consumption in VLSI circuits. It limits the flow of current with low voltage drop across the device. A single-phase sinusoidal energy recovery clocked flip-flop considerably reduces delay, power and area **[51]**. FIGURE 13 shows energy recovery clocking circuit. The clock generator consists of a NMOS transistor M1, its drive circuitry and a lumped inductor connected to the DC supply which is half of V_{dd}. Transistor M1 gets a pulse to flatten the clock signal to ground when the clock goes to its minimum. Thus the oscillation of the resonant circuit is maintained. This transistor is a properly large sized transistor and is driven by an inverter. Thus by using Energy Recovery Clock for generating clock pulse, we further reduce the power consumption in our work.

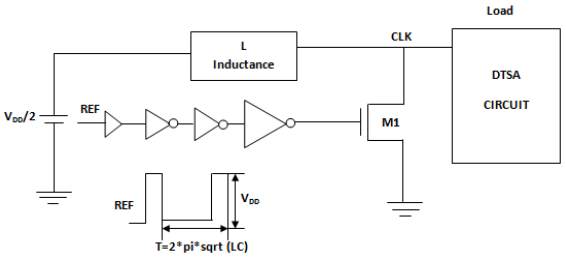
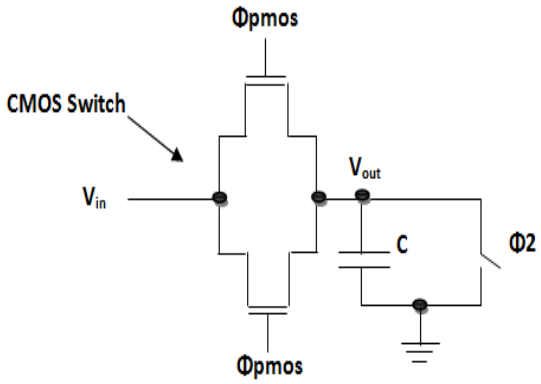


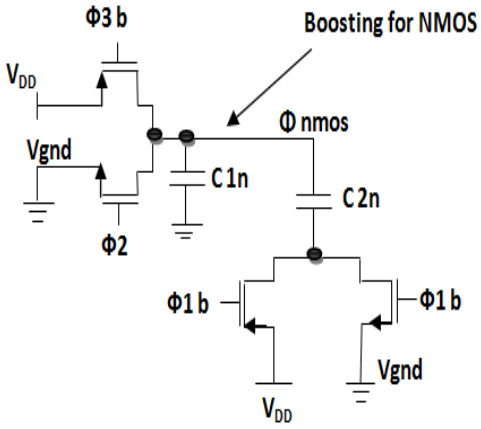
FIGURE13. Energy Recovery Clocking [51]

Clock Enable and Clock Boosting

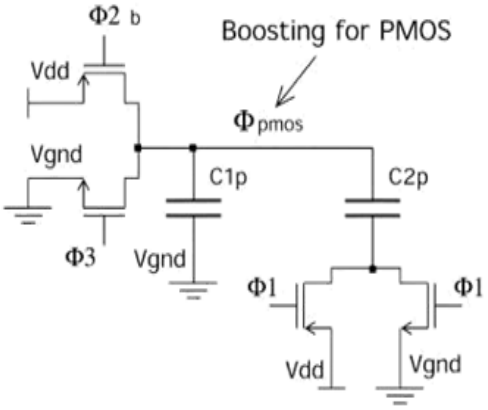
Clock enable pulse can also be given to the transistors of Sleepy Lector circuit. FIGURE 14 shows Switched Capacitor circuit for clock boosting with CMOS switch **[34]**. The nodes ϕ_{NMOS} and ϕ_{PMOS} of CMOS have actual boosted clock voltages for NMOS and PMOS switches of CMOS. CMOS switch is off when ϕ_2 by charging ϕ_{NMOS} to ground (V_g) and ϕ_{PMOS} to V_{dd}. The remaining clock phase available for sampling is separated into two intervals known as ϕ_1 and ϕ_3. During ϕ_3, the upper plates of capacitors at node ϕ_{NMOS} are charged to V_{dd}, whereas the upper plates of capacitors at node ϕ_{PMOS} are charged to V_g. When ϕ_1 is low and ϕ_{1boost} is high, the bottom plate of C2n is connected to V_g and that of C2p is connected to V_{dd}. Similarly when ϕ_1 is high, the bottom plate of C2n is connected to V_{dd} and that of C2p is connected to V_g. Finally the voltages are shifted to the top plates of capacitors by C2.(Vdd)/(C1+C2). Hence the value of boosted voltage will become as Vdd + C2.(V_{dd})/(C1+C2) and V_g - C2.(V_{dd})/(C1+C2) at ϕ_{NMOS} and ϕ_{PMOS}. Some leakage occurs through substrate terminals of switches connected to ϕ_{NMOS} and ϕ_{PMOS}. Due to this leakage the gate voltage is reduced. Hence C2.(V_{dd})/(C1+C2) should be kept lower than the threshold voltage of junction diodes. Generation of clock pulse by a non-overlapping clock generator, the time intervals of two phases, ϕ_1 and ϕ_3 do not require any particular settling condition until gate voltages are gained with proper on-resistance. In addition an extra non-overlapping clock generator must be used to ensure non-overlapping between ϕ_1 and ϕ_3.



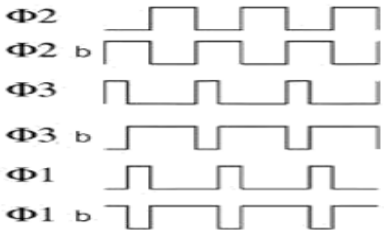
a) CMOS Switch



b) NMOS Boosting



c) PMOS Boosting



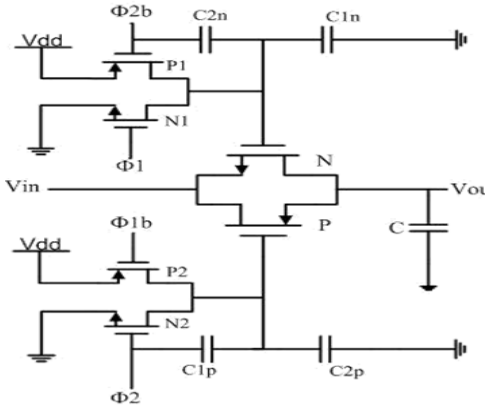
d) Clock phase generator

FIGURE14. Clock Boosting [34]

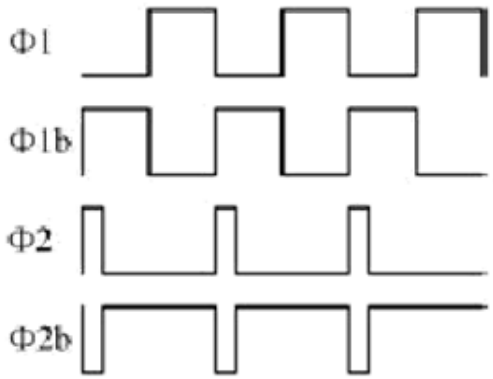
In **[35]**, AmirEhsan et al proposed a clock boosting scheme and corresponding waveforms of required clock signal as shown in FIGURE 15. CMOS switch becomes off when ϕ_1 is high as N1 becomes ON. Hence C1n and C2n are discharged and the gate of switch N is connected to ground. Similarly P2 becomes ON to charge C1p and C2p and connects the gate of P to V_{dd}. Then N2 becomes ON and discharges C1p and C2p. due to the transition of ϕ_{2boost} from 0 to V_{dd}, the gate voltage of N is increased by Vb.

$$V_b = \frac{c2}{c1+c2} - V_{dd} \quad \text{---------- (8)}$$

At the same time ϕ_2 becomes low and the gate voltage of P reduces by V_b. So the gate voltages of N and P switches become $V_{dd} + V_b$ and $V_{dd} - V_b$.



a) Clock Boosting circuit by AmirEhsan et al



b) Required Clock signals

FIGURE15.Clock Boosting Circuit

VI. EXPERIMENTAL EVALUATION

In this section, the effectiveness and performance accuracy of proposed research work is analyzed and also it was compared with existing work. The four different configurations of the proposed optimal V_{body} control system is implemented and simulated in HSPICE using 32nm N-MOSFET with 0.9nm oxide thickness and the applied V_{dd} is 0.9V. HSPICE is a simulation tool used to simulate the electronic circuits. Five ISCAS85 benchmark circuits C432, C499, C1908, C1355, and C5315 are used to evaluate the results. The leakage power for all configurations are evaluated at zero body bias and optimal body bias and compared with the existing method in reference

[4]. It is observed well that the leakage power is reduced in the proposed method. For each configuration the results are compared and represented as tables. It is also observed that when the temperature changes from 25ºC to 100ºC, the leakage power also changes. Thus it implies that the temperature variations have an adverse impact on leakage power. The leakage power at zero body bias increases when the temperature rises from 25ºC to 100ºC. It is also observed that the leakage power consumption at optimal body bias is extremely lower than the value at zero body bias. The results also illustrate that the leakage power dissipation increases with the number of gates.

The following tables compare the leakage power for the existing method of **[4]** and proposed methods CESL, CGSL, CBSL, and ERCSL correspondingly. The highest reduction in leakage power for CESL when compared with the existing work **[4]** is 92.33% and it is obtained for C1908 benchmark at 100ºC. The maximum reduction in leakage power for CGSL when compared with the existing work **[4]** is 99.41% and it is attained for C5315 benchmark at 100ºC. The maximum reduction in leakage power for CBSL, while comparing with the existing work **[4]** is 99.70% and it is achieved for C5315 benchmark at 100ºC. The maximum reduction in leakage power for ERCSL when compared with the existing work **[4]** is 99.93% and it is achieved for C5315 benchmark at 100ºC.

Table 1: Comparison of Leakage power for existing and CESL design at temperature 25ºC and 100º C

No of gates	Function Specification	Circuits	Leakage power at 25ºC		
			Zero Body Bias (ZSS) [4]	Optimal Body Bias (OBB)	% of Reduction
			CESL	CESL	
160	27-channel interrupt controller	C432	4.123	0.0021	83.84%
202	32-bit SEC circuit	C499	12.011	0.0041	86.33%
880	16-bit SEC/ DED circuit	C1908	12.33	0.0033	91.75%
546	32-bit SEC circuit	C1355	18.6	0.0034	91.28%
2307	9-bit ALU	C5315	45.8	0.015	88%

			Leakage power at 100ºC		
			Zero Body Bias (ZSS) [4]	Optimal Body Bias (OBB)	% of Reduction
			CESL	CESL	
160	27-channel interrupt controller	C432	11.10	0.0020	83.33%
202	32-bit SEC circuit	C499	30.7	0.0030	91.67%
880	16-bit SEC/ DED circuit	C1908	30.1	0.0033	92.33%
546	32-bit SEC circuit	C1355	47.3	0.0031	91.39%
2307	9-bit ALU	C5315	107.6	0.015	88.89%

Table 2: Comparison of Leakage Power for existing and CGSL design at temperature 25ºC and 100º C

	Function		Leakage power at 25ºC		
			Zero	Optimal	

No of gates	Specification	Circuits	Body Bias (ZSS) [4]	Body Bias (OBB)	% of Reduction
			CGSL	CGSL	
160	27-channel interrupt controller	C432	3.15	0.0010	93
202	32-bit SEC circuit	C499	11.01	0.003	9 %
880	16-bit SEC/ DED circuit	C1908	11.13	0.0021	94. 7 %
546	32-bit SEC circuit	C1355	17.6	0.0022	94. 36 %
2307	9-bit ALU	C5315	40.1	0.010	9 %
			Leakage power at 100°C		
			Zero	Opti	

			Body Bias (ZSS) [4]	mal Body Bias (OBB)	% of Reduction
			CGSL	CGSL	
160	27-channel interrupt controller	C432	9.6	0.0017	85.83%
202	32-bit SEC circuit	C499	27.3	0.0026	92.78%
880	16-bit SEC/ DED circuit	C1908	27.1	0.0031	92.79%
546	32-bit SEC circuit	C1355	38.6	0.0021	94.17%
2307	9-bit ALU	C5315	96.1	0.0008	99.41%

Table 3: Comparison of Leakage power for existing and CBSL design at temperature 25ºC and 100º C

No of gates	Function Specification	Circuits	Leakage power at 25ºC		
			Zero Body Bias (ZSS) [4]	Optimal Body Bias (OBB)	% of Reduction
			CBSL	CBSL	
160	27-channel interrupt controller	C432	2.10	0.0008	93.85 %
202	32-bit SEC circuit	C499	9.01	0.001	96.67 %
880	16-bit SEC/ DED circuit	C1908	8.10	0.0010	97.5 %
546	32-bit SEC circuit	C1355	15.3	0.0010	97.44 %
2307	9-bit ALU	C5315	35.2	0.008	93.6 %
			Leakage power at 100ºC		
			Zero Body Bias (ZSS) [4]	Optimal Body Bias (OBB)	% of Reduction
			CBSL	CBSL	
160	27-channel interrupt controller	C432	8.3	0.0006	95%
202	32-bit SEC circuit	C499	25.1	0.0011	96.94 %
880	16-bit SEC/ DED circuit	C1908	25.0	0.0012	97.21 %
546	32-bit SEC circuit	C1355	33.1	0.0012	96.67 %
2307	9-bit ALU	C5315	90.1	0.0004	99.70 %

Table 4: Comparison of Leakage power for existing and ERCSL design at temperature 25ºC and 100º C

No of gates	Function Specification	Circuits	Leakage power at 25ºC		
			Zero Body Bias (ZSS) [4]	Optimal Body Bias (OBB)	% of Reduction
			ERCSL	ERCSL	
160	27-channel interrupt controller	C432	1.10	0.0001	99.23%
202	32-bit SEC circuit	C499	7.3	0.0001	99.67%
880	16-bit SEC/ DED circuit	C1908	6.1	0.0006	98.5%
546	32-bit SEC circuit	C1355	10.1	0.0007	98.2%
2307	9-bit ALU	C5315	28.1	0.0001	99.92%
			Leakage power at 100ºC		
			Zero Body Bias (ZSS) [4]	Optimal Body Bias (OBB)	% of Reduction
			ERCSL	ERCSL	
160	27-channel interrupt controller	C432	4.2	0.0001	99.17 %
202	32-bit SEC circuit	C499	17.3	0.007	80.56 %
880	16-bit SEC/ DED circuit	C1908	17.6	0.0011	97.44 %
546	32-bit SEC circuit	C1355	21.3	0.007	80.56 %
2307	9-bit ALU	C5315	80.6	0.0001	99.93 %

Table 5: Comparison of Leakage power reduction for proposed implementations at 25ºC and 100º C

No of gates	Function Specification	Circuits	At 25ºC				At 100ºC			
			CESL	CGSL	CBSL	ERCSL	CESL	CGSL	CBSL	
16	27-	C43	83	92.3	93.	99.	83.	85.	95	

0	channel interrupt controller	2	.84 %	%	85 %	23 %	33 %	83 %	%	%
202	32-bit SEC circuit	C499	86.33 %	90%	96.67 %	99.67 %	91.67 %	92.78 %	96.94 %	80.56 %
880	16-bit SEC/ DED circuit	C1908	91.75 %	94.75%	97.5%	98.5%	92.33 %	92.79 %	97.21 %	97.44 %
546	32-bit SEC circuit	C1355	91.28 %	94.36%	97.44 %	98.2%	91.39 %	94.17 %	96.67 %	80.56 %
2307	9-bit ALU	C5315	88 %	92%	93.6%	99.92 %	88.89 %	99.41 %	99.7 %	99.93 %

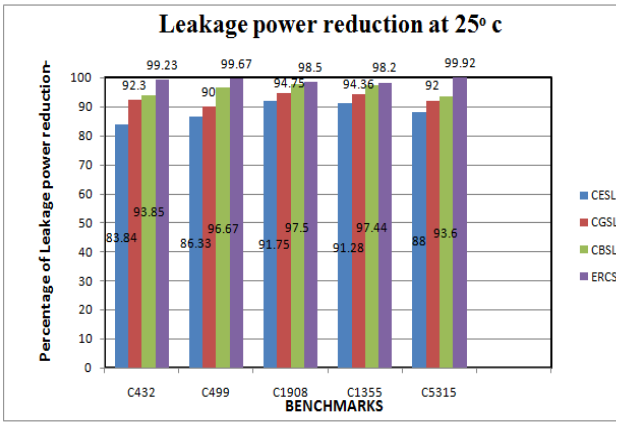


FIGURE16. Comparison of leakage power reduction for CESL, CGSL, CBSL, and ERCSL at 25°C

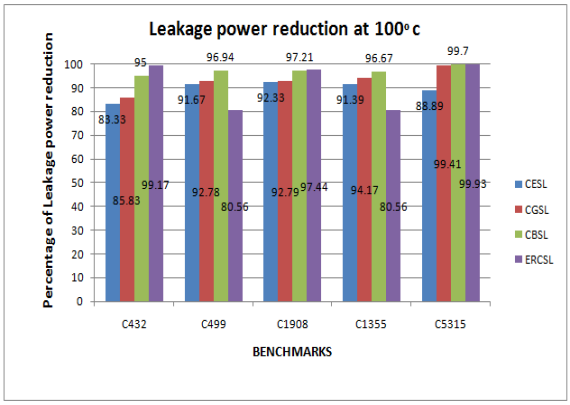


FIGURE17. Comparison of leakage power reduction for CESL, CGSL, CBSL, and ERCSL at 100°C

VII. CONCLUSION

With the ever increasing technology of VLSI Circuits, the power dissipation becomes a major problem with reduced device size. The ultimate goal of developed V_{body} control system thrust is to low power design of CMOS circuits due to advancement in Core devices & wireless communication technology. Because, personal communication devices such as mobiles, digital camera, GPS (Global Positioning Devices), multi media devices and their features creates challenging power consumption problem. To satisfy those requirements, it is important to minimize standby leakage power of those devices. In order to reduce standby leakage power of VLSI components, research work has designed a V_{body} control system in which optimal reverse body bias voltage is considered to accomplish low power dissipation. The proposed a novel technique to reduce standby leakage power by using Sleepy Lector, and energy efficient clocking circuits. The optimal V_{body} control system is designed and implemented in HSPICE simulation tool and the simulations results are validated that the CBSL and ERCSL offers good efficiency in reduction of leakage power dissipation. The maximum reduction of 99.93% is achieved in ERCSL.

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