# MEMRISTOR BASED TERNARY CONTENT ADDRESSABLE MEMORY DESIGN USING ROBUST DYNAMIC SIGNAL SEARCH METHOD

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***Abstract:*** *One of the content addressable memories (CAM) is ternary CAM (TCAM), used for searching in networking. Demanding TCAM application is increasing day by day in search spaces. Application specific FPGA platform needs to execute TCAM. However, the existing design of TCAM based on FPGA are not efficient regarding storage and time. In this proposed strategy, hybrid design for a TCAM that uses both Transistors and memristors to overcome all issues. The proposed TCAM memory cell is investigated concerning several features, for example, memristance range and voltage threshold of the memristors to process quickly and effectively ternary information. A far-reaching simulation-based assessment of this TCAM is developed by Xilinx programming language utilizing Robust Dynamic Signal Search (RDSS) Method. Simulation work came out to exhibit that the execution of the proposed algorithms is better than past methods for improving the performance of search applications. Comparison with other memristor-based CAMs and also CMOS-based TCAMs demonstrates that the proposed memory cell consumes low power, reduced transistor count and increase search activity execution.*

***Key words:*** *Memristor Ternary content addressable Memory (MeTCAM), Xilinx, Search pattern, FPGA, Power, Robust Dynamic Signal Search (RDSS)*

## 1. INTRODUCTION

One of the special kinds of computer memory is CAM (Content Addressable Memory). CAM is used in searching applications due to its high-speed operations. CAM is also called as associate memory. It is also used for storing data structure's data. Another type of CAM is binary CAM where it stores data having only 0's and 1's. The most type of CAM is TCAM where it includes don't care of one or more bits in the data stored. Hence the flexibility of searching method increases in TCAM. Let us consider the stored data in TCAM is "10XX0" can be matched with 10000, 10010, 10100, and 10110. XX in the stored data can be adapted for 00, 01, 10 and 11. Thus, the searching flexibility is increased in TCAM. Opposite to RAM is CAM. To access the data from RAM, OS provides the address of the memory in which the data is stored. But to fetch a data stored in CAM, a query is passed within the content and the memory attains the address of the data. Due the parallel process of CAM and TCAM which is very fast than RAM. Because of cost, power and heat production it is not used in more electronic devices.

TCAM inside network routers is used for speedy routing by looking the address speedily. Comparing with CAM, TCAM enables the address searching process without considering the length of the prefix. Because the main behaviour of TCAM is, it can do searching parallelly. It shows that TCAM stores any length and amount or addresses stored, the router will search the port within a single iteration. This is the speciality of the TCAM based searching. Hence, this paper aimed to use TCAM based searching methods. Advantages of the TCAM are, it uses don't care bit will match 0 or 1, it follows CAM internally, it is fast and it is power hungry. The following figure shows two entries such as prefix stored in TCAM and next hop stored in SRAM. The prefix "?" can be matched with "0" or "1" in a single iteration, where it saves searching time, memory utilization and hence power.

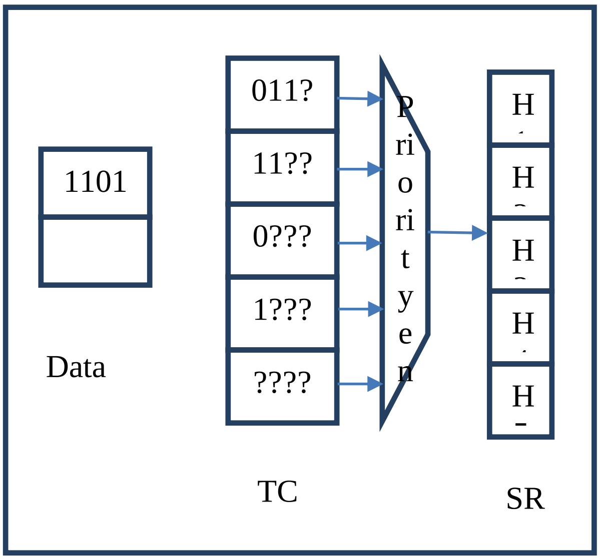

Fig.1. Data Forwarding

In this research work proposes another hybrid design for a ternary CAM that uses both Transistors and memristors to overcome all issues of previously designed TCAM using Robust Dynamic Signal Search

Method. The proposed RDSS have new bit cell structure that limits the bit cell region as well as is equipped for execution enhancements on the latency and energy utilization. Detailed configuration issues, for example, voltage consistency to guarantee correct write/search activities, parameter-subordinate detecting edges and device variations are also discussed.

## 2. RELATED WORKS:

In this section to discuss some of the existing Ternary Content addressable memory design techniques.

A low-power SRAM-construct CAM design usage in light of FPGA was displayed in a past work [1-3]. It plays out a different levelled lookup of the design-arranged SRAM squares. It accomplishes low power utilization by ceasing resulting SRAM lookup activities if a match is found in the present SRAM square. Although it decreases the average power utilization of the design, its most pessimistic scenario power utilization stays high, which isn't advantageous for the designed equipment as the equipment is designed in light of the most pessimistic scenario power utilization spending plan. Conversely, the proposed work accomplishes a noteworthy decrease in the most worst-case power utilization of the actualized TCAM design [4].The design procedures displayed in [5– 8] utilizes different unmistakable SRAM blocks for actualizing TCAM usefulness. These stores the TCAM word's presence and address data independently in distinct arrangements of SRAM blocks. The Input TCAM word is connected to the primary method of SRAM blocks to read its reality data, and the location data is read from the second arrangement of SRAM blocks [9-11]. These TCAM design systems utilizing various particular SRAM blocks uses over the top SRAM memory. These works experienced higher power utilization as the whole used over the top SRAM memory is enacted for the approaching TCAM word lookup. In [12-13] differentiation of proposed work stores the TCAM word's presence and address data in a single RAM, along these lines acknowledging effective memory utilization. Also, the proposed work accomplishes significantly decreased power utilization by enacting at most one column of SRAM blocks for approaching TCAM words [14].

In any case, these works [15-17] energize all utilized SRAM memory blocks in the design for every approaching TCAM word's lookup. In this manner, expends higher power utilization. Interestingly proposed TCAM engineering empowers explicitly a piece of SRAM memory blocks utilized, accomplishing a significant decrease in the general dynamic power utilization of the design. An ongoing work exhibited in [18-20] utilizations multi-pumping empowered multiport SRAM memory for actualizing memory-productive TCAM design on FPGA. It stores the sub-blocks of parcelled TCAM table in the shallow sub-blocks of SRAMs arranged as multi-ported recollections on FPGA [21-23]. All the above-discussed methods have the problem of time complexity and power overhead in the sequence identity.

## 3. MATERIALS AND METHOD

A general architecture of Ternary Content Addressable program memory is shown in **Figure 2.** Normally, CAM is prescribed into two types such as binary CAM and TCAM. TCAM used search engines assume an essential job in networking router and switches. In this work introduce Robust Dynamic Signal Search method to design TCAM using two transistor and two memristor cells. The Proposed TCAM memory cells can store three states such as ‘Zero,' ‘One,' and don't care. In this proposed work don't care state is used to matching the values either zero or one in an input search application process. As compared with other memories a TCAM is utilized for applications that permit both exact and fractional matches. In this work present a TCAM design using two memristor cells. It expands on a bipolar memristor display with storing and bringing capacities given the good current-voltage conduct.

### 3.1. MEMRISTOR – TCAM CELL

The accompanying Figure. 3 exhibits the improvement of a memristor TCAM. In this design, the memristor can act as in storage component and a switch in the meantime. As featured previously, the basic necessity for a TCAM exhibit is to deal with the area of matches with a search word: the data searched information will be given into the memory, in the event that they are coordinated with the put away information, a match signal will be enacted to demonstrate the stored data has a matched data.

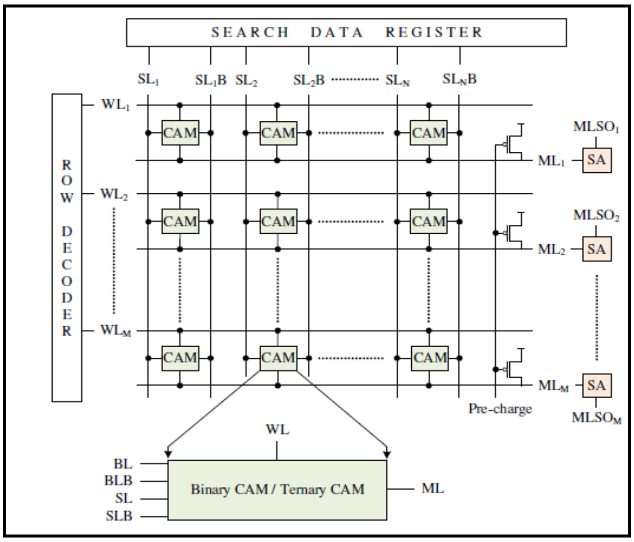

**Fig.2. The architecture of General Ternary content addressable Memory**

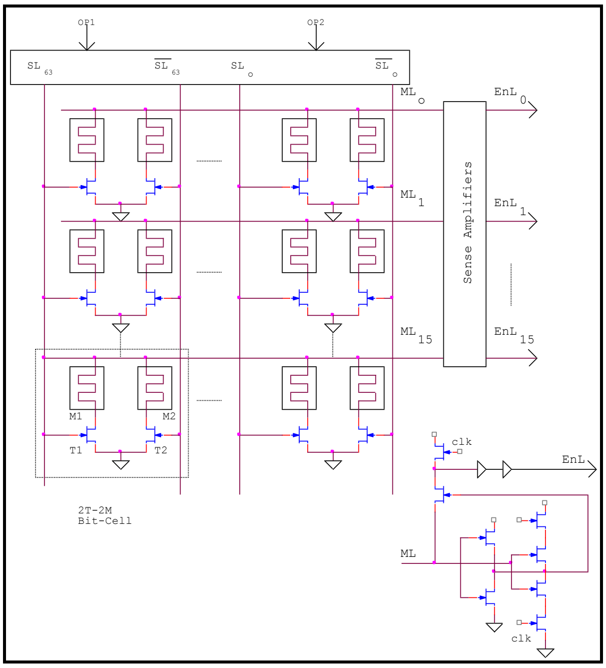

**Fig.3. The cell structure of MeTCAM**

The above Figure. 3 demonstrates the development of a memristor-based TCA. The read and write operation of the memristor-based TCAM circuit diagram is shown in the following figure 4.

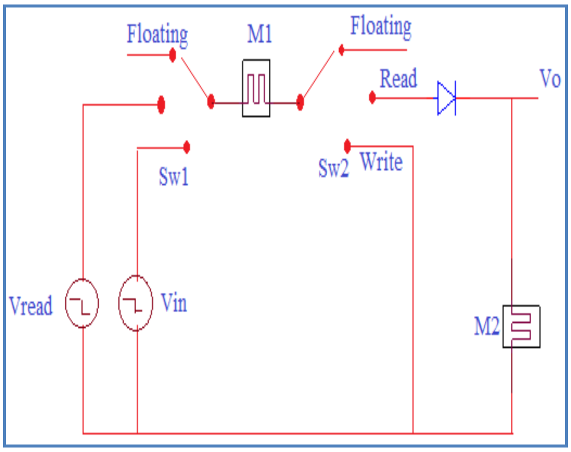

**Fig. 4. Read and write operation diagram for memristor**

### 3.2 MTCAM - Write Operation

The schematic diagram of memristor's write operation is demonstrated in Figure.5. During the writing process, the memristor operations rely upon the supply voltage and clock pulse duration. The mathematical expression of the write operation as

$$\frac{\partial \omega}{\partial t} = \mu_v \times \frac{R_{on}}{D} \times i(t) \quad \ldots (1)$$

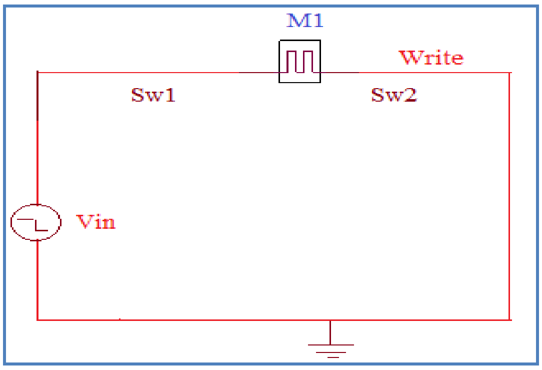

**Fig 5: Memristor Write operation**

Where

$\mu_v$ = dopant mobility

$i(t)$ = Memristor current

$D$ = Data

$R_{on}$ = Resistive Value of Memristor

The above said parameters are characterized for switch state of the inner devices within the composition procedure. In accordance to the current and voltage attributes, the memristor devices changes the state from low-resistive into high-resistive. The changes of the voltage and current parameters needs to be written in the memristor. The changes on the pulse duration is from logic '0' to '1' are ascertained and the most astounding qualities are selected to accomplish both written work tasks, which are meant by $v_{wr}$ (i.e., $v_{in}$ = $v_{wr}$ within the composition procedure) for voltage size and $T_{wr}$for the pulse term as depicted in **Figure 6.**

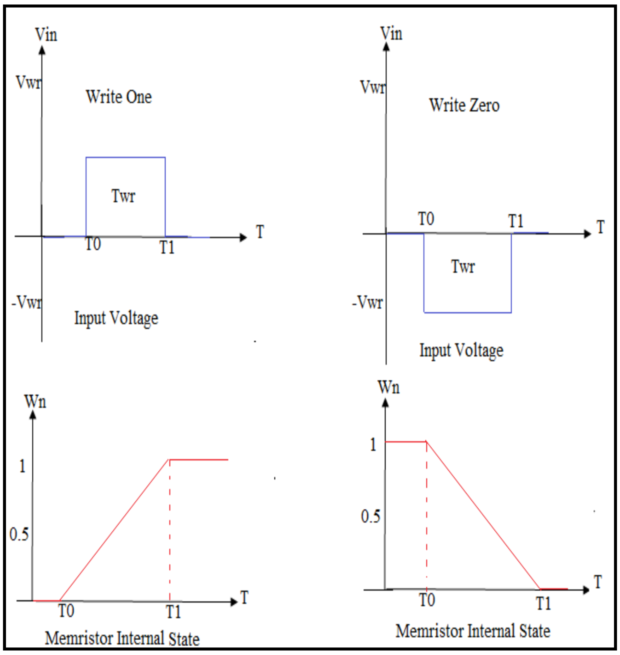

**Fig 6: write one and zero to a memristor**

### 3.3 Read operation

One of the critical tasks in memristor is read operation. The read operation-based memory application is non-unstable, because the voltage variation of rad operation will intensify the data persisted due to the properties of memristor. Figure-7 shows the proposed circuit model of the memristor – read operation. In order to read the stored data, a positive voltage Vread (i.e., $V_{in} = V_{read}$ amid the reading procedure) is connected for $T_{read}$ pulse term, and two unique situations are viewed as in light of the stored data.

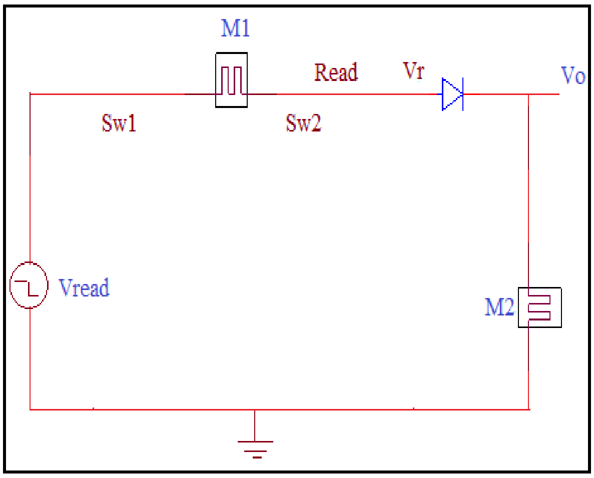

Fig 7. Memristor Read operation

### 3.3.1 Data search ‘1.'

Figure-7 shows the read operation of the memristor. There are two memristor M1 and M2 are used. If M1 becomes ON, then there will be a voltage drop in Vr which is equal to Vread. The voltage drop is measured as 0.7V, and it makes the current flow through the diode and M2. M2 is considered as a heap resistor where it obtains the positive aspect of the memristor comparing with the conventional resistors. The voltage drop at M2 defines the stored data in the memory for example, if $V_o = V_L$ logic '0' is stored and if Vo = VH, logic '1' is stored. From Figure-7, M2 is located as a dependable in high resistive state.

The voltage gained as the output, Vo = VH, is given by:

$$V_o = V_H = V_r - n \times V_T \times l_n \frac{I_d}{I_{sat}} \quad \ldots. (2)$$

### 3.3.2 Data search ‘0.'

In this situation, Memristor M1 in the OFF state and the voltage drop on it is, and thus Vr is small. Vread is outlined so that after the voltage drop on M1, Vr is under 0.7V and as needs are the diode turns OFF and goes about as an open circuit where no present flows through M2.

The non-dangerous element of the proposed circuit exists on the grounds that the reading voltage will influence memristor M1 only amid perusing logic one, there will be no impact amid perusing logic zero in light of the fact that the diode will go about as an open circuit and henceforth no current will course through the memory component (M1).

As the circuit utilizes a positive voltage to compose logic one, at that point the reading voltage polarity and the written work voltage extremity is the same. The only principle concern is to pick Vread, so it turns ON the diode while reading logic one and OFF while reading logic zero.

Also, the diode is utilized to ensure that the current flow through the load Memristor M2 in one direction to keep up its OFF state and furthermore to give invulnerability of the memory Read/Write circuit to leakage current.

### 3.3.3 Algorithm Steps for Robust Dynamic Signal Search

```
Input:  Search line Address
Output: Search word or sequence
Method: Robust Dynamic Signal Search (key)
Step 1: Prepare search Information list:
            K ← {‘XX . . . XX’}
Step 2: While (K is not empty)
Step 3: K ← K.pop (). Let d represent the range's, e].
Step 4: K ← Ternary Content Addressable Memory Search (K, key)
Step 5: If (K! = NULL)
         Let i be the index of rule K
 Step 6: Let K be the collection of discriminator prefixes
                    For the range [i + 1, e]
Step 7:  K ← K.push (D)
End-while
Step 8: Return Ternary Content Addressable Memory Matched List
```

This paper presented a novel MT-CAM cell design for low power searching method. MT-CAM used two memristors and transistors. Also, it separates the search line in accordance to search logic 0 and 1.

## 4. RESULTS AND DISCUSSION:

The whole layer structure and memory architecture are developed utilizing Verilog programing language in Xilinx ISE Design Suite and to confirm the functionality of the outline. Each proposed module is outlined using Structural and behavioural models. The following figures 8, 9 and 10 shows the simulation results of the proposed system.

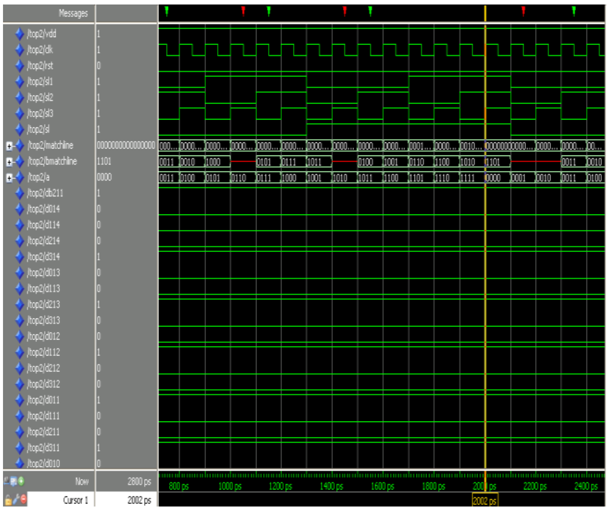

**Fig. 8. MeTCAM – Empty Content Result**

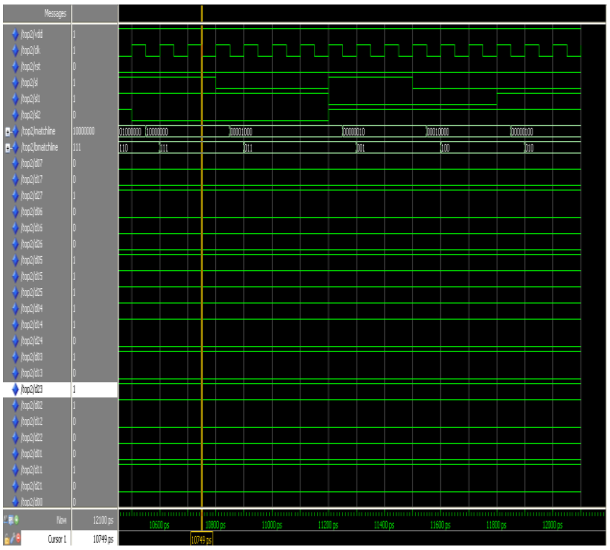

**Fig.9.: MeTCAM – Not Matched Content Result**

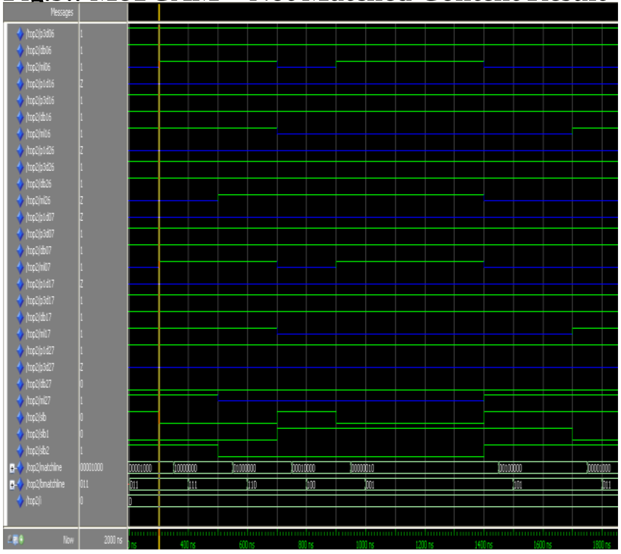

**Fig. 10. MeTCAM – Matched Result**

The above-discussed figures 8, 9 and 10 demonstrated the simulation results of the proposed Memristor-based TCAM system. From this simulation results figure, 10 demonstrates matched results that matched data has indicated in blue lines, figure 8 shows unmatched contents that indicate in red lines and figure 9 shows an empty data content result.

**Table-1: Power analysis of stimulator circuits**

| Parameters | Robust Dynamic Search MeTCAM | Deep Search pattern based MeTCAM | BITCAM | MLTCAM |
|---|---|---|---|---|
| Avg power(w) | 2.012E-05 | 2.2490E-05 | 4.3727E+02 | 9.2658E-06 |
| Peak power(w) | 2.523E-05 | 2.9007E-05 | 4.3727E+02 | 2.6789E-04 |
| Avg current(I) | 3.0.32E-05 | 3.2053E-05 | 1.2151E-04 | 1.1446E-05 |
| Peak current(I) | 1.430E-05 | 1.5896E-05 | 1.2122E-04 | 1.0836E-03 |

Table-1 discuss the performance comparison results of Average power, peak power, average current and peak current obtained from existing and proposed a method. As compared with existing methods the proposed Robust Dynamic Signal Search techniques give the perfect results.

**Table-2: Performance Analysis of Delay and Power Delay Product (PDP)**

| Circuit Name | Delay(S) | | Power delay product (S) | |
|---|---|---|---|---|
| | 0.8V | 1V | 0.8V | 1V |
| Prop.MeTCAM | 43.02 E-09 | 1.25 E-09 | 4.65 E-14 | 6.25 E-14 |
| Deep Search Pattern MeTCAM | 64.729E-09 | 1.4186E-09 | 5.6039E-14 | 8.5174E-14 |
| BITCAM | 73.662E-12 | 75.926E-12 | 3.221E-08 | 3.32E-08 |
| MLTCAM | 183.34E-12 | 166.78E-12 | 1.6987E-15 | 5.78156E-15 |

The performance comparison among delay (D) and power delay product (PDP)is given in Table-2. As compared with existing methods the proposed Robust Dynamic Signal Search techniques gave the perfect results for every working condition.

**Table-3: Details of performance comparison in Power reduction**

| Process/method | Search method | Power(%) | Delay(sec) |
|---|---|---|---|
| CAM | Hierarchical search | 55 | 80 |
| TCAM | Segmented Match line | 47 | 70 |
| BiTCAM | PF-CDPD | 39 | 60 |
| MeTCAM | Deep search algorithm | 16 | 25 |
| MeTCAM | Robust dynamic signal search | 14 | 20 |

The above-discussed Table-3 demonstrates the power consumption and search time utilization results for proposed and existing frameworks. As compared with existing algorithms the proposed robust dynamic signal search strategy creates great outcomes with all parameters against all data search sets.

**Table-4: Area overhead Comparison**

| Logic Utilization | MLTCAM | BITCAM | Deep Search pattern MeTCAM | Proposed Metcam |
|---|---|---|---|---|
| No. of IOS | 131 | 131 | 128 | 125 |
| No. of Bonded IOB's | 117 out of 190 | 116 out of 190 | 106 out of 190 | 106 out 185 |
| Min. Period | 6.972ns | 20.650ns | 6.900ns | 6.52 ns |
| Min. I/P Arrival time | 6.935ns | 21.750ns | 6.928ns | 6.03 ns |
| Max. O/P Required time | 4.880ns | 4.283ns | 3.982ns | 3.8ns |
| Max. Combinational Path Delay | 15.153ns | 15.113ns | 15.013ns | 14.23 ns |

Table-4 discuss the Area overhead comparison results for an existing and proposed method. As compared with existing methods the proposed Robust Dynamic Signal Search technique was to achieve low area overhead.

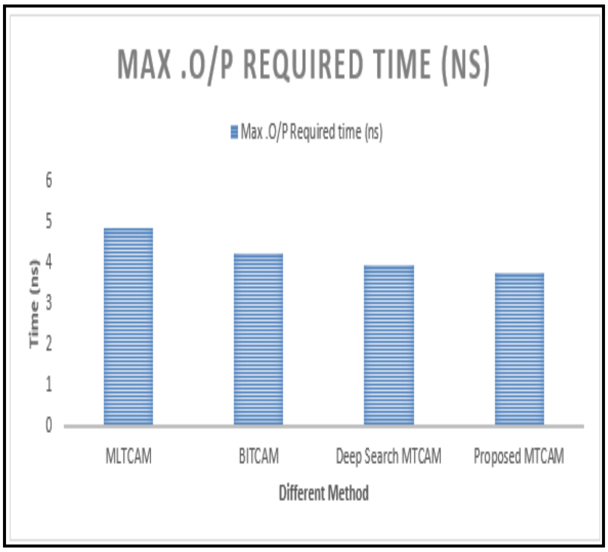

**Fig. 11. Search Time analysis**

The above Figure 11, shows the comparative result of time utilization for data in TCAM with different methods. As compared with existing TCAM methods the proposed RDSS method utilizes minimum time for data searching.

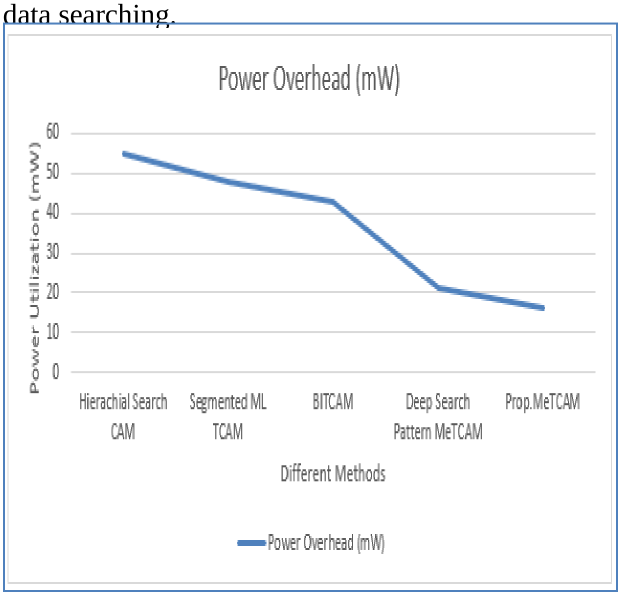

**Fig.12. Comparison of power consumption in Search time (mW)**

The performance evaluation of the proposed TCAM regarding power consumption is given in Figure-12. Power consumption is calculated in terms of searching time (mW) for different methods. As compared with existing TCAM methods the proposed RDSS method consumes low power while searching.

## 5. CONCLUSION:

In this work proposes a hybrid design for a ternary CAM (TCAM) that uses both Transistors and memristors to overcome all issues. The proposed TCAM memory cell is investigated concerning several highlights, for example, memristance range and voltage threshold of the memristors to process quickly and effectively ternary information. A far-reaching simulation-based assessment of this TCAM is developed by Xilinx programming language utilizing Robust Dynamic Signal Search (RDSS) Method. Simulation work came out to exhibit that the execution of the proposed algorithms is better than past methods for improving the performance of search applications**.** The proposed Memristor-based TCAM design has consumed an average of 16% power utilization as compared with existing and BiTCAM consumes 39%.

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