ANALYSIS OF AN ASYMMETRICAL REDUCED SWITCH MULTILEVEL INVERTER TOPOLOGY WITH DIFFERENT MODULATION TECHNIQUES USING dSPACE

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Abstract: *Multilevel inverters are noteworthy in high voltage industrial applications now a day. This study is an experimental analysis of a reduced switch asymmetrical multilevel topology when applied with different modulation schemes. Sinusoidal Pulse width modulation (SPWM) and Space vector pulse width modulation (SVPWM) Techniques are employed to control the MLI. The space Vector algorithm applied here is a general one which can applied to any N- level inverters without much complexity as compared with conventional space vector techniques. The Total Harmonic Distortion (THD) of the MLI output is evaluated for different modulation techniques. The topology can generate 7 level output voltage which is simulated in MATLAB/simulink tool and verified with experimental test setup results. The closeness of simulation value of %THD with the experimental test setup %THD verifies the effectiveness space vector algorithm over SPWM technique.*

Keywords: *Multilevel Inverter (MLI), Sinusoidal Pulse width Modulation (SOWM), Space Vector Pulse width Modulation (SVPWM), Total Harmonic Distortion (THD).*

1. Introduction

Multilevel inverters are the wise choice for the quality power sources. Conventional multilevel inverter topologies include Diode Clamped Multilevel Inverter, Flying Capacitor Clamped Multilevel Inverter, and Cascaded Multilevel inverter [1-2]. But they share a common disadvantage of high number of power switches and DC sources with increased output levels. This difficulty will contribute high switching losses and also increase the overall expense [2-6]. In this paper a reduced MLI topology is considered to get rid of the above difficulties [7]. This topology improves the power quality and dynamic stability of the utility system. Also it helps to reduce switching stress and EMI.

Studies are carried out for meeting the requirement of inverters such as reduce harmonic content in the output, switching frequency of the inverter and better consumption of the available dc voltage. One of the most common methods used for inverter switching is Pulse width modulation (PWM) Techniques. In this technique we control the output voltage by varying the on-off time of the switching elements in the inverter. The most popular PWM techniques used today are Sinusoidal PWM (SPWM) and Space Vector PWM (SVPWM) [8-9]. The complexity of conventional sinusoidal PWM and Space Vector PWM will increase drastically with increase in number of output levels in the MLI. Recently in literature [10-11] a new, general, low computational space vector algorithm is introduced which can be applied to any number of levels of MLI with less computation.

This study envisages analysing and comparing the performance of an asymmetrical rescued switch MLI presented in literature [7], when controlled by SPWM and space vector algorithm introduced in [11].

2. Multilevel Inverter Topology

A new reduced switch multilevel inverter topology introduced in literature [12-13] is considered for the experimental analysis. The single phase structure which produces a seven level output is shown in phase in Fig. 1. The inverter topology incorporates six unidirectional power switches and to asymmetrical dc input sources to produces the seven level output as shown in Fig.1.

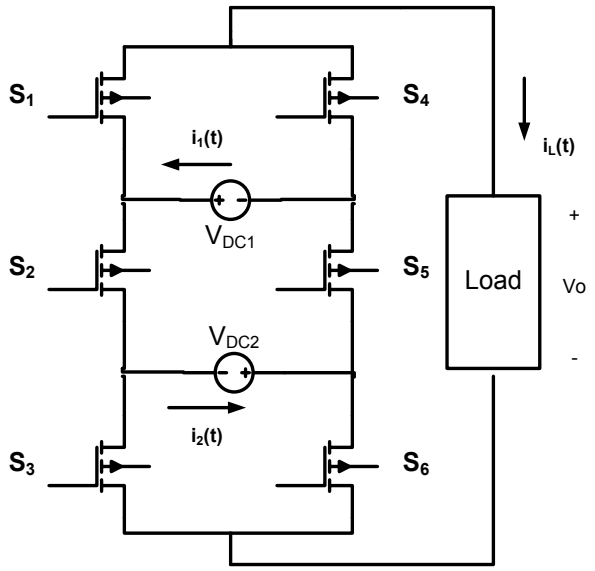

Fig.1. Single phase MLI with two input sources

Selection of power switches for the topology is merely depends on the power ratings and type of application. The switches can either be IGBT or be MOSFET. Table-1 describes and summarizes all the eight possible modes of operation of the MLI topology with switching states in the asymmetrical mode.

3. Pulse Width Modulation

Pulse width modulation techniques are intended to generate variable frequency variable magnitude ac voltages. Even though the selection of PWM method to modulate the inverter is greatly depends on the number of desired voltage levels of MLI [14]. Among various PWM techniques available, Sinusoidal PWM and Space vector PWM techniques are widely accepted and largely employed in industry.

A. Sinusoidal PWM Technique

It's the simplest and most accepted PWM technique modulated signal is generated by comparing a low frequency modulating signal and a high frequency carrier signal. The idea of multi carrier sinusoidal PWM is came in to picture when the larger number of control pulses is required. A multicarrier SPWM requires M-1 carriers to produces M level control signal. Various Multi carrier SPWM methods includes Alternate Phase opposition Disposition (APOD) PWM, Phase Disposition (PD) PWM, Carrier Overlapping PWM (COPWM) and Phase Shift PWM (PSPWM). This study considered Phase Disposition (PD) PWM as Sinusoidal multicarrier PWM to modulate the MLI [15-16].

B. Space Vector Pulse Width Modulation

The space vector PWM techniques are aim to produce variable AC voltages with minimum harmonic distortion in the inverter output. For a three phase system SPWM considers all the phases separately and hence separate modulators are required for each phase but SVPWM does not requires separate modulation as it considers all the phases as a whole. This study applies a general SVPWM algorithm for seven three phase multi level inverter topology. The algorithm applied is considered to be a non conventional method of space vector modulation technique because it does not need any lookup table or any other complex mathematical functions [17-18].

Since the switching states of any inverter topology reside at discrete states, the SVPWM algorithm method is used to produce a reference voltage vector by means of a sequence of space vector during each modulation cycle [10-11].

The Steps of this algorithm [19-20] are summarized in the flowchart shown in Fig. 4.

The steps and equations involved in the low computational space vector algorithm are as follows:-

- The reference voltage vector Vr is calculated using the expression given below

$$Vr = \frac{Vr}{Vdc} = \left[vr^1, vr^2, ...vr^p\right]^T \quad (1)$$

- Express the reference voltage vector as the sum of its integer (V_i) and fractional (V_f) parts, which is given by

Table 1 Switching States of multilevel inverter

Mode	Switch States (1=ON; 0=OFF)						Output Voltage
	S_1	S_2	S_3	S_4	S_5	S_6	
Mode 1	0	0	0	1	1	1	0
Mode 2	1	1	1	0	0	0	0
Mode 3	1	0	0	0	1	1	V_{dc1}
Mode 4	0	0	1	1	1	0	V_{dc2}
Mode 5	1	0	1	0	1	0	$V_{dc1}+V_{dc2}$
Mode 6	0	1	1	1	0	0	$-V_{dc1}$
Mode 7	1	1	0	0	0	1	$-V_{dc2}$
Mode 8	0	1	0	1	0	1	$-(V_{dc1}+V_{dc2})$

$$Vi = \text{int}(Vr) \in Z^P$$
$$Vf = Vr - Vi \in R^P \quad (2)$$

- Obtain the permutation matrix P which arranges the components of the reference voltage vector in the descending order.

$$P\begin{bmatrix}1\\ Vf\end{bmatrix} = \begin{bmatrix}1\\ \hat{Vf}\end{bmatrix} \quad (3)$$

where

$$\hat{Vf} = [\hat{Vf}^1, \hat{Vf}^2, ...\hat{Vf}^P]^T \quad (4)$$

is the sorted vector in which

$$1 > \hat{Vf}^1 \geq .....> \hat{Vf}^{K-1} \geq \hat{Vf}^K \geq .....\hat{Vf}^P \geq 0$$

- Rearrange the rows of the triangular matrix D in order to obtain the matrix D by means of

$$D = P^T \hat{D} \quad (5)$$

- Calculate the displaced switching vectors, Vdj, from the matrix D by using the expression-

$$D = \begin{bmatrix} 1 & 1 & ... & ... & 1 \\ vd_1^1 & vd_2^1 & ... & ... & vd_{p+1}^1 \\ vd_1^2 & vd_2^2 & ... & ... & vd_{p+1}^2 \\ ... & ... & ... & ... & ... \\ vd_1^p & vd_2^p & ... & ... & vd_{p+1}^p \end{bmatrix} \quad (6)$$

- The sum of integer part(Vi) of reference Voltage vector and displaced switching vectors (Vdj) gives final switching vectors

$$Vsj = Vi + Vdj \quad (7)$$

- From the fractional part (Vf) of the reference voltage vector obtain the time corresponding to each switching vectors.

$$t_j = \begin{Bmatrix} 1 - \hat{v}_f^{\,1}, & if ...j = 1 \\ \hat{v}_f^{\,j-1} - \hat{v}_f^{\,i}, & if ...2 \leq j \leq p \\ \hat{v}_f^{\,p}, & if ...j = p+1 \end{Bmatrix} \quad (8)$$

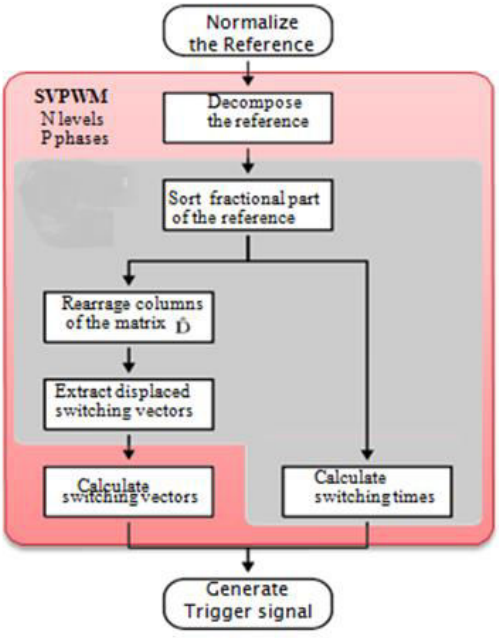

Fig.2. Flow chart for the SVPWM implementation

4. Simulation

The implementation of the whole system is done using the MATLAB/Simulink software tool. Seven level Multilevel inverter is modeled based on the theoretical concepts explained. Pulses are generated using both SPWM and SVPWM methods for comparative analysis. The pulses are given to the switches in one phase leg of a three level inverter. Similarly the pulses are generated for remaining two phases, just by changing phase shifting angle of modulating signal by 120 degrees. The simulation parameters for the model in MATLAB/Simulink are specified in Table 2.

A resistive load of R=150Ω and an inductive load of R=150 Ω and L = 20mH is considered to load the inverter.

Table 2 Simulation Parameters

	Parameter	Value
MLI	V_{dc1}	5
	V_{dc2}	10
	R Load	R = 150 Ohms
	R L Load	R = 150 Ohms L = 20 mH
SPWM/ SVPWM	Switching Frequency	2000 Hz
	Modulation Index	0.85
	Reference frequency	50 Hz

5. Simulation Results of MLI with SPWM Control

For sinusoidal PWM carrier and reference frequencies are 2 KHz and 50 Hz respectively. The sinusoidal PWM switching pulses obtained for the switches S_1, S_2 and S_3shown in Fig.3, Fig.4 and Fig.4 respectively.

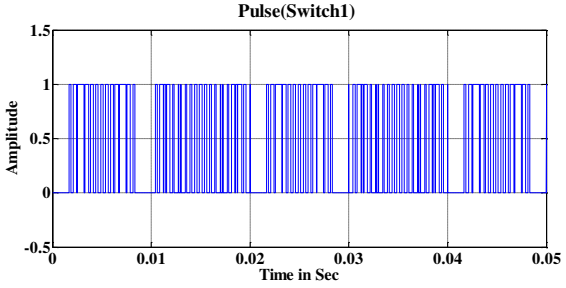

Fig.3. Pulse for Switch S_1-SPWM

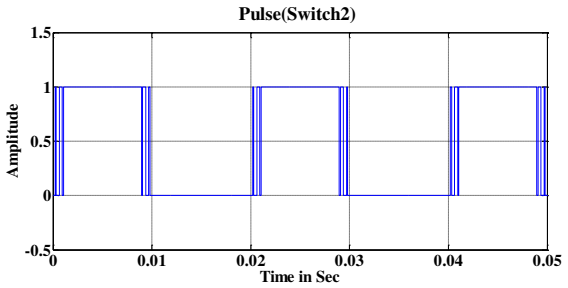

Fig.4. Pulse for Switch S_2-SPWM

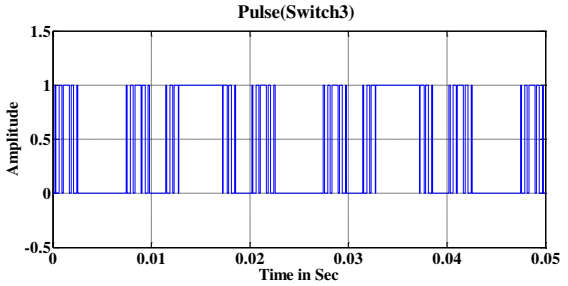

Fig.5. Pulse for Switch S_3-SPWM

The pulses for the switches S_4, S_5 and S_6 will be complementary to the pulses S_1, S_2 and S_3 respectively.

Fig.6 and Fig.7 respectively shows the load current and load voltage obtained at the inverter terminals when connected to a resistive load of R=150 Ohms.

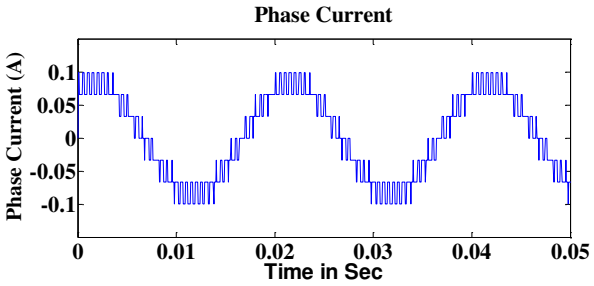

Fig.6. Load Current with R Load – SPWM

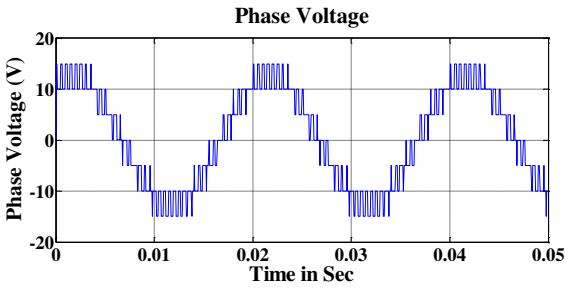

Fig.7. Voltage Output with R Load – SPWM

It can be observed that the inverter output voltage consist of seven level with equal steps of 5V and having frequency of 50Hz. The harmonic spectrum analysis of load current is shown in Fig.8. THD of the load current is obtained to be 18.82%

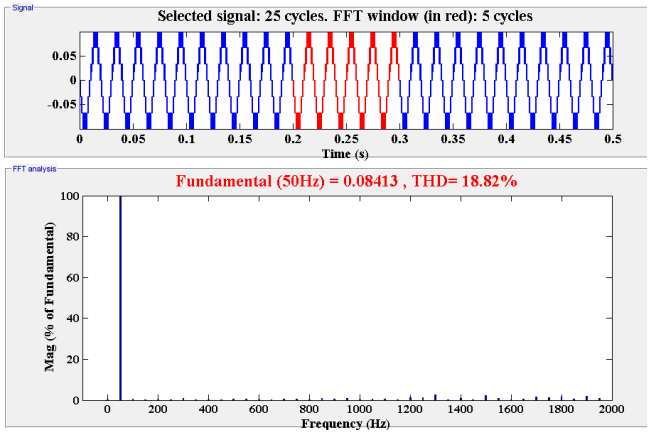

Fig.8. THD of Load Current with R Load – SPWM

A resistive inductive load of R=150 Ω and L=20mH is considered to load the inverter. Fig.9 shows load current obtained at the inverter terminals and Fig.10 Shows the harmonic spectrum analysis of the load current

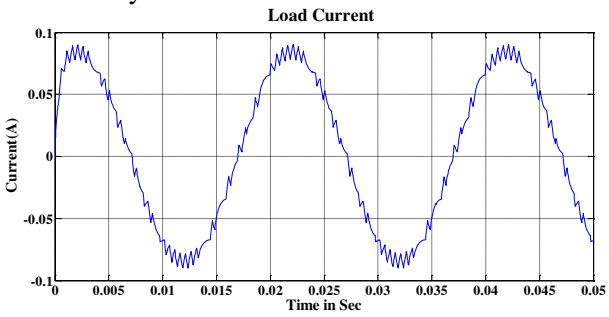

Fig.9. THD of Load Current with R Load – SPWM

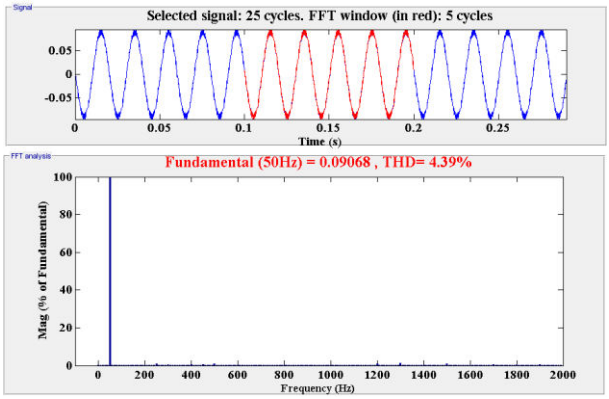

Fig.10 THD of Load Current with R Load –SPWM

THD of the load current obtained is 4.39 %.

6. Simulation Results of MLI with SVPWM Control

Retaining all system parameters to be the same pulses are generated using SVPWM technique. The sinusoidal PWM switching pulses obtained for the switches S_1, S_2 and S_3 shown in Fig.11, Fig.12and Fig.13 respectively.

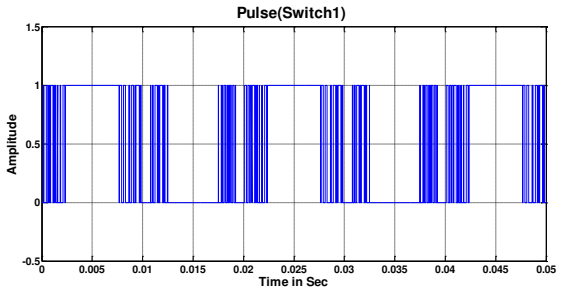

Fig.11. Pulse for Switch S_1-SVPWM

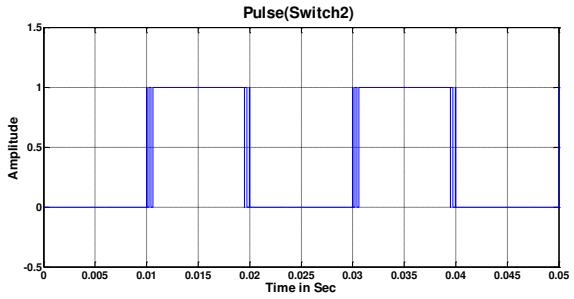

Fig.12. Pulse for Switch S_2-SVPWM

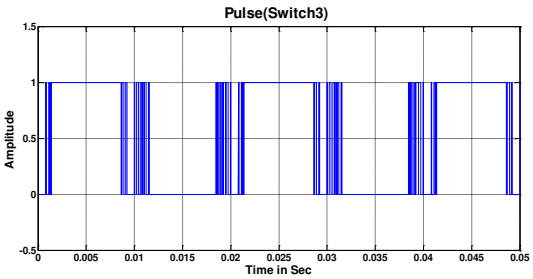

Fig.13. Pulse for Switch S_3-SVPWM

The pulses for the switches S_4, S_5 and S_6 will be complementary to the pulses of switches S_1, S_2 and S_3 respectively.

Fig.14. and Fig.15 respectively shows the load voltage and load current obtained at the inverter terminals when connected to a resistive load of R=150 Ohms.

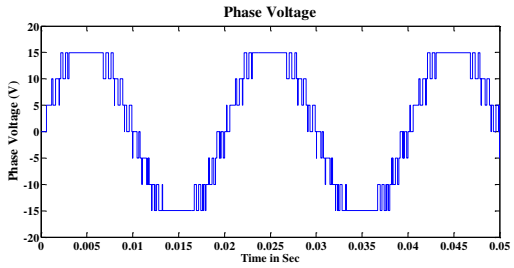

Fig.14. Voltage Output with R Load – SVPWM

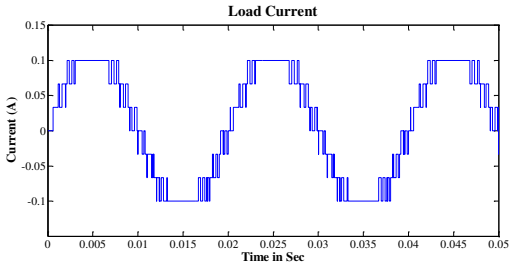

Fig.15. Load Current with R Load – SVPWM

The harmonic spectrum analysis of load current is shown in Fig.16. THD of the load current is obtained is 13.97%

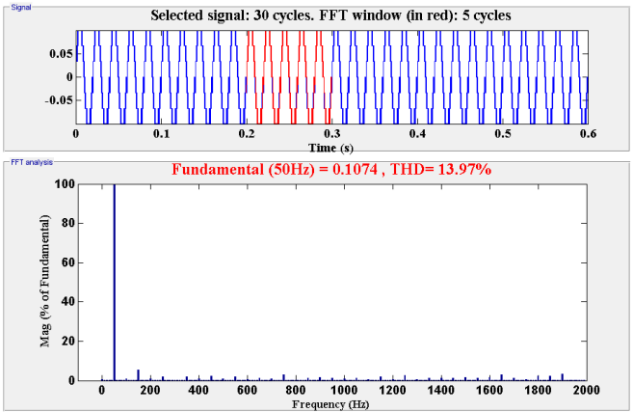

Fig.16 THD of Load Current with RL load- SVPWM

Load current obtained at the inverter terminals for RL load is shown in Fig.17 and Fig.18 shows the harmonic spectrum analysis of the load current. It is seen that current THD obtained is 3.86 %.

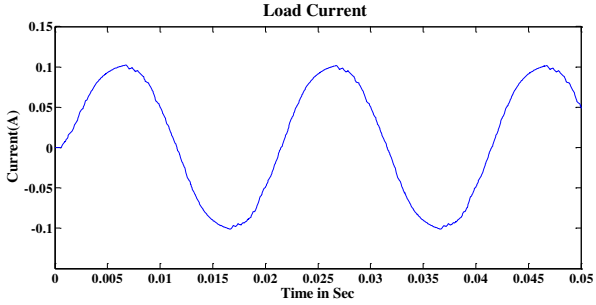

Fig.17. THD of Load Current with RL Load – SVPWM

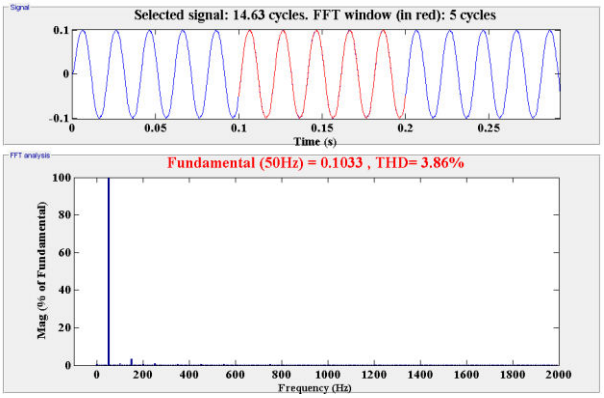

Fig.18 THD of Load Current with RL load SVPWM

7. Experimental Test Set Up

To validate the simulation results, a low power prototype of the model executed in the laboratory. MATLAB/simulink model developed to generate the switching pulses. dSPACE RTI 1104 used with MATLAB/simulink tool for real time interface to generate hardware switching pulses.

The seven level inverter shown in Fig.1executed with V_{dc1}=5V and V_{dc2}=10V. Fig.19 shows the block schematic and Fig.20 shows the photograph of experimental test setup which consists of a dSPACE platform for real time interface, driver circuit, inverter and the load.

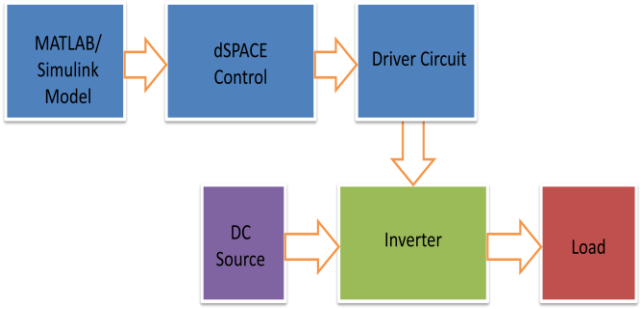

Fig.19. Experimental set up – Block Schematic

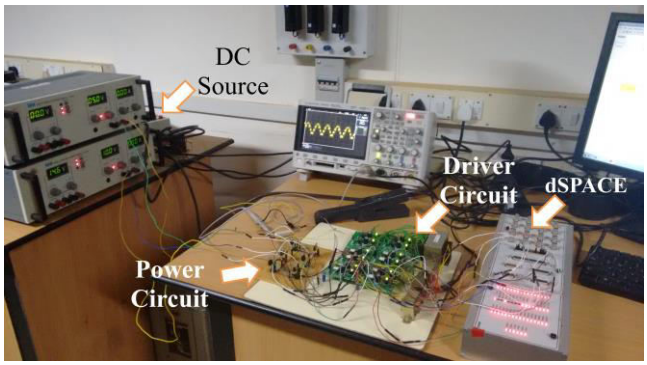

Fig.20. Experimental set up Photograph

The inverter is loaded with resistive load of R=150 Ω and inductive load of R=150 and L=20mH for analysis. Table.3 shows the components required and its specification for the experimental test setup.

Table 3 Hardware Requirements

SLNo:	Item	Specification	Quantity (for 1 phase)
1	MOSFET	IRF840 V_{DS} = 500 V I_D = 8 V	6
2	Opto isolator	TLP250 V_{CC} = 10-35 V I_O = 1.5 A	6
3	DC Voltage Source	5 V, 10 V	1 Each
4	Isolation Board	12 V, 500 mA	6 Isolated I/O
5	Resistor	150 Ω	1
6	Inductor	20mH	1
7	dSPACE Kit	RTI1104	1

8. Experimental Results of MLI with SPWM

The pulses are generated using SPWM techniques. The trigger signals produced for switches S1, S2 and S3 at the gate driver terminal is shown in fig.21, Fig.22 and Fig.23 respectively. Fig.24 and Fig.25 respectively shows the load voltage and load current obtained at the inverter terminals with resistive loading. Inverter output voltage consists of seven levels with equal steps of 5V and having frequency of 50Hz.

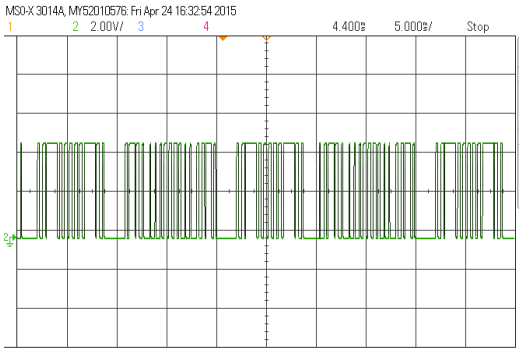

Fig.21 Pulse for Switch S_1-SPWM

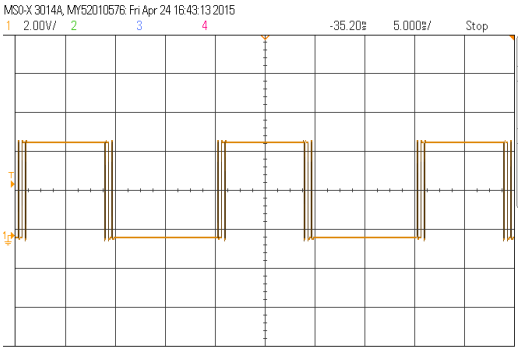

Fig.22 Pulse for Switch S_2-SPWM

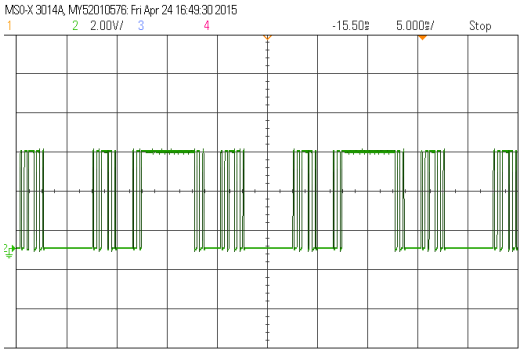

Fig.23 Pulse for Switch S_3-SPWM

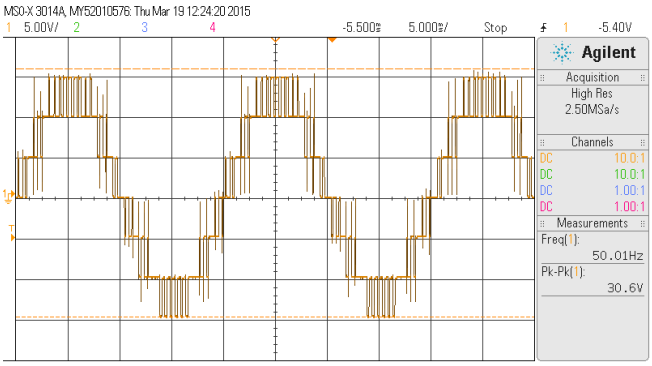

Fig.24 Load Voltage with R Load – SPWM

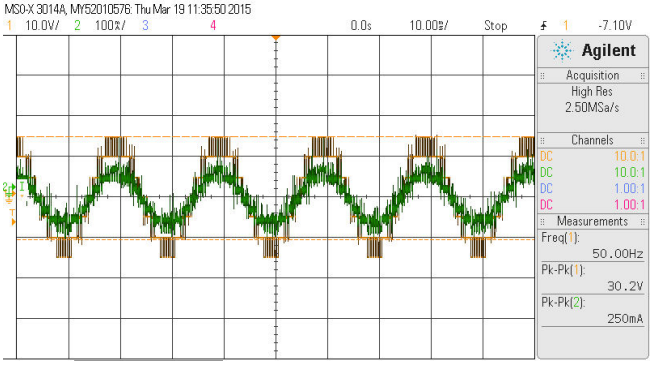

Fig.25 Load Current with R Load – SPWM

Fig.26. shows the harmonic spectrum analysis of the load current. Current THD obtained is 18.87 % and is in close agreement with the simulation result of the same.

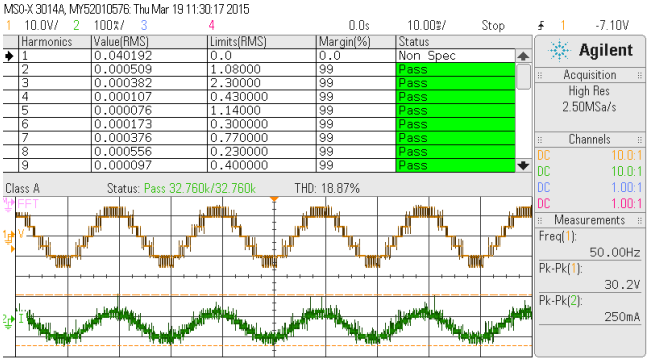

Fig.26.THD analysis of Load Current with R Load – SPWM

Fig.27 shows the load voltage and load current obtained at the inverter terminals with inductive loading.

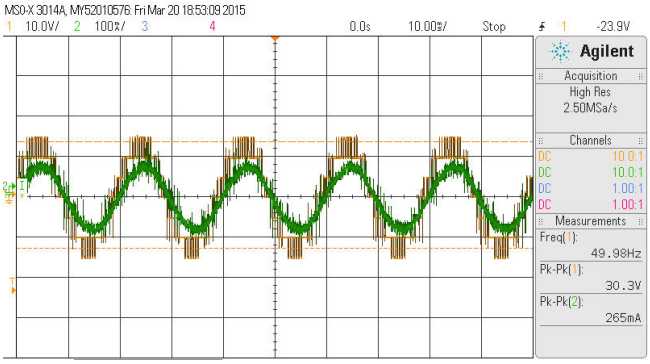

Fig.27.Load Voltage and Load current with RL Load – SPWM

Fig.28. shows the harmonic spectrum analysis of the load current with inductive load. The Current THD obtained is 5.89 %

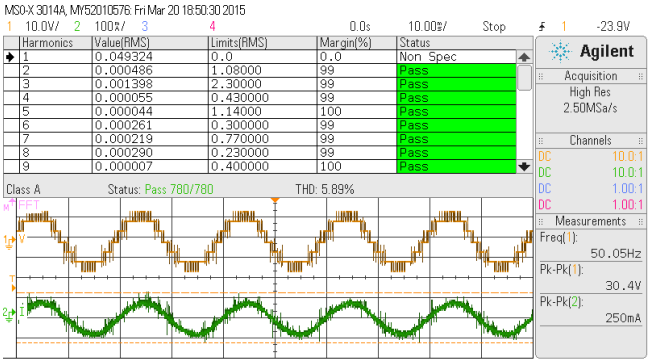

Fig.28.THD analysis of Load Current with RL Load – SPWM

9. Experimental results of seven level MLI with SVPWM

The pulses are generated using SVPWM algorithm. Fig.29, Fig.30 and Fig.31 shows the trigger signals produced for switches S_1, S_2 and S_3 at the gate driver terminal. Fig.32 and Fig.33 respectively shows the load voltage and load current obtained at the inverter terminals with resistive loading.

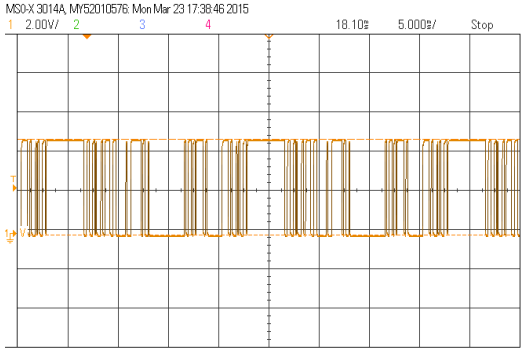

Fig.29 Pulse for Switch S_1-SVPWM

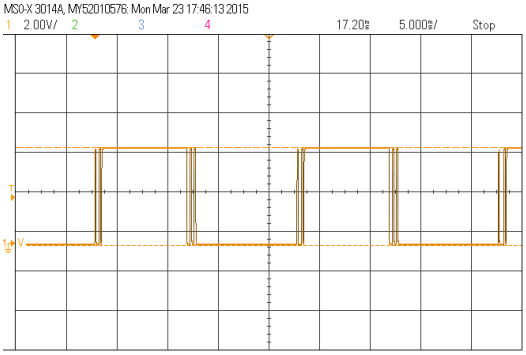

Fig.30 Pulse for Switch S_1-SVPWM

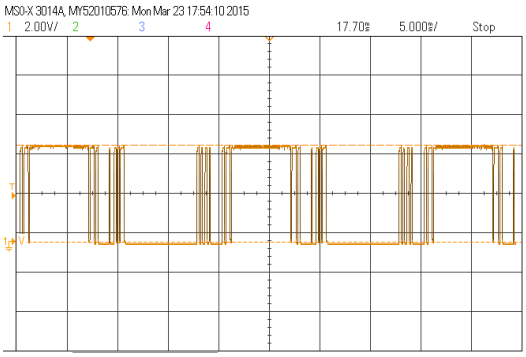

Fig.31 Pulse for Switch S_1-SVPWM

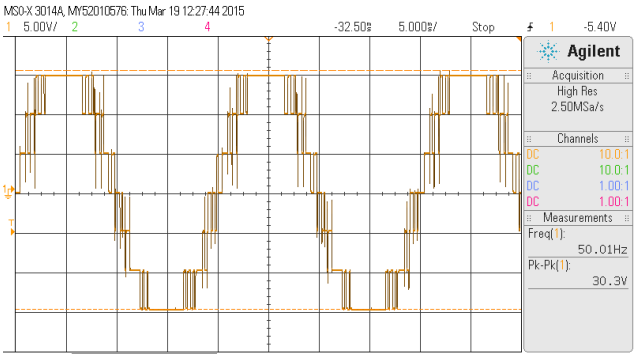

Fig.32 Load Voltage with R Load - SVPWM

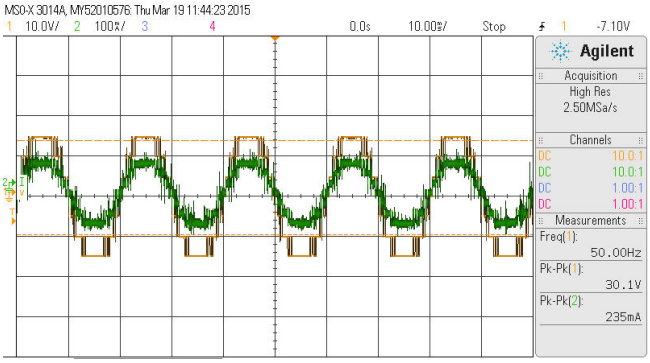

Fig.33 Load Current with R Load – SVPWM

Fig.34. shows the harmonic spectrum analysis of the load current. Current THD obtained is 14.14 % and is in close agreement with the simulation result of the same.

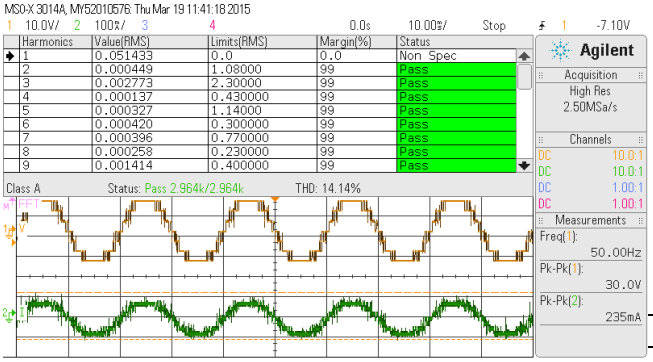

Fig.34.THD analysis of Load Current with R Load - SVPWM

Fig.35 shows the load voltage and load current obtained at the inverter terminals with inductive loading.

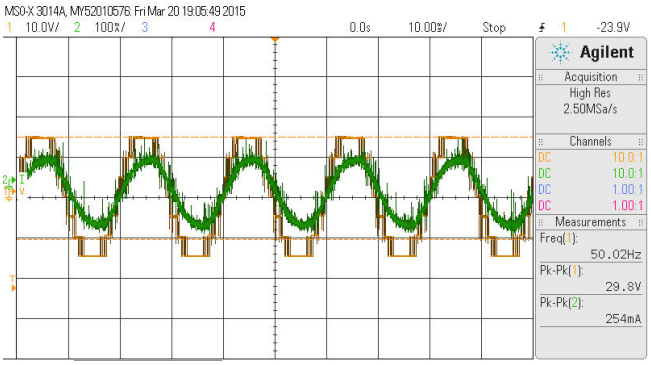

Fig.35.Load Voltage and Load Current with RL Load – SVPWM

Fig.36. shows the harmonic spectrum analysis of the load current with inductive load. The Current THD obtained is 5.19 %

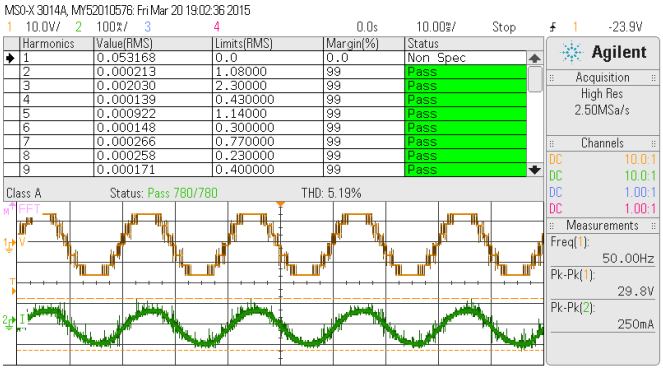

Fig.36.THD analysis of Load Current with RL Load – SVPWM

10. Result Analysis and Conclusion

Software and laboratory set up of MLI with sinusoidal PWM and Space vector PWM techniques done successfully. Table 4 shows a comparative analysis load current THD obtained with the simulation and experimental results.

Table 4 Result Analysis

	R Load		R - L Load	
	Simulation	Experiment	Simulation	Experiment
SPWM	18.82%	18.87%	4.39%	5.89%
SVPWM	13.97%	14.14%	3.86%	5.19%

The analysis is done with R Load and R-L Load. It can observe that space vector PWM algorithm offers lower current THD compared to sinusoidal PWM scheme in both simulation and experimental setup. Hence the effectiveness of the space vector PWM is verified.

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