DESIGN AND PERFORMANCE ANALYSIS OF SINGLE BIT FULL ADDER CIRCUIT USING HYBRID TECHNIQUE

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Abstract: *In this paper, an enhanced single bit full adder circuit is designed using hybrid technique. The hybrid technique is formed by replacing the n-MOS pull down network of constant delay logic with p-MOS pull up network. In the integrated design, the propagation delay of the signals which affect the performance of the circuit and the excessive power dissipation discourages their use in the systems. The glitches are a major component to increase the power consumption and delay in the complex circuit such as arithmetic operations. The proposed hybrid technique is used to remove the glitches in digital circuits which reduce delay, power and has high performance. Delay and Power–delay product is minimized than previous technologies. The 0.25um technology is used to design a circuit. The circuit simulated by using Tanner EDA Tool, 13v. The applied voltage is 1.0V. The simulation result illustrates that the hybrid design techniques have 27.8% of delay reduction compared to dynamic domino logic design and work at a speed of 0.499GHz.*

Keywords: *Single bit Full adder, Hybrid technique, Dynamic Domino Logic, Constant Delay logic, n-MOS pull down, p-MOS pull up network, Delay, Power.*

I. Introduction

In many VLSI Designs such as Microprocessors and Logic Circuits, Random Access Memories (RAMs), Application Specific ICs (ASICs) and Digital Signal Processors (DSP), addition is a basic arithmetic operation that is broadly used. The adder cell is also an element of multipliers, dividers, multiplier-accumulators (MACs) and address generation.

The overall performance of the digital circuits is determined by the adder circuit which is the crucial path and noticeable component in most of the applications. It is a great concern to build high performance single bit full adder cell.

To minimize the power consumption, the supply voltage appears is to be reduced. However, as reduce the supply voltage, the power delay product of the circuit decreases and the delay increases repetitively. It disgraces the drivability of cells designed with convinced logic styles. To design high performance single bit full adder cell the designers are faced with more constraints like reliability, high speed and low power consumption [6, 7].

To meet the growing demand, the new high speed and energy efficient full adder is proposed using hybrid technique.

This paper is organized as follows. Section 2 discusses the delay and power considerations. Section 3 follows the internal logic structure for the design of the existing full adders in the literature. Section 4 gives the internal logic design of the proposed hybrid technique. Section 5 deals the performance analysis of different logics. Section 6 draws the conclusion of the work.

II. Delay and Power Considerations

2.1 Time Delay

To measure the cell delay, one should consider the previous values of the inputs together with the current values. If the inputs are unchanged, the outputs will not

change, and accordingly no delay can be measured. Accurate measurements are obtained, if all the transitions from one input combination to another are tested, and the maximum is taken to be the cell delay.

2.2 Power dissipation

For analyzing full adder cell for power dissipation, consider only with dynamic power. This component depends on the input pattern applied to circuit, which will cause its transistors either to switch (consume power), or keep their previous state (no dynamic power consumed).

The dynamic power is described by the following equation

$$P_{dynamic}=V_{dd}.f_{clk}.\sum C_i.V_i.AF_i \quad (1)$$

Where,

V_{dd} is the supply voltage,
f_{clk} is the systemclock frequency,
C_i is the capacitance at node i,
V_i is thevoltage swing, and
AF_i is the transition activity factor.

The term (f_{clk}. AF_i) represents the number of transitions at node **i** (n_i).Fair comparison of power consumption, n should be the same for all the input nodes. This is to provide uniform switching activity [**6**].

III. Previous Full Adder Designs

Many papers have been discussed in literature regarding full adders. In this paper, the Dynamic Domino logic (DDL), Complementary Pass transistor Logic (CPL), Feed through Logic (FTL), Compound Domino Logic (CDL) and Constant Delay (CD) Logic designs of full adder are studied.

The static, dynamic domino logics are mainly used for designing the CMOS logic circuits. The dynamic domino logic is used to avoid the glitches. The invention of dynamic domino logic in 1980s, it allows the designer to design a high performance block such as addition at an operating frequency [**2**]. The static CMOS and pass transistor logic does not achieve the better result. Several variations of dynamic domino logics are used to design the circuit such as NP domino, zipper domino, dynamic data driven logic [**3**]. The disadvantage of dynamic domino logic is, Due to switching activity, it has excessive power dissipation and requirement of inverters during the cascading of logic blocks. Feed Through Logic (FTL) [**8, 9**], has been proposed to improve the speed and power of the CMOS logic circuits.

Dynamic and static gates are alternating between each other in Compound Domino Logic (CDL), All the dynamic stages can be footless in CDL expect the first stage, If conducting complex logic operations without wasting the one inverter delay then it satisfies the monotonicity requirement by replacing output inverter with a more complex inverting static gate (NAND).[4]

The major disadvantage of Compound Domino Logic is power consumption to be increased high due to the possible significant path and it has reduced noise margin and excessive power dissipation. The first generation of FTL exhibits. Constant Delay (CD) logic is the combination of a local window technique and self reset technique. Compound Domino Logic is not energy efficient to implement any system with Compound Domino logic. The critical path in any circuit block is replaced only when it is used. To identify these problems, high performance technique has been proposed. In this paper, the existing logic styles are beats by the proposed logic with high performance design.

IV. Design Methodology

4.1 CD Logic

The schematic of CD logic is shown in **Fig. 1, 2**. Static power dissipation is reduced with the help of Timing Block (TB) that creates an adjustable window period. The unwanted glitch is reduced and also makes cascading is possible with help of Logic Block (LB).In CD logic a buffer is inserted between TB and LB. The output of dynamic domino logic gates is IN signal which is given to NMOS Pull down Network. While CLK is “Logic High”, Compound Domino Logic pre discharges the signals X and Y to GND. While CLK is “Logic Zero”, Compound Domino Logic goes for the evaluation period. This sequence of events occurs specifically, the contention, C-Q delay and D-Q delay. X and Y will go to “logic high,” if CLK_d reach a higher value much previous than X and

Y and turn off the M1. The outcome of this state is a calculation of the logic is false. It resolves back to "logic zero". Y will initially rise, if CLK_d reach a higher value slower than X, and considerably turn off the M1. The outcome of this state is a calculation of the logic is true. [**1**]

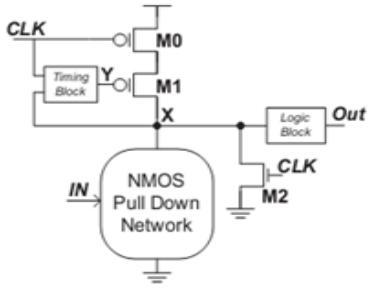


Fig. I. Block diagram of CD logic buffer.

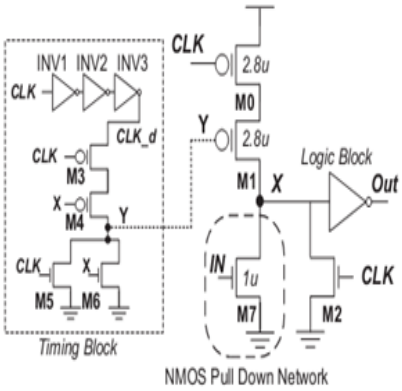


Fig.II. Buffer circuit using CD logic**.**

4.2 Proposed technique

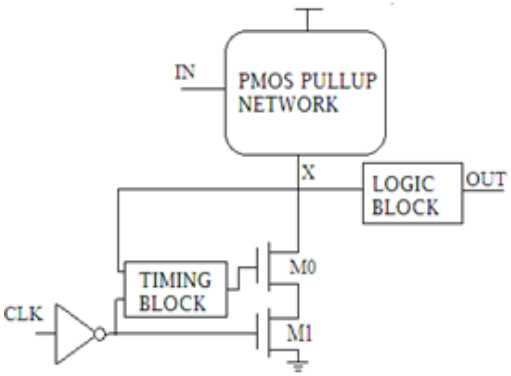


Fig.III. Block diagram of hybrid technique.

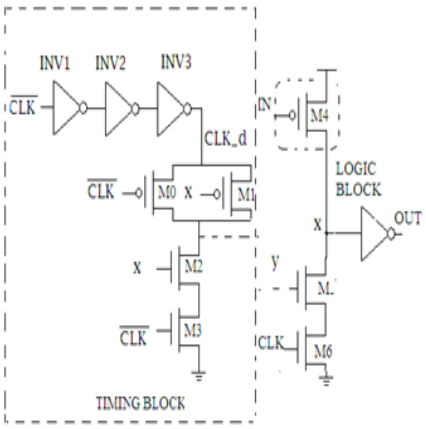


Fig. IV. Buffer circuit using hybrid technique.

The proposed logic is designed by replacing the n-MOS pull down network of constant delay logic is p-MOS pull up network. The hybrid logic is proposed with a schematic Timing block (TB) which reduces the static power dissipation and the unwanted glitch is reduced and also makes cascading is possible with help of Logic Block (LB). **Fig. 3, 4 shows** the block diagram and buffer circuit using hybrid technique. While CLK is "Logic zero", Hybrid Logic pre discharges the signals X and Y to GND. While CLK is "Logic high", the hybrid logic enters the estimation period. The IN remains constant when the clock is logic high which causes exposed to occurrence a momentary glitch where X is at a nonzero voltage level. The local window width is used to calculate the duration of this glitch. The delay between CLK and CLK_d. is called duration of the glitch. When the contention period is over, and the temporary glitch at output is ignored if X remains "logic low", then Y becomes to "logic high". When IN is "0", the evaluation period starts and perform the given operation. The clock circuit consists of using static CMOS NAND gate and tapered inverter chain. The NAND gate is better than the NOR gate because the parallel PMOS reduce the power consumption. The chain of inverter helps to avoid the glitches in the circuit. The hybrid logic obtained the minimum delay due to the tapered inverter chain method. The advantage of hybrid technique is to obtain the minimum delay and power consumption (shows in **Table 1**).

V. Performance Analysis

The 0.25um technology is used to design a circuit. The circuit is simulated using Tanner EDA Tool, 13v. The applied voltage is 1.0V. And a clock speed of 0.499GHz.

5.1 Existing method

5.1.1 Dynamic Domino Logic

In this circuit there is no direct path between VDD and GND and discharge of transistor depend on the clock signal. In dynamic domino logic circuit when clock is low it's a pre charging phase at this point dynamic node is charge up to VDD, when clock is high known as evaluation phase then according to the input values V(A),V(B),V(C) get the output(V(SOUT,COUT) of full adder. **Fig. 5, 6** represents the schematic diagram and output waveform of the dynamic domino logic.

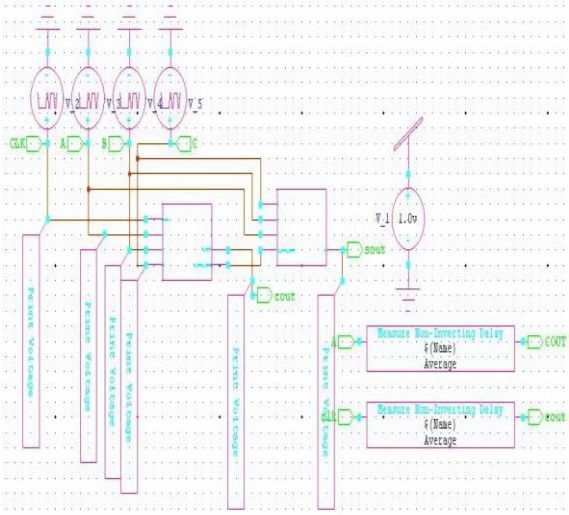


Fig.V. Schematic diagram of Dynamic Domino Logic

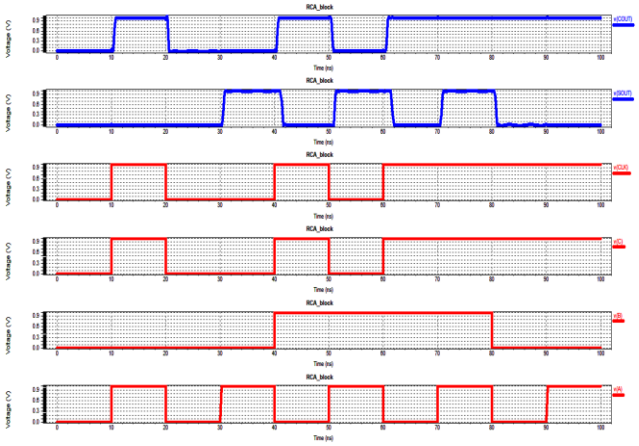


Fig.VI. Output waveform of Dynamic Domino Logic.

5.1.2 Constant Delay Logic

SUM section is mainly designed using DPL logic style and
CARRY section is designed using Constant delay logic style.

SUM Section: In DPL logic, redundant transistors are eliminated by different logic gates that are made of less number of transistors. Usage of pass transistor is attractive as lesser transistors are needed to execute vital logic functions, the requirements are smaller capacitors and smaller resistors, and this is much faster than the existing CMOS. Instead of switches connected directly to supply voltages, the logic levels are passed between nodes of a circuit then transistors are used as switches. **Fig.7** represents the circuit diagram of Constant delay logic. (Sum section)

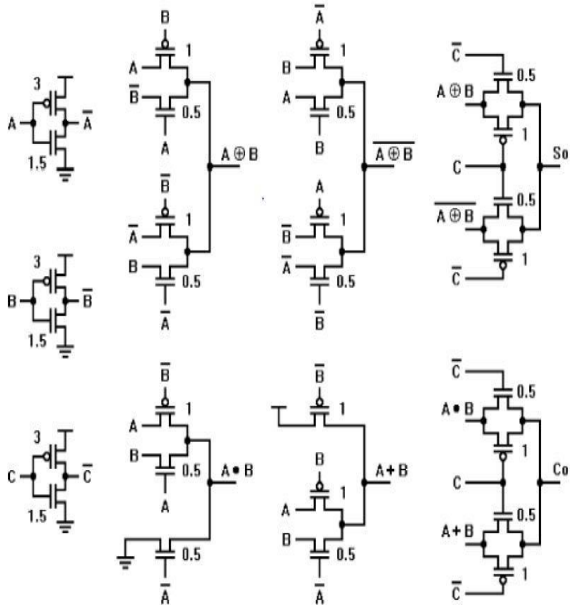


Fig. VII. Circuit diagram of Constant Delay Logic (Sum section)

CARRY Section: Constant delay logic circuit is used in CARRY section. Carry section is designed and simulated its result using constant delay logic. When CLK=1, circuit enters in pre discharge mode and CARRY is always 1 and when CLK=0 then Circuit enters in evaluation mode which is helpful and taken into consideration. So, always check the result of CARRY section on when CLK=0. **Fig. 8, 9** represents the schematic diagram (Carry section) and output waveform of the constant delay logic.

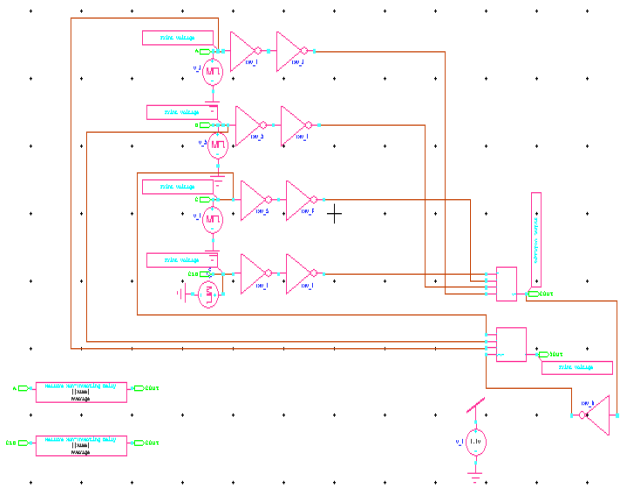


Fig.VIII. Schematic diagram of Constant Delay Logic

(Carry section)

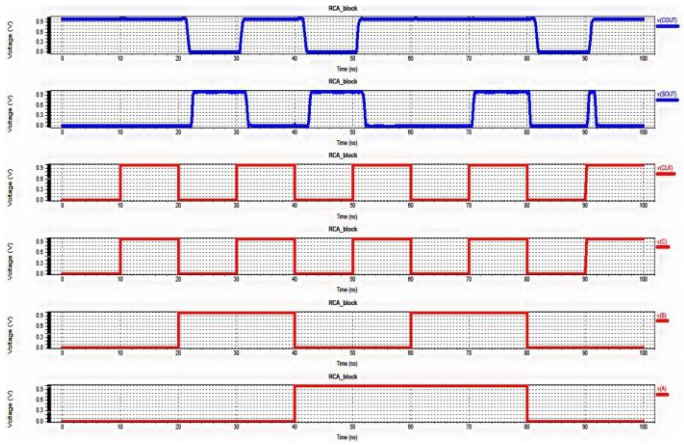


Fig. IX. Output Waveform of Constant Delay Logic.

5.2 Proposed method

Hybrid logic full adder is designed using two blocks such as sum block and carry block. The sum block is designed using a static logic because the sum output is not given in different stages. The carry is one of the input given to the next stage full adder. The schematic diagram of hybrid technique is shown in **Fig. 10**.

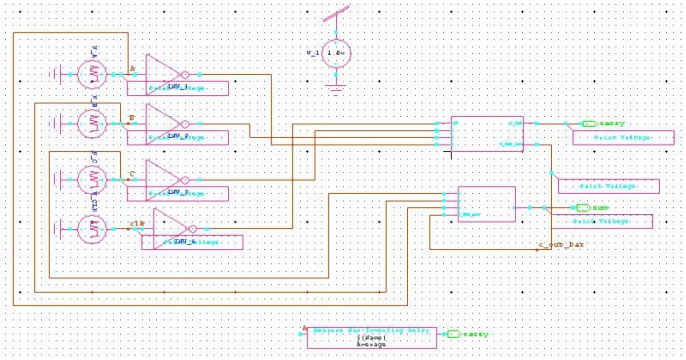


Fig.X. Schematic diagram of Hybrid Technique.

5.2.1 Carry Block

The carry block (**shown in Fig. 11**) consists of clock circuit and p-MOS pull up network. The full adder p-MOS pull up network is connected with the series NMOS device. The clock signal is connected only to carry block. The inverted input signal is applied to the circuit for adjusting the arrival time of the signals because the arrival time of the different signal is varied. The output of the circuit is inverted for eliminating the glitches in the circuit.

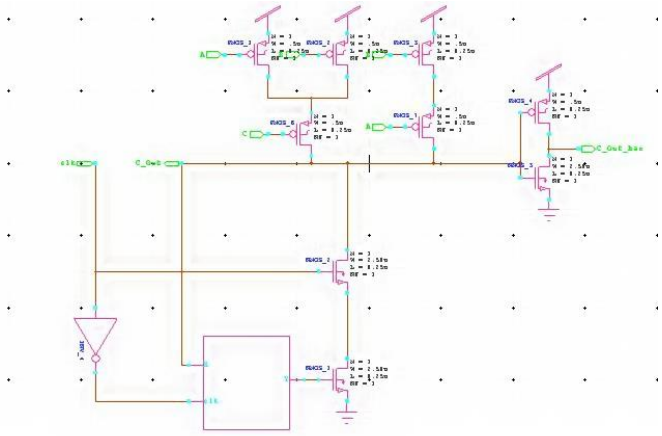


Fig. XI. Carry block of Hybrid Technique.

5.2.2 *Clock Circuit*

The Clock circuit (**shown in Fig. 12)** designed by using either NAND gate or NOR gate. The NOR gate has a series connection of PMOS and parallel connection of NMOS. The series connection of PMOS increases the power dissipation so the NAND gate is used to design the clock circuit. The tapered inverter chain is given to the

parallel connection of NMOS because it gives the minimum delay signal to the circuit.

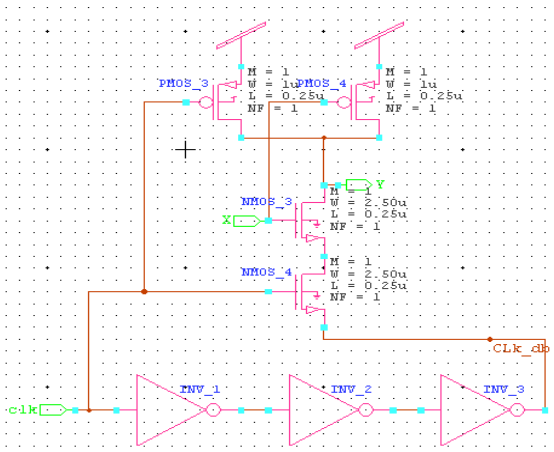


Fig. XII. Clock circuit of Hybrid Technique.

5.2.3 *Sum Block*

The sum block is designed using a static CMOS logic. The number of transistors is reduced in the logic. The inverter circuit is used for eliminating the glitches in the circuit. The sum output is not given to the next stage so it is designed using a static CMOS logic. The sum block of hybrid technique is shown in **Fig. 13.**

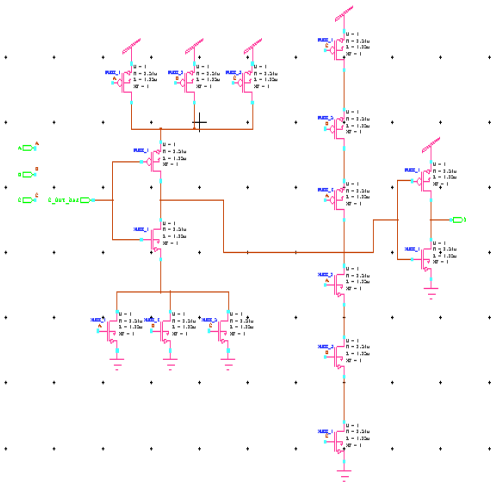


Fig.XIII. Sum block of Hybrid Technique.

5.2.4 Output Waveform

The **Fig. 14, 15** shows the output waveform and power and delay results of Hybrid logic in T-spice window respectively with three inputs (V(A),V(B),V(C)) and one clock signal. The clock signal V(CLK) acts as a control signal. The two outputs are denoted as V(COUT), V(SUM).

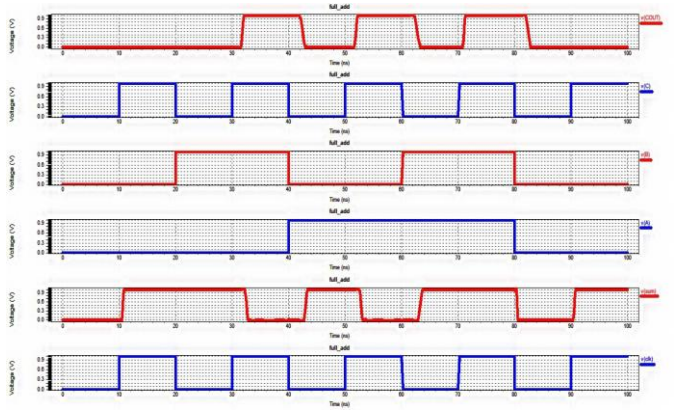


Fig. X IV. Output waveform of hybrid Technique

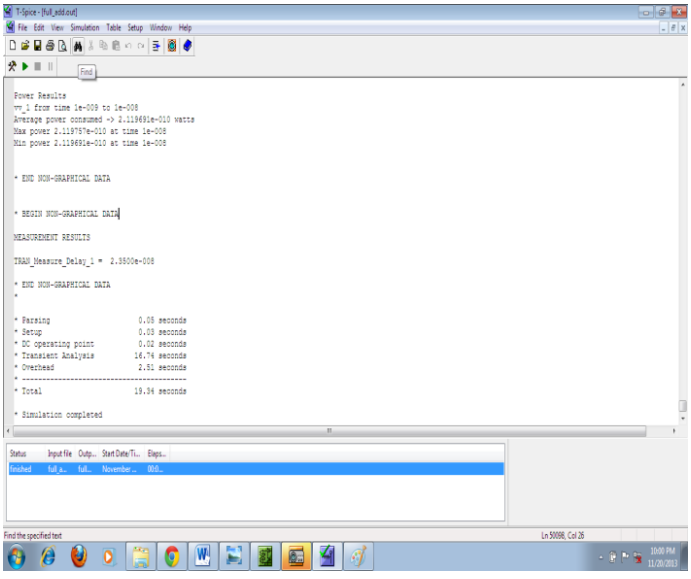


Fig. XV. Power and delay results of Hybrid technique**.**

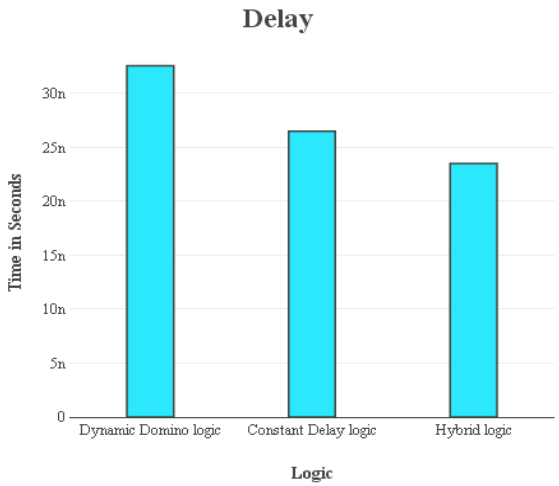
5.2.5 Comparison table and graph

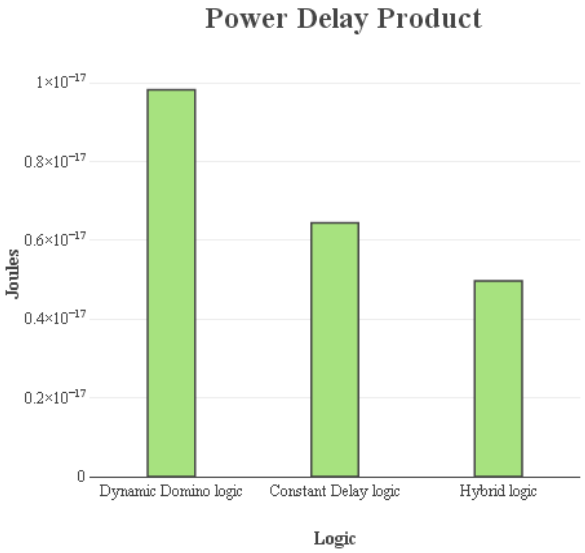
The comparison table (shown **in Table 1**) shows the different parameters of the dynamic domino logic, constant delay logic and hybrid logic.

Table 1: Power consumption, Delay and Power delay product comparison of different logics.

LOGIC	FREQUENCY (GHz)	SUPPLY VOLTAGE (V)	POWER CONSUMPTION (W)	DELAY (s)	PDP (J)
Dynamic Domino logic	0.499	1.0	**3.0162 e -010**	**3.2550e-008**	**9.8177 e-018**
Constant Delay logic	0.499	1.0	**2.4285 e -010**	**2.650e-008**	**6.4355 e-018**
Hybrid logic	0.499	1.0	**2.1196e -010**	**2.3500e-008**	**4.9747 e-018**

Table 1 gives the state-of-the-art comparison like power consumption, delay and power delay product. Various parameters of the comparison show that the proposed hybrid technique of 1 bit full adder design outperforms the previous designs with decrease in **27.8%** delay and **49.32%** energy efficient. **Fig. 16** shows the results of the different parameters of the existing and proposed design of single bit full adder.





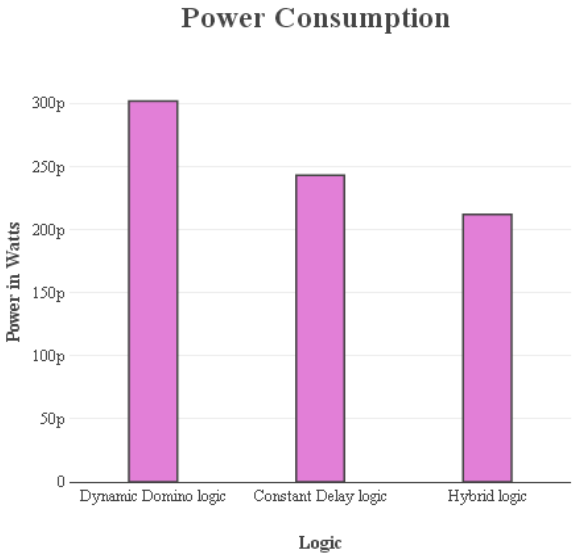


Fig. XVI. Power consumption, Delay and Power delay product when supply voltage at 1v and frequency at 0.499 GHz

The proposed design is consuming low power, low delay and low PDP and has better performance over existing designs shown in **Figure 16.**

VI. Conclusion

The high performance 1-bit full adder circuit has been designed using a hybrid technique which produces better result than existing design which includes the design of dynamic domino and constant delay logic. The 1-bit full adder circuit is simulated using Tanner EDA tool. The power consumption is minimized by using hybrid logic. The applied voltage of the hybrid logic was 1.0V. The delay in the circuit was in nano seconds and frequency is 0.499GHz. The future work includes the designing of high speed adder circuit using hybrid technique full adder. The carry look ahead adder is frequently used high speed adder in VLSI circuits. The 32 bit carry look ahead adder will be designed using hybrid technique with minimum power and delay.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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