A ROBUST DYNAMIC CONTROLLER DESIGN OF SYNCHROUS BUCK CONVERTER FOR EXTREME LOADED CONDITION

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Abstract:

Buck converters are the powering unit for consumer and medical electronics systems however they will have considerable switching and power losses. The power losses occurring on diodes in such converter can be avoided by designing Synchronous Buck Converter (SBC). In this proposed work two types of controller namely dual loop and Dynamic Evolution (DE) control is designed for SBC. Dual loop control has very faster response with very good set point tracking for normal load variations. But for drastic load variations or extreme load conditions; the controller performance of dual loop controller degrades. SBC with DE control however provides robust performance for drastic load variations. This robust performance measures are compared with Simulink as well as hardware results. In this paper, the drastic load changes are designed in hardware circuit using a programmable switch to create a load variation environment and the SBC with proposed DE controller is tested for robustness in this environment. The efficiency of proposed controller has been found to be greater than any conventional converter with satisfied performance measures.

Keywords: *PI, PID, Dual Loop Control (DLC), Dynamic Evolution Controller (DE), Robust control, synchronous buck converter (SBC).*

1. Introduction

Consumer electronics, communication systems and medical electronics has made dc-dc converters as essential power source especially a buck topology [1-3].On board voltages 3.3, 5 and 12 V has made the application of buck converter world-wide due to its high-quality, reliability, compact size and efficient adaptive nature. Buck converters and synchronous converters are most commonly used as step down switching converters due to its high efficiency and compact size [1,7] and ousted the output power linear voltage regulators. Due to parasitic components such as (i) Equivalent Series Resistance (ESR), (ii) Equivalent Series Inductance (ESL) there is a need for closed loop control architecture in a buck converter topology. Initially, Proportional Integral (PI) controllers were employed to improve the closed loop performance of buck converters and found to have better tracking control [2]. The PI controllers were found to have restriction in allowable over shoot for specific applications. In order to avoid the above said problem, state space controllers were explored. The state space controller for buck converter has fast transient response and guarantees better dynamic performance.

Switching converters are time variant and nonlinear due to parasitic nature of inductor, capacitor and switching operation. Linear control technologies are state of art technology and so many classical approaches are developed in both time domain and frequency domain. But controller performances deteriorate under various disturbances in the dc–dc converter circuit. However, nonlinear control is a highly interesting research domain fast emerging with techniques such as back stepping control, adaptive control; model predictive control [6], sliding mode control [13-14], fuzzy logic control [5]and optimal control.

Literature surveys show that PID is not uncommon in the feedback control of dc-dc converters and 97% regulatory controllers are PID controllers. However the derivative part of PID always injects high frequency noise into the closed loop path due to ESR, ESL of the filter capacitor. These parasitic properties cause large over shoot and undershoot during the large signal transient. Discrete jumps occur during small signal transient due to ESR during the switching transition with an alternation. This discrete jump makes the derivative gain added to improve the phase margin inadequate [4].The dc–dc converters are nonlinear and time varying due to nonlinear magnetics of the inductor parasitic elements ESR and ESL [5].

The system uncertainties are not included while designing the controller. The characteristic requirement of good controller is to have faster dynamical response, smaller steady-state error, lower overshoot, and milder noise susceptibility in addition to the above it should have high input and output disturbance rejection ration and would uncertainty attenuation ability. So controller design needs to include parameter uncertainties in plant models due to modelling errors, variation in operating conditions, uncertainty due to sensor measurement noise and so on [6]. Reference [7] has proposed a dynamic evolution control for synchronous buck converter to reduce error signal exponentially as a function of time. This controller's superiority over conventional PI and cascaded control structure for voltage tracking for various load change is discussed [7]. Oliva et.al [8] have developed a DSP based control algorithm for synchronous buck converter (SBC) which will superimpose a small control signal to the reference value of the control parameter at each switching cycle in order to cancel out the perturbations. This control strategy is applied SBC for different load conditions and selecting closed loop poles for a desired transient response. Synchronous buck converter for an electrolysis process is proposed by Sahin et.al and this process requires 2 V and 25 A which is produced from 12 V input by the synchronous buck converter through PIC 16F877 micro controller. Synchronous buck converter is used to reduce conduction loss of the converter [9]. Time-optimal digital (PTOD) control is proposed in paper [10] which combines control of linear or nonlinear switching surface with standard linear PID control to have advantages of arbitrary load disturbances and parameter variation of components. Yang et.al has proposed a novel resonant gate drive circuit for synchronous buck converter to reduce both switching loss and gate drive loss [11]. In this drive MOSFET input capacitor is charging and discharging through constant current. In addition to this advantage this drive is simple in design, less influenced by parasitic inductance and better *dv/dt* turn on immunity. Parametric uncertainties such as variations in operating temperature, system load, line resistance and system modelling uncertainties affects the robust stability margin of the dc/dc buck converter which is overcome by a robust controller using μ synthesis [12]. The sudden load changes introduced by modern processors make the dynamic response of a conventional power-supply system too slow to track the changes, so dynamic response of power supplies is so significant in this respect [2].Reference [15] have introduced an auxiliary circuit for the synchronous buck converter to provide zero-current, zero-voltage switching conditions for the main and synchronous switches while providing zero-current condition for the auxiliary switch and diodes.

The power converter requires very tight output voltage regulation during change in supply and load conditions. This enforces challenge of very good controller to meet the parameter variations. Conventional PID controllers use single loop voltage control as feedback loop. The demand of parameter variations, large supply and load variations, non-linearity in the converter operation makes PID controllers are not suitable. The ideal characteristic of a controller is to operate at an infinite switching frequency while tracking reference signal to achieve the better performance for both dynamic as well as steady state operation [3]. This extreme switching frequency of power converters leads to high switching losses, core losses in inductor and transformer, and electromagnetic interference (EMI) problems. The commercially viable analog controllers use P or PI control with voltage feedback in control loop. The compensator is designed based on phase margin criteria and location of roots depends on the root locus technique. To place the poles in any arbitrary location feedback should be applied on all the state variables [4].Current mode controllers are independent of current or voltage loops and apply feedback on both states. Hence the pole location is limited to root locus technique.

The classical PID controllers are well established concept however efficient tuning parameters are always hard to achieve. Also, with classical PID controller, tuned parameters will not vouchsafe for all working environment such as drastic variation of input and output voltage and sensors noises (i.e. current and voltage sensor) in the feedback loop. The dual loop which provides faster current loop and outer voltage loop for good tracking performance and dynamic error control algorithm which forces the error signal in decaying path and achieving faster control are explored here. SBC is designed instead of ordinary Buck converters which reduces considerable power loss

in the diode. In this paper, SBC with Dual loop controllers are designed and realised using hardware circuits and found to produce much faster controller response due to faster inner current loop [1]. However, it was found that, the dual loop controller performance degrades as the loading pattern varies drastically. These drastic load variations are achieved using programmable switches and load combination in both Simulink and hardware. The drawback of dual loop controller for SBC leads to a requirement of a controller with simplified structure to carry over the satisfied control performance and also to meet out extreme load patterns. Hence, in the proposed work, a dynamic control structure namely DE controller that has inherent PID nature in its control equation and can provide very satisfied control performance even for drastic load varying conditions is designed. The SBC with DE controller is found to produce better set point tracking performance with better output rejection along with robustness to extreme load variations. This DE controller for SBC is realised with both MATLAB Simulink and hardware circuits to compare with the dual loop controller performance and found to produce lesser peak overshoot and better efficiency.

This paper is organised as section 2 discusses the problem formulation for a synchronous buck with dual loop control. In the following sub sections 2.1 dual loop structure, section 2.1.2 - 2.1.3 describes the PI with outer voltage loop and inner current loop design respectively. The controller design with dual loop for SBC is given in section 2.1.4. The various process of design steps are discussed in section 3. The results and discussions are given in section 4 and hardware results in section 5 and finally follow the conclusion in the last part of this paper.

2. Problem formulation

In this proposed work two control schemes are considered dual loop control and dynamic evolution control for synchronous buck converter with extreme load variation conditions. Buck converters of (3.3V, 6Vand 12 V etc.) are very universal in consumer and medical electronics applications. However a loss occurring in buck converter freewheeling diode is substantial which in turn reduces the efficiency of the converter. The synchronous buck converter differs from conventional buck converter by freewheeling rectifier, usually a Schottky device, is replaced by a power MOSFET, main switching device is usually a power MOSFET and is driven in the same manner as in a traditional buck converter which increases the conversion efficiency. The important design issue involved in the SBC is cross-conduction of the two power MOSFETs i.e., turning on of both MOSFETs simultaneously. So it requires a small amount of dead time is necessary between consequent switching.

2.1. Dual Loop control structure (DLC)

Any second order converter can be designed as a cascaded structure of two first order systems representing current and voltage dynamics. The inner current loop and slower outer voltage loop. Designing PI or PID controller for this cascade structure is much simpler than considering the complex second order systems [1-5] and the state space equations of second order system is given by

$$L\frac{di_L}{dt} + V_o(t) = \delta(t)V_i(t) \qquad (1)$$

$$C\frac{dV_o}{dt} = i_L(t) - \frac{V_o(t)}{R} \qquad (2)$$

In equation (1) and equation (2), $i_L(t)$ is inductor current, $V_o(t)$, $V_i(t)$ are output and supply voltage, L , C is the inductance, capacitance respectively, $\delta(t)$ is the duty cycle of the converter. Excessive oscillation is produced in the feedback control loop due to the variation of supply or load voltage. To limit this oscillation, either the proportional P controller or Proportional plus Integral PI controllers with small value of proportional gain is set. Derivative control is not often used in order to avoid high frequency switching noise. Proportional controllers result in very swift output response but with higher steady-state errors. However PI results slower response with zero steady-state errors. The equations (1)-(2) provides necessary voltage and current dynamics respectively.

2.1.2. Outer voltage loop dynamics

The outer loop is voltage feedback loop with slower in control action. The transfer function of outer voltage loop is the ratio of the output voltage $V_o(t)$ to the inductor current $i_L(t)$ in ' s ' domain [1] is given in equation (3)

$$G_{vc}(s) = \frac{V_o(s)}{i_L(s)} = \frac{R}{RCs+1} \quad (3)$$

The classical PI structure [1] is given in equation (4) as

$$G_{VPI}(s) = \frac{K_V(R_oCs+1)}{R_o s} \quad (4)$$

In equation (4), K_v, R_o are gain coefficient and output load resistance. Using equation (3)-(4) the closed loop transfer function is

$$H(s) = \frac{G_{vc}(s)G_{VPI}(s)}{1+G_{vc}(s)G_{VPI}(s)} \quad (5)$$

The second order characteristic equation formed from the closed loop path is given as

$$\nabla(s) = R_oRCs^2 + (R_o + K_vR_oRC)s + K_vR \quad (6)$$

$$\nabla_s(s) = s^2 + 2\varsigma w_n s + w_n^2 \quad (7)$$

Comparing equation (6) with standard classical second order system in equation (7) the following results are obtained. The un-damped natural frequency is

$$\omega_n = \sqrt{\frac{K_v}{R_oC}} \quad (8)$$

$$K_v = \frac{1}{R_oC} \quad (9)$$

2.1.3. Inner current loop dynamics

The inner current loop dynamics is given in equation (1) based on this control loop is designed. The slower voltage loop generates the current reference command for this loop. Current loop is much faster than outer primary loop. So the output voltage $V_o(t)$ is considered as constant load disturbance. The PI control for the constant disturbance takes the form of

$$G_{PC} = \frac{K_c(Ts+1)}{s} \quad (10)$$

$$T = \frac{2}{N\omega_n} = 1.6 \text{ x } 10^{-04} \quad (11)$$

For better performance the inner loop should be at least four times faster than the primary voltage loop. The un-damped natural frequency is related between voltage and current loop's as given below

$$\omega_C = N\omega_v = \sqrt{\frac{K_oU_i}{L}}, \quad N \geq 4 \quad (12)$$

ω_C and ω_v is un-damped natural frequency current and voltage loop respectively in equation (12).The gain of the current loop is given as

$$K_c = \frac{N^2\omega_n^2 L}{U_i} \quad (13)$$

2.1.4. Dual loop Controller design for SBC

The transfer function for the SBC is given in equation (14).

$$G_{synb}(s) = \frac{240 * 10^7}{s^2 + 625s + 5 * 10^6} \quad (14)$$

The PI controller is designed for voltage loop [1] using the equation (4) and (8) to (9) is given as,

$$G_{VPI}(s) = 0.25 + \frac{156.25}{s} \quad (15)$$

The Table 1 gives the value for the SBC converter taken from [7]. Let N= 20 i.e. the current loop dynamics is 20 times [1] faster than outer primary loop. The PI control structure [1] using equation (10) – (12) for inner current loop is

$$G_{CPI}(s) = 0.2604 + \frac{1628}{s} \quad (16)$$

Table 1 Component values for SBC

S. No	Particulars	Value
1	Input voltage	50V
2	Output voltage	13.8 V
3	L	0.5 mH
4	C	400 µF
5	R_o	4 Ω

The primary voltage loop and faster current loop controller transfer function are given in equation (15) and equation (16) respectively. Figure 1 shows dual loop controller for SBC comprising of inner current loop and outer voltage loops. The transfer function of the synchronous buck converter is given in equation (14).

3. Dynamic evolution control

In any dc-dc converter capacitor voltage and inductor current are dynamic parameters to be controlled to stabilize any abnormality occurring in input and output voltage parameters. Let us define converter dynamics by [7]

$$\varphi(t) = Ae^{-\beta t} \quad (17)$$

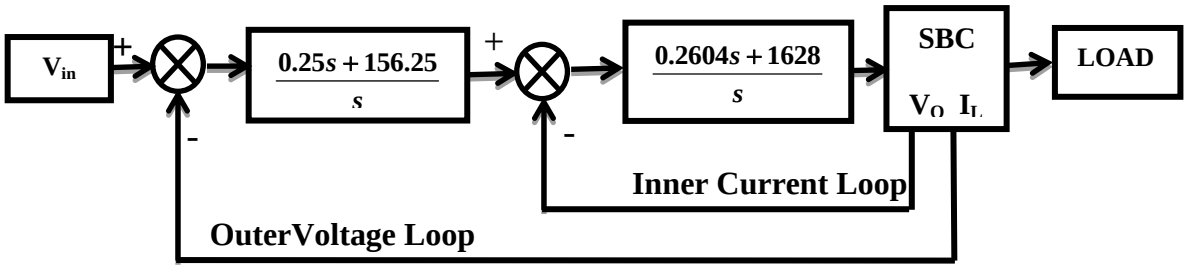


Fig.1. Dual loop controller for SBC

Any abnormality of the converter dynamics is made to reach zero i.e. $\varphi(t)=0$, and the decay rate depends on the parameter β and A be the initial value of the function $\varphi(t)$.

$$\frac{d\varphi(t)}{dt}+\beta\varphi=0 \quad \text{and} \quad \beta \succ 0 \qquad (18)$$

The converter dynamics $\varphi(t)$ is forced to follow the evolution path that is decaying exponentially to zero as a function of time. It is aimed to obtain duty cycle of the converter δ(t) as function of states of the output voltage V_o, input voltage V_{in}, and the inductor current I_L.
Using equations (1) and (2)

$$V_o=\delta V_{in}-L\frac{dI_L}{dt} \qquad (19)$$

The error voltage is taken as a dynamic component

$$\varphi(t)=mV_{error} \qquad (20)$$

$$V_{error}=V_{ref}-V_o \qquad (21)$$

$$m\frac{dV_{error}}{dt}+m\beta V_{error}=0 \qquad (22)$$

Utilizing equations (17) - (22) applying some algebraic manipulation the duty cycle δ(t) is obtained by

$$\delta(t)=\frac{m\frac{dV_{error}}{dt}+\beta mV_{error}+V_o+L\frac{dI_L}{dt}}{V_{in}} \qquad (23)$$

3.1 Controller design DEC for SBC

The duty cycle δ(t) invokes the controller dynamics in such a way that the dynamics of capacitor voltage and the inductor current are stabilised. The set point tracking of output voltage V_o is made to track reference voltage of 13.8 V even though the input and output dynamics are changing. The control action provided by equation (15)-(16) of dual loops are giving faster response however not sufficient for drastic load conditions of converter. The controller represented in equation (23) inherently has PID action if one carefully observes the equation. The structure of the implemented controller is shown in Figure 2, with output feedback signals. The capacitor voltage which is the output voltage V_o and inductor I_L are taken as feedback signals for establishing controller action.

4. Results and discussion

The controller design scheme for SBC is implemented in MATLAB R10a Simulink in an Intel(R) Core (TM) i3-2328M CPU with 2.20GHz processor. The SBC in the proposed work operates at an input voltage of 50 V and output voltage of 13.8 V which is meant for 12 V battery charging applications.

The simulations of SBC are carried out for two control actions, as given in equations (15) - (16) for dual loop controller and equation (23) for DE controller. Implementing both the controller for set point tracking as well as output load rejection against robust control performance measures such as peak overshoot, under shoot, settling time, rise time are observed.

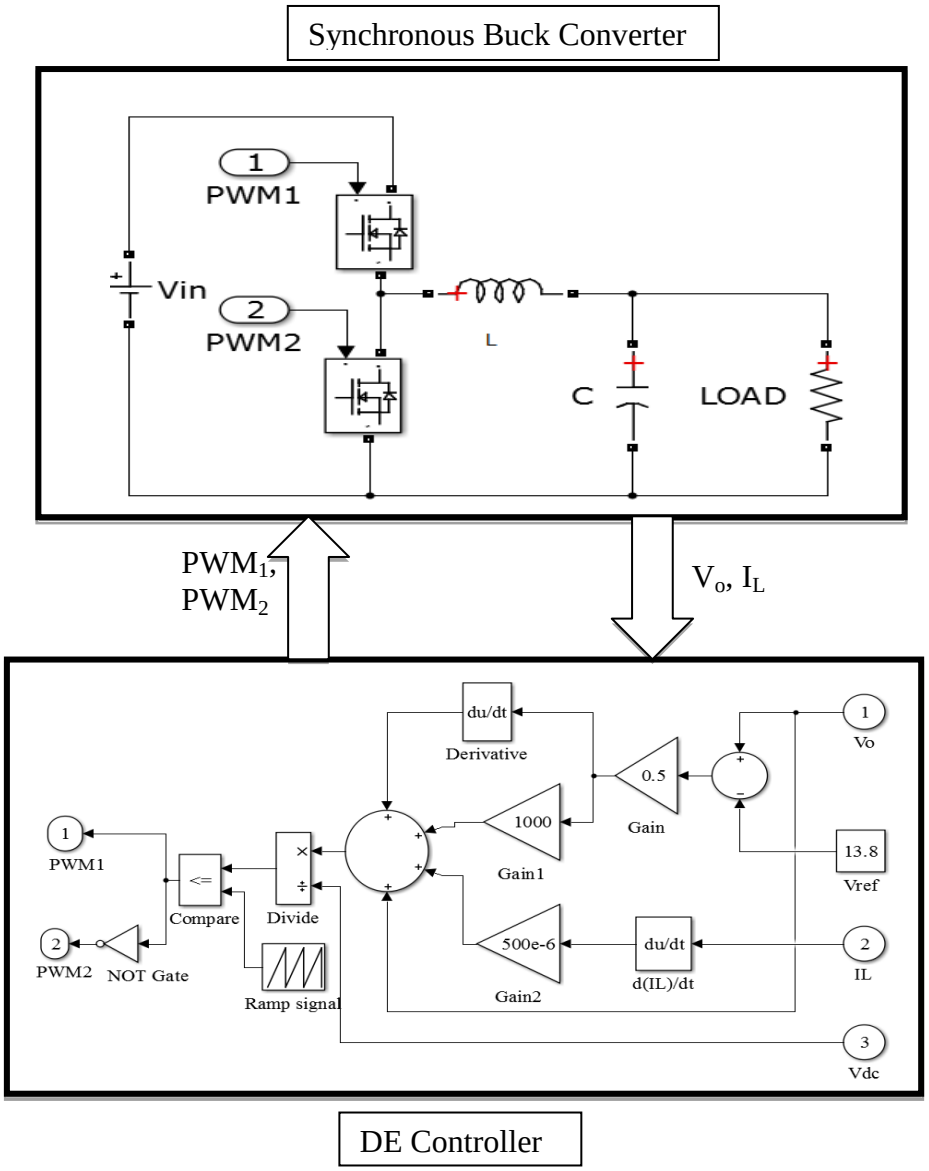


Fig.2.Dynamic Evolution controller with output load rejection for SBC

4.1 Step change of load variations

The control action for SBC is studied for drastic variation of load condition in order to test the robustness of the proposed control scheme. Different extreme loading conditions are simulated and categorised as four cases as given in Table 2.

Table 2 Load variations for dual loop control for SBC

Samples	Load Variations %	Load values Ω
Case1	100-200	4 -8
Case2	100-200-400	4 -8-12
Case3	100-400	4-16
Case4	100-50	4-2

The load is changed as step load pattern at each 200 msec. This is implemented by means of switching the programmed load pattern both in MATLAB Simulink as well as in hardware implementation. This load pattern is chosen in-order to show the competence of the robustness of a controller for SBC.

4.2. Simulation results for SBC with Dual Loop control algorithm

The SBC is implemented with dual loop controller for extreme loading conditions as given in Table 2. Output voltage with peak overshoots and undershoots corresponding to the step load variations for case 1 and case 2 are given in Figure 3a and Figure 3c respectively. Similarly the peak

overshoots and undershoots in output voltage for case 3 and case 4 are given in Figure 4a and Figure 4c respectively. The controller tracks the reference voltage with reduced peak overshoot, undershoot, and settling time even though load patterns is changing abruptly.

Figure 3a shows the output voltage overshoots to 14.1 V and settles in 5 msec, to the 13.8 V. The inductor current is 4.1A from 0-0.2second after that it comes to 3.5A 0.2-0.4 second which is shown in Figure 3b.The output voltage is tracked by controller to reference voltage however there will be peak and under shoots are present, the numerical values are mentioned in Table 3. The load pattern for case 2 is 4Ω-8Ω-16Ωthis periodic step change of load pattern is switched at constant interval of every 200 msec.

Table 3 Performance of Dual Loop and DE control

Samples	Over-shoot		Under shoot	
	Dual loop	DE	Dual loop	DE
Case1	12.1	1.80	0.72	0.50
Case2	12.31	1.88	1.45	0.60
Case3	24.63	15.94	2.89	0.70
Case 4	36.57	30.43	0.72	0.72

The load pattern is 4Ω-16Ω-4Ω i.e. 100-400% step load variation is given for case 3. Figure 4a and 4b shows the output voltage and inductor current for case 3 respectively. The highest peak overshoot is observed in case 4 as given in Figure 4c. Also, lowest undershoots are observed in case 2 and case 3. The value of these overshoots and undershoots for the gradual as well as drastic load pattern is given in Table 3.

The variation of inductor current for various load patterns is shown in Figures 3b, Figure 3d, Figure 4b and Figure 4d. The highest value of over shoot is registered for case 4 and highest value of under shoot for case 3, which is drastic step change in load. First one is for 2 times reduction in load and the later one is for 4 times increase in load.

4.3. Simulation results for DE control algorithm

The SBC is implemented with DE controller as given in equation (23) and the results are observed. Figure 5a, Figure 5c, Figure 6a, Figure 6c shows output voltage for case1 to case4 and corresponding inductor current waveforms are given in Figure 5b, Figure 5d, Figure 6b, Figure 6d respectively for the DE control algorithm. The SBC with DE control exhibits smooth current transition with reduced peak and under shoots. Also, SBC with DE controller exhibits more robust output line regulations than SBC with dual loop controller given in Section 4.2.

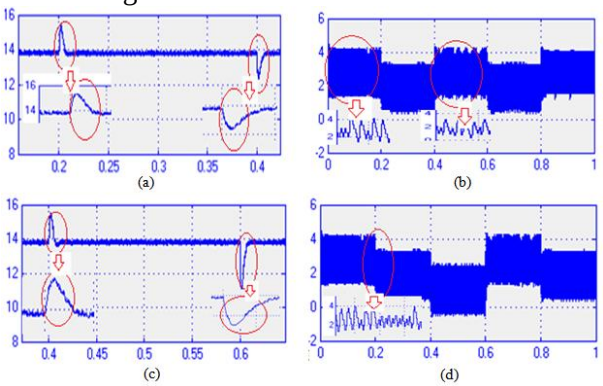


Fig. 3. SBC output for case1 and case2 (a) Voltage waveform case1 (b) Inductor current waveform for case1 (c) Voltage waveform for case2 (d) Inductor current waveform for case2

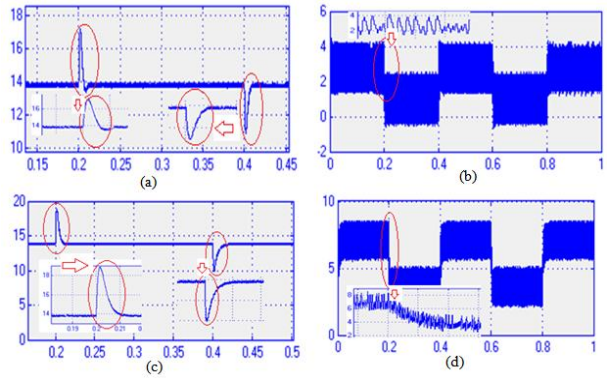


Fig. 4.SBC output for case3 and case4 (a) Voltage waveform for case3 (b) Inductor current waveform for case3 (c) Voltage waveform for case4 (d) Inductor current waveform for case4

Figure 5a shows case 1 for DE control algorithm which shows very tight voltage regulation with only least percentage of over shoot which is given in Table 3. The inductor current is smoothly varying from 3.8 A to 1.9A which is depicted in Figure 5b. Figure 5c shows output voltage waveform for case 2 and its peak overshoot is very low compared to Dual loop controller for SBC. Inductor current transitions are shown in Figure 5d which shows up to 0.2 sec the current is 4.1 A then from 0.2 to 0.4 sec it is 3.8 A and finally comes to 2.5 A with few m.sec, of negative current transition of 0.5 A which is evident from the Figure 5d.

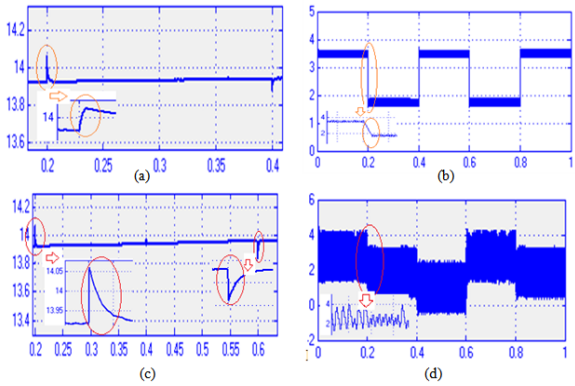


Fig.5. Output of SBC with DE control for case1 and case2 (a) Output Voltage case1 (b) Inductor current case1 (c)Output Voltage for case2 (d) Inductor current case2

Figure 6a shows drastic load variation which gives the maximum overshoot however this is much lower compared to Dual loop controller algorithm. The inductor current changes from 3.9A to 1A from 0.2sec to 0.4 sec which is given in Figure 6b. Figure 6c and Figure 6d are drastic load condition of 100-50 % load. The maximum overshoot occurs for this case 4 however it is lower than the dual loop controller with SBC. The current transition occurs at 0.2 sec- 0.4sec which is 8.1 A to 4A.

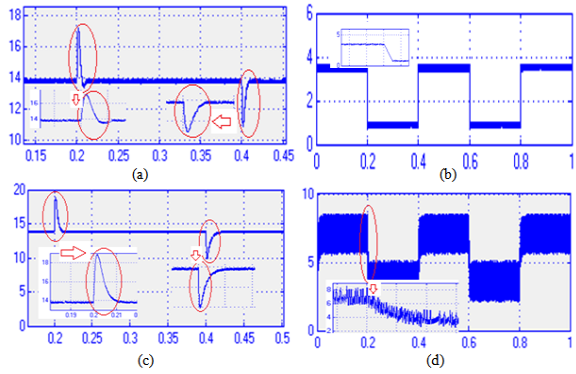


Fig.6. Output of SBC with DE control for case3 and case4 (a) Voltage waveform case3(b) Inductor current waveform case3 (c) Voltage waveform case4 (d) Inductor current waveform case4

The Bode plot analysis for different performance measures have been considered in this paper. The Bode plot for output rejection of SBC with proposed DE controller for various peak overshoots are given in Figure 7. The controller effort needed to achieve various performance measures are plotted in Figure 8. The performance measures for Figure 7 and Figure 8, peak overshoots, settling time, rise time and the corresponding phase margin and gain margins is given in Table 4. The fastest settling and rise time is obtained for the peak over shoot of 1.80 and 1.88 % the largest settling time is corresponding to the peak overshoot of 30.43% for case 4 load pattern.

Table 4 Performance measures for proposed controller

Sample	Rise time ms	Settling time ms	Peak Over-shoot %	ϕ_m deg	Gain Margin dB
Case 1	0.458	2.50	1.80	63	Inf
Case 2	0.918	5.67	1.88	68	Inf
Case 3	0.856	5.82	15.94	59	16.30
Case 4	0.799	8.48	30.43	47	7.44

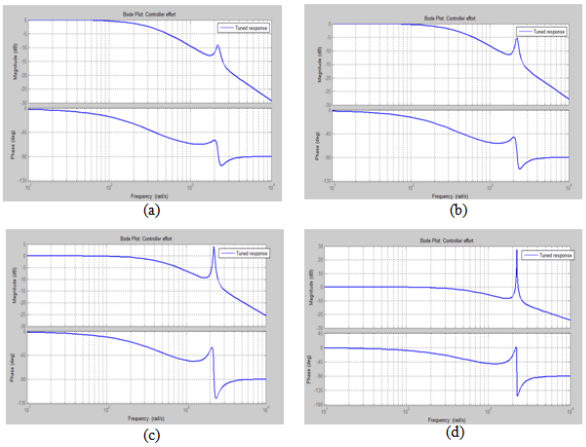


Fig. 7. Bode plot for output disturbance rejection for proposed controller (a) case 1 (b) case 2 (c) case 3 (d) case 4

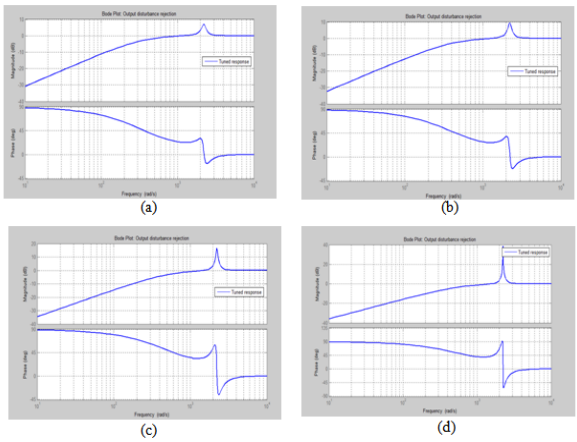


Fig.8. Bode plot for controller effort for proposed controller (a) case 1 (b) case 2 (c) case 3 (d) case 4

5.Hardware results:

SBC with the two control scheme: dual loop and DE controller are implemented in hardware and compared with the results from MATLAB Simulink. The hardware results are given in Figure 9. The output voltage is given in Figure 9a without control algorithm having large amount of overshoots. These overshoots are reduced with dual loop controller whose results are given in Figure 9c. Figure 9e shows tightly regulated output voltage from SBC with DE control action has 1.88% peak overshoot and is given in Table 3 in comparison with the dual loop controller. This shows that the SBC with DE controller produces overshoots much lower than the prescribed 5% overshoot for any classical control design application.

The inductor current transition for various time interval are given in Figure 9b, Figure 9d, Figure 9f without controller, with dual loop controller and with DE controller respectively. The results from hardware circuits for SBC with both the controller is nearly comparable with software results However there is slight deviation from Simulink results and corresponding hardware results. This is due to two reasons, (i) In MatlabR10a Simulink environment, the MOSFET is considered as ideal switch.(ii) The inductor taken in the MatlabR10a Simulink is with zero series resistor however in the present hardware it will be of few micro ohms.

In the present work, the control algorithms for SBC are implemented through an Atmega16A processor whose speed is optimum for the control loop sampling. However any DSP processor will provide much better control speed compared to this processor. This Atmel processor provides cost optimised solution for this application. The step load change is done through switching a load via MOSFET switch with programmed time sequence of 200m.sec. The proposed controller with SBC hardware is shown in Figure 10a. The comparison graph for efficiency of both dual loop controller and DE controller for various load current achieved with hardware circuits is given in Figure 10b. SBC with classical dual loop gives 88% efficiency however with the proposed controller gives 92% of efficiency even under drastic load variations.

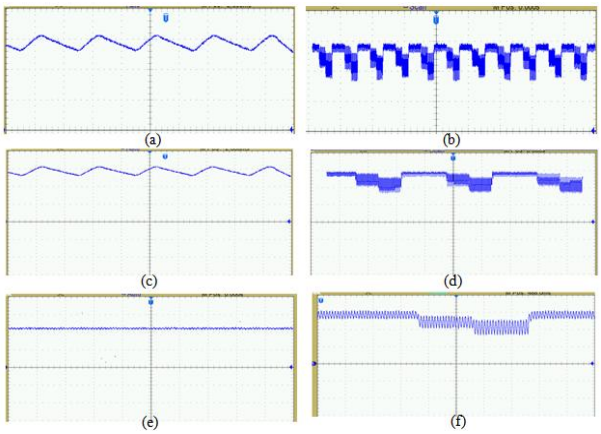
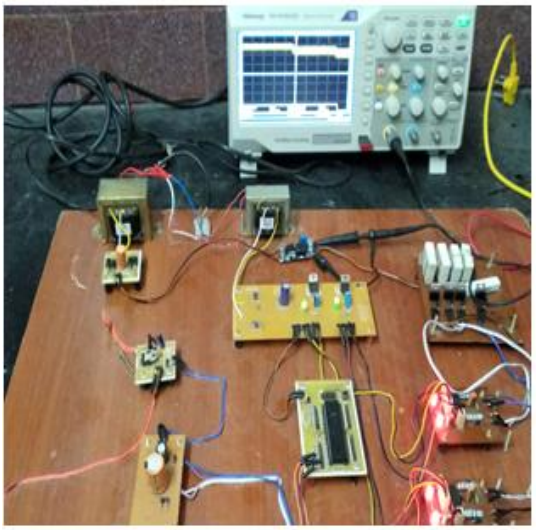
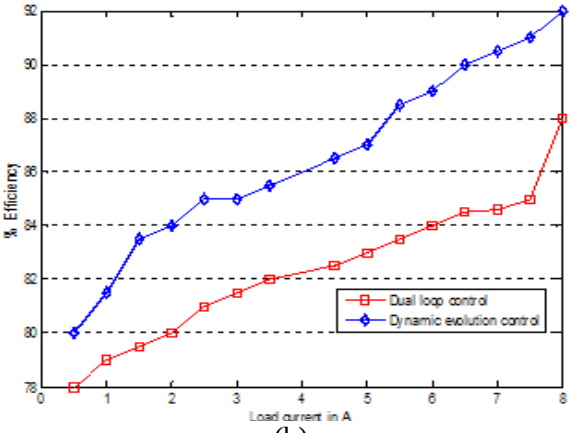


Fig.9. Hardware results of SBC for case 4(a) Output voltage without controller (b) Inductor current without controller (c) Output voltage Dual loop controller (d) Inductor current with Dual loop controller (e) Output voltage DE controller (f) Inductor current with DE controller



(a)



(b)

Fig.10. SBC with proposed DE controller (a) Hardware setup(b) Efficiency of two prototype controller

Conclusion:

Buck converters are work horse of commercial, consumer and medical electronics however converter freewheeling diodes produce considerable power loss. Replacing this schotky diode with MOSFET switch reduce the power loss which is an inviting property in power electronic industry. Even though classical controller provide sophisticated controller design, however tuning of PID gain is difficult to achieve. In this paper, two controllers are designed for SBC, namely, dual loop controller and DE controller that overcomes the difficulty in PID tuning. The Dual loop control scheme provides faster control response but the controller performances degrade with extreme and abrupt load changes. The DE control scheme provides peak overshoots less than 5% and also it is proved that the DE control scheme has better performance measures than Dual loop control scheme even for extreme load conditions. Simulation is carried out in Matlab2010Ra. Hardware results are compared with Matlab Simulation output results. The robust control performances are obtained for different extreme load conditions which are checked with two popular control algorithms Dual loop control and DE control. The SBC with DE controller could achieve 92% of efficiency even for drastic load variations which is very much better than any conventional SBCs.

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