

# **CONTRIBUTIONS to the OPTIMIZATION of PERMANENT MAGNET BRUSHLESS DC MOTOR CONTROL SYSTEMS**

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## PREFACE

This thesis presents contributions to Brushless DC motor control systems, dedicated to the automotive industry. It presents several ideas and methods starting with a novel initial rotor position estimation algorithm, a complex architecture proposal for BLDC motor driver ASIC, alternating freewheeling concept evaluation and a new hardware implemented field weakening drive mode of BLDC motors.

### Outline of the thesis

The thesis is organized in seven chapters and deals with major issues in the Brushless DC motor control units specialized for the automotive industry.

The *first chapter* presents an overview of brushless motor types and drive strategies, with a special focus on Brushless DC motor applications, describing various commutation methods, sensed and sensorless drive modes, from initial position sensing to high speed commutation moment detection methods based on Back-EMF evaluation.

In *the second chapter* a novel very fast initial rotor position sensing method is presented, based on four voltage pulses and requiring only measurement of phases and power supply voltage.

In *the third chapter* a complex Brushless DC motor driver ASIC architecture for automotive applications is proposed. The proposed architecture includes a power MOSFET's gate driver unit, a load current measurement block based on synchronous sample and hold circuit, a novel diagnosis system including on and off state diagnosis circuits, a sensed and sensorless block commutation unit and a serial communication protocol proposal.

In *the fourth chapter* a new alternating freewheeling concept is presented for BLDC motor driver three phased power inverter circuits. The proposed calculation method, the simulation and experimental result proves the better power (thermal) distribution among the three phased bridge switching elements.

In *the fifth chapter* a new hardware implemented field weakening drive of BLDC motors is presented and evaluated. The method is based on controlled de-calibration of an intelligent rotor position sensor, gaining the great advantage of a precise phase advance control and in the same time a reduced computational power required from the system microcontroller.

In *the sixth chapter* a new interface circuit for hall cell based speed sensors is presented. The great benefit of the method is derived from the adaptive threshold feature, which offers a considerable improvement of the EMC performances, as demonstrated by the presented simulation and laboratory experiment results.

In the last, *seventh chapter* of this thesis the original contributions of this work are summarized.

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Timișoara, Novemeber 26<sup>th</sup> , 2011

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### **CONTRIBUTIONS to the OPTIMIZATION of PERMANENT MAGNET BRUSHLESS DC MOTOR CONTROL SYSTEMS**

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**Keywords:** BLDC, initial rotor position, hall sensor, automotive, ASIC, sensorless control, BLDC diagnosis, phase advance, alternating freewheeling.

### **Objectives of the thesis**

The main objectives of the thesis are:

- To present an overview of Brushless DC motor drive methods and systems;
- To present a novel rotor initial position estimation method;
- To evaluate a new alternating freewheeling drive concept for BLDC motor driver three phased power inverters;
- To propose a complex BLDC motor driver ASIC architecture;
- To present a new hardware implemented field weakening drive of BLDC motors;
- To present a new speed sensor interface circuit with improved EMC performance;

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## Abbreviations

**ABS** - Anti-lock Braking System  
**ADC** - Analog to Digital Converter;  
**ASIC** - Application Specific Integrated Circuit;  
**Back-EMF or BEMF** - Back Electro Motive Force;  
**BLDC** - Brushless Direct Current;  
**CAN** - Controller Area Network;  
**CMOS** - Complementary Metal Oxide Semiconductor - ASIC technology;  
**CPLD** - Complex Programmable Logic Device;  
**CTS** - Commutation Trigger Signal;  
**DSP** - Digital Signal Processor;  
**ECU** - Engine Control Unit or Electronic Control Unit;  
**EMC** - Electro Magnetic Compatibility;  
**ESP** - Electronic Stability Program;  
**FOC** - Field Oriented Control;  
**GND** - Ground connection;  
**GUI** - Graphical User Interface;  
**HS** - High Side - MOSFET or switching element;  
**HW** - Hardware;  
**IO** - Input Output;  
**LED** - Light Emitting Diode;  
**LPF** - Low Pass Filter;  
**LS** - Low Side - MOSFET or switching element;  
**MOSFET** - Metal Oxide Semiconductor Field Effect Transistor;  
**OFFSM** - OFF State Monitoring;  
**ONSM** - ON State Monitoring;  
**OL** - Open Load;  
**PC** - Personal Computer;  
**PM** - Permanent Magnet;  
**PMAC** - Permanent Magnet Alternative Current;  
**PMSM** - Permanent Magnet Synchronous Machine;  
**PWM** - Pulse width Modulation;  
**RPM** - Revolution or Rotation per Minute;  
**SCD** - Short Circuit Detection;  
**SCB** - Short Circuit to Ground;  
**SCG** - Short Circuit to Battery;  
**SCL** - Short Circuit of the Load;  
**SPI** - Serial Peripheral Interface;  
**SW** - Software;  
**S&H** - Sample and Hold  
**TCS** - Traction Control System;  
**TCU** - Transmission Control Unit;  
**TTL** - Transistor-transistor Logic;  
**WSC** - Weak Short Circuit;  
**XCU** - Axle Control Unit - four wheel drive control unit;  
**ZCD** - Zero Crossing Detection;  
**μC** -Microcontroller;

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# 1 Brushless DC motor driving methods

This chapter presents an overview of the BLDC (Brushless DC) motor driving strategies and control methods, from automotive applications perspective. The use of DC motors for fan, pump or electro-mechanical actuator applications is very common in automotive applications. Today's trend is to replace the conventional DC with BLDC motors because of their higher efficiency, higher generated torque per mechanical size, longer lifetime, silent operation and low electromagnetic emissions.

## 1.1 Introduction

In the last decades BLDC motors using permanent magnets have become more and more employed in a large number of applications like industrial automation, consumer electronics, automotive, mainly because their superior performance over the conventional DC motors. On the other hand the technology applied for the BLDC motors and its control electronics has evolved significantly thus making possible the design of cheap BLDC motor based control systems, keeping all the advantages of the BDLC motor.

Two major BL (Brushless) motor types exist according to the Back-EMF (Back - Electro Motive Force) signal shape [12],[13]. Permanent Magnet Sinusoidal Machine (PMSM or PMAC – Permanent Magnet Alternative Current) with sinusoidal shape of the Back-EMF signal and Brushless DC (BLDC) with trapezoidal shape of the Back-EMF voltage. PMSM motors are driven with sinusoidal shaped phase voltages and currents in contrast to the BLDC motor types which are driven with trapezoidal shaped phase voltages and rectangular current waveforms. In most of the cases the drive signals are generated using conventional three phased power inverter circuits as presented in Fig. 1.14.

The control of these motor types requires information about the rotor position in order to generate the correct phase's voltage and current signals/sequences to drive the motor in a certain direction with a desired speed and torque. This chapter presents an overview of the rotor position sensing methods with a special focus on the methods applicable in the automotive industry. Such methods as the *Sensored* control, based on rotor position sensing devices or *sensorless* solutions based on the estimation of the rotor position by evaluating various parameter changes (phase voltages, currents, phase inductance, flux linkages etc.) of the motor control unit and the BLDC motor itself.

## 1.2 Characteristics of brushless DC motors

This chapter relates the base characteristics of the BLDC motors with a special focus on their characteristics which facilitate the sensorless driving operation.

### 1.2.1 Permanent magnet brushless DC motor types

The Back-EMF is the voltage induced in the motor phase windings by the rotor magnets while the rotor is in motion. The amplitude of this voltage is proportional with the number of turns in the phase coil and the flux variation through the area of the coil (Fig. 1.1).

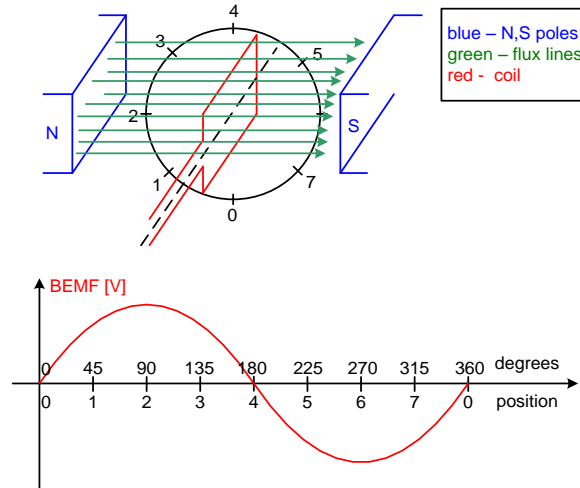


Fig. 1.1 Back-EMF signal generation principle

The Back-EMF voltage for the case in above figure (Fig. 1.1) can be expressed as follows:

$$V_e(bemf) = -N \frac{d\phi}{dt} \quad (1.1)$$

For an electric motor having sinusoidal shaped Back-EMF (Fig. 1.1) the voltage can be expressed as follows:

$$V_{e\text{peak value}} = \omega_e \cdot \psi_{PM} \cdot p \quad (1.2)$$

- where  $V_e$  - denoting the Back-EMF voltage;  $p$  - the number of pole pairs;  $\omega$  [rad/s] - the rotor electrical rotational speed;  $\psi_{PM}$  [Vs] - permanent magnet flux.

The shape of the Back-EMF signal is influenced by the rotor configuration as described in the next sub-chapter. The first category requires continuous rotor information, the motor is supplied with sinusoidal shaped phase voltages and currents, generated using sinusoidal modulated (the duty cycle) PWM (Pulse Width Modulation) control signal. The ideal Back-EMF signal of these motors is sinusoidal, therefore the interaction of it with the sinusoidal shaped phase currents produces a constant torque with very low ripples. This method is called sinusoidal drive and is applied to PMSM (Permanent Magnet Synchronous Machine) or PMAC (Permanent Magnet Alternative Current) motor types. In Fig. 1.1 the phase voltage and currents are presented for the sinusoidal driven permanent magnet motors.

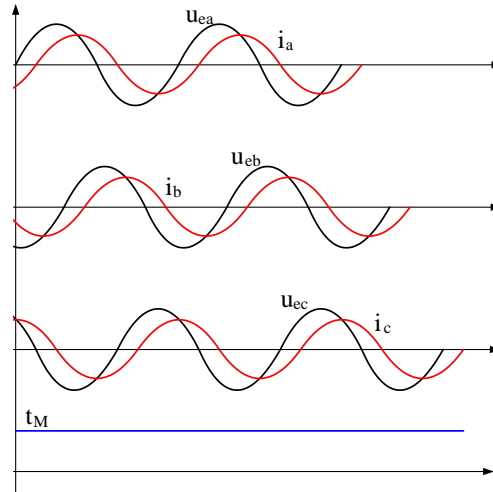


Fig. 1.2 Sinusoidal driven machine phase voltage and current waveforms

The second category of Brushless motors with permanent magnets uses commutated DC phase voltages (BLDC - Brushless DC), also called trapezoidal control method. For the three phase BLDC motor type, block commutation is applied with  $120^\circ$  electrical duration for each commutation sequence having in total six commutation sequences. The shape of the Back-EMF signal induced by the rotor is trapezoidal where the plateaus of the Back-EMF correspond to the constant phase current intervals. For this motor types rotor position information is only needed at the block commutation (phase commutation) points (every  $60^\circ$  electrical – for the  $120^\circ$  or  $180^\circ$  electrical block commutation and every  $30^\circ$  electrical for the  $60^\circ$  block commutation method). The ideal phase voltages and currents waveforms of a BLDC motor are presented in the below figure (Fig. 1.3).

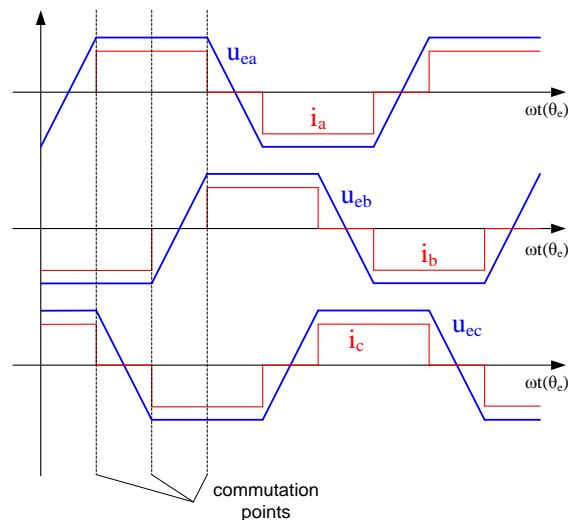


Fig. 1.3 Trapezoidal driven machine phase voltage and current waveforms

Each PM brushless motor and driving method has its own advantages and disadvantages, the actual option being mostly driven by the application requirements and implementation cost. In the below Table 1.1 a comparison between the driving methods are presented [14]. In the table the Field Oriented Control (FOC) method is also presented which is basically also an improved sinusoidal control method. The basic idea behind this method is that the phase currents and voltages are manipulated in the d-q reference frame of the rotor. This method improves the motor controller performance at high speeds [15].

Table 1.1 Characteristics of commutation methods for PMSM and BLDC machines

Commutation method	Speed control	Torque Control		Required Feedback Devices	Algorithm Complexity
		Low Speed	High Speed		
Trapezoidal	Excellent	Torque ripples	Efficient	Hall	Low
Sinusoidal	Excellent	Excellent	Inefficient	Encoder, Resolver	Medium
FOC	Excellent	Excellent	Excellent	Current sensor, Encoder	High

### 1.2.2 Configurations of permanent magnet motors

We can categorize the configurations of the permanent magnet brushless motors according to the configurations of their stator windings and the rotor configuration.

According to the stator winding configuration we have two possibilities for a three phased brushless motor, star and delta connection. In Fig. 1.4 are presented the connection schemes, a) delta and b) star winding configurations. The configuration choice influences the torque and speed characteristic of the motor for a given operating voltage. Fig. 1.5 presents this characteristic in a graphic form.

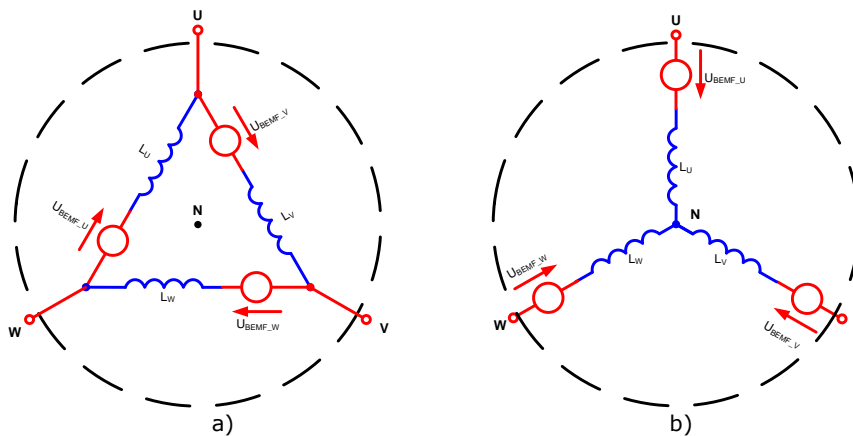


Fig. 1.4 Stator windings connection configurations  
 a) Delta configuration; b) Star configuration;



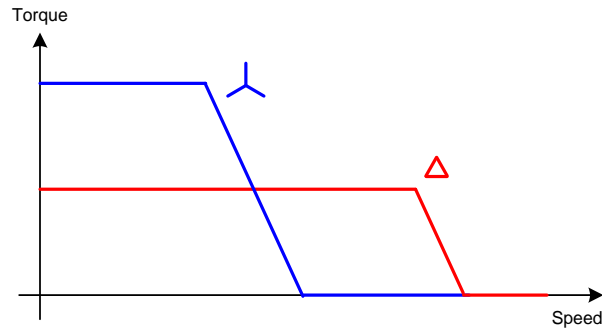


Fig. 1.5 Torque and speed characteristic for a given supply voltage

From Fig. 1.5 it can be observed that at a given supply voltage the maximum speed limitation of the delta configuration is higher than the maximum speed of the star configuration, however the max torque produced by the star configuration in comparison to the delta is higher at lower speeds.

The equivalent circuit of a phase winding regardless of delta or star configuration is as presented in Fig. 1.6, where the supply voltage  $v$  induces the phase current  $i$ . The phase winding equivalent circuit consists of a series resistance  $R$ , the winding inductance  $L$  and the electro-motive voltage source  $e$ .

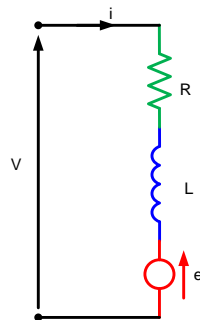


Fig. 1.6 Equivalent circuit of one phase of a PM brushless motor

The torque output of a brushless motor is constant over a speed range limited by the power electronic converter's ability to maintain the demanded phase currents at the required level [17]. Of course we cannot have a very high output torque for long time which requires larger phase currents than the windings can physically sustain. Fast and accurate control of the phase winding current is only possible if the supply voltage is larger than the Back-EMF voltage amplitude so the supply voltage forces the current changes into the motor phases. The speed, at which the Back-EMF voltage effective amplitude is equal to the supply voltage, is referred as the maximum normal operating speed or *base speed*. The motor can run over its base speed in the field-weakening mode, in which a component of the phase winding current produces a magnetic field opposing the permanent magnet field and reduces the effective Back-EMF voltage amplitude. Field weakening can be accomplished for both sinusoidal and trapezoidal driven motors by increasing the phase angle by which the current leads the Back-EMF voltage. This method is also called *phase-*

advanced drive [16]. Fig. 1.7 presents the speed and torque characteristics of a BLDC motor.

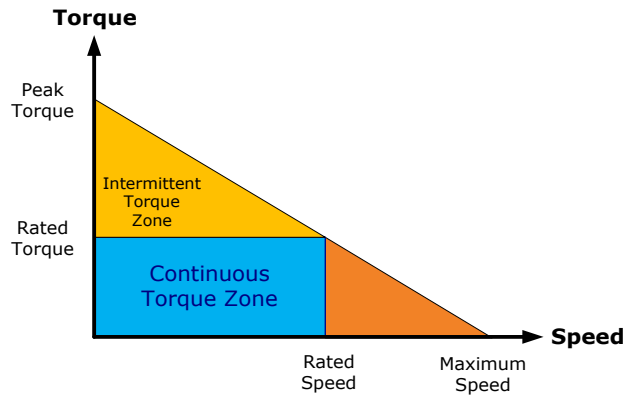


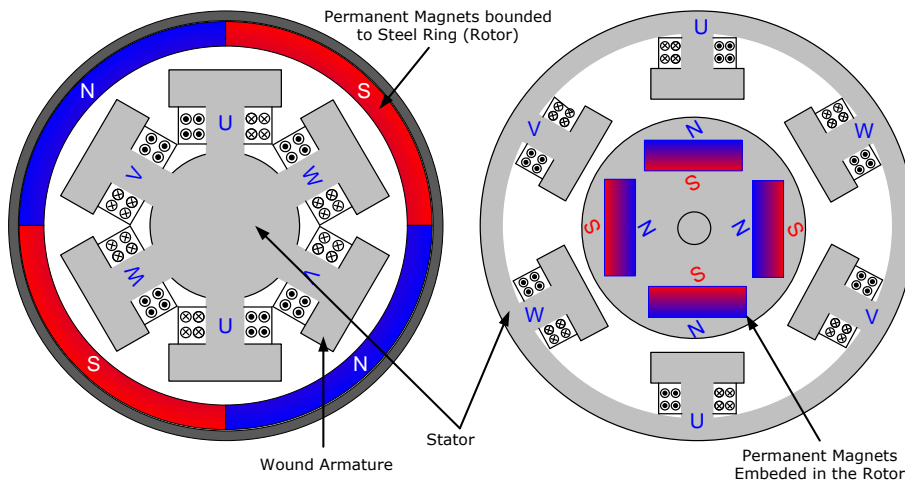
Fig. 1.7 BLDC motor torque VS speed characteristic

Another very important construction parameter of the BL motor is the rotor configuration. This influences the motor cogging torque amplitude; the Back-EMF voltage amplitude and shape; the maximum torque and its ripple magnitude and the phase's winding inductance change over the rotor position. In case of brushless motors with permanent magnets (BLDC, PMSM) the magnetic field of the rotor is generated using permanent magnets attached to it. The magnetic field generated by the stator winding interacts with the static magnetic field of the rotor causing the movement of the rotor.

According to the motor construction we have two possibilities [18]:

- Outer rotor configuration (Fig. 1.8 (a));
- Inner rotor configuration (Fig. 1.8 (b));

In automotive actuator applications based on brushless motors the inner rotor configuration is the most preferred option [19]. For these motor types, there are four commonly used rotor construction categories, as presented in Fig. 1.9 [13].

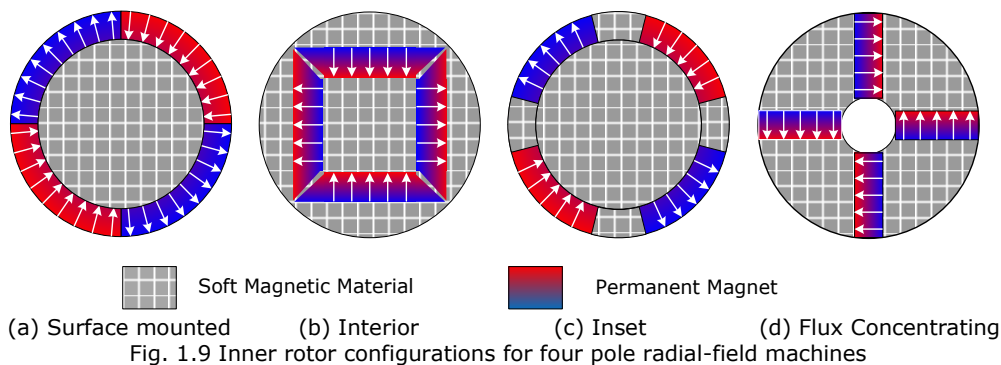


(a) Outer rotor configuration (b) Inner rotor configuration  
Fig. 1.8 Brushless motor rotor configurations

Table 1.2 Comparison of outer versus inner rotor configurations [18]

Nr.	Outer rotor.	Inner Rotor.
1	Can be wound with dc armature-winding equipment (also mounted on PCB).	Requires special winding tool which is more expensive.
2	Available cooper space on distributed winding motors is less than on inner-rotor types.	Distributed-winding motors provide smother performance and better cooper utilization.
3	Shorter end turns resulting in lower phase inductance, resistance and less cooper loss.	Longer end turns resulting in higher phase inductance, resistance and cooper loss.
4	High rotor inertia.	Low rotor inertia.
5	Low torque ripples.	Significant torque ripples.
6	Slow acceleration.	Fast acceleration.
7	Low energy magnets can be used.	High energy magnets required.
8	Poor heat dissipation characteristics	Very good heat dissipation characteristics
9	Low cogging torque	High cogging torque
10	Low driving dynamics	High drive dynamics

In case of the surface mounted magnets (Fig. 1.9 (a)) using high performance rare-earth magnets with very high magnetic permeability (close to unity), the effective air gap is equal to the sum of the physical air gap between the rotor and stator plus the magnet depth. This fact causes the current flowing into the phase winding conductors to generate a small amount of magnetic-flux component, therefore the inductance of the phase winding is very small and the change of this inductance with the rotor position is insignificant if the complete surface of the rotor is covered with magnet with a constant depth. This configuration is preferred for sinusoidal drive applications with high driving performance. The disadvantage of the method is the lack of salience which is very benefic for sensorless operation which at low speeds and startup facilitates the rotor position estimation.



The interior magnet configuration has its magnets buried inside the rotor core (Fig. 1.9 (b)), the direction of the magnetization is radial. This makes it a favorite solution for sinusoidal PM machines, because it is very easy to obtain the sinusoidal variation of the flux density around the air-gap periphery. The high permeability magnetic material adjacent to the air-gap leads to higher value of the machine inductances than in case of the other configurations.

The inset magnet configuration (Fig. 1.9 (c)) is often preferred for trapezoidal drive (BLDC motors) because the magnet arc can be adjusted to assist in shaping

the Back-EMF waveform. The presence of the soft magnetic material at the physical air-gap in the regions between the magnet poles causes a substantial variation of the winding inductance, with maximum inductance appearing at rotor positions where the magnet pole arcs are misaligned with the winding axis. This fact causes a significant saliency for the machine which facilitates the sensorless drive of the BLDC motor. Based on this saliency effect the initial position of the rotor is very easy to estimate and at low speeds where voltage generated by the saliency replaces the Back-EMF voltage whose amplitude is too low to be sensed.

Finally the flux concentrating configuration (Fig. 1.9 (d)) has magnets located with their axes in the circumferential direction, so that the flux over a rotor pole arc is contributed by two separate magnets. This configuration exhibits also very significant saliency and cogging torque, causing a substantial change of the phase's windings inductance with the rotor position.

Saliency is given by the magnetic permeability difference between the  $d$  and  $q$  axis of the rotor which results in winding inductance change with rotor position. Fig. 1.10 present two sections of a BLDC motor, one salient (Fig. 1.10 (a)) and one non salient pole (Fig. 1.10 (b)) configuration.

In sensorless BLDC motor drive applications the salient pole rotor construction is much preferred because in the absence of detectable Back-EMF the inductance changes of the phase winding can be used to extract rotor position information as demonstrated in the next chapters of this thesis (subchapters 1.4, 1.5 and chapter 2).

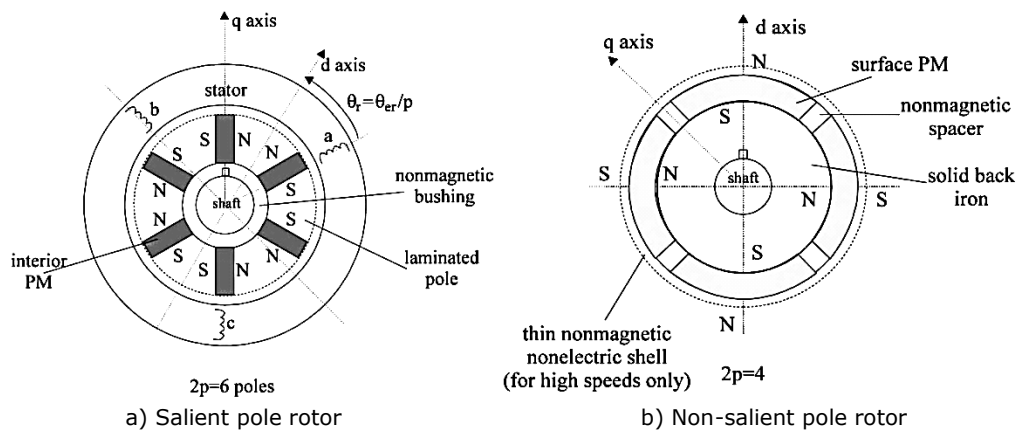


Fig. 1.10 Salient and non-salient pole rotor construction [177]

### 1.2.3 Brushless DC motor construction

A very important category of the brushless machines is represented by the BLDC (Brushless DC) motors. Fig. 1.11 presents a cross section of a typical BLDC motor [20], [21]. The stator magnetic circuit is made of steel sheets stacked up with multiple winding slots. The magnets bounded to the rotor are magnetized and shaped in order to obtain the trapezoidal shape of the Back-EMF voltage which makes possible to drive the motor with three phased rectangular DC voltages with low ripple currents and good efficiency. Fig. 1.12 presents a picture of a BLDC motor employed in most of the experiments presented in this thesis.

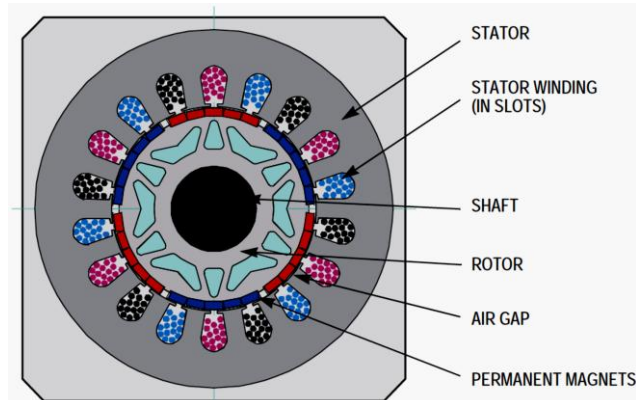


Fig. 1.11 BLDC motor cross section [20]



Fig. 1.12 Picture of a BLDC motor

The motor can have multiple pole pairs. This defines the relationship between one complete mechanical revolution and the corresponding electrical revolutions. The motor presented in Fig. 1.11 has three pole pairs therefore three complete electrical rotations are required for one complete mechanical revolution.

The rectangle shaped phase voltages offer simplicity to the BLDC control algorithm and driver module, because attention to the motor driver signals is needed only at the phase commutation points (at certain angles in order to align the applied voltage with the Back-EMF) or when the conditions of the motor operation are changed (change of speed/torque). The alignment between Back-EMF and commutation event is very important. Between the commutations points the motor acts as a DC motor and runs at its best working points. Fig. 1.13 presents the magnetic flux linkage, the phase Back-EMF and the phase to phase Back-EMF voltage waveforms. As it can be seen, the shape of the Back-EMF signals is approximately trapezoidal and its amplitude is a function of the actual speed. During rotation reversal, the amplitude and sign of the back-EMF changes together with the phase sequences [20]. The filled areas in the tops of the phase back-EMF voltage waveform indicate the intervals where the phase power stage commutation occurs.

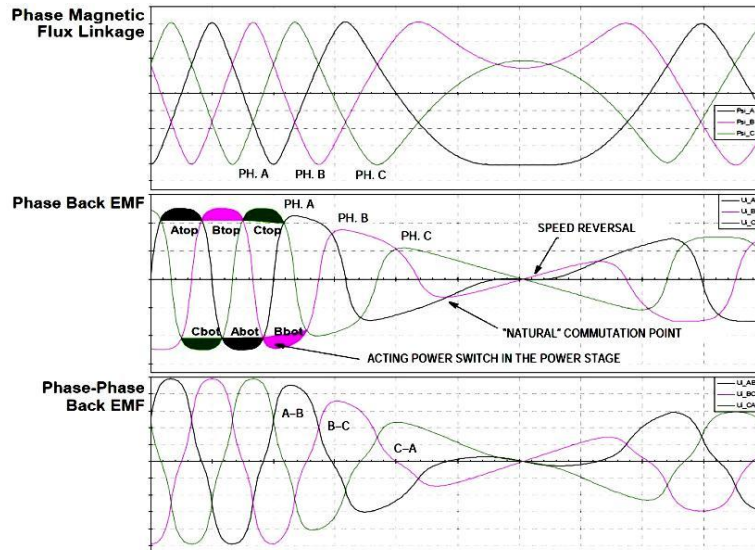


Fig. 1.13 BLDC motor Back-EMF and Magnetic Flux [21]

In normal operation mode (no phase advance) the commutation points of the power MOSFET's coincide with the points where the Back-EMF waveforms of the phases intersect. The phases voltage, regardless of the control method of the BLDC motor (trapezoidal or sine-wave) is obtained using three phased power inverter (three half-bridges) as presented in Fig. 1.14 which is controlled usually using an ASIC (Application Specific Integrated Circuit) or a microcontroller, equipped with PWM generator modules. The equation of the three phased brushless motor is [24]:

$$\begin{bmatrix} u_{Sa} \\ u_{Sb} \\ u_{Sc} \end{bmatrix} = R_S \cdot \begin{bmatrix} i_{Sa} \\ i_{Sb} \\ i_{Sc} \end{bmatrix} + \frac{d}{dt} \cdot \begin{bmatrix} \psi_{Sa} \\ \psi_{Sb} \\ \psi_{Sc} \end{bmatrix} \quad (1.3)$$

- where with  $u_{sx}$  denoting the phase voltage (regarded to the motor neutral point);  $R_s$  – phase resistance;  $i_{sx}$  – phase current;  $\psi_{sx}$  – magnetic flux;

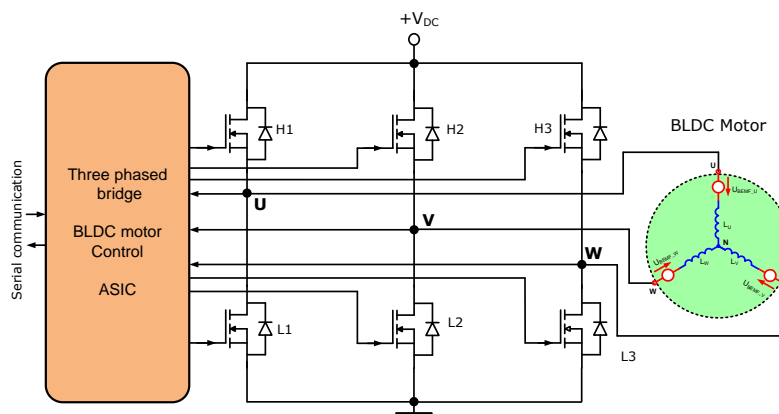


Fig. 1.14 Three phased power inverter configuration

## 1.3 Brushless DC motor rotor position detection methods

From principle point of view there are two methods used to detect the rotor position of a permanent magnet brushless motor. The first category of methods uses an actual sensor, which provides rotor position information to the control electronics (also called *sensored* driving method). Most commonly used position sensors are the Hall Effect based position sensors [22],[23]. The second category of methods use no rotor position sensors at all (also called *sensorless* driving mode), it extracts the rotor position information from the phases current and voltage waveform evaluation, or in some cases evaluating the response of the brushless motor to high frequency current injection.

The next section provides a comprehensive overview of the methods employed in permanent magnet brushless (BLDC) motor driving strategies, with and without position sensors, from the stand still up to high speeds.

### 1.3.1 Position detection using hall sensors

There are several implementations of the hall sensors according to the BLDC motor driving method as follows:

- Six step commutation - 120° block commutation -> uses three hall sensors;
- Six step commutation - 180° block commutation -> uses three hall sensors;
- Twelve step commutation - 60° block commutation -> uses six hall sensors;

#### 1.3.1.1 Six step commutation implementation

The most commonly implemented sensed rotor position detection is using three hall sensors [25]. Each of these sensors provide one digital output signal (high or low), together encoding the six commutation steps (for a complete electrical revolution) of a trapezoidal controlled BLDC motor (Fig. 1.16). Each hall commutation period corresponds to a phase commutation period. The six step control vectors are graphically represented in Fig. 1.15 and the terminal voltage levels according to the hall positions are presented in Fig. 1.17, where U, V and W represent the phase voltages. HALL1, HALL2 and HALL3 are representing the position signals provided by the three hall sensors. The control electronics decode the hall signals and activates the corresponding switches of the three phased power inverter in correspondence with the desired rotation direction.

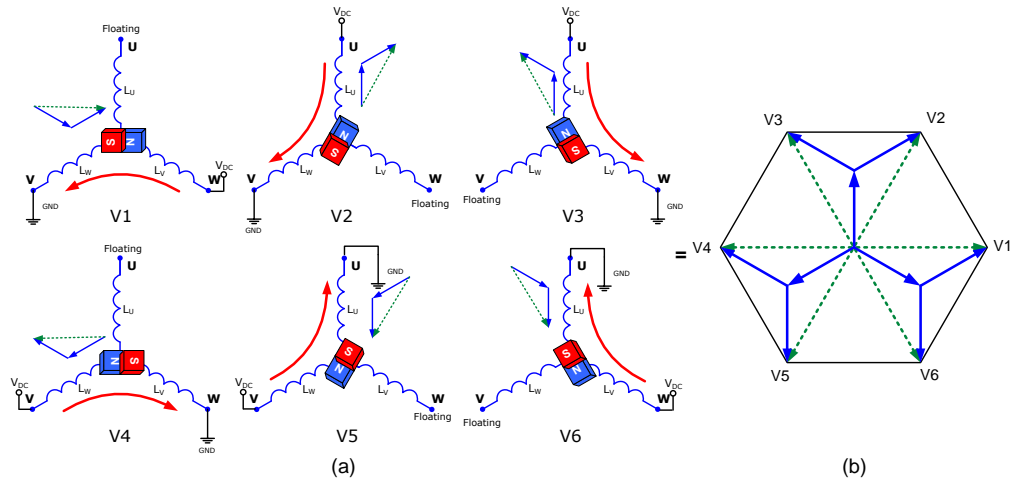


Fig. 1.15 Six step commutation vectors, graphical representation

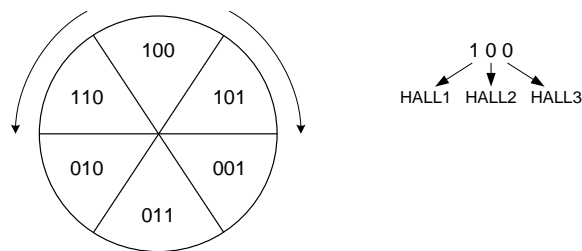


Fig. 1.16 Six commutation steps encoding with the hall signals

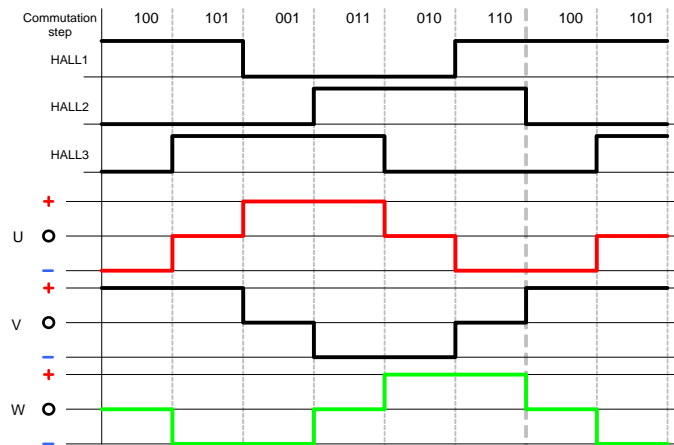


Fig. 1.17 Six step commutation signals

Note that the hall sensors encode the rotor position using gray code, this is the basis for failure condition detections of the hall signals. From one sequence to the next (regardless of rotation direction) only one hall signal changes its level, in case of two hall signals change their level in the same time this means the rotor skipped some commutation steps (does not follows the commutation pattern) resulting in a



sequence error. The hall signal diagnosis methods are more detailed in subchapter 3.2.3.5 to 3.2.3.8.

The placement of the hall sensors for six step commutation (BLDC motor with four pole pairs) is presented in Fig. 1.18. Fig. 1.19 presents for inner rotor configured BLDC motor.

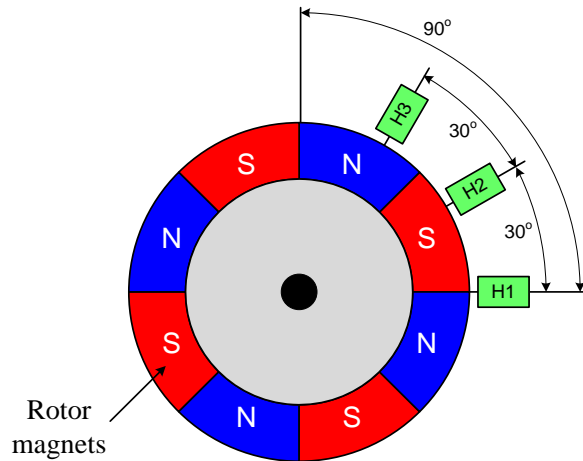


Fig. 1.18 HALL sensors displacement for six step commutation

The hall sensors must be placed with a certain electrical angle difference to each other, according to the driving strategy. The actual mechanical angular distance between them is dependent on the motor construction. The following equation shows how to determine the actual mechanical angle ( $\theta_{Hall}$ ) distance between two hall sensors:

$$\theta_{Hall} = \frac{360^\circ}{hall\_number \cdot polepairs} \quad (1.4)$$

- In case of six step commutation (three hall sensors) and four pole pairs the result will be:

$$\theta_{Hall} = \frac{360^\circ}{hall\_number \cdot polepairs} = \frac{360^\circ}{3 \cdot 4} = 30^\circ \quad (1.5)$$

- In case of twelve step commutation (six hall sensors) and four pole pairs:

$$\theta_{Hall} = \frac{360}{6 \cdot 4} = 15^\circ \quad (1.6)$$

- In case of twelve step commutation and 8 pole pair:

$$\theta_{Hall} = \frac{360}{6 \cdot 8} = 7.5^\circ \quad (1.7)$$

From equations (1.4 - 1.7) we can conclude that increasing the number of commutation steps and the number of rotor magnet pole pairs the control rotor positioning precision is improved but in the same time the mechanical angle distance between two hall sensors is decreased dramatically, making impossible to physically place the hall sensors. Furthermore any small error in the hall sensor positioning is translated into a much higher electrical angle error (mechanical displacement error multiplied with the pole pairs) which will lead to inefficiency and poor performance of the BLDC motor.



Fig. 1.19 Hall sensor placement of an outer rotor spindle floppy disk driver BLDC motor [17]

**1.3.1.2 180° block commutation method**

**Phasor diagram for max torque:**

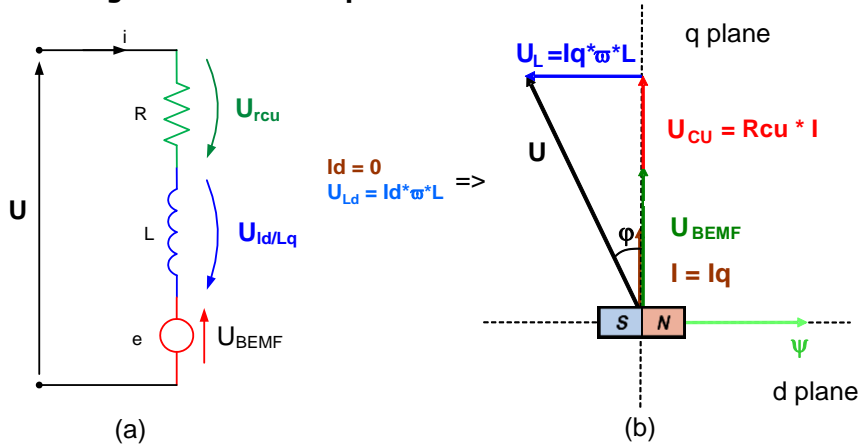


Fig. 1.20 Phasor diagram for max torque

The magnetic flux  $\Psi$  generates the  $U_{BEMF}$  voltage in q axis (Fig. 1.20). For maximal torque production, the current has to be in phase with the generated  $U_{BEMF}$ , so only q current is produced. This current causes a voltage drop on the resistance of the windings  $U_{cu}$ . This vector is obviously in the same plane as the current I. The

voltage on the inductance  $U_L$  (note  $I_d = 0$ ) is advanced by  $90^\circ$  to this current, so the vector addition of all voltages results in the voltage vector  $U$  that needs to be applied for maximum torque output.

**Phasor diagram in block drive for  $0 < \text{speed} < \text{no load speed}$**

In BLDC operation, current angle is not known. So the voltage angle is set according to rotor position. The current vector is a resulting product from this voltage and the motor inductance. For  $0^\circ$  phase advance the voltage vector  $U$  is aligned with  $U_{BEMF}$ . As a result of the motor behavior as discussed before the current vector, that occurs can be split into the force producing vector  $I_q$  component and the flux producing component  $I_d$ .

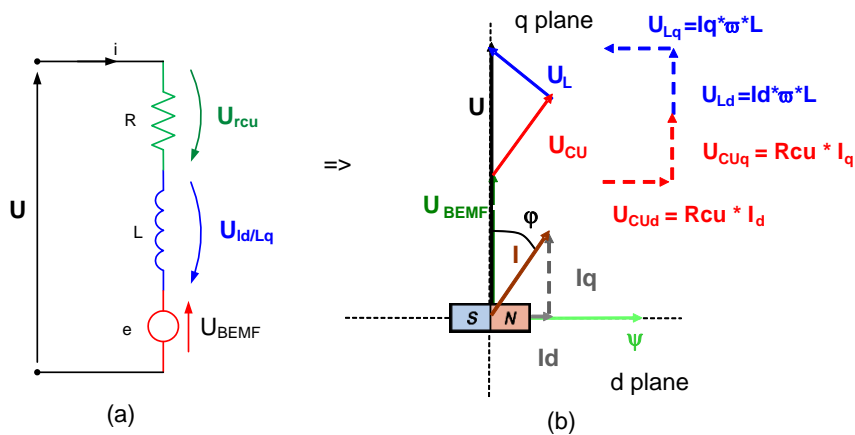


Fig. 1.21 Phasor diagram in block commutation

Obviously the flux producing component is useless and increases the length of the voltage vector  $U$  required for the given speed. The following Fig. 1.21 presents the Phasor diagram for this situation.

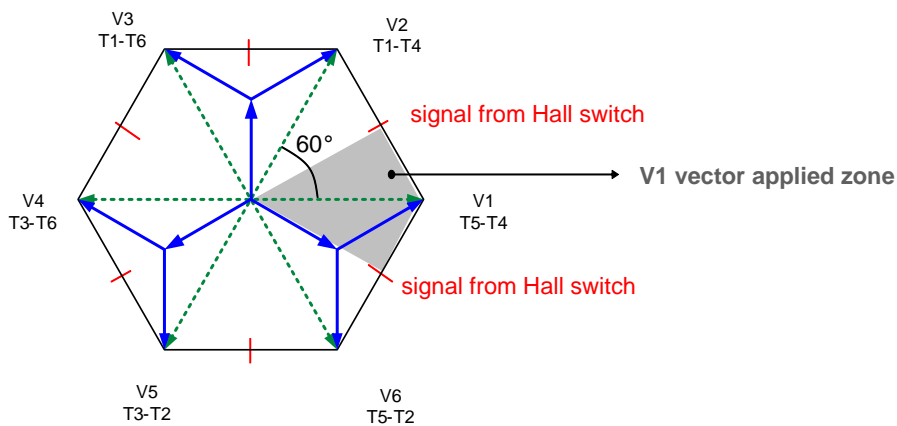


Fig. 1.22 Six step operation vector diagram at zero speed

For zero speed, the influence of the inductance is waived. Then obviously the angle between voltage and current =  $0^\circ$ . When the voltage  $U$  is aligned as shown in Fig. 1.23, the current vector is force producing only. However the voltage is not

perfectly aligned with the rotor position due to the 6 step operation (see Fig. 1.21 and Fig. 1.22) the resulting current  $I'$ , will be between  $-30^\circ$  to  $+30^\circ$  off from ideal q axis. In this case the torque is reduced by  $\cos 30^\circ$  compared to the ideal sinusoidal Back-EMF shaped motor (around 15% torque loss).

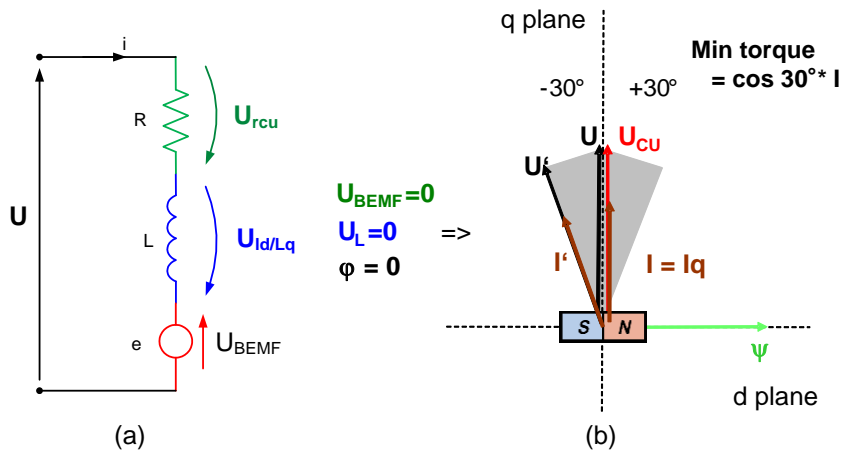


Fig. 1.23 Phasor diagram in BLDC operation at zero speed

The compensation of this torque loss can be achieved using six step  $180^\circ$  block commutation instead of  $120^\circ$  block commutation, as presented in Fig. 1.15.

The six possible  $180^\circ$  block commutation base vectors are represented in Fig. 1.24. In Fig. 1.25 the two base vectors for  $120^\circ$  (Fig. 1.25 (a)) and  $180^\circ$  (Fig. 1.25 (b)) block commutation are presented where the difference between them can clearly be observed.

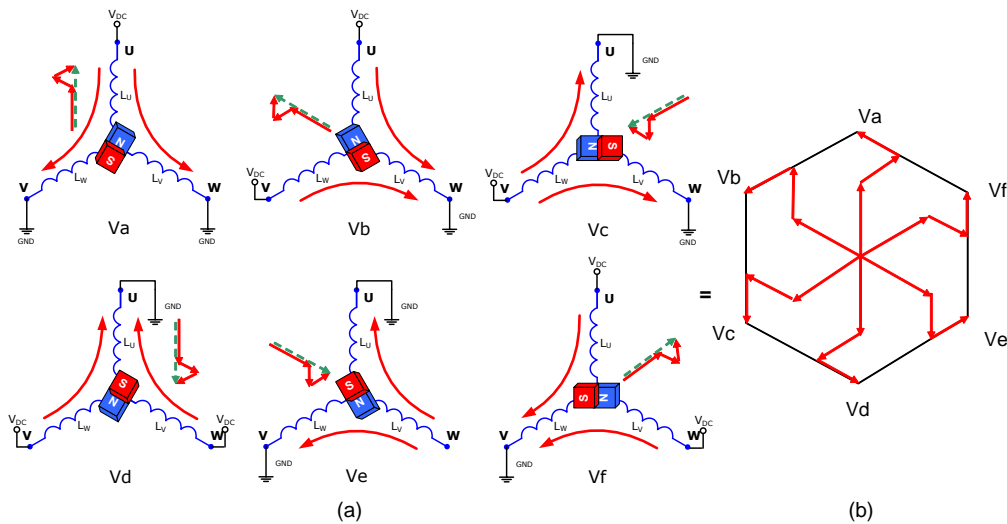


Fig. 1.24 Six possible base vectors of  $180^\circ$  block commutation

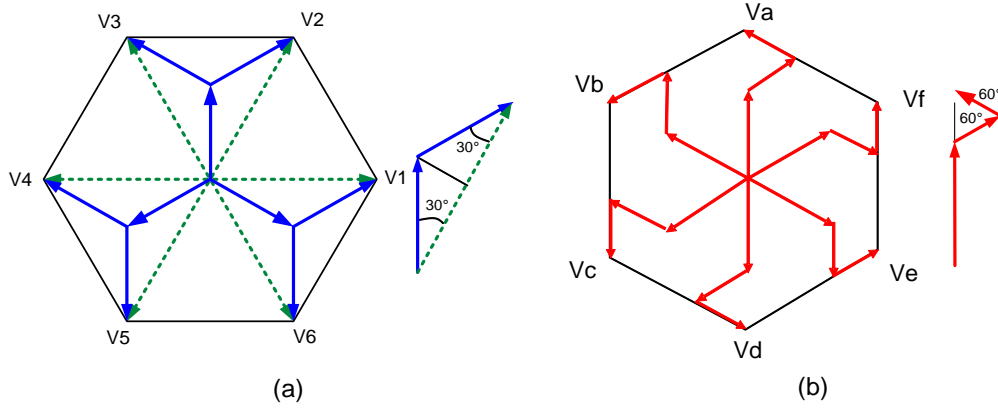


Fig. 1.25 120° VS 180° vector commutation comparison

Based on the vector representation from the above Fig. 1.25 we can express the phase current limits  $I_{CL}$  as follows:

$$I_{CL\_120^\circ} = \frac{U}{2 \cdot R_{phase}} \quad (1.8)$$

$$I_{CL\_180^\circ} = \frac{U}{1,5 \cdot R_{phase}} = \frac{4}{3} I_{CL\_120^\circ} = 1,33 \cdot I_{CL\_120^\circ} \quad (1.9)$$

$$T_{120^\circ} = \cos(30^\circ) \cdot 2 \cdot I_{CL\_120^\circ} = \sqrt{3} \cdot I_{CL\_120^\circ} \quad (1.10)$$

$$T_{180^\circ} = \cos(60^\circ) \cdot \left( \frac{I_{CL\_180^\circ}}{2} + \frac{I_{CL\_180^\circ}}{2} \right) = \frac{3}{2} I_{CL\_180^\circ} = \frac{\sqrt{3}}{2} T_{120^\circ} \quad (1.11)$$

From the above equation (1.10) and (1.11) we can conclude that the torque given by the same current limit is decreased around 15% in case of 180° block commutation, nevertheless for the same supply voltage equations (1.8) and (1.9) demonstrates that the max current can be increased by 33%, therefore for the same supply voltage the maximum achievable torque is increased with around 15%.

### 1.3.1.3 Twelve step commutation method principle.

The twelve step commutation method commutation signals are presented in Fig. 1.26. This method brings better efficiency and performance for the BLDC motor as presented in Fig. 1.27. The shape of the phase current is not rectangular, and also the shape of the phase voltage is not a simple trapeze, is it between a sine-wave and trapezoidal shape. This has the benefit of a better motor driving performance because the shape of the phase voltage is much closer to the real shape of the Back-EMF signal. From construction point it is very difficult to build the motor with a perfect trapezoidal Back-EMF shape, therefore using the twelve step commutation method for the BLDC motor drive, compensates the imperfections of the Back-EMF signal of a real BLDC motor.

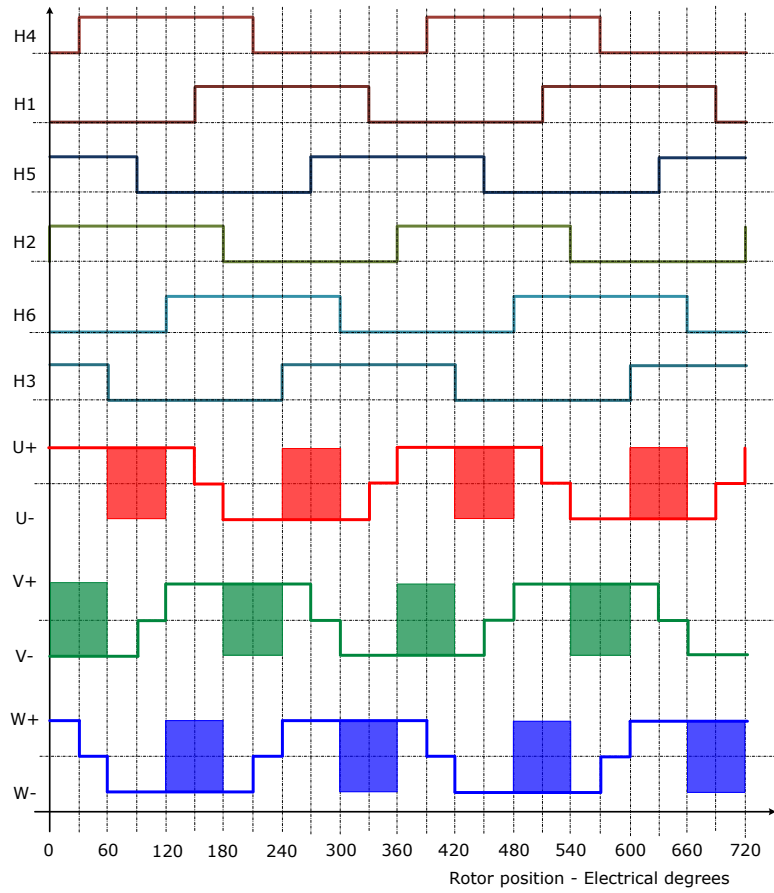


Fig. 1.26 Twelve step commutation signals

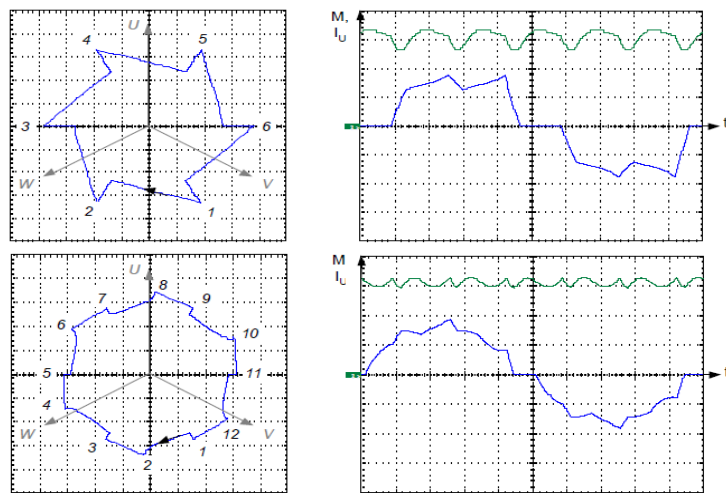


Fig. 1.27 Six VS twelve step commutation performance

Next Fig. 1.28 presents the twelve commutation step configurations, each commutation step being applied for 30° electrical.

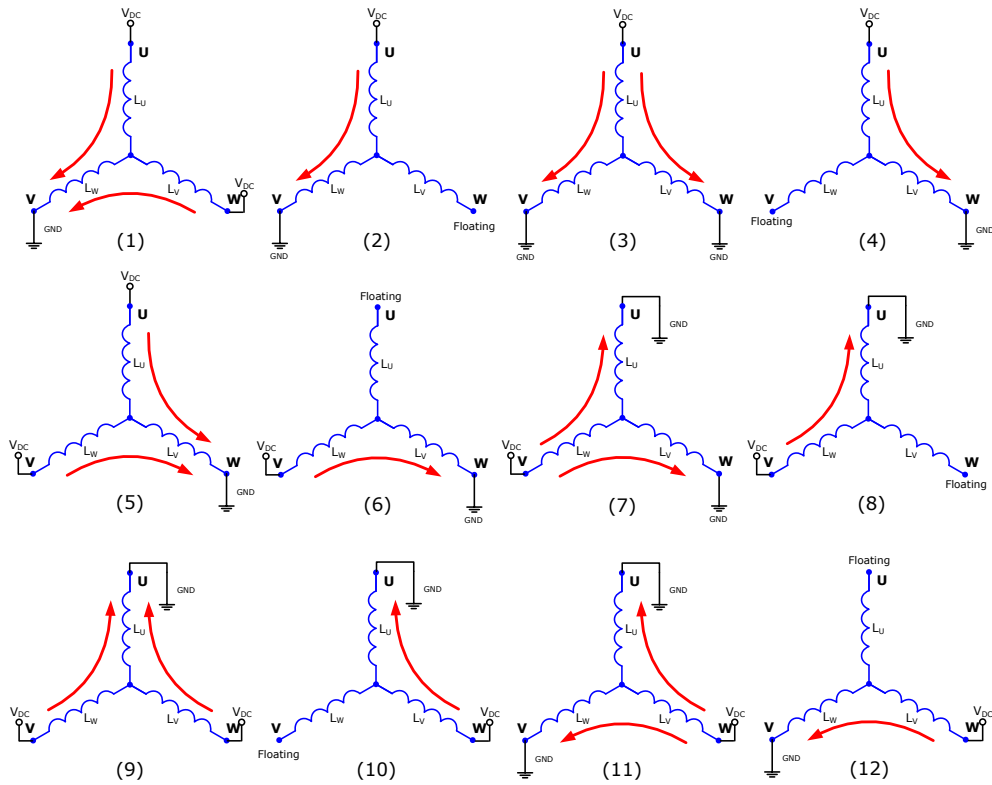


Fig. 1.28 Twelve step block commutation voltage vectors path

## 1.4 Sensorless driving methods

The sensed driving method of a BLDC motor has the obvious advantage of the driving algorithm simplicity, the rotor position is clearly known in all situations in which the motor can be. It is always possible to accurately track the rotor movement in any case for all speed ranges of the motor even at stand still. This fact makes the sensed drive methods preferred for electric actuator applications. However the total cost of such a system is higher due to the HALL sensors and the surrounding electrical and mechanical components (holding mechanics, filters, power supply, connecting wires, additional hall sensor connectors, etc.). The lifetime of such a sensed BLDC motor is often limited by the sensor system itself. This is the most common cause of a sensed BLDC motor failure.

To overcome these limitations sensorless drive of the BLDC motors have been introduced [104]. In recent years several sensorless driving techniques of BLDC motors have been introduced and developed. The following sections present a brief review of sensorless driving strategies including initial position estimation, startup procedures and driving strategies at higher speed based on Back-EMF voltage evaluation [61]-[82], [96]-[105], [108], [206].

A comparison between sensed and sensorless commutation methods for BLDC-SPM machines is done in [194]-[196].

### **1.4.1 Commutation moment detection methods using back-EMF evaluation**

In case of brushless PM machines, the movement of the rotor magnets relative to the phase windings causes the motional EMF to be induced (Back-EMF). The amplitude of this voltage is dependent on the rotor magnets movement speed and position. Therefore the Back-EMF signal contains rotor position information. In practice the extraction of the rotor position information from the motional EMF is very difficult, because of the fast switching phase voltages and currents. A further obstacle is that the amplitude of the Back-EMF signal is directly proportional with the rotor speed. When the motor operates at stand still the amplitude of the back-EMF is zero, at very low speed the amplitude of the back-EMF signal is too low (buried in noise) to be sensed, therefore it is a usual practice to accelerate the motor under open-loop condition using a ramped-up frequency signal [26][27], the parameters of which, should be chosen to match the drive and load parameters. This open loop startup method assumes that the rotor follows the rotating magnetic field induced by the ramped-up frequency phase currents.

This acceleration procedure is very problematic and difficult to implement for all possible operating conditions especially for automotive applications where we have a wide range of operating battery voltage (typically 6 to 18V); ambient temperature (typically for transmission control units  $-40^{\circ}\text{C}$  to  $120^{\circ}\text{C}$ ); and load conditions. It is possible that initially the motor will start to turn in the reverse direction, or show vibrations or even fail to start. To overcome these limitations some driving schemes involve auxiliary sensing methods of high frequency excitation tests to establish the rotor position and define the appropriate initial winding excitation pattern.

The first commutation moment detection methods were described by Lizuka [28]. The proposed method is presented in Fig. 1.29. The phase signals are presented in the upper part of the figure. In this method the zero crossing of the back-EMF of each phase is used as base information for the phase commutation moments detection. These zero crossing moments are independent of the rotor speed, because they occur at rotor positions where the phase winding is not excited (are left open). However this zero crossing positions, as it can be observed in the bottom part of Fig. 1.29., do not correspond to those rotor positions where the commutation between two phases should take place. Therefore the signals must be shifted by  $30^{\circ}$  electrical before they can be used for phase commutation. At the moment when the method was published the shift of the  $30^{\circ}$  electrical was very difficult to implement using only analogic circuits, therefore in the original work [28] a  $90^{\circ}$  electrical shift was used which is very easy to implement using a first order low pass filter (LPF), presented in Fig. 1.30.

The  $90^{\circ}$  electrical delayed signals are used as trigger input for the phase commutation. Because of the  $90^{\circ}$  electrical shift instead of the  $30^{\circ}$  electrical positive zero crossings of the Back-EMF is used to trigger commutation negative currents and vice versa.

This simple back-EMF zero crossing method presents a series of drawbacks making it unpractical implementation for a high performance BLDC motor driving system. The R-C network used to implement the  $90^{\circ}$  electrical phase shift only works at specific frequencies, below this specific frequency the phase shift is too small and over the specific frequency the phase shift is too high and the back-EMF



signals amplitude is hardly attenuated. In addition the heavy filtering inherent in the signal processing limits the dynamic performance of the motor control system.

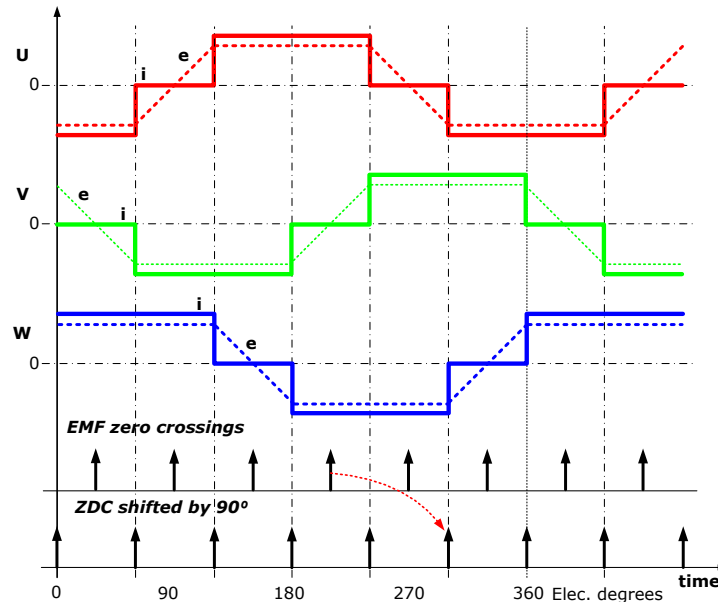


Fig. 1.29 ZCD from the back-EMF signal of a trapezoidal controlled machine

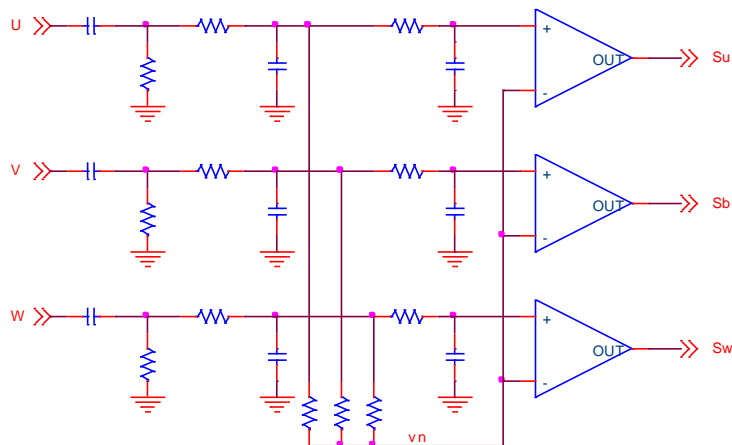


Fig. 1.30 ZCD circuit and the 90° electrical delay circuit (LPF)

On the other hand this method assumes that the phase current decreases very fast when the phase voltage is switched off, so the voltage appearing across the unexcited phase winding is equal to the back-EMF. This may not be true near the motor base speed or in the field-weakening region. Therefore there is an upper speed limit to which the method can be applied. Another drawback is that the motional EMF is measured across the windings of the motor. In case of a star connected machine it is necessary to have a connection to the motor star point,

therefore a fourth connection wire is needed rather than the conventional three phase connections.

Despite these restrictions this method described by Lizuka can be successfully implemented into applications with low required driving performances. As example in the original work [28] a 1.2 kW four pole BLDC motor driving is presented for an air-conditioning fan with speed range from 1950 to 5700 rpm.

An improved method is introduced by Shao [29] who proposed a starting method for the BLDC motor. The open-loop startup method was experimentally determined in an automotive fuel pump application. This algorithm helps to speed up the motor to speeds at which the back-EMF signal amplitude is high enough to be sensed. The algorithm is based on a simple controlled acceleration of the BLDC motor, the acceleration speed being determined experimentally.

The drawback of the low pass filter (LPF) of Lizuka's method is improved with a proposal presented by Amano [30] by changing the LPF with a digital PLL system, by which a constant phase shift of 30° or 90° electrical can be precisely obtained for the zero crossings, regardless to the rotational speed of the rotor. Nevertheless the dynamic range of the sensorless operation was still limited by the low-pass characteristic of the PLL system. Similar limitation where experience in methods presented in [31][32].

For machines with interior magnet rotor configurations (like presented in Fig. 1.9 (b)), armature reaction can cause distortion of the air gap flux distribution and consequently causing errors in the rotor position detection. In the work of Shen and Chen this error source has been analyzed and an armature reaction compensation method was introduced [33].

Most of the sensorless driving methods based on back-EMF sensing have been implemented in laboratory conditions using either analog and digital circuits or digital signal processors (DSPs). In the paper elaborated by Cheng and Tzou [34] a mixed mode integrated circuit is presented in a standard 0,35µm technology in which the back-EMF sensing method is implemented. During the years several commercial integrated circuits has been developed based on this method like those in [35], [159].

A new and innovative method based on the back-EMF sensing is presented by Cheng in [36] with improved dynamic performance of the control system and a much simpler back-EMF zero crossing detection circuit. The method does not require the motor neutral point or the phase shifting of the detected zero crossing positions. The phase commutation signals are directly extracted from the average voltage differences between the phases of the motor, obtained using simple RC filters. The RC filters in this case have higher corner frequency as in the application presented by Lizuka [27] since this method [36] uses the filter to eliminate the high frequency PWM, used to control the speed of the BLDC motor.

The ideal average voltage of the phases for different duty cycles of the PWM control signal are presented in Fig. 1.31. The average of the phase voltages can be described as follows:

- For *I* and *II* position intervals of the rotor the current through the phase is positive therefore:

$$V_{U_{AVG}} = V_{DC} \cdot PWM_{DC} \rightarrow \theta_e = 30^\circ \div 150^\circ \quad (1. 12)$$

- In case of intervals *III* and *VI*, free terminal:

$$V_{U_{AVG}} = \frac{(\theta_e + 30)}{60} \cdot (V_{DC} \cdot PWM_{DC}) \rightarrow \theta_e = -30^\circ \div 30^\circ \quad (1.13)$$

$$V_{U_{AVG}} = PWM_{DC} \cdot V_{DC} - \frac{(\theta_e - 150)}{60} \cdot (PWM_{DC} \cdot V_{DC}) \rightarrow \theta_e = 150^\circ \div 210^\circ \quad (1.14)$$

- For intervals IV and V, the voltage through the phase is negative, therefore:

$$V_{U_{AVG}} = 0 \rightarrow \theta_e = 210^\circ \div 330^\circ \quad (1.15)$$

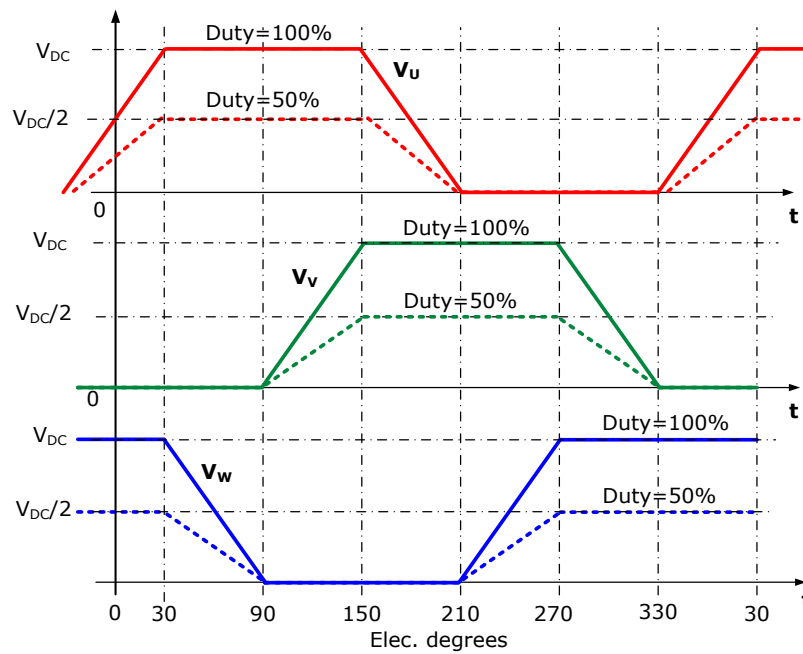


Fig. 1.31 Ideal average phase voltage waveforms

Concluding based on equations (1.12) – (1.15) the average voltage between two motor phases can be expressed as follows [36]:

$$V_{UW_{AVG}} = PWM_{DC} \cdot V_{DC} \rightarrow \theta_e = 90^\circ \div 150^\circ \quad (1.16)$$

$$V_{UW_{AVG}} = (-PWM_{DC} \cdot V_{DC}) + \frac{(\theta_e + 30)}{120} \cdot (2 \cdot PWM_{DC} \cdot V_{DC}) \rightarrow \theta_e = -30^\circ \div 90^\circ \quad (1.17)$$

$$V_{UW_{AVG}} = (PWM_{DC} \cdot V_{DC}) - \frac{(\theta_e - 150)}{120} \cdot (2 \cdot PWM_{DC} \cdot V_{DC}) \rightarrow \theta_e = 150^\circ \div 270^\circ \quad (1.18)$$

The equation (1.18) demonstrates that zero crossings appear at  $30^\circ$  and  $210^\circ$  electrical. In the same way zero crossings are detected at the other two phase signals (average between the other phase voltage combinations). Based on

equations (1.16)-(1.18) Fig. 1.33 presents the relationship between the back-EMF voltage ( $e_a$ ) and the average voltage difference between two phases ( $a$  and  $c$  phases) in a graphical form. In the figure it can be clearly seen that the zero crossings of the average voltage difference between the two phases coincide with the zero crossings of the back-EMF voltage, the ideal commutation points of the phase voltages.

Fig. 1.32 shows the zero crossing detection circuit proposed in the original work [36]. At the output of the circuit we obtain the virtual hall signals  $H1$ ,  $H2$  and  $H3$ , which are used to drive the block commutation (in the original work the six step commutation method is implemented).

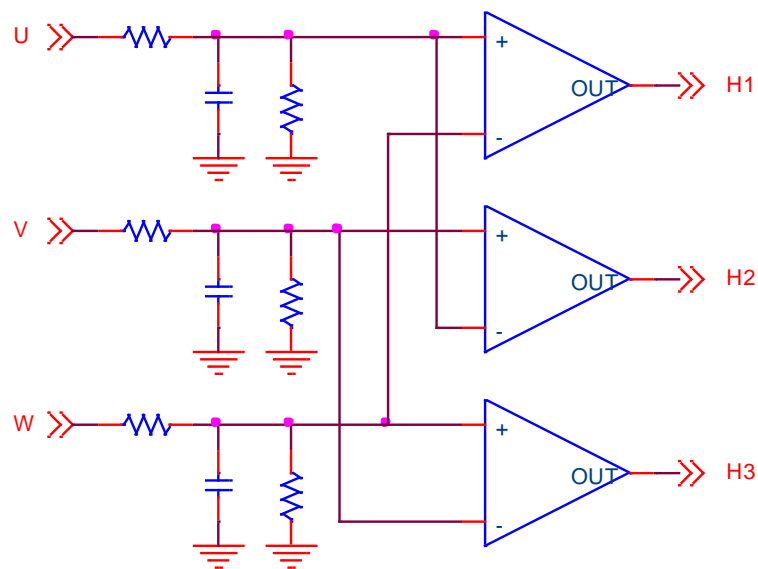


Fig. 1.32 Zero crossing detection circuit proposed in [36]

The performance of the above method is still limited by the rejection performance of the RC LPF network, being a first order filter it may not be able to reject all the disturbances of the PWM signal to obtain a smooth average value. In case we decrease the cutoff frequency we can obtain a better PWM disturbance rejection but it leads to a degraded dynamic performance of the driving system, especially at high rotational speeds where the delay caused by the LPF is becoming significant.

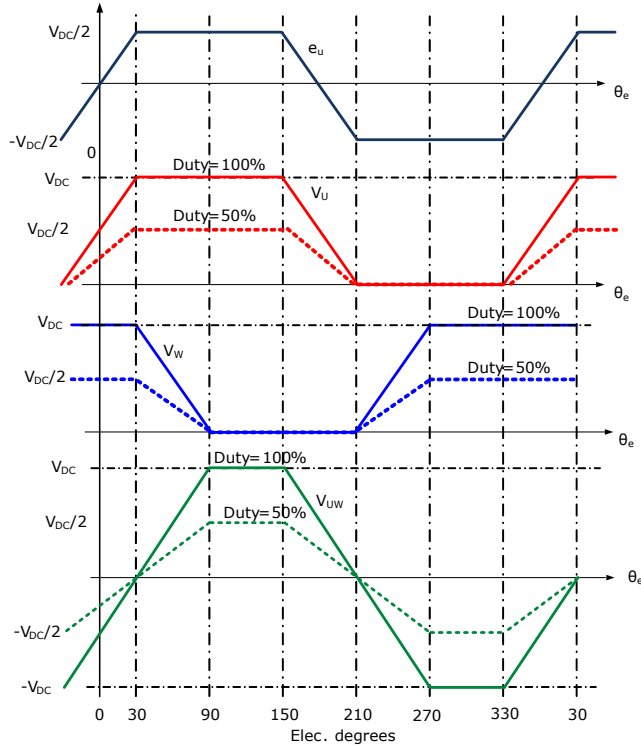


Fig. 1.33 Back-EMF and average voltage between two phase relationships [36]

To overcome this limitation in [37] a similar method is presented in which the three R-C low pass filters used to suppress the PWM signal are replaced with three synchronized sample and hold stages. The next Fig. 1.34 presents the signal process sequence proposed by the author in the original work [37].

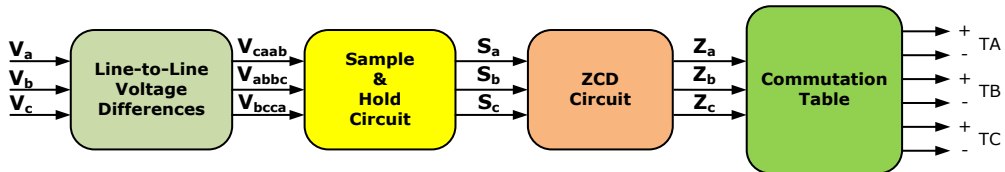


Fig. 1.34 Signal processing sequence proposed in [37]

In this work a startup procedure is also defined, which consist in the alignment of the rotor position to a predefined position by applying a known voltage vector to the motor phase windings for a predefined time period. The rotor then will align with the induced magnetic field. Now with a known initial position a voltage vector advanced with  $120^\circ$  electrical is applied (with two commutation steps ahead). This will ensure that the rotor will turn  $120^\circ$  electrical and makes possible the next zero crossing detection of the back-EMF at  $60^\circ$  electrical, continuing the procedure until the rotor gain enough speed that induces high enough back-EMF signal amplitude that can be detected at every  $60^\circ$  electrical. In Fig. 1.35 the startup signals

sequence is presented, where with TA+, TA-, TB+, TB-, TC+ and TC- denoting the three phased inverter control signals, one corresponding to each switching element.

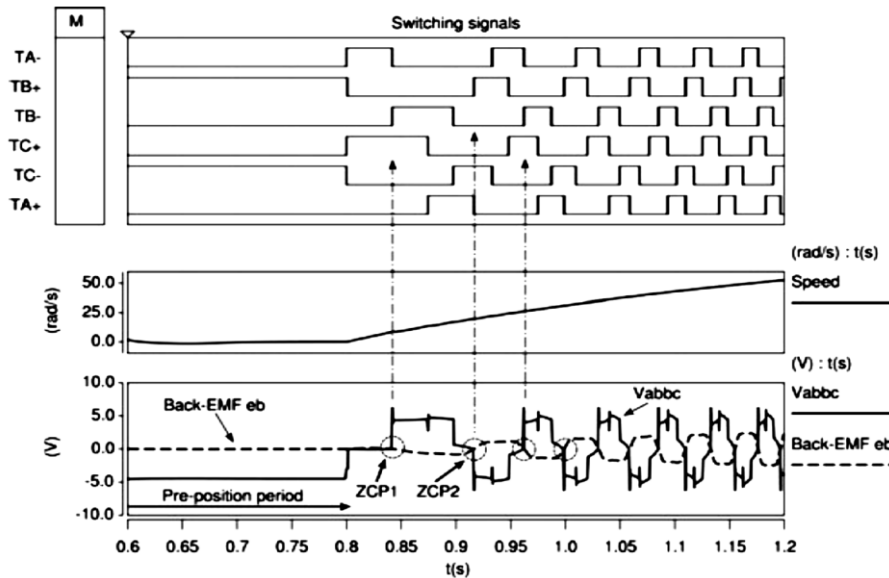


Fig. 1.35 Startup sequence of the method proposed in [37]

This method still presents some drawbacks, like failing to align the rotor if the initial rotor position is with  $180^\circ$  electrical distance (or close to) from the applied alignment vector. In this case the electro motive force is in the rotor shaft direction not causing any motional force. At startup voltage vectors with  $120^\circ$  advance are applied which generates much less torque than the motor would be capable of, combined with a possible high static load and friction, the motor may fail to start. Improvements regarding this issue are presented in the next subchapter which briefly presents the most representative initial position estimation methods.

#### 1.4.2 Commutation moment detection methods based on the third harmonic

Commutation moment estimation method for BLDC permanent magnet machines based on the third harmonic of the back-EMF signal first was introduced by Moriera [38]. This method resolves the need of the zero crossing detection signals phase shifting, described in the previous subchapter (the first three methods). Fig. 1.36. presents the star connected machine windings (star connection point denoted with  $N$ ) and the three star connected resistors parallel to the motor terminals (star connection point denoted with  $VN$ ).

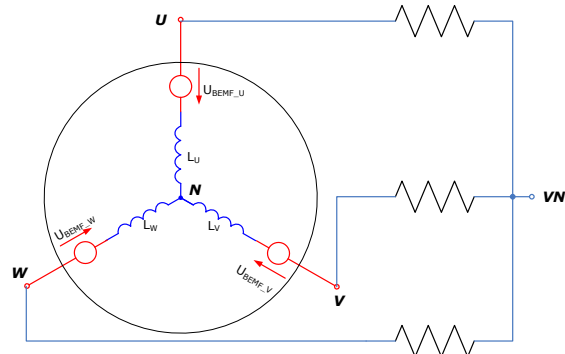


Fig. 1.36 Generation of reference voltage for the third harmonic evaluation

Assuming that the resistance of the three star connected resistors and three windings inductance, are equal, furthermore the phase voltages and the induced back-EMF waveforms are as shown in Fig. 1.37, it can be demonstrated that voltage between the two star points  $N$  and  $VN$  is equal to the mean of the three phases back-EMF. Fig. 1.37 shows the  $V_{N-VN}$  voltage relationship to the rotor position. The  $V_{N-VN}$  voltage has three times the frequency of the phase fundamental (base) frequency component from where the method name is derived as the “third harmonic” of the back-EMF, though it also contains higher order frequency harmonics. The  $V_{N-VN}$  voltage zero crossings to be useful as phase commutation signal trigger must be shifted with  $30^\circ$  electrical. This is achieved by integrating the  $V_{N-VN}$  voltage as shown in Fig. 1.37, the integrated voltage zero crossings being used as trigger for the phase commutation.

A limitation of the method is given by the assumption that the phase inductances and resistor resistances from the star network are equal, which is not true, in practice they are not equal because of their manufacturing tolerances, which is even degraded over temperature and lifetime. The method cannot be successfully applied to BLDC motors which present significant saliency, because this causes differences in the motor phase inductances [13]. Furthermore the integration of the  $V_{N-VN}$  voltage being implemented with low pass filters, the constant  $30^\circ$  electrical shift cannot be ensured for all speed ranges of the motor. However the filtering requirements are much reduced compared to the method introduced by Lizuka [28] (presented in the last subchapter), therefore the speed range is extended with a better dynamic performance of the driving system. In addition current flowing in the third phase (left open) does not disturb the zero crossing detection method. This makes the method suitable also at high speeds or in the field weakening region of the BLDC motor (using phase advancing, over the base speed of the motor). The weakening drive of a BLDC motor using the third harmonic was demonstrated by Shen [39] even up to very high speed when current flows through all the three phases all the time.

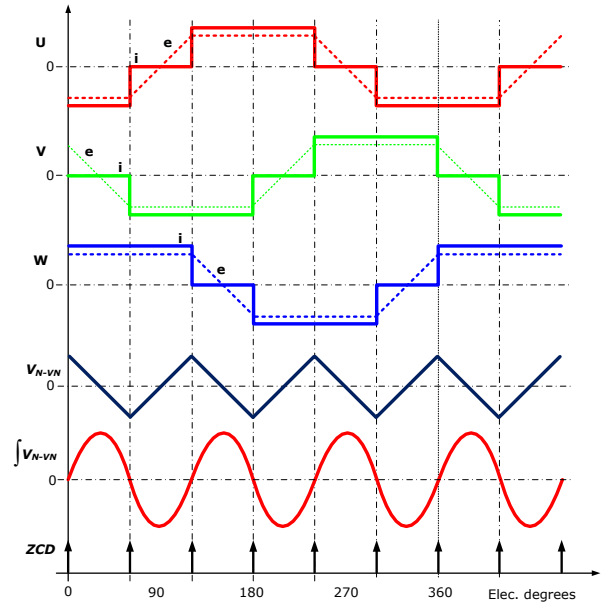


Fig. 1.37 Commutation point detection based on the third harmonic of the back-EMF

### 1.4.3 Commutation detection methods using the floating terminal voltage

In case of six step trapezoidal driving of a BLDC motor with permanent magnets at any given moments only two of the motor terminals are supplied. One is connected to high supply voltage  $V+$  ( $V_{BATT}$ ) and the other to low supply voltage  $V-$  or GND, the third terminal is left in high impedance, floating (see Fig. 1.38).

From the voltage amplitude and waveform at this free terminal the back-EMF signal can be extracted and evaluated for rotor position information.

In Fig. 1.38 are presented the three back-EMF voltages having as reference voltage the star connection between the windings denoted with  $N$ . The amplitude of these back-EMF voltages is directly proportional to the rotor speed. For every complete electrical revolution there are two zero crossings of the back-EMF signal for each phases of the motor. One is a positive zero crossing and second a negative zero crossing (see Fig. 1.39).

In most cases, access to the neutral terminal voltage is not possible because of the missing connection to the motor star point in case of a star connected machine, or in case of a delta connected motor, the physical neutral point doesn't exist. In these cases the back-EMF voltage zero crossing detections are referred to the negative supply voltage (GND).

A method already considered as classic, is the comparison of the floating terminal voltage with a zero crossing reference voltage equal with the half of the supply voltage ( $V_{BATT}$ ) [20]. The reference voltage can be expressed as follows:

$$V_{REF\_ZCD} = \frac{V_{BATT}}{2} \quad (1.19)$$



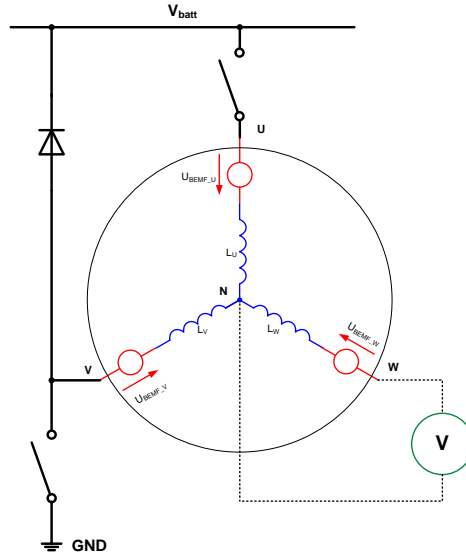


Fig. 1.38 Measurement procedure of the Back-EMF voltage at the third terminal

Using this method, zero crossing detection is only possible during the ON time of the driving PWM signal, as shown in Fig. 1.39. The below Fig. 1.40 presents the zero crossing moments during one commutation cycle, for both positive (Fig. 1.40 (a)) and negative (Fig. 1.40 (b)) zero crossing possibilities.

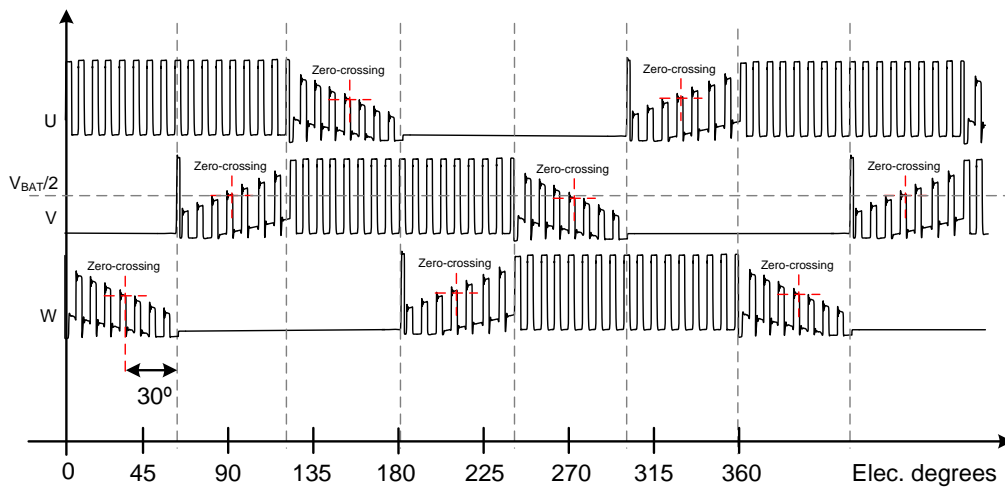


Fig. 1.39 ZCD comparing the floating terminal voltage with  $V_{batt}/2$

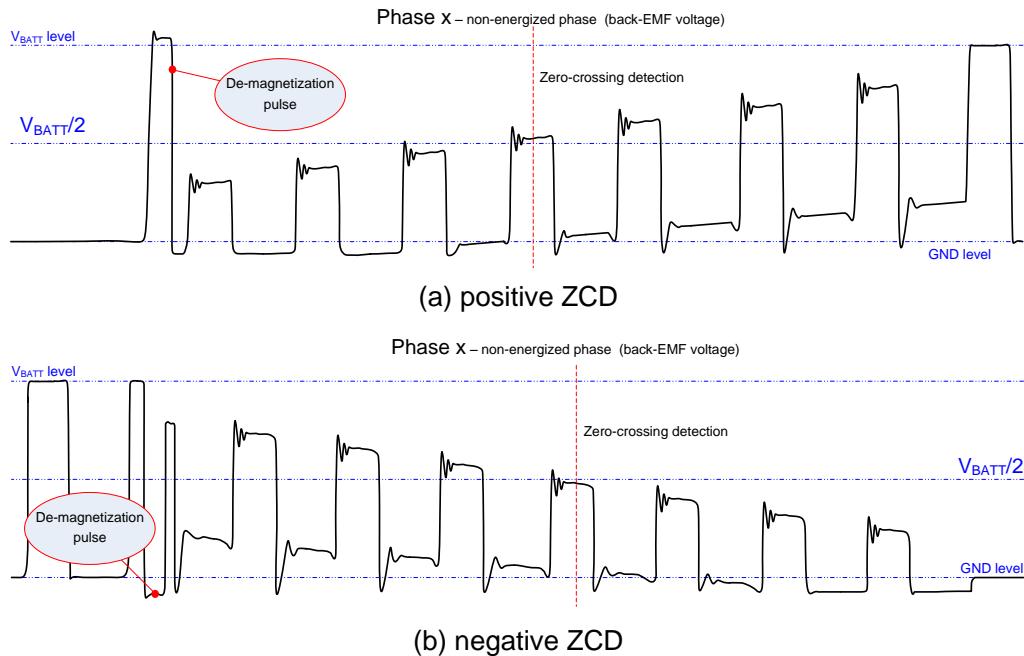


Fig. 1.40 ZCD at the floating terminal during one commutation period

In the figures some parasitic oscillations (high frequency ringing) can be observed after every rising edge of the floating terminal, which can lead to early zero crossing detections. To overcome this problem the floating terminal voltage is filtered using a low pass filter (LPF). The cutoff frequency of this LPS must be set to a higher frequency than the base frequency of the PWM signal not to influence significantly the rise time of the voltage at the floating terminal. Another technique which can be applied to compensate this error source is to disable the zero crossing detection mechanism for a predefined "blank time" after each PWM rising edge, blank time equal to the ringing period. These small ringings are caused by the resonance between the parasitic capacitances and inductances in the motor and the power inverter itself.

The main drawback of this method is that zero crossings detection is only possible during the ON time of the PWM signal. Therefore zero crossings of the back-EMF signal during the OFF time of the PWM will remain undetected until the next ON phase of the PWM. This fact can cause significant delays in the phase sequence commutation moments, especially at high speeds, degrading the motor speed and torque performance. The usage of low frequency PWM control signals further worsen the control circuit performance, therefore it is preferred that this zero crossing detection method is used together with a high enough PWM signal which causes insignificant delays in the zero crossing detections.

This method requires a minimum rotational speed. The average voltage "ramping" at the floating terminal is speed dependent, equal with the back-EMF voltage amplitude. At low speeds (In Fig. 1.41 (a)) having very low amplitude for the back-EMF, the voltage at this terminal is constant. In Fig. 1.41 it can be clearly seen the back-EMF signal effect and its amplitude for low and high RPMs, this can be observed by the ramping of the floating terminal voltage.

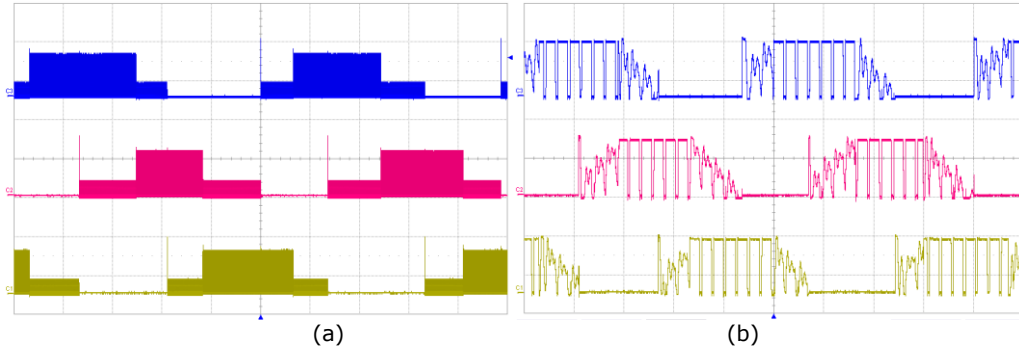


Fig. 1.41 Amplitude of the Back-EMF voltage at low and high speeds

In case of Fig. 1.41 (a) because of the very low amplitude of the back-EMF the ZCD is not possible therefore the motor cannot be driven with the above described method.

In Fig. 1.39, Fig. 1.40 and Fig. 1.41 it can clearly be observed that the ZCD points does not coincide with the phase commutation points. Ideal the detected zero crossings are in the middle of a commutation period. Therefore the phase commutations should happen with a 30° electrical delay. In practice for most applications this is implemented by software in the system control DSP (Digital Signal Processor) or microcontroller.

An improved method based on ZCD at the floating terminal is introduced by ST Microelectronics patented as “3 Resistor Method” [24][40][41]. The basic idea is to sense the presence of a freewheeling current through the LS MOSFET (substrate diode) of the floating output (Fig. 1.42). So ZCD of the back-EMF signal happens during OFF phase of the PWM when a crossing from negative to positive voltage, as presented in Fig. 1.43.

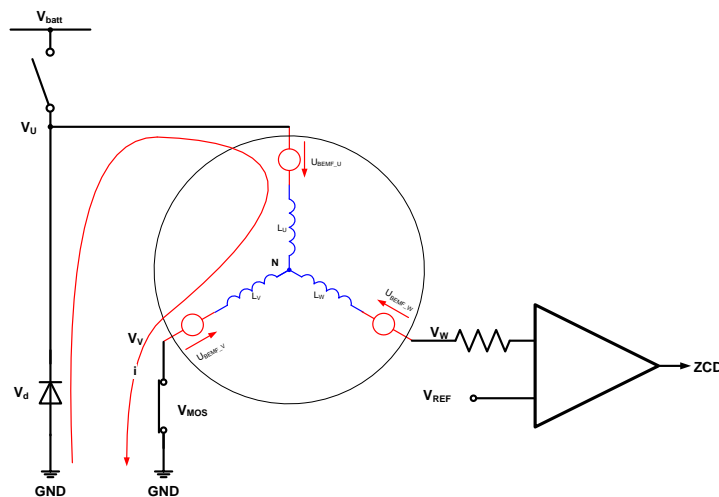


Fig. 1.42 Clamping of Back-EMF voltage, during OFF state of the PWM

When the HS MOSFET is OFF, the freewheeling current will flow through the corresponding LS MOSFET (from the same half-bridge) substrate diode. During this

period the voltage at the W terminal of the motor is considered to be the back-EMF voltage of phase W because no current flows through this phase.

The voltage at this terminal ( $V_W$ ) for this case can be expressed:

$$V_W = U_{BEMF\_W} + v_n \quad (1.20)$$

From this equation results, that the voltage ( $V_W$ ) at the W terminal is equal to back-EMF voltage only when the voltage at the neutral point of the motor,  $V_n$  is zero.

- the phase U effect  $V_n$ :

$$v_n = 0 - v_d - ri - L \frac{di}{dt} - u_{BEMF\_U} \quad (1.21)$$

- the phase V effect on  $V_n$ :

$$v_n = v_{mos} + ri + L \frac{di}{dt} - u_{BEMF\_V} \quad (1.22)$$

Where with  $V_d$  denoting the MOSFET transistor reverse diode (body diode) drop voltage and  $V_{MOS}$  representing the D-S drop voltage of the MOSFET during ON state.

Combining the above two equations (1.21 and 1.22) we obtain:

$$2v_n = v_{mos} - v_d - (u_{BEMF\_U} + u_{BEMF\_V}) \quad (1.23)$$

$$v_n = \frac{v_{mos} - v_d}{2} - \frac{u_{BEMF\_U} + u_{BEMF\_V}}{2} \quad (1.24)$$

- From the three phased system balance we have:

$$u_{BEMF\_U} + u_{BEMF\_V} + u_{BEMF\_W} = 0 \quad (1.25)$$

- therefore results:

$$v_n = \frac{v_{mos} - v_d}{2} - \frac{u_{BEMF\_W}}{2} \quad (1.26)$$

$$v_W = u_{BEMF\_W} + v_n = \frac{3}{2} u_{BEMF\_W} + \frac{v_{mos} - v_d}{2} \quad (1.27)$$

If we ignore the second term from equation (1.27) the result will represent the back-EMF voltage itself. This method as all previous ones is not valid at low speeds where we have very small amplitude of the back-EMF, where also the second term of equation (1.27) becomes significant. In case of MOSFET transistors with very low ON resistance  $R_{DS(ON)}$  the  $V_{MOS}$  term will become insignificantly small, therefore the voltage at  $V_C$  (from equation (1.27)) will be:

$$v_c = e_c + v_n = \frac{3}{2}e_c - \frac{v_d}{2} \quad (1.28)$$

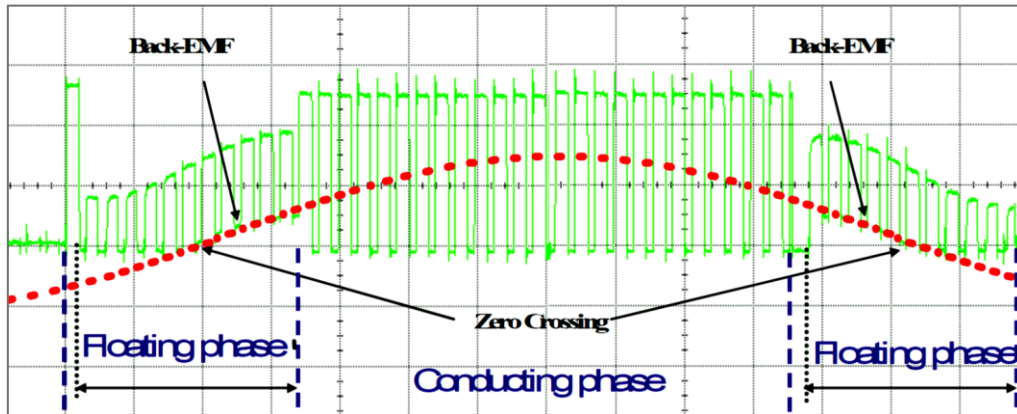
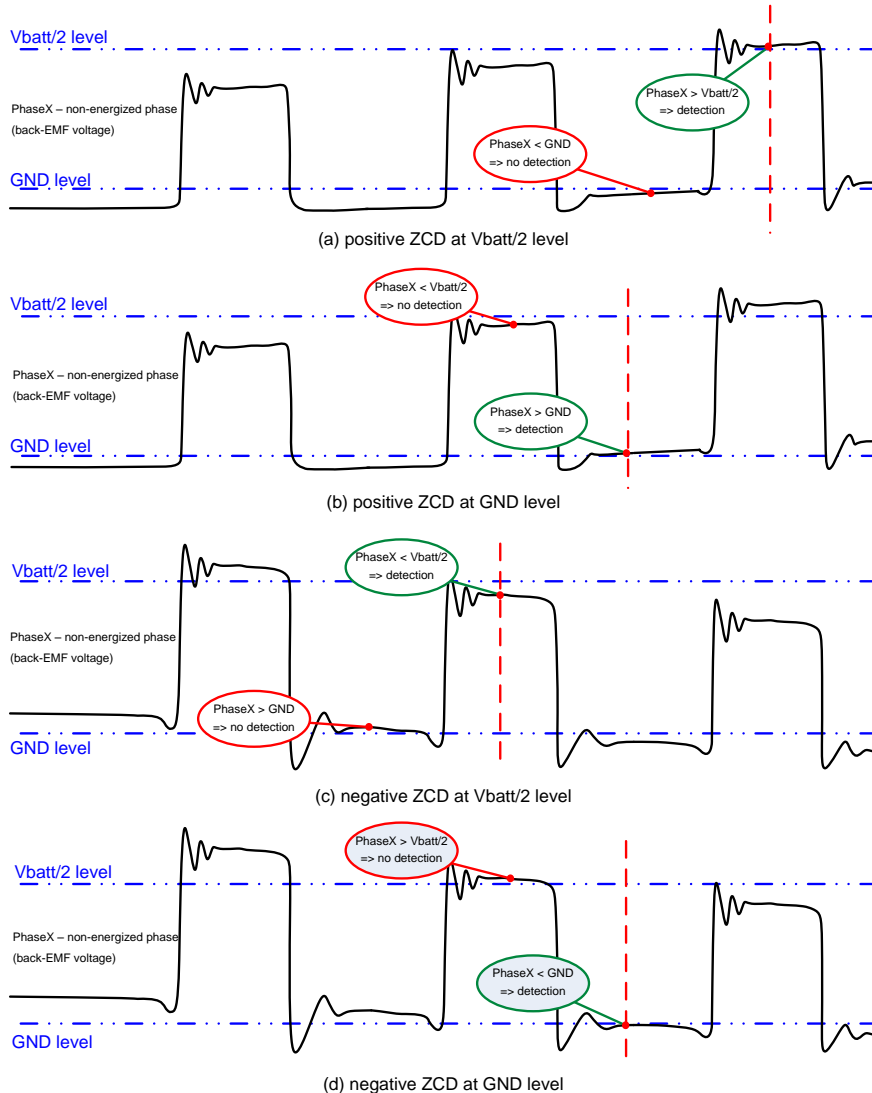


Fig. 1.43 ZCD during OFF state of the PWM at the floating terminal [40]

In conclusion back-EMF zero crossings in this method are detected during the OFF time of the PWM signal, during the freewheeling period by sensing the negative to positive crossing of the voltage at the floating terminal. The advantage of this, compared with the method in which the floating terminal voltage is compared to the half of the battery voltage is that the back EMF has a higher value due to the freewheeling back-EMF current path which goes through a diode. The presence of the negative drop voltage on this diode is very easy to sense. Therefore the speed range to which the method can be applied goes to lower speeds than the other methods.

A disadvantage of this method is that it cannot be applied at very high or at 100% duty cycle, because there is no or very short freewheeling period and the control electronics isn't fast enough to sense it. Another drawback in case the real ZCD moment happens during the ON phase of the PWM signal, it will not be detected until the next OFF phase of the PWM.

Shao propose an improved version of the above two presented ZCD detection method by combining them together [24], [42], [43]. Therefore we obtain a method in which the advantages from both methods are combined. The ZCD detection in this case will be active for both states of the PWM period (during ON and OFF).

Fig. 1.44 ZCD at  $V_{batt}/2$  and GND level

In Fig. 1.44 the commutation method and ZCD detection points are presented for all possible cases, positive ZCD detection at  $V_{batt}/2$  level (Fig. 1.44 (a)), at GND level (Fig. 1.44 (b)) and negative ZCD at  $V_{batt}/2$  level (Fig. 1.44 (c)), at GND level (Fig. 1.44 (d)). As it can be observed the detected ZCD points do not coincide with the phase sequence commutations. Therefore the ZCD points must be delayed with  $30^\circ$  electrical in order to be used as direct commutation step trigger signal.

At the moment this ZCD detection method is considered as the best applicable solution for industrial and automotive applications, fact proven by the multitude of sensorless BLDC motor driver ASIC's and control electronics which have been recently developed [44], [45], [135]-[146], [158]-[160].

### 1.4.4 Sensorless drive methods based on flux linkage variation

Implementation of BLDC motor drive methods based on flux linkage variation is not very common. Such methods offer a very high performance drive of the brushless motor, requiring in the same time high computational power and continuous measurement of phase voltages and currents. Because of this aspect sensorless drive of brushless motors based on flux linkage variation is mainly applied for PMAC (Permanent Magnet Alternative Current) or PMSM (Permanent Magnet Synchronous Machine) motors drive, using sinusoidal shaped phase currents and voltages. However a simplified version of such methods can be implied in case of sensorless implementation of 180° and twelve step block commutation methods because in these cases the back-EMF evaluation methods based on floating terminal voltage evaluation is not possible because of the missing floating phase.

#### 1.4.4.1 Flux linkage based drive principle

The operation principle of flux linkage based control is not a very recent idea. But the implementation of such methods has been adopted just recently, made possible by the increased real time computational power offered by modern embedded systems.

The fundamental idea of the methods is based on the phase voltage equation [13]:

$$v = R \cdot i + \frac{d\psi}{dt} \quad (1.29)$$

- where  $v$  represents the phase voltage,  $i$  the phase current,  $R$  the phase resistance and  $\psi$  the flux linkage;

The flux linkage is a function of phase current and rotor position, therefore the equation (1.29) can be reformulated as:

$$\psi = \int \{v - R \cdot i\} \cdot dt \quad (1.30)$$

From the above two equation if the voltage drop on the phase resistance is extracted and the result integrated, a continuous flux linkage estimation is obtained.

For some systems due to high phase voltages the measurement of the phase voltages is difficult to implement because of electrical isolation issues between the power inverter and control electronics, so the phase voltages are estimated knowing the DC supply voltage value and control signals of the power inverter (applied duty cycles at each phase).

The small offset errors of the voltage and current measurements can lead to saturation of open loop implemented integrators (as eq. 1.30), because these small offsets are summed in time. This problem can be solved using analog integrator circuits or alternative integration methods as presented in [47], however these limit the minimum operational speed at which the motor can be efficiently driven.

The main preferred implementation of such methods is the closed loop flux linkage estimation, part of the rotor estimation process. There are two categories of drive methods based on flux linkage variation. The first includes a mechanical model of the system requiring deep knowledge about the mechanical system and behavior

driven by the motor. The second category is independent from the system mechanical model, thus being less sensitive to mechanical load variations.

#### 1.4.4.2 Flux linkage observer using mechanical model

The next Fig. 1.45 presents the control loop principle based on a closed loop flux linkage observer. The system has as input parameters the supply voltage and current of the power converter, which are used to calculate the phases initial flux linkage. The flux linkage and current can be used to calculate the generated torque, which is an input parameter for the system mechanical model (1.31).

$$\frac{d\omega}{dt} = \frac{1}{j} \cdot (T - B\omega - T_L), \frac{d\theta}{dt} = \omega \quad (1.31)$$

- where with  $j$  denoting the mechanical inertia,  $B$  the viscosity constant and  $T_L$  the load torque.

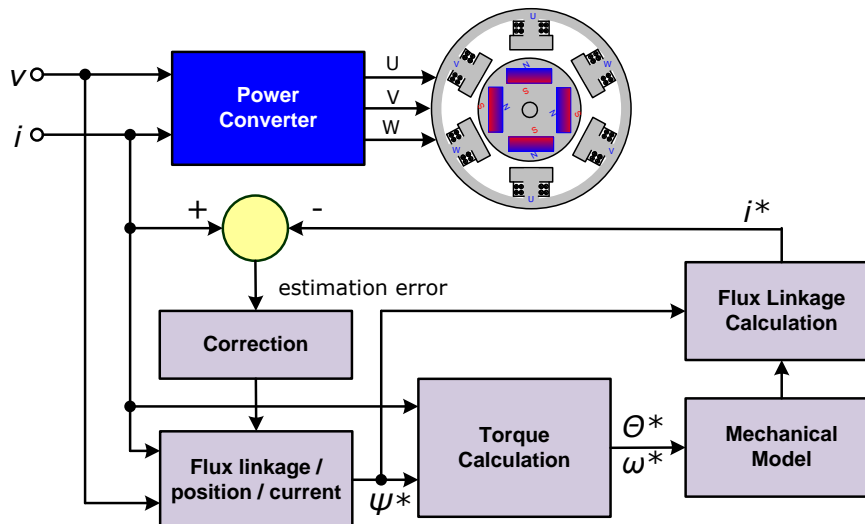


Fig. 1.45 Closed loop flux linkage observer using the system mechanical model

Next the rotor speed  $\omega$  and position  $\phi$  is estimated. To close the loop, from the rotor estimated position and flux linkage the phase currents are estimated which are compared to the actual measured phase currents, from which the estimation error results. This estimation error is then applied to the initial flux estimator and the saturation tendencies of the integrator, caused by the measured parameters offsets are compensated.

First implementation of methods based on the presented concept has not given promising results due to the lack of real time computational power of the existing embedded systems of that time [48], [49], [63]. Advances in DSP technology made possible the successful implementation of such methods. In [50] the author presents an extended Kalman filter which has been successfully implemented on a DSP. The stator winding resistance has been also included in the control algorithm to compensate its errors from the flux linkage estimation.



### 1.4.4.3 Flux linkage observer without mechanical model

The observers including the system mechanical model suffers from errors caused by the used mechanical model accuracy and its parameters definition tolerances, therefore new methods have been introduced avoiding the necessity of an accurate mechanical model.

The basic principle of such an observer without the need of the system mechanical model is presented in Fig. 1.46. The flux linkage is calculated by integrating the input voltage and current, then the rotor position is estimated using pre-stored characteristic values of the flux/position/current. The estimated phase currents are then compared with the measured currents generating an estimation error which is used to compensate the integrator saturation caused by the input parameters measurement offsets.

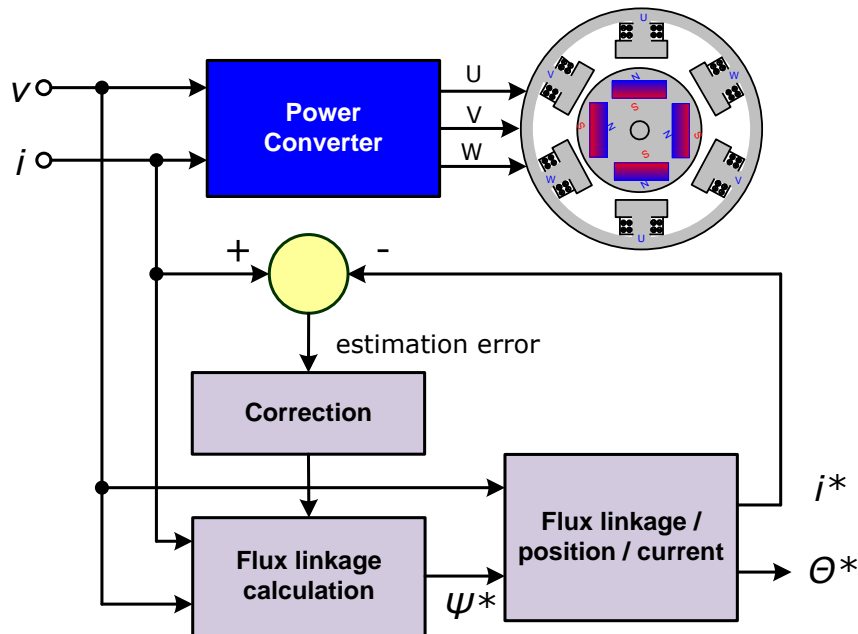


Fig. 1.46 Rotor position observer based on flux linkage without mechanical model

In [51] the authors present a “Luenberger” observer type, successfully applied in the sinusoidal drive of a surface mounted permanent magnet machine. The flux/position/current characteristic values have been represented in a sinusoidal form. In absence of saliency, the control of the motor below 100 RPM was not possible. Below 100 RPM the rotor position estimation was done using position hall sensors with a 30° electrical resolution. In a later work [52] the same authors propose a real time correction method of the position estimation errors caused by the motor parameter changes, implemented using neural networks.

## 1.5 Sensorless initial rotor position estimation methods

The sensorless driving methods presented in the last subchapter can be applied only when the motor has a minimum rotational speed, otherwise the back-EMF signal amplitude is too small to be sensed. At standstill of the rotor the problem is even higher because there is no back-EMF voltage at all, but the control electronics has to apply the correct phase vector to move the rotor in the desired direction. In order to cope with these problems several initial position detection methods and startup procedures have been developed over the last years. The most classic method is the acceleration of the rotor in open loop mode, by injecting phase currents with a controlled ramped up frequency [13]. The ramping frequency and phase current amplitude in most of the cases is defined by experimental investigations. However with an unknown initial position combined with a possible high static friction and variable mechanical load, the rotor may temporary start to rotate in the opposite direction, present mechanical vibrations, or even may fail to startup.

### 1.5.1 Rotor pre-alignment process

A very simple solution to the rotor initial position definition is to pre-align it with a predefined known position and startup the rotor from there [53]. The procedure described in the original work is based on the energization of two of the motor phases (like in Fig. 1.47 (a)), which theoretically will cause the rotor to align with this energization direction (voltage vector).

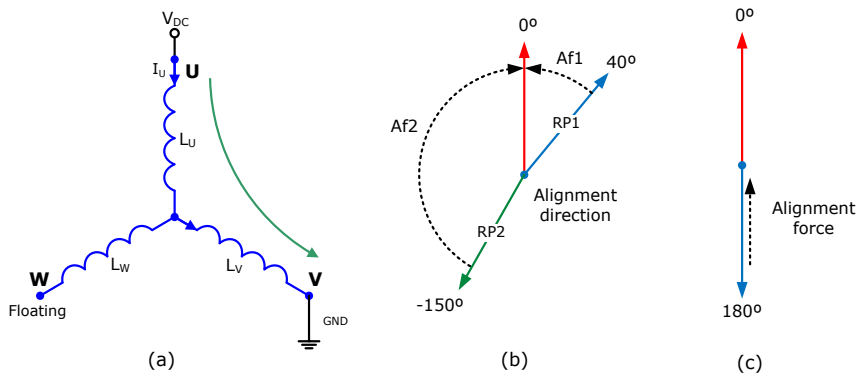


Fig. 1.47 One stage pre-alignment process

This phase alignment process has the disadvantage that it creates a very weak alignment force when there is a big distance between the applied pre-alignment voltage vector and the actual rotor position. In case of Fig. 1.47 (b) the first initial position example (**RP1** at  $40^\circ$  electrical distance) is close to the applied voltage vector direction and the generated torque will cause the alignment of the rotor (turn it in counter clockwise direction until aligned). In case of an initial rotor position represented by **RP2** (Fig. 1.47 (b)) the generated torque by the applied voltage vector is very weak, because the initial rotor position is too far away from the applied voltage vector direction. The EMF force decreases drastically for angle

differences between the induced field and actual rotor position orientation higher than  $90^\circ$  electrical. Therefore the rotor will never align with the applied voltage vector direction because of the large static friction and mechanical load, or further increase of the load current can generate enough force to align the rotor but this may cause permanent demagnetization damage to the rotor magnets. On the other hand in case that the rotor orientation is exactly with  $180^\circ$  electrical in the opposite direction regarding the applied voltage vector direction the generated force is in the direction of the rotor central shaft, generating no motional force at all.

This weakness of the single vector pre-alignment process can be eliminated by using two or three stage pre-alignment process. The basic idea behind is to pre-align the rotor with two (Fig. 1.48 (a)) or three (Fig. 1.48 (b)) predefined positions with  $60^\circ$  electrical angle between them. The last alignment position being the desired initial position from which the motor will be started-up.

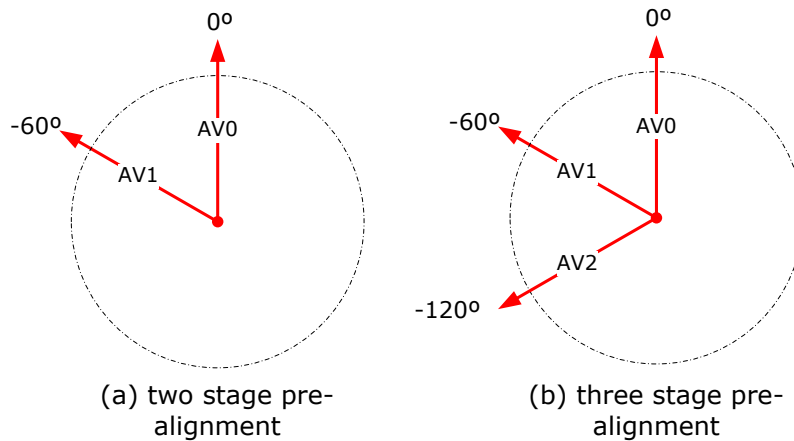


Fig. 1.48 Multi stage pre-alignment vector directions

Fig. 1.49 presents a two stage pre-alignment process example, with two initial rotor position examples, denoted with RP1 and RP2. The first pre-alignment vector AV1 applied is with  $60^\circ$  electrical in advance from the desired final position (Fig. 1.49 (a)). This will cause the rotor from the first position RP1 to align with the voltage vector, the second rotor at RP2 position is not able to align with this first vector because the force is toward its shaft direction (center). Therefore after the first pre-alignment stage we end-up in rotor positions as shown in Fig. 1.49 (b). The second pre-alignment vector has the same direction with the desired initial rotor position (Fig. 1.49 (c)). For both presented rotor position cases, the rotors will be able to align with the final position. However the alignment forces are not equal, AF3 (alignment force of RP1) is much bigger than AF4 (alignment force of RP2). In case of high static friction and mechanical load the rotor aligned initially to RP2 is most likely to fail to align to the predefined position. The three stage pre-alignment process ensures a maximum of  $60^\circ$  electrical angle difference between the last pre-alignment voltage vector (AV0) direction and rotor position, in which circumstances the rotor will always align with the desired position. However the three stage pre-alignment process lasts almost three times longer than the one stage pre-alignment process.

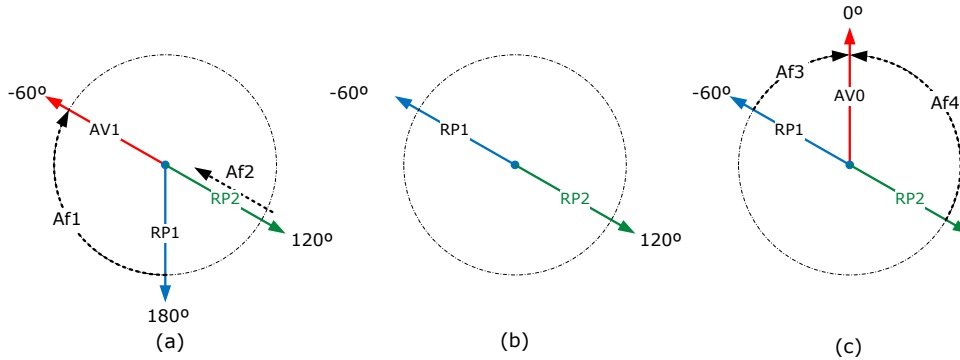


Fig. 1.49 Two stage pre-alignment process

A major problem for some applications like electric vehicles, sensitive actuators, is the possibility of reverse rotation of the rotor during the alignment process. On the other hand if the application has requirement to startup in very short time like in case of automotive oil and fuel pumps, the pre-alignment process consumes precious startup time, and doesn't help in the successful startup of the motor in the desired time frame.

A solution to this problem is given by initial rotor position estimation algorithms. Several methods has been developed and successfully applied, the next subchapters present a comprehensive overview of the existing initial rotor position estimation and startup methods.

### 1.5.2 Initial position detection using phase inductance variation

Rotor position influences the phase windings inductance in case of BL motors which present saliency. This can be sensed by evaluating the rate of phase current change.

The current change speed through a coil is limited by the coil inductance and resistance itself. Therefore, because the rotor position causes changes in the winding inductance (motors with saliency), the rotor position can be estimated from the evaluation of the phases winding inductance or the rate of current change through the phases. The great benefit of the idea is that it can be applied also at stand still or at very low speeds where the methods based on back-EMF detection cannot be applied.

In case of motors without saliency the phase winding inductance will still change (just with a much smaller amount) with the rotor position, but it can be evidenced only at high phase currents which causes saturation of the phase windings magnetic core [13], [59]-[81], [88]-[90].

The total flux-linkage of a BLDC motor  $\lambda_{phase}$  is the sum of the magnetic flux given by the rotor permanent magnets  $\lambda_{PM}$  and the magnetic flux generated by the phase currents ( $i$ ) [54], therefore:

$$\lambda_{phase} = \lambda_{PM} + L \cdot i \quad (1.32)$$

- where  $L$  represents the energized phase inductance.

This presents a very nonlinear characteristic mainly given by the saturation effect of the windings magnetic core. With  $i^+$  and  $i^-$  denoting the phase currents which generate magnetic fluxes of the same respectively opposite directions to the magnetic flux direction of the rotor permanent magnets.

From Fig. 1.50 we can observe that the change of the flux linkage in case of  $i^+$ ,  $\Delta\lambda^+$  is smaller than for  $i^-$ ,  $\Delta\lambda^-$ . From equation (1.29) the phase inductances  $L^+$  and  $L^-$  given by  $i^+$  and  $i^-$  can be expressed as follows:

$$L^+ = \frac{\lambda_{phase} - \lambda_{PM}}{i^+} = \frac{\Delta\lambda^+}{i^+} \quad (1.33)$$

$$L^- = \frac{\lambda_{phase} - \lambda_{PM}}{i^-} = \frac{\Delta\lambda^-}{i^-} \quad (1.34)$$

From these equations results that  $L^+$  is smaller than  $L^-$  because  $\Delta\lambda^+$  is smaller than  $\Delta\lambda^-$ .

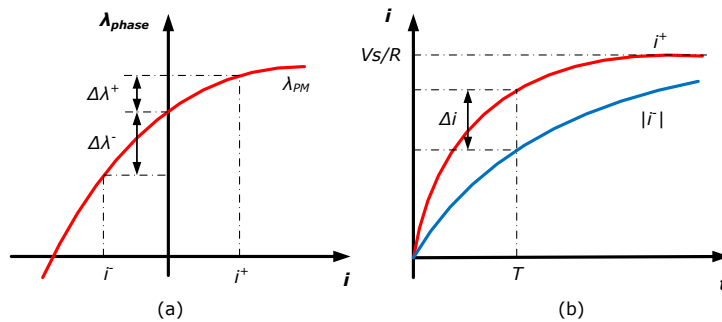


Fig. 1.50 Flux linkage and phase current change according to phase current direction

The phase current response to the phase inductance change can be extracted from the phase voltage expression:

$$v_s = R \cdot i + L \frac{di}{dt} + e \quad (1.35)$$

- with  $V_s$  denoting the phase voltage,  $R$  the phase resistance and  $e$  the back-EMF voltage. When the rotor is at stand still there is no back-EMF voltage therefore equation (1.32) will be:

$$i = \frac{v_s}{R} \left( 1 - e^{-\frac{R}{L}t} \right) \quad (1.36)$$

The phase currents show different reaction for different phase inductance values which is a function of rotor position. Fig. 1.51 presents the variation of the various components of the flux linkage over two cycles of a two pole PM machine [13]. The minimum value of the incremental inductance occurs at rotor positions of both  $0^\circ$  and  $180^\circ$  electrical. The magnet flux linkage is maximum positive at position  $0^\circ$  and

maximum negative at  $180^\circ$  electrical position. As it can be observed from this figure the incremental inductance has two periods during a complete electrical revolution, therefore creating an ambiguity in the initial position sensing (there are two rotor positions giving the same inductance). Despite these obvious difficulties, there have been several initial rotor position estimation methods proposed and successfully implemented, based on the incremental inductance variation.

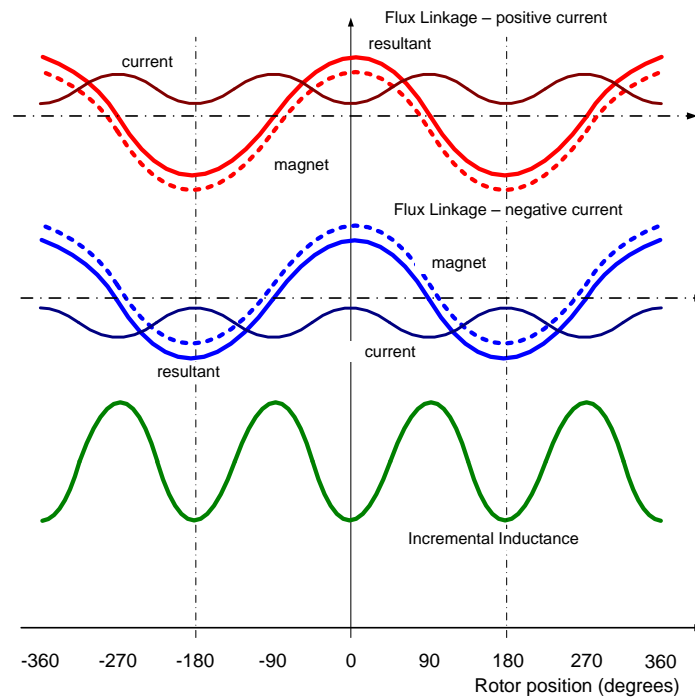


Fig. 1.51 Flux linkage and incremental inductance as function of rotor position in a BLDC motor with saliency

The next figure (Fig. 1.52) presents the pulse current amplitude according to rotor position, where it can be clearly seen that the phase current amplitude shows two complete periods over a complete electrical revolution. The two periods of the incremental inductance and pulse phase current are given by the rotor alignment first with north and second with south magnetic pole.

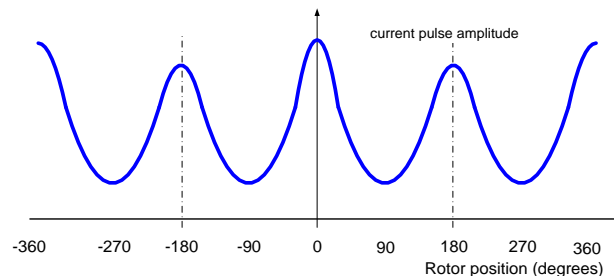


Fig. 1.52 Phase current pulse amplitude as function of rotor position

In case we further increase the phase pulse current it causes the magnetic saturation of the stator core which will affect the inductance value of the phase winding, resulting in different peak value of the pulse current, as presented in Fig. 1.53 [54].

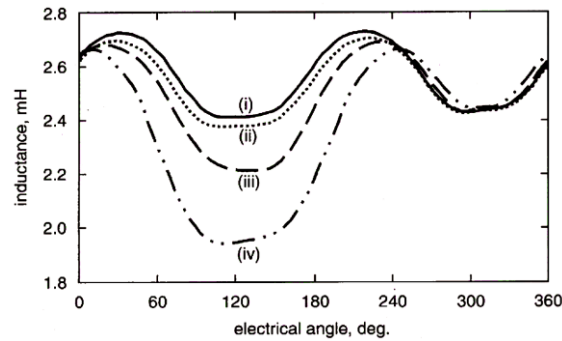


Fig. 1.53 Phase inductance change due to stator magnetic saturation (i) < (ii) < (iii) < (iv) [54]

G.H. Jang proposes an initial position detection method based on phenomena presented in Fig. 1.51 and Fig. 1.53.

At each of the motor phase's test pulses are applied with around  $20\mu\text{s}$  delay between them. Using equation (1.33) the phase current responses are calculated, results presented in Fig. 1.54. There are six test pulses applied in total (all possible phase combinations), the motor response to each of them is dependent on the initial rotor position.

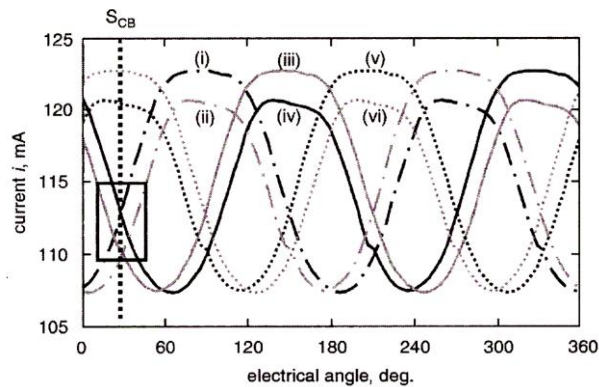


Fig. 1.54 Calculated phase currents (i) - U-V; (ii) - V-U; (iii) - W-U; (iv) - U-W; (v) - V-W; (vi) W-C [54]

Fig. 1.55 presents the first order phase current difference change  $\Delta i$  over the rotor position (complete electrical revolution of  $360^\circ$ ). The current differences are calculated according to equation (1.34). The  $\Delta i$  polarity contains rotor position information, in every  $60^\circ$  electrical angle interval the sign of one  $\Delta i$  changes its polarity.

It is very difficult to estimate the rotor position in points where one of the  $\Delta i$  value is zero (equilibrium points P1-P6 from Fig. 1.55), points in which the rotor tends to stop due to its saliency. For these cases the second order difference of the current responses are used  $\Delta\Delta i$ . Fig. 1.56 presents the change of  $\Delta\Delta i$  over a

complete electrical revolution. The polarity of  $\Delta\Delta i$  is changing every  $60^\circ$  electrical with a  $30^\circ$  electrical shift, compared to  $\Delta i$  polarity changing points, therefore offering rotor information in the rotor equilibrium points.

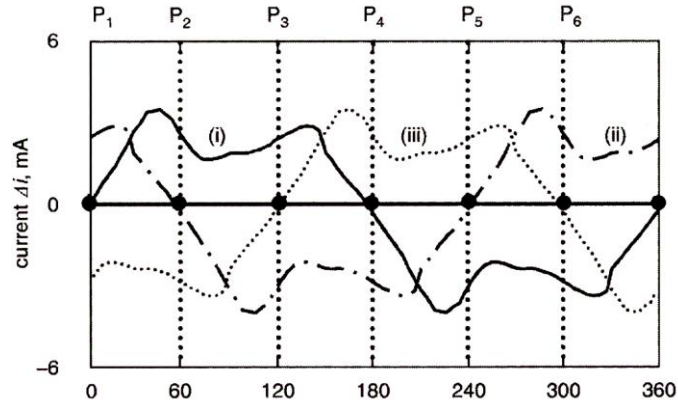


Fig. 1.55 First order current difference change over the rotor position  
(i) -  $\Delta i_1$ ; (ii) -  $\Delta i_2$ ; (iii) -  $\Delta i_3$  [54]

$$\begin{aligned} \Delta i_1 &= i_1^+ - i_1^- \\ \Delta i_2 &= i_2^+ - i_2^- \\ \Delta i_3 &= i_3^+ - i_3^- \end{aligned} \quad (1.37)$$

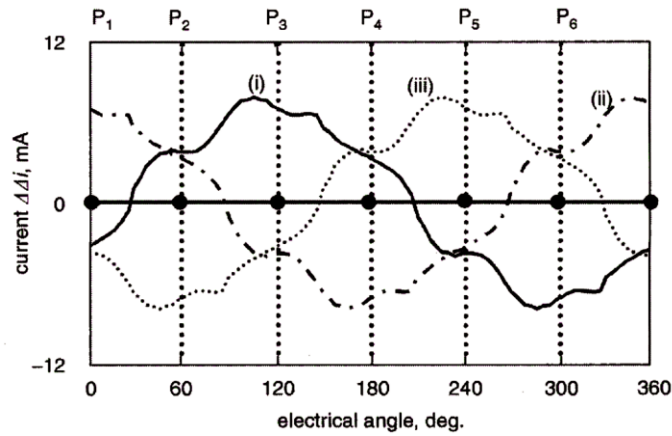


Fig. 1.56 Second order current difference change over the rotor position  
(i) -  $\Delta\Delta i_1$ ; (ii) -  $\Delta\Delta i_2$ ; (iii) -  $\Delta\Delta i_3$  [54]

$$\begin{aligned} \Delta\Delta i_1 &= \Delta i_1 - \Delta i_2 \\ \Delta\Delta i_2 &= \Delta i_2 - \Delta i_3 \\ \Delta\Delta i_3 &= \Delta i_3 - \Delta i_1 \end{aligned} \quad (1.38)$$



Table 1.3 summarizes the sign of the  $\Delta\Delta i$  signals over the rotor position.

Table 1.3 The sign of  $\Delta\Delta i$  over the rotor position

Electrical Rotor Position	$\Delta\Delta i_1$	$\Delta\Delta i_2$	$\Delta\Delta i_3$
30°-90°	+	+	-
90°-150°	+	-	-
150°-210°	+	-	+
210°-270°	-	-	+
270°-330°	-	+	+
330°-390°	-	+	-

In the original work [54] the author proposes also a closed loop startup method. Once the initial rotor position is known the corresponding voltage vector is applied, in order to produce the maximum possible torque. Consecutively the commutation positions must be detected at every 60° electrical rotation of the rotor. The above described algorithm used for the initial rotor position estimation cannot be used because there is not enough time to apply all six test pulses, in addition three out of the six voltage vectors would generate negative torque.

Fig. 1.57 presents the six voltage torque strength and sense over a complete 360° electrical revolution the rotor.

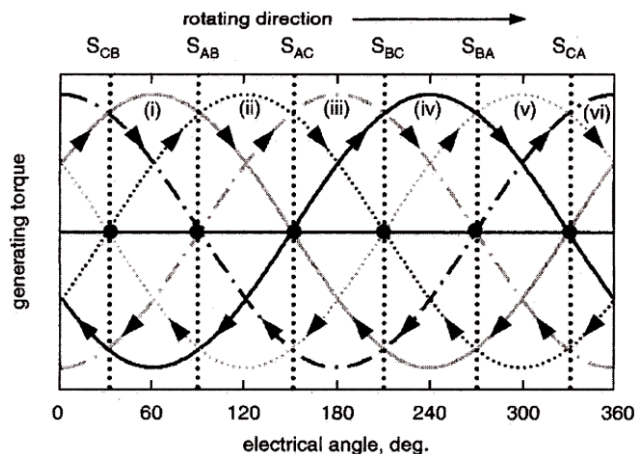


Fig. 1.57 Torque curves  
 (i) - U-W; (ii) - V-W; (iii) - V-U; (iv) - W-U; (v) - W-V; (vi) U-V [54]

Beside the current voltage vector there are two other voltage vectors which can create positive torque in each commutation phase, of course with smaller amplitude. The commutation point's detection can be derived from the amplitude of the voltage vector torques. This can be sensed by measuring the current generated by the voltage vectors which generates positive torque. As example in Fig. 1.57 the commutation from the current phases U-V to U-W ( $S_{CB}$  commutation point). Before the  $S_{CB}$  commutation point voltage vectors U-W and W-V can generate positive torque and commutation phase U-W is next. As it can be observed in the framed area of Fig. 1.54 there are four intersections of the response signals to the six voltage vectors in the neighbor of  $S_{CB}$ , one of them is the intersection between the

current voltage vector response  $U-V$  and the next voltage vector response  $U-W$ . Applying the two voltage vectors alternatively positive torque is generated and the commutation point will be the moment where the value of the two induced currents by voltage vectors  $U-V$  and  $U-W$  will be equal.

The pulse sequence used at the motor startup was composed as shown in Fig. 1.58. It is composed of short ( $P_{pulse}$ ) and long ( $P_{phase}$ ) pulses which energizes the motor phases in a way that it always generates positive torque (applying the current and the next commutation step), accelerating the motor and facilitate the commutation moment detection. The time period to which the  $P_{pulse}$  is applied is chosen as short as possible since this creates less torque, it is only needed to provide rotor position information by comparing it with  $P_{phase}$ . When the current amplitude induced by  $P_{pulse}$  is smaller than the current amplitude induced by  $P_{phase}$  for a period longer than the  $P_{pulse}$  the optimum phase commutation moment is reached.

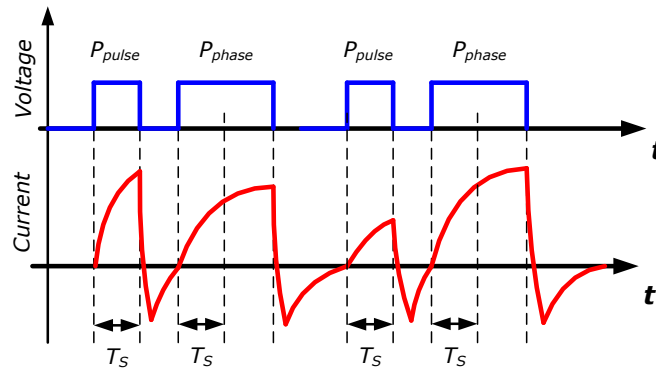


Fig. 1.58 Pulse sequence and current response

Using these pulses the rotor is accelerated in a closed loop to speeds at which the commutation points can be detected using the back-EMF voltage zero crossings evaluation. The following Table 1.4 presents, the pulse sequence composition as function of rotor position.

Table 1.4 Pulse sequence composition according to rotor position

Electrical position	$P_{phase}$	$P_{pulse}$
$30^\circ-90^\circ$	U-W	V-W
$90^\circ-150^\circ$	V-W	V-U
$150^\circ-210^\circ$	V-U	W-U
$210^\circ-270^\circ$	W-U	W-V
$270^\circ-330^\circ$	W-V	U-V
$330^\circ-390^\circ$	U-V	U-W

With the above described method the initial rotor position is estimated with  $60^\circ$  electrical resolution. The worst case startup torque given by this resolution is 87% from the maximum possible torque value [55]. In [56] the author proposes an improvement to this classic method, making possible the  $30^\circ$  electrical resolution initial rotor estimation. This way the maximum startup torque can be increased.

The initial rotor position estimation method proposed in [56] is based on two separate processes. The first is a gross estimation based on the above described method and second the fine estimation proposed by the author of that paper.

During the first gross estimation procedure, two voltage vectors are applied with opposite directions for a predefined time period. As example  $V_1$  and  $V_4$  may be applied consecutively. At the end of each voltage vector the peak value of the DC current is measured and stored as  $I_1$  and  $I_4$ . In case  $I_1$  is smaller than  $I_4$  we can conclude that a magnetic North pole is aligned closer to  $V_4$  than to  $V_1$  (Fig. 1.59 (a)). With this test the magnetic North position of the rotor is estimated with 180° electrical accuracy.

Next, two other voltage vectors are applied consecutively for a predefined and equal time period, voltage vectors in the half of the  $d$ - $q$  plane where the  $d$ -axis of the motor lies. The DC link current is sampled and stored at the end of the voltage pulse in each case. In case of Fig. 1.59 (a)  $V_2$  and  $V_6$  are applied and the current samples  $I_2$  and  $I_6$  are stored. The voltage vector at which the sampled peak current is the largest among all the stored values is the vector whose direction is closest to the  $d$ -axis of the motor. For example if  $I_1$  is the largest sampled current value results that the rotor  $d$ -axis lies in the region shown in Fig. 1.59 (b).

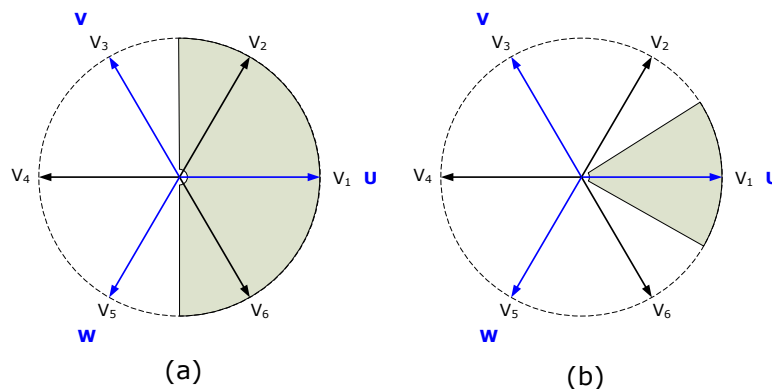


Fig. 1.59 Gross initial position estimation procedure

With this classic method the initial rotor position can be estimated with a 60° electrical resolution. If we take into consideration that the phase inductance is maximum at the rotor  $q$ -axis (Fig. 1.60 (b)), the resolution of the estimation can be further improved without any additional pulse application or complex mathematical calculations.

If  $I_2$  is bigger than  $I_6$  as in the above example, we can conclude that the  $d$ -axis of rotor is in the region highlighted in Fig. 1.61 (a), because  $V_6$  is closer to  $q$ -axis (or  $-q$ -axis) than  $V_2$ . On the other hand if  $I_2$  is smaller than  $I_6$  the rotor lays in positions highlighted in Fig. 1.61 (b).

If after the first measurement process,  $I_1$  is almost equal to  $I_4$ , the measurement result cannot be trusted, because the measurement noises may alter the decision result. Therefore in these cases the measurements has to be repeated with other sets of voltage vectors. As example instead of  $V_1$  and  $V_4$  also  $V_2$  and  $V_5$  can be used or  $V_3$  and  $V_6$ . Even with these considerations the maximum number of needed test pulses is five. Therefore the initial rotor position with 30° electrical resolution can be estimated in 5ms time considering 1ms pulse time.

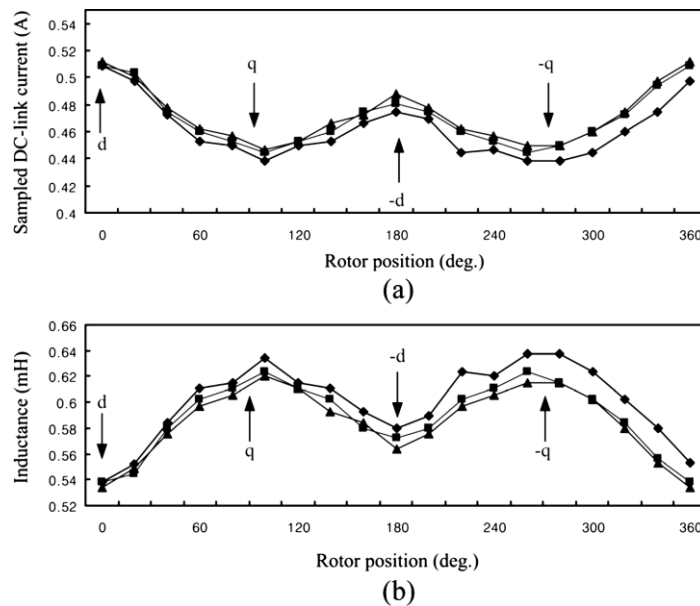


Fig. 1.60 Stator inductance as function of rotor position [56]  
 (a) Measured dc-link current samples. (b) Measured stator-winding inductance.

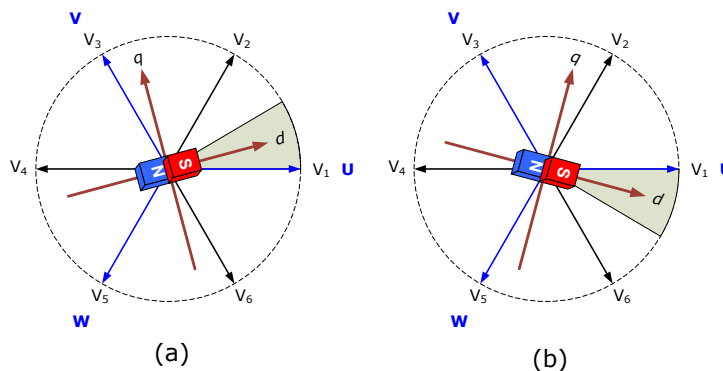


Fig. 1.61 Fine estimation procedure

The time interval to which the pulses (voltage vectors) are applied is essential for this method because it uses the current response of the motor windings. The current response of the winding is influenced by its time constant. This time constant is influenced by the rotor saliency, in case the rotor is designed without saliency, the phase winding time constant is almost equal for any rotor positions if the stator magnetic core is not saturated. Therefore the time interval in which the voltage vector pulses are applied should be defined in a way to create maximum difference between the current responses to the different voltage vectors. Of course this can cause also saturation of the stator windings magnetic core. With this measure the noise effect on the initial position estimation is also minimized.

Fig. 1.62 presents the current response for  $i_1$  and  $i_2$  resulted from application of voltage vectors  $V_1$  and  $V_2$  for a defined time period. The two currents  $i_1$  and  $i_2$  can be expressed as follows:

$$i_1(t) = \frac{V_{DC}}{R_{eq}} \left( 1 - e^{-\frac{t}{\tau_1}} \right) \quad (1.39)$$

$$i_2(t) = \frac{V_{DC}}{R_{eq}} \left( 1 - e^{-\frac{t}{\tau_2}} \right) \quad (1.40)$$

- Where with  $V_{DC}$  denoting the supply voltage,  $R_{eq}$  the equivalent resistance between two phase terminals of the motor,  $\tau_1$  and  $\tau_2$  are the time constants of the equivalent R-L circuit of the phase windings to which the voltage vectors  $V_1$  and  $V_2$  are applied.

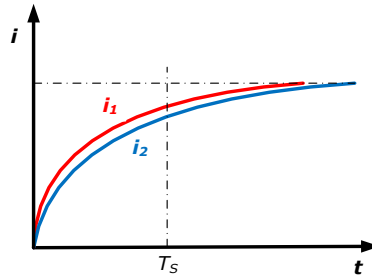


Fig. 1.62 Current rise time for two different time constants

The difference between the current responses  $\Delta i$  can be expressed based on the above equations (1.36),(1.37) as follows:

$$\Delta i = i_2(t) - i_1(t) = \frac{V_{DC}}{R_{eq}} \left( e^{-\frac{t}{\tau_1}} - e^{-\frac{t}{\tau_2}} \right) \quad (1.41)$$

Because of the small difference between the two time constants ( $\tau_1$  and  $\tau_2$ ),

$$\tau_2 = \tau_1 + \Delta \text{ and } \Delta \approx 0.$$

By time derivation of the (1.38) equation we can find the point where the current difference is maximum. Therefore the time to which each voltage vector should be applied can be calculated using the following equation:

$$T_s = \lim_{\Delta \rightarrow 0} \frac{\ln \frac{\tau_1}{\tau_1 + \Delta}}{\frac{\tau_1}{\tau_1 + \Delta} - \frac{1}{\tau_1}} = \tau_1 \quad (1.42)$$

From this equation we can conclude that the time interval to which these voltage vector pulses should be applied is equal to the phase windings time constant. If the pulse time is longer than the winding time constant, the rotor will start to rotate and change its initial position. As result if during the voltage vector application process,

movement of the rotor is noticed, the time to which each individual voltage vector is applied has to be decreased, even below the motor winding time constant.

The startup method suggested for this initial position estimation method [56] is based on closed loop acceleration until the back-EMF signal is strong enough to be easily detected. Next Fig. 1.63 presents the rotor acceleration process.

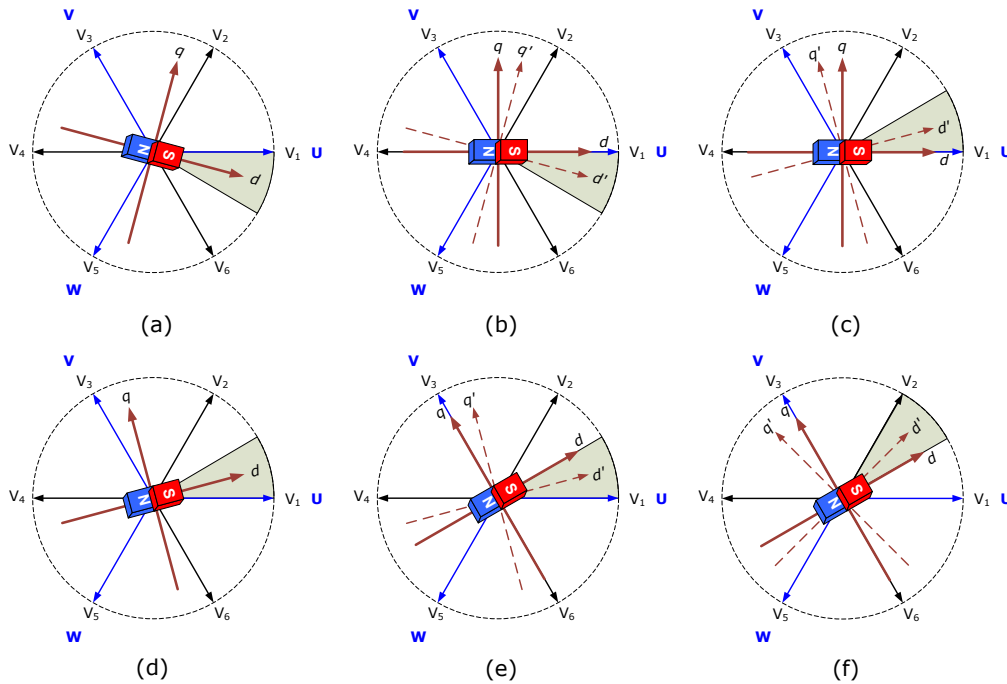


Fig. 1.63. Real and estimated (dotted vector) rotor position

Considering that the initial position estimation procedure concluded that the initial rotor position corresponds with the grey region of Fig. 1.63 (a). Then a voltage vector which creates the maximum possible torque is applied which moves the rotor in the desired direction. The applied voltage vector direction coincides with the average direction in time of the  $q$ -axis. For this given case, the voltage vector applied is at  $75^\circ$  electrical in advance to the rotor  $q$ -axis. The rotor will turn and at the point when it intersects the voltage vector " $V_1$ " direction, Fig. 1.63 (b), the inductances of the motor given for voltage vectors direction  $V_2$  and  $V_3$  are almost equal, given by the fact that the  $q$ -axis of the rotor lies exactly between these two voltage vectors. In this moment the estimated rotor position has to be advanced with  $30^\circ$  electrical to the next sector as shown in Fig. 1.63 (c). Therefore the rotor will continue to rotate as shown in Fig. 1.63 (d). When the real  $q$ -axis of the rotor intersects the direction of voltage vector  $V_3$  (Fig. 1.63 (e)) the inductance measurement given by  $V_3$  voltage vector direction is at its minimum value, the estimated rotor position is again advanced with  $30^\circ$  electrical (Fig. 1.63 (f)). With this procedure the rotor position is continuously followed with  $30^\circ$  electrical resolution, which facilitates the acceleration of the rotor with a maximum possible torque. The next diagram presents the estimation process (Fig. 1.65).

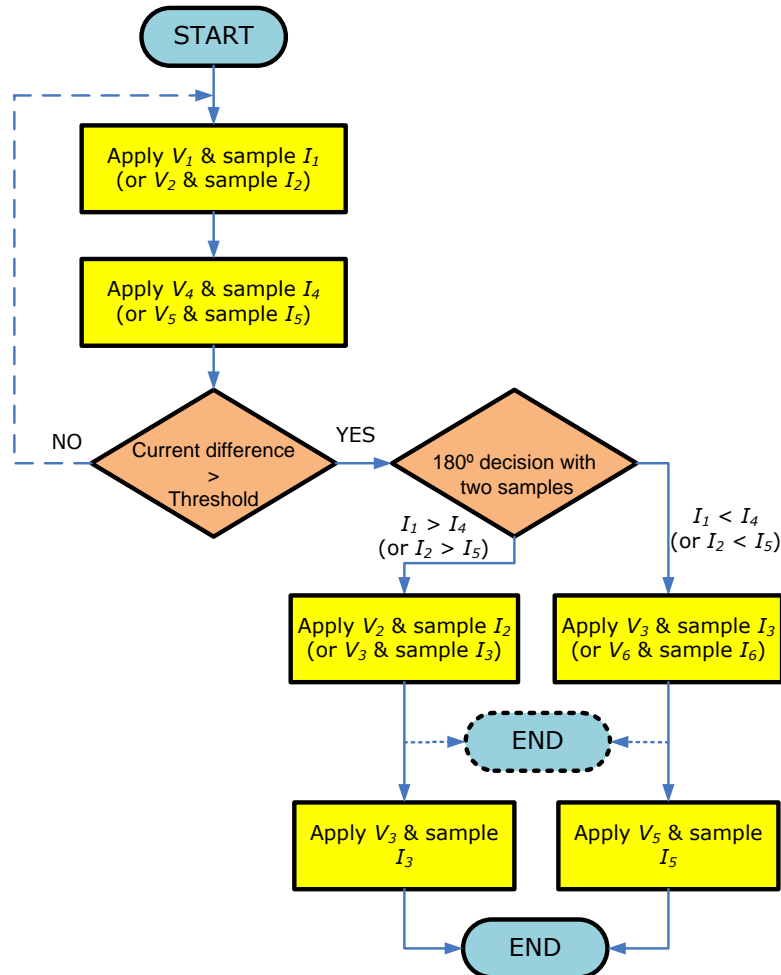


Fig. 1.64. Flowchart of the initial position estimation method proposed in [56]

The startup procedure consists in application of three voltage vectors (including one zero voltage vector and two non-zero voltage vectors) during a complete switching cycle as presented in Fig. 1.65. According to the position of the rotor, the phase's inductance is measured once or twice according to above description. In case of Fig. 1.63 (b) the shape of the voltage vectors and phase currents are presented in Fig. 1.65. The angle to which the applied vector is advanced is  $75^\circ$  electrical compared to the  $q$ -axis of the rotor.

In order to improve the noise immunity of the described method, the algorithm decides to advance the estimated rotor position only after ten consecutive coinciding results. With this measure the vulnerability of the method to noises and current measurement errors is minimized. The delay caused by the ten successive measurements is not influencing the rotor startup performance, being very short compared to the rotation speed of the rotor.

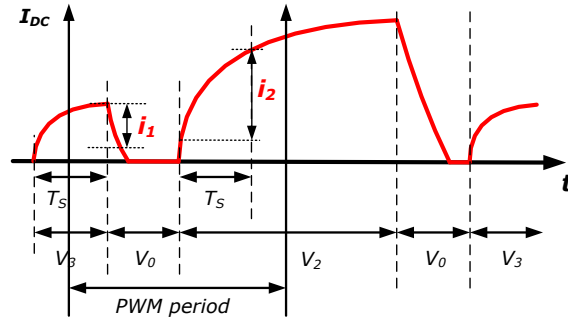


Fig. 1.65 Startup voltage vector sequence and induces phase current

Another initial position estimation method using the phase inductance variation proposed by Yen-Chuan Chang in [57][57] is based on application of twelve test pulses (Fig. 1.66) and evaluation of the current responses to these pulses.

The initial rotor position can be estimated comparing the peak current amplitudes induced by the twelve excitation pulses. The next Fig. 1.67 presents the twelve voltage vectors direction and the initial position evaluation process. The voltage vector for which the measured peak current response (in the DC line) is the biggest corresponds to the voltage vector to which the rotor is aligned. Fig. 1.68 presents an example of the DC-link current response for the twelve voltage vectors. As it can be observed the peak current measured for the second voltage vector is the biggest, therefore we can conclude that the rotor is aligned with this vector direction.

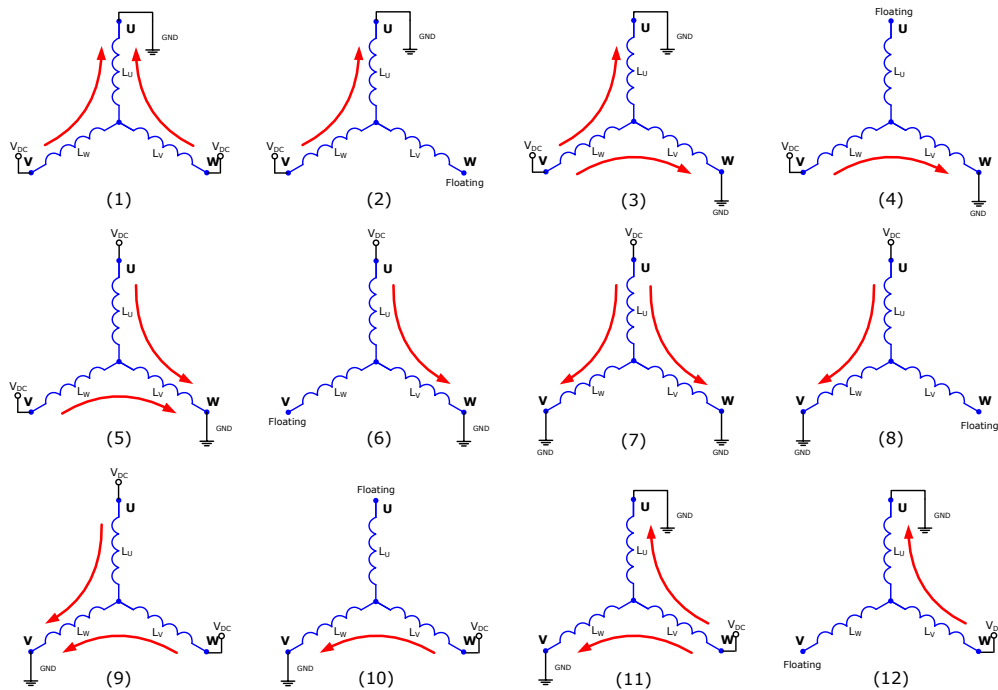


Fig. 1.66 Twelve voltage vectors



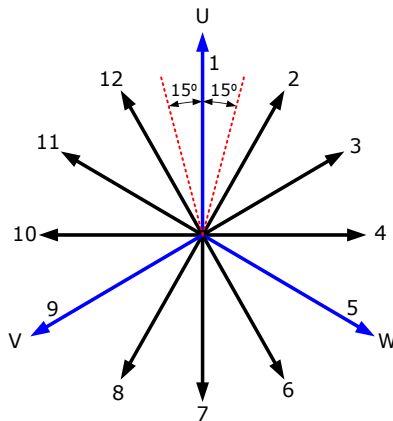


Fig. 1.67 Voltage vectors and the estimation process

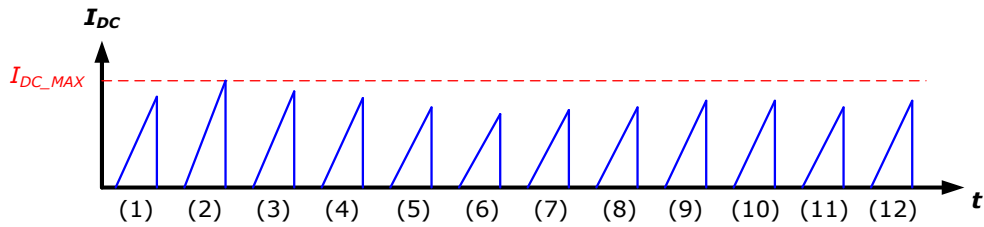


Fig. 1.68 DC link current response for the twelve voltage vectors

For this method the time to which the voltage vectors are applied is essential. The voltage vector configurations can be divided into two classes. The first class contains voltage vectors (from Fig. 1.66) (1), (3), (5), (7), (9) and (11). The second class contains voltage vectors (2), (4), (6), (8), (10) and (12). The major difference between the two classes is the equivalent resistance and inductance to which the voltage vectors are applied. According to Fig. 1.69 the first category of voltage vectors (Fig. 1.69 (a)) equivalent inductance is  $1,5 \cdot L$  and resistance of  $1,5 \cdot R$ . The second category of voltage vectors (Fig. 1.69 (b)) equivalent inductance will then be  $2 \cdot L$  and resistance  $2 \cdot R$ .

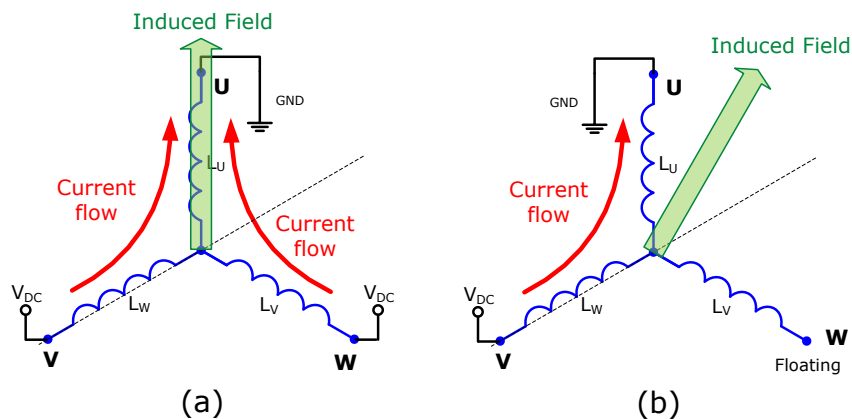


Fig. 1.69 Current paths for the two voltage vectors category

In order that each voltage vector can induce the same peak currents, the time to which the voltage vectors are applied has to be different for the two categories of the voltage vectors. The current responses  $i_1(t)$  and  $i_2(t)$  for the voltage vectors presented in (Fig. 1.69) can be expressed as follows:

- for the voltage vector categories from case (a):

$$i_1(t) = \frac{V_{DC}}{1.5R} \left( 1 - e^{-\frac{R}{L}t_1} \right) \quad (1.43)$$

- for the voltage vector categories from case (b):

$$i_2(t) = \frac{V_{DC}}{2R} \left( 1 - e^{-\frac{R}{L}t_2} \right) \quad (1.44)$$

- where  $t_1$  and  $t_2$  represents the time to which the voltage vectors are applied. To equalize the responses is necessary that:

$$i_1(t) = i_2(t) \quad (1.45)$$

- therefore:

$$t_2 = -\frac{L}{R} \ln \left( \frac{4e^{-\frac{R}{L}t_1} - 1}{3} \right) \quad (1.46)$$

With this above equation (1.43) the relation between the two voltage pulses is presented, using this formula the timings of the vectors can easily be calculated.

The overall initial rotor position estimation resolution of the above described method is  $30^\circ$  electrical. The time needed for the estimation procedure is quite long compared to other methods, mainly because of the needed twelve voltage pulses to be applied for long enough time periods to saturate the phase windings magnetic core.

In the original work a closed loop startup procedure is also proposed. Using the already known initial position, a voltage vector with an advance of  $90^\circ$  electrical is applied to the motor to produce a maximum startup torque. The voltage vector must be advanced with the rotor rotation in order to maintain the high startup torque. The above estimation method cannot be applied anymore because there are voltage vectors which produce negative torque regarding the desired startup rotation direction, therefore a special startup procedure is applied.

The startup algorithm is based on the application of two voltage vectors consecutively. As example in case the initial rotor position is  $90^\circ$  electrical, two voltage vectors are applied to the motor, first at  $180^\circ$  electrical, second at  $210^\circ$  electrical. In this moment the relation of the peak currents values induced by the two voltage vectors in the DC-link is:  $I_{DC}(180^\circ) < I_{DC}(210^\circ)$ , Fig. 1.71 (a).

When the rotor reaches the  $120^\circ$  electrical position the relation between the two induced currents changes and results:  $I_{DC}(180^\circ) > I_{DC}(210^\circ)$ , Fig. 1.71 (b).

This is the moment when the voltage vector sequence is advanced, and the next two voltage vectors combinations at 210° and 240° electrical are applied. The procedure is repeated until the speed of the rotor is high enough to generate detectable back-EMF signal.

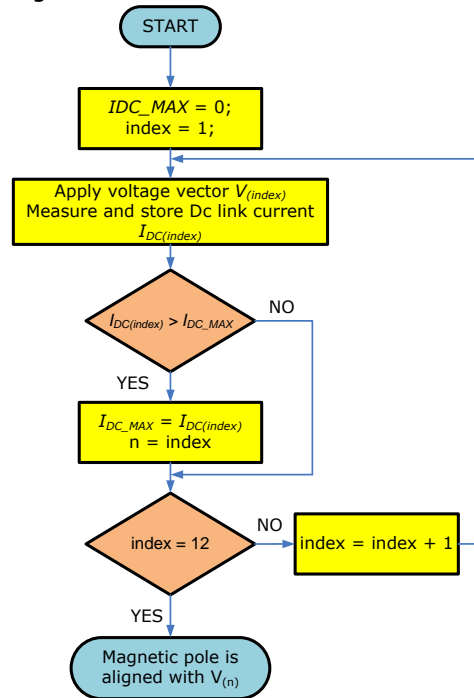


Fig. 1.70 Flowchart of the proposed initial position detection method [57]

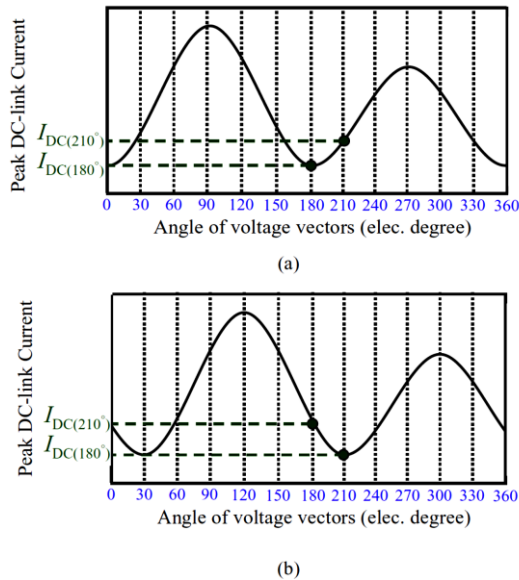


Fig. 1.71 DC-link current for the voltage vectors at different rotor positions (a) 90° electrical; (b) 120° electrical;

Another method for initial position estimation is introduced in [82], using the phase voltages and DC link current for the estimation. The basic idea behind the method is still the measuring and comparison of the stator phase winding inductances. The comparing of the inductances is done using the voltage measured at the third terminal.

The proposed process [82] starts with the application of two voltage vectors for a pre-defined time period. The first voltage pulse is injected between phase  $U$  and  $V$  as shown in Fig. 1.72 (a) ( $U$  terminal connected to  $V_{DC}$ ,  $V$  terminal connected to GND and  $W$  terminal left floating without any current flow).

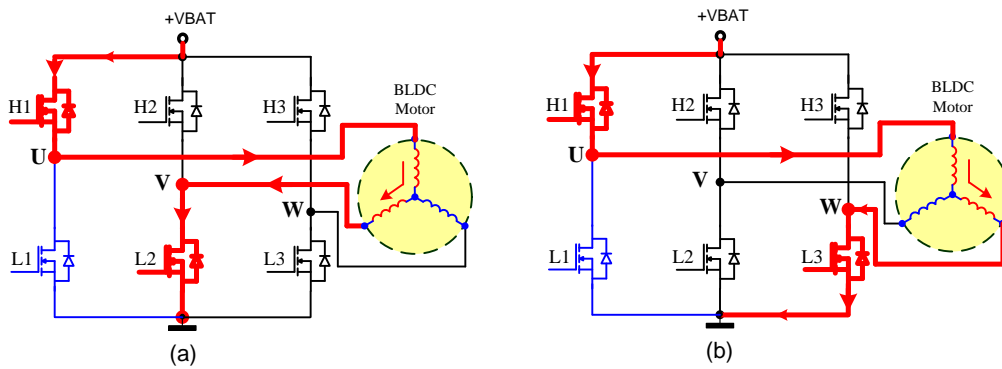


Fig. 1.72 Voltage pulses of method proposed in [82]

The voltage across the  $V$  winding can be measured at the floating terminal  $W$ . Since the winding resistance and the current sensing resistor are very small, the DC bus voltage  $V_{DC}$  during the pulse injecting interval can be expressed as follows:

$$V_{DC} \approx [L_U(\theta_0) + L_V(\theta_0)] \frac{di_1(on)}{dt} \approx V_{UN1(on)} + V_{NV1(on)} \quad (1.47)$$

From this equation we can conclude that the winding voltage regarded to ground of  $V$  phase terminal (for Fig. 1.72 (a)) will be:

$$\left. \begin{aligned} V_{UN1(on)} &= \frac{L_U}{L_U + L_V} \cdot V_{DC} \\ V_{NV1(on)} &= \frac{L_V}{L_U + L_V} \cdot V_{DC} \end{aligned} \right\} \quad (1.48)$$

After this first pulse the corresponding freewheeling interval follows. The freewheeling current is forced to flow via  $L1$  and  $L2$  MOSFET's (by turning the MOSFET's ON).

With the same principle the second voltage pulse is applied between  $U$  and  $W$  phases as shown in Fig. 1.72 (b), with phase  $U$  terminal connected to  $V_{DC}$ , phase  $V$  terminal left floating and phase  $W$  terminal connected to GND.

During the first two test pulses the voltage at the floating terminal and the peak DC link current is measured and stored. The inductance comparison is done comparing the measured voltages during these first two pulses. However this single inductance comparison can map into two opposite rotor position sectors as

presented in Fig. 1.73. For example in the condition  $L_V > L_W > L_U$  the possible initial positions are  $0^\circ \div 30^\circ$  or  $180^\circ \div 210^\circ$ . In one of the position intervals the rotor is aligned with North magnetic pole in the other with South magnetic pole. To distinguish between these two positions intervals an additional estimation process is required which consist of a third voltage pulse.

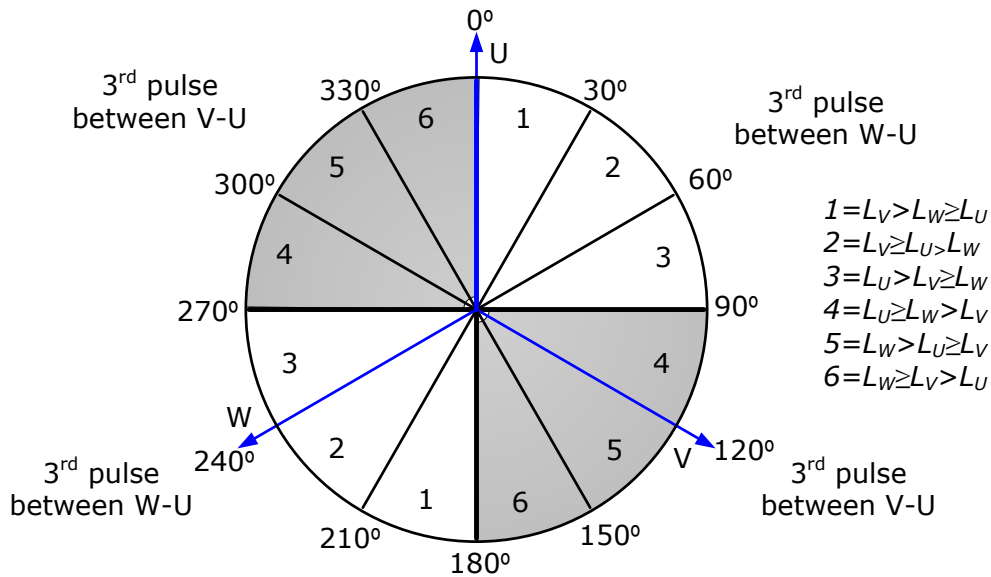


Fig. 1.73 Determination of initial position based on [82]

The peak current of all three voltage pulses are recorded, comparing them we can discriminate between the two rotor magnet polarity alignments which can be determined based on the magnetic saturation of the stator core. This cause the winding currents given by the voltage pulse to further increase or decrease the stator saturation and slightly change the winding inductance, depending on the rotor magnet pole polarity as stated in [83], [84].

The third pulse has to be chosen according to the two previous voltage pulses results as follows:

- If  $0^\circ < \theta_0 \leq 90^\circ$  or  $180^\circ < \theta_0 \leq 270^\circ$ , then the voltage pulse should be applied between  $W-U$  with phase  $W$  connected to  $V_{DC}$  and phase  $U$  connected to GND and compare  $I_2$  with  $I_3$ .
- If  $90^\circ < \theta_0 \leq 180^\circ$  or  $270^\circ < \theta_0 \leq 360^\circ$ , then the voltage pulse should be applied between  $V-U$  with phase  $V$  connected to  $V_{DC}$  and  $U$  phase to GND, and compare  $I_1$  with  $I_3$ .

According to the measured voltages and peak currents, Table 1.5 summarizes the possible relationships and the resulting initial position. Fig. 1.74 presents an example of the voltage pulses and the corresponding dc-link current sequence of the method proposed in [82], for an initial rotor position of  $43^\circ$  electrical.

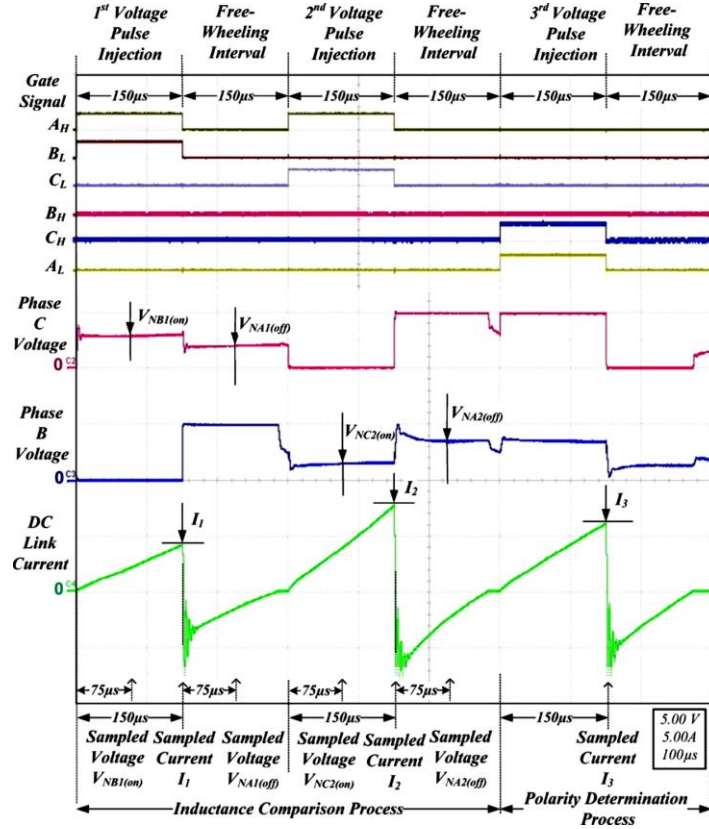


Fig. 1.74 Actual phase voltages and dc-link current of the method proposed in [82]

Table 1.5 Determination of the initial rotor position proposed in [82]

Phase Voltage Comparison	Inductance Comparison	Possible Initial position	3 <sup>rd</sup> Injec tion	Peak Current	Initial Rotor Position
$V_{NV1} > V_{NU1}$ $V_{NW2} \geq V_{NU2}$ $V_{NV1} > V_{NW2}$	$L_V > L_W \geq L_U$	$0^\circ < \theta_r \leq 30^\circ$ $180^\circ < \theta_r \leq 210^\circ$	W-U	$I_2 > I_3$	$0^\circ < \theta_r \leq 30^\circ$
$V_{NV1} \geq V_{NU1}$ $V_{NW2} < V_{NU2}$ $V_{NV1} > V_{NW2}$	$L_V \geq L_U > L_W$	$30^\circ < \theta_r \leq 60^\circ$ $210^\circ < \theta_r \leq 240^\circ$		$I_2 < I_3$	$180^\circ < \theta_r \leq 210^\circ$
$V_{NV1} < V_{NU1}$ $V_{NW2} < V_{NU2}$ $V_{NV1} \geq V_{NW2}$	$L_U > L_V \geq L_W$	$60^\circ < \theta_r \leq 90^\circ$ $240^\circ < \theta_r \leq 270^\circ$		$I_2 > I_3$	$30^\circ < \theta_r \leq 60^\circ$
$V_{NV1} < V_{NU1}$ $V_{NW2} \leq V_{NU2}$ $V_{NV1} < V_{NW2}$	$L_U \geq L_V > L_W$	$90^\circ < \theta_r \leq 120^\circ$ $270^\circ < \theta_r \leq 300^\circ$		$I_2 < I_3$	$210^\circ < \theta_r \leq 240^\circ$
$V_{NV1} \leq V_{NU1}$ $V_{NW2} > V_{NU2}$ $V_{NV1} < V_{NW2}$	$L_W > L_U \geq L_V$	$120^\circ < \theta_r \leq 150^\circ$ $300^\circ < \theta_r \leq 330^\circ$	V-U	$I_3 > I_1$	$60^\circ < \theta_r \leq 90^\circ$
$V_{NV1} > V_{NU1}$ $V_{NW2} > V_{NU2}$ $V_{NV1} \leq V_{NW2}$	$L_W \geq L_V > L_U$	$150^\circ < \theta_r \leq 180^\circ$ $330^\circ < \theta_r \leq 360^\circ$		$I_3 < I_1$	$90^\circ < \theta_r \leq 120^\circ$
				$I_3 > I_1$	$270^\circ < \theta_r \leq 300^\circ$
				$I_3 < I_1$	$120^\circ < \theta_r \leq 150^\circ$

The above presented initial position detection methods based on phase current or DC-link current measurements all need the current measurement path. Which in some applications is not implemented and therefore different initial position estimation method must be used. The next section describes such methods based only on phase voltage or/and time measurement.

### 1.5.3 Initial position detection without current sensing

The initial position evaluation method described in this sub-chapter does not require any current measurement, therefore reducing the price of the BLDC motor control unit. The basic principle of the method is the measuring of the time taken to discharge the energy from the pre-energized phase windings of the motor [58]. The method is based on the phase winding inductance change over the rotor position. Charging the phase winding with energy from a voltage vector applied for a predefined time period, the overall energy stored in the winding is dependent on the peak current and the phase inductance. On the other hand a saturated core stores less energy than an unsaturated magnetic core, for the same inductance and peak current due to the magnetic pre-saturation caused by the rotor permanent magnets. The associated phase inductance of a stator winding (Fig. 1.76) for the linear (non-saturated) case, shown in Fig. 1.75 (a) is greater than that for the saturated case shown in Fig. 1.75 (b).

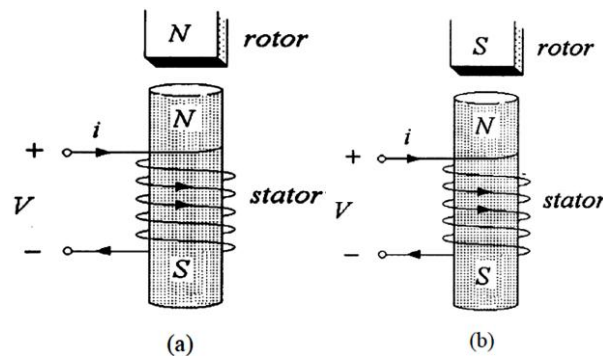


Fig. 1.75 Saturated versus unsaturated magnetic fields [58]  
(a) Linear (unsaturated) magnetic field; (b) Saturated magnetic field

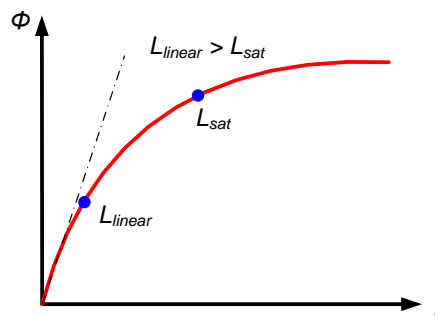


Fig. 1.76 Inductance of stator windings dependent on the magnetic saturation

Once the phase current stabilizes during the excitation pulse, the energy stored in the winding is bigger in the winding with higher inductance, therefore the time needed to discharge the stored energy in the coils increases with the winding inductance value. The saturation current is only dependent on the wiring DC resistance, is not influenced by the windings inductance, therefore the time taken to discharge the energy from the windings will be different according to rotor position. The energy stored into a winding inductance can be expressed as follows:

$$E_L = \frac{L \cdot i_p^2}{2} \quad (1.49)$$

- where with  $E_L$  denoting the stored energy in the windings;  $L$  – the windings inductance;  $i_p$  the peak winding current.

The next figure shows the discharging behavior of an excited coil according to its magnetic saturation state. As it can be observed the discharge time in case of a saturated core winding is shorter than the discharge time for the unsaturated core winding  $T_{sat} < T_{linear}$ .

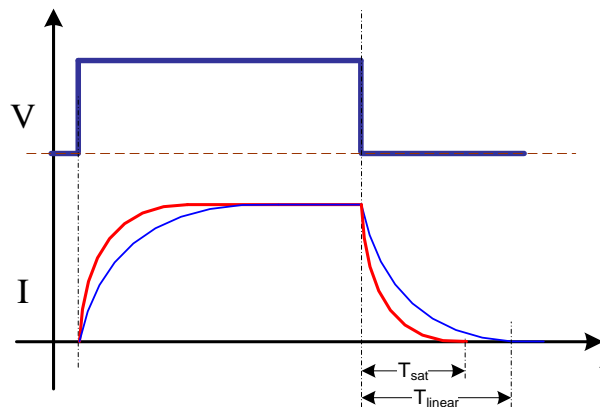


Fig. 1.77 Discharging time of the stator inductance

For the proposed method in [58] there are three combinations of pulses which are applied. One of them is shown in Fig. 1.78 (a). The second part of Fig. 1.78 (b) presents the excitation voltage vector current path, this is applied during  $T_1$  time period. The current goes into phase U, then to the neutral point of the motor and goes to GND via the other two phase windings (V and W) which are connected in parallel for this configuration.

For the second part of the excitation pulse  $T_2$  the power transistors are switched OFF. The freewheeling current flows via the reverse body diodes of the inverter power MOSFET's as shown in Fig. 1.78 (c). The voltage at the high level output is equal with  $V_{DC} + V_d$  (at the corresponding HS MOSFET) and is  $-V_d$  at the low level output terminal. After this  $T_2$  period no current flows through the windings and the voltage levels at the motor terminals are equal to zero.

The freewheeling period is equal to the time to which the voltage at the motor terminals is higher than the battery voltage or lower than zero volt. As remark, this voltage difference is much easier to sense than differences between the phase currents.



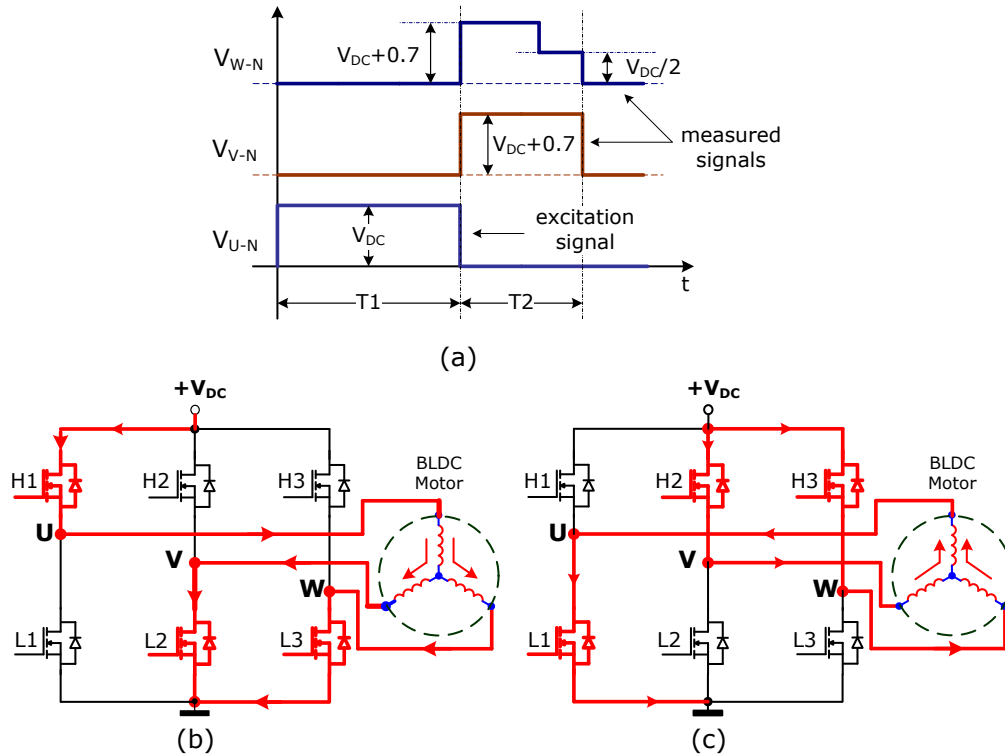


Fig. 1.78 Excitation configuration and the corresponding current paths  
 (a) Excitation configuration; (b) Current path for "T1" period;  
 (c) Associated freewheeling period "T2" current path;

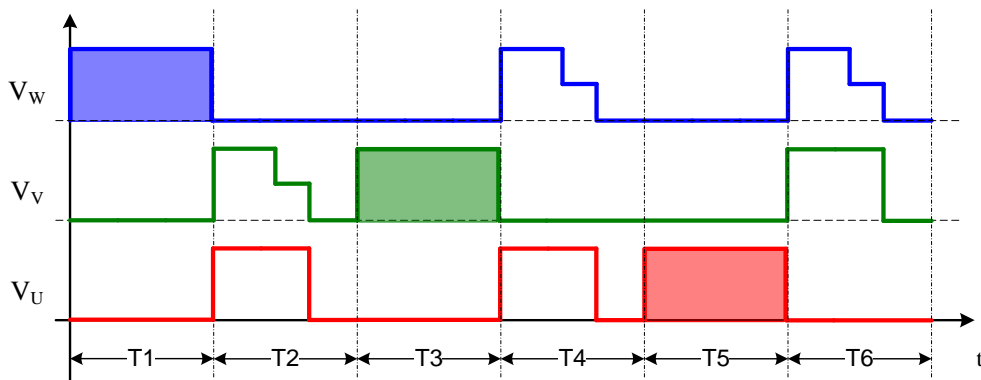


Fig. 1.79 Initial rotor position evaluation sequence of [58]

Fig. 1.79 presents the voltage vectors sequence, for the proposed initial position estimation method. Fig. 1.80 presents the voltage vector configurations for the time intervals  $T_1$ ,  $T_3$ , and  $T_5$ . The phase in which the stored energy is highest, results from the longest measured freewheeling period and this is the phase to which the rotor is aligned to. Because two phases are energized in the same time, only three

test pulses are necessary to estimate the initial rotor position, thus considerably reducing the estimation time and complexity.

Next Fig. 1.81 presents the implementation diagram of the proposed method in the original paper [58]. The initial estimation method was implemented using an FPGA (Field Programmable Gate Array) circuit, which proves the method implementation possibility in a specialized ASIC. The overall resolution of the estimation process is  $60^\circ$  electrical.

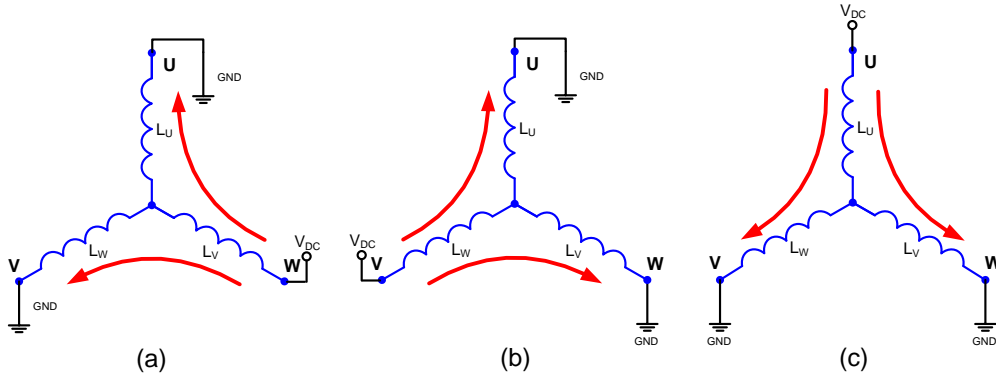


Fig. 1.80 Voltage vectors configuration for method in [58]

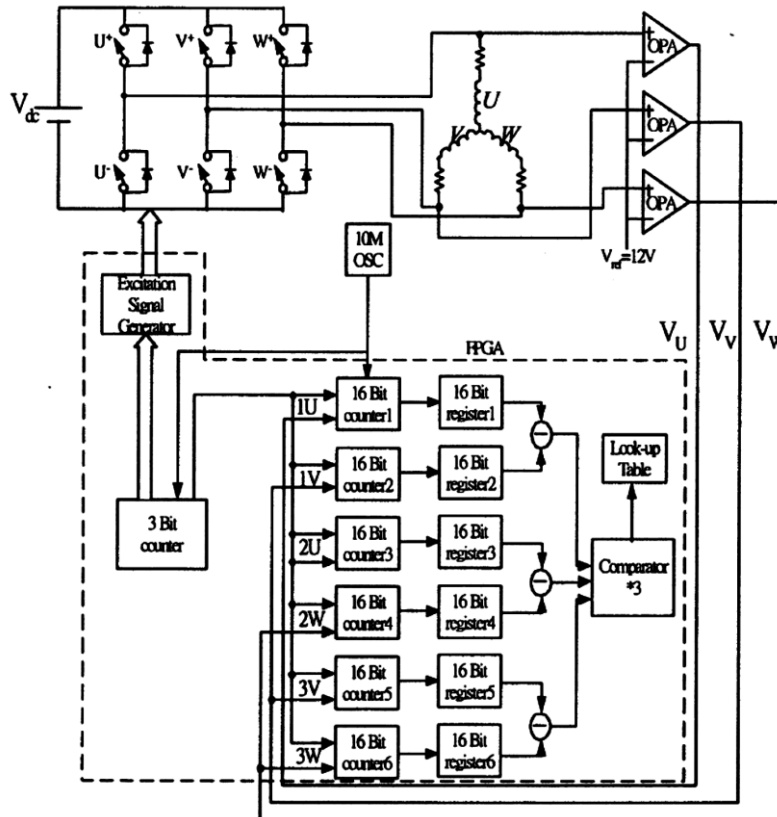


Fig. 1.81 Block diagram of the experimental system [58]

## Summary

The first part of this chapter presents the brushless motor operation principles and basic driving methods, strategies with a special focus on permanent magnet three phased Brushless DC motor drives. The overview of the brushless motor rotors presents the most employed rotor construction types, highlighting their advantages and disadvantages for various brushless motor applications and drive methods.

The next part of this chapter presents a comprehensive overview of the state of the art in BLDC motor driving methods including sensed and sensorless drive methods.

The presented sensorless drive methods include:

- Initial rotor position pre-alignment processes
- Initial rotor position estimation methods based on the phases inductance change over the rotor position and the magnetic saturation effect of the stator core;
- Open and closed loop acceleration methods, from stand still to speed where the back-EMF is high enough to be evaluated;
- Closed loop control methods based on various Back-EMF evaluation methods and strategies;



## 2 Novel initial rotor position estimation method

This chapter presents an original contribution to initial rotor position estimation methods of BLDC motors. The validity of the idea is demonstrated by theoretical demonstrations and laboratory experiments. The first concept of the idea was presented at the international conference "Dr.-ETC" of university of "Politehnica" Timisoara in 2009 [1], in the paper named "A Novel Initial Rotor-Position Estimation Method for BLDC Motors Utilizing the Neutral Terminal Voltage". The more improved and optimized version of the idea was presented and published at the international conference "OPTIM 2010" co-sponsored by IEEE Industry Applications Society, IEEE Power Electronics Society and IEEE Industrial Electronics Society, held in Moieciu, Braşov county, with the paper named "A Novel Initial Rotor-Position Estimation Method for BLDC Motors Based on Four Voltage Pulses" [2].

### 2.1 The initial rotor position estimation principle

The estimation of the rotor position is based on two properties of a BLDC motor which presents salience. The first is the stator windings inductance dependency on the rotor position and second the nonlinear magnetization characteristics of the stator core [56]. Fig. 2.1 presents the stator winding inductance in function of rotor position for two injected current values (for the actual machine used in the experiments). In case of low test currents the inductance of the stator winding is mainly influenced by the salience effect of the rotor. The difference between North and South magnetic pole alignment cannot be detected with small test currents. The parameters of the machine used for the test are listed in the next Table 2.1.

Table 2.1 Parameters of the employed BLDC motor for initial position method evaluation

Number of stator poles	12
Number of rotor poles	8
Rated DC voltage	12V
Max phase current	50A
Back-EMF	$k_E=3,7V/krpm$ ( $E_{lpk}/krpm$ )

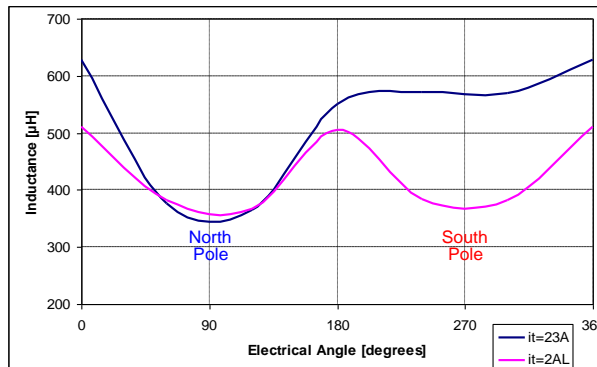


Fig. 2.1 Stator inductance as function of rotor position

Discrimination between South and North magnetic pole can be done using the magnetic saturation effect of the stator core. The stator core close to a magnetic pole is strongly magnetized. The rate of change of the current in the winding flowing in the magnetizing direction is large compared with that in the opposite direction because of magnetic saturation [54]. Therefore the peak value of the current measured at the end of a pre-defined voltage vector will be different in case of North or South magnetic pole alignment. The test current amplitude is defined by the time period to which the voltage vector is applied to the stator winding. To reach the magnetic core saturation voltage vector must be applied for a long time period (depending on the motor time constant).

At standstill, with two phases energized (and neglecting the mutual inductances  $L_{UV}(\theta_r) = L_{VU}(\theta_r)$ ), the brushless dc motor mathematical model is:

$$V_{DC} = 2R_S I_S + \frac{di_S}{dt} \cdot (L_U - L_V) \quad (2.1)$$

- where with  $R_S$  denoting the phase resistance;  $I_S$  the phase current;  $L_U, L_V$  – the  $U$  and  $V$  phase self-inductances;  $V_{DC}$  – Supply voltage;

According to equation (2.1) the voltage deviation in respect to  $V_{DC}/2$  is proportional to the inductance difference.

$$V_{DC} \cong \frac{di_S}{dt} \cdot (L_U - L_V) \quad (2.2)$$

## 2.2 Proposed method principle

The presented method doesn't need any current measurement, it relies only on the measurement and evaluation of phase and battery voltages.

Considering a BLDC motor in a star configuration, applying a voltage vector between two of the motor phases (e.g.  $U$ - $V$ ), the voltage at the neutral point of the motor is defined by the relationship between the two phases inductance (see Fig. 2.3 (a)). The two phase inductances form a voltage divider. The winding resistance compared with the inductance of the phases is insignificant so it can be neglected. The rotor being at stand still and no current flowing into the third terminal (this case  $W$ ) the divided voltage can be measured at this third, floating terminal.

The phase-to-ground voltage at the floating terminal can be described as follows:

$$V_{WN} = \frac{L_V}{L_V + L_U} \cdot V_{DC} \quad (2.3)$$

- where with  $V_{WN}$  denoting  $W$  phase-to-ground voltage;  $L_U, L_V$  – the  $U$  and  $V$  phase self-inductances;  $V_{DC}$  – Supply voltage;

Fig. 2.2 shows an example of voltage at the motor floating terminal according to rotor position assuming 12V  $V_{DC}$  supply voltage and no core saturation. Considering that the phase inductances have a sinusoidal change according to rotor position and  $0^\circ$  electrical ( $d$ -axis) is represents North Pole aligned to phase  $U$ , the inductances variation can be described as follows:

$$\begin{aligned}
L_U &= \frac{L_d + L_q}{2} + \left[ \left( \frac{L_q - L_d}{2} \right) \cdot \sin \left( 2 \cdot \theta_r + \frac{\pi}{2} \right) \right] \\
L_V &= \frac{L_d + L_q}{2} + \left[ \left( \frac{L_q - L_d}{2} \right) \cdot \sin \left( 2 \cdot \theta_r - \frac{\pi}{6} \right) \right] \\
L_W &= \frac{L_d + L_q}{2} + \left[ \left( \frac{L_q - L_d}{2} \right) \cdot \sin \left( 2 \cdot \theta_r - \frac{5 \cdot \pi}{6} \right) \right]
\end{aligned} \quad (2.4)$$

- where with  $\theta_r$  denoting the electrical rotor position;  $L_d$  – winding inductance for  $d$ -axis;  $L_q$  – winding inductance for  $q$ -axis, (see Fig. 2.5).

In Fig. 2.2 it can be observed that the divided voltage at the phase terminals does not change with a symmetrical sinusoidal shape over the rotor position. For phase  $W$  this can be described combining equations (2.3) and (2.4) as follows:

$$V_W(\theta_r) = \frac{(L_d + L_q) + \left[ (L_q - L_d) \cdot \sin \left( 2 \cdot \theta_r - \frac{\pi}{6} \right) \right]}{2 \cdot (L_d + L_q) + (L_q - L_d) \cdot \left[ \sin \left( 2 \cdot \theta_r - \frac{\pi}{6} \right) + \sin \left( 2 \cdot \theta_r + \frac{\pi}{2} \right) \right]} \cdot V_{DC} \quad (2.5)$$

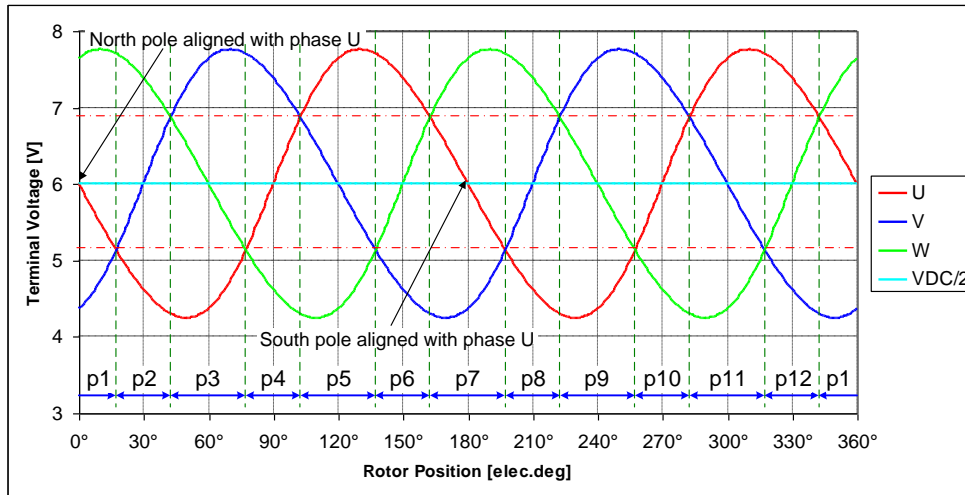


Fig. 2.2 Floating terminal voltage as function of electric rotor position

The proposed estimation principle is based on the detection of the position interval to which the rotor is aligned. One position interval represents the angle between the intersections of two floating terminal voltages as it can be seen in Fig. 2.2 (position intervals  $p1 - p12$ ). Therefore the intersection points of the waveforms have to be calculated. These points can be found based on equations (2.3), (2.4) and (2.5) by solving  $V_U = V_V$ ,  $V_V = V_W$  and  $V_W = V_U$  equations.

Table 2.2 summarizes the results of the equations and the position interval angles (rounded).

Table 2.2 Position angle intervals definition

Position interval	Electrical Angle	Position interval	Electrical Rotor Position
p1	$342^\circ \div 18^\circ$	p7	$162^\circ \div 198^\circ$
p2	$18^\circ \div 42^\circ$	p8	$198^\circ \div 222^\circ$
p3	$42^\circ \div 78^\circ$	p9	$222^\circ \div 258^\circ$
p4	$78^\circ \div 102^\circ$	p10	$258^\circ \div 282^\circ$
p5	$102^\circ \div 138^\circ$	p11	$282^\circ \div 318^\circ$
p6	$138^\circ \div 162^\circ$	p12	$318^\circ \div 342^\circ$

## 2.3 Proposed initial-rotor position estimation algorithm

The estimation procedure consists of two pulse injecting intervals. The first consist of three very short voltage pulses and the second, one long pulse for North and South magnetic pole discrimination.

### 2.3.1 Short pulses injection

Three short test pulses are applied to the motor terminals consecutively as presented in Fig. 2.3 , first between  $U$ - $V$  (Fig. 2.3 (a)), second  $V$ - $W$  (Fig. 2.3 (b)) and third between  $W$ - $U$  (Fig. 2.3 (c)).

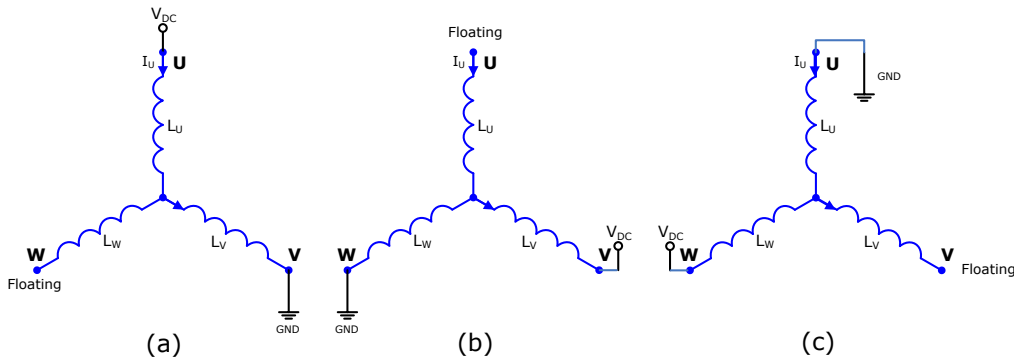


Fig. 2.3 Short test pulse configurations

Fig. 2.4 presents the voltage waveform at the floating terminal according to the relationship between the two phases inductance to which the voltage pulse is applied (in this case  $U$  and  $W$ ). During the second time interval of Fig. 2.4 the test voltage vector is applied, the third time interval is the corresponding freewheeling period. When the inductance of phase  $U$  winding is lower than phase  $W$  winding inductance ( $L_U < L_W$ , Fig. 2.4 case (a)), the voltage measured at the floating terminal  $W$  is higher than half of the supply voltage ( $V_W > V_{DC}/2$ ). If the inductance of phase  $U$  is bigger than the inductance of phase  $W$  winding ( $L_U > L_W$ , Fig. 2.4 case (b)), the voltage at the floating terminal is smaller than half of the supply voltage ( $V_W < V_{DC}/2$ ). In case the winding inductances are equal ( $L_U = L_W$  Fig. 2.4 case (c))



the voltage at the floating terminal  $W$  is equal with the half of the supply voltage ( $V_W = V_{DC}/2$ ).

During the three combinations of the applied short pulses the voltage at the corresponding floating terminal and the supply voltage amplitude is measured and stored. This is used to calculate the delta value between the floating phase and the half of the battery voltage. Equation (2.6) expresses the applied calculation method.

$$\left. \begin{aligned} \Delta_U &= V_U - V_{DC} / 2 \\ \Delta_V &= V_V - V_{DC} / 2 \\ \Delta_W &= V_W - V_{DC} / 2 \end{aligned} \right\} (2.6)$$

- where  $V_U, V_V, V_W$ , - phase-to-ground voltages measured during the short test pulses;  $V_{DC}$  - supply voltage;  $\Delta_U, \Delta_V, \Delta_W$  - phase delta voltages;

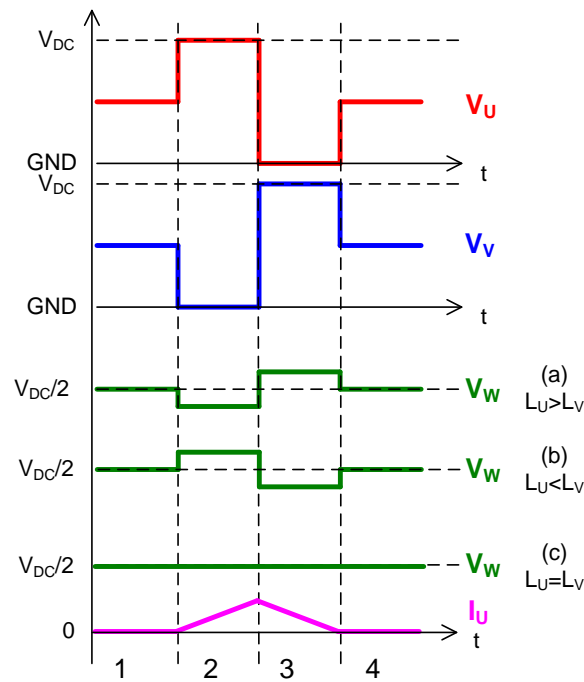


Fig. 2.4 Voltage at the floating terminal for different rotor positions

These delta values are used to establish in which position interval according to Fig. 2.2 rotor magnet is aligned, and which long pulse vector should be applied for North and South Pole discrimination. First the minimum modulus delta ( $\Delta_{min}$ ) is calculated using eq. (2.7).

$$\Delta_{min} = \text{MIN}(|\Delta_U|, |\Delta_V|, |\Delta_W|) \quad (2.7)$$

For example if  $\Delta_{min}$  is given for the voltage measured at U phase, the rotor might be aligned to position intervals  $p1$  ( $342^\circ \div 18^\circ$ ),  $p4$  ( $78^\circ \div 102^\circ$ ),  $p7$  ( $162^\circ \div 198^\circ$ )

or  $p10$  ( $258^\circ \div 282^\circ$ ) from Fig. 2.2. In case of position intervals  $p1$  and  $p7$  a rotor magnet (d-axis) is aligned with phase  $U$ . Fig. 2.5 (a) presents the case for position interval  $p1$  from Fig. 2.2. For position intervals  $p4$  and  $p10$  the rotor is aligned with  $q$ -axis between  $V$  and  $W$  phase core. Thus makes their inductance to be equal ( $L_U = L_W$ ) and the calculated delta value at the floating terminal  $U$  is zero. But this does not mean that rotor magnet is aligned with phase  $U$ , actually the rotor magnets are aligned exactly between phase  $V$  and  $W$ . Now to distinguish between these two alignment cases (shown in Fig. 2.5), the sign of the delta voltages, measured at the other two phases has to be considered (this case  $\Delta V$  and  $\Delta W$ ). So if the sign of  $\Delta V$  is positive and the sign of  $\Delta W$  is negative the rotor is aligned to position intervals  $p4$  or  $p10$ , in the other hand if  $\Delta V$  is negative and  $\Delta W$  if positive the rotor is aligned to positions according to interval  $p1$  or  $p7$ , from Fig. 2.2. Theoretically the delta value sign of only one phase (this case  $\Delta V$  or  $\Delta W$ ) is enough to distinguish between this two position intervals, both of them are used for higher estimation redundancy.

This can be expressed as follows:

$$\left. \begin{aligned} \Delta_{min} = |\Delta U|, \Delta V < 0, \Delta W > 0 &\Rightarrow \left. \begin{aligned} p1(342^\circ \div 18^\circ) \\ p7(162^\circ \div 198^\circ) \end{aligned} \right\} \\ \Delta_{min} = |\Delta U|, \Delta V > 0, \Delta W < 0 &\Rightarrow \left. \begin{aligned} p4(78^\circ \div 102^\circ) \\ p10(258^\circ \div 282^\circ) \end{aligned} \right\} \end{aligned} \right\} \quad (2. 8)$$

As it can be observed from Fig. 2.2 position intervals  $p1, p3, p5, p7, p9$  and  $p11$  are  $36^\circ$  electrical and position intervals  $p2, p4, p6, p8, p10$  and  $p12$  are  $24^\circ$  electrical wide.

If we take as example when a magnet is aligned with phase  $U$  during the first  $18^\circ$  electrical of  $p1$ , call it  $p1'$ , the modulus delta value of  $\Delta V$  is higher than  $\Delta W$  ( $|\Delta V| > |\Delta W|$ ) and in the last  $18^\circ$  electrical of  $p1$ , let's call it  $p1''$ , the modulus value of  $\Delta V$  is lower than  $\Delta W$  ( $|\Delta V| < |\Delta W|$ ). With this procedure all position intervals of  $36^\circ$  electrical can be split into two intervals of  $18^\circ$  electrical, improving the estimation resolution. In case of magnet aligned with  $U$  phase this can be expressed as follows:

$$\left. \begin{aligned} \Delta_{min} = |\Delta U|, |\Delta V| \geq |\Delta W| &\Rightarrow \left. \begin{aligned} p1'(342^\circ \div 360^\circ) \\ p7'(162^\circ \div 180^\circ) \end{aligned} \right\} \\ \Delta_{min} = |\Delta U|, |\Delta V| < |\Delta W| &\Rightarrow \left. \begin{aligned} p1''(0^\circ \div 18^\circ) \\ p7''(180^\circ \div 198^\circ) \end{aligned} \right\} \end{aligned} \right\} \quad (2. 9)$$

With the above procedure the position intervals of  $24^\circ$  electrical ( $p2, p4, p6, p8, p10$  and  $p12$ ) can also be split into two  $12^\circ$  electrical position intervals. When the motor  $q$ -axis is aligned with phase  $U$ :

$$\left. \begin{aligned} \Delta_{min} = |\Delta U|, |\Delta V| \geq |\Delta W| &\Rightarrow \left. \begin{aligned} p4'(78^\circ \div 90^\circ) \\ p10'(258^\circ \div 270^\circ) \end{aligned} \right\} \\ \Delta_{min} = |\Delta U|, |\Delta V| < |\Delta W| &\Rightarrow \left. \begin{aligned} p4''(90^\circ \div 102^\circ) \\ p10''(270^\circ \div 282^\circ) \end{aligned} \right\} \end{aligned} \right\} \quad (2. 10)$$

### 2.3.2 Long pulse injection

With the three short pulses, the rotor position is estimated with 18° electrical resolution, but there are two position interval possibilities for each result, with 180° electrical difference. In one case the rotor is aligned with North and other with South magnetic pole. To distinguish between these two cases a long voltage vector is applied which induces high enough current to reach the magnetic saturation of the stator core. In order to avoid the movement of the rotor during this pulse the time interval for which this pulse is applied should be no longer than the phase winding time constant [56].

The path of the current has to include the phase to which a magnet is closest aligned. As an example if after the short pulses is concluded that rotor magnet (*d*-axis) is close to phase *U*, rotor position intervals *p1* or *p7*, the long pulse should be applied to phases *U-V*, with *U* phase connected to  $V_{DC}$  and *V* phase connected to GND. Now because the *U* phase is aligned with the rotor *d*-axis and phase *V* is closer to *q*-axis the change of their inductance with the rise of phase current is not equal. This can be expressed as follows:

$$\frac{dL_U}{di} \neq \frac{dL_V}{di} \quad (2.11)$$

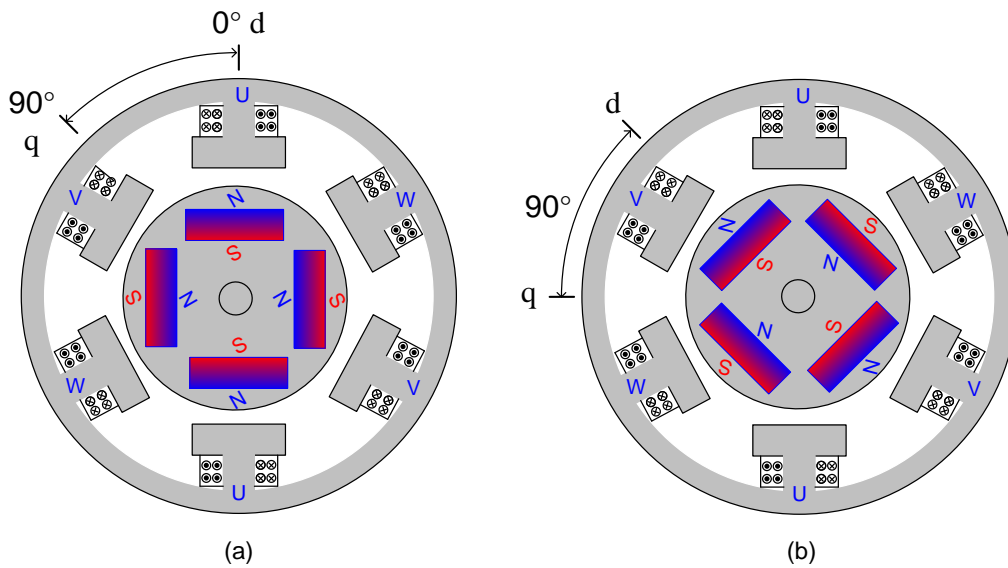


Fig. 2.5 Delta voltage zero crossing positions

When the rotor is aligned with *q*-axis to a phase core, the core lays into a neutral magnetic field, so its saturation is not affected by the rotor magnets. On the other hand, if the rotor is aligned with *d*-axis to a phase core, its magnetic saturation behavior is strongly affected. Therefore it can be concluded that the voltage divider factor of such two aligned phase windings changes with the rotor position. The response during magnetic saturation is different if the rotor is aligned with North or South magnetic pole. For example if a rotor magnet is aligned with phase *U*, the long voltage pulse is applied to phases *U-V* (*U* connected to  $V_{DC}$  and *V* connected to

GND), equation (2.12) expresses the difference between North and South pole alignment. Fig. 2.6 shows the waveform differences between North (a) and South (b) pole alignment to phase  $U$ .

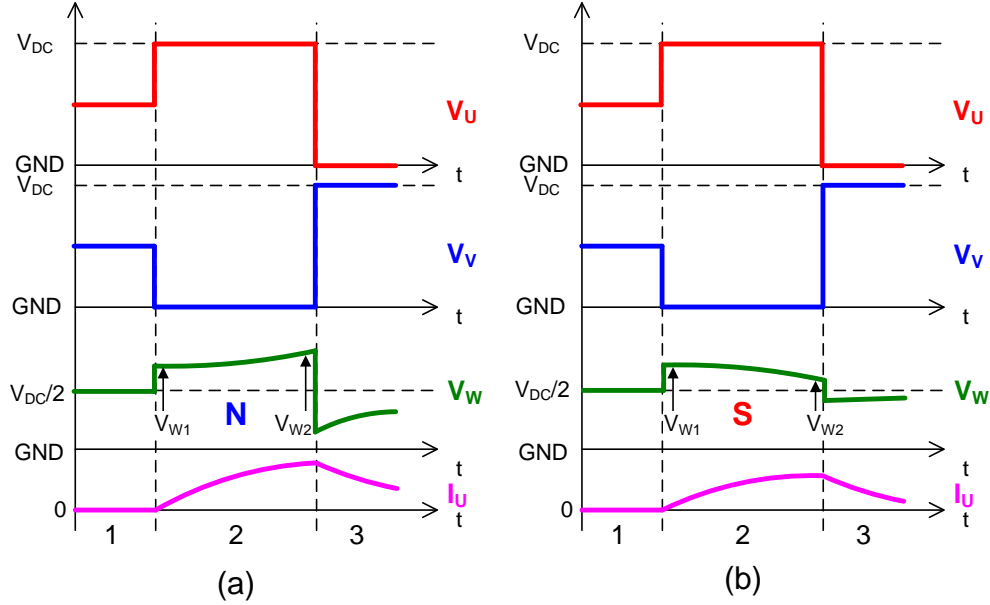


Fig. 2.6 Long pulse waveform according to magnet pole alignment  
(a) -  $U$  phase aligned with north pole, (b)  $U$  phase aligned with south pole.

$$\left. \begin{aligned} \frac{dL_U}{di} > \frac{dL_V}{di} &\Rightarrow U - \text{South} \\ \frac{dL_U}{di} < \frac{dL_V}{di} &\Rightarrow U - \text{North} \end{aligned} \right\} \quad (2.12)$$

During the long pulse, the voltage at the corresponding floating phase has to be measured at the beginning (Fig. 2.6  $V_{W1}$ ) and at the end of the pulse (Fig. 2.6  $V_{W2}$ ). In the case presented in Fig. 2.6 magnet aligned with  $U$  phase ( $d$ -axis) and voltage vector applied to  $U$ - $V$  phases, the voltage at the  $W$  phase is measured. It can be observed that in case of North Pole alignment the voltage at  $W$  phase raises in time and for South Pole alignment decreases. Therefore North and South Pole discrimination can be done using the following equations:

$$\left. \begin{aligned} (V_{W1} - V_{W2}) < 0 &\Rightarrow U - \text{North} \\ (V_{W1} - V_{W2}) > 0 &\Rightarrow U - \text{South} \end{aligned} \right\} \quad (2.13)$$

In most of the applications high load currents causes the supply voltage to drop. When this drop voltage is two times higher than the increase of the terminal voltage, in case of North Pole alignment the system may wrongly conclude that the rotor is aligned with South Pole. Therefore in equation (2.13) the supply voltage

drop effect is compensated in order to make the estimation process robust to battery voltage variation. The resulted equation:

$$\left. \begin{aligned} \left[ (V_{W1} - V_{W2}) - \frac{V_{DC1} - V_{DC2}}{2} \right] < 0 &\Rightarrow U - North \\ \left[ (V_{W1} - V_{W2}) - \frac{V_{DC1} - V_{DC2}}{2} \right] > 0 &\Rightarrow U - South \end{aligned} \right\} \quad (2.14)$$

Table 2.3 summarizes the estimated rotor alignment position ( $\theta_r$ ) intervals according to the short and long pulses result evaluations.

Table 2.3 Estimation of the initial rotor position

$\Delta_{min}$	Voltage comparison		Possible initial positions	Long pulse path	Voltage Comparison	Estimated position	
<b> \Delta U </b>	$\Delta V < 0$ $\Delta W > 0$	$ \Delta V  <  \Delta W $	$0^\circ < \theta_r \leq 18^\circ$ $180^\circ < \theta_r \leq 198^\circ$	U-V	$V_{W1} < V_{W2}$ $V_{W1} > V_{W2}$	$0^\circ < \theta_r \leq 18^\circ$ $180^\circ < \theta_r \leq 198^\circ$	
		$ \Delta V  >  \Delta W $	$342^\circ < \theta_r \leq 360^\circ$ $162^\circ < \theta_r \leq 180^\circ$	U-V	$V_{W1} < V_{W2}$ $V_{W1} > V_{W2}$	$342^\circ < \theta_r \leq 360^\circ$ $162^\circ < \theta_r \leq 180^\circ$	
	$\Delta V > 0$ $\Delta W < 0$	$ \Delta V  <  \Delta W $	$90^\circ < \theta_r \leq 102^\circ$ $270^\circ < \theta_r \leq 282^\circ$	V-W	$V_{U1} < V_{U2}$ $V_{V1} > V_{V2}$	$90^\circ < \theta_r \leq 102^\circ$ $270^\circ < \theta_r \leq 282^\circ$	
		$ \Delta V  >  \Delta W $	$78^\circ < \theta_r \leq 90^\circ$ $258^\circ < \theta_r \leq 270^\circ$	W-U	$V_{V1} > V_{V2}$ $V_{V1} < V_{V2}$	$78^\circ < \theta_r \leq 90^\circ$ $258^\circ < \theta_r \leq 270^\circ$	
	<b> \Delta V </b>	$\Delta W < 0$ $\Delta V > 0$	$ \Delta W  <  \Delta U $	$120^\circ < \theta_r \leq 138^\circ$ $300^\circ < \theta_r \leq 318^\circ$	V-W	$V_{U1} < V_{U2}$ $V_{U1} > V_{U2}$	$120^\circ < \theta_r \leq 138^\circ$ $300^\circ < \theta_r \leq 318^\circ$
			$ \Delta W  >  \Delta U $	$102^\circ < \theta_r \leq 120^\circ$ $282^\circ < \theta_r \leq 300^\circ$	V-W	$V_{U1} < V_{U2}$ $V_{U1} > V_{U2}$	$102^\circ < \theta_r \leq 120^\circ$ $282^\circ < \theta_r \leq 300^\circ$
$\Delta W > 0$ $\Delta V < 0$		$ \Delta W  <  \Delta U $	$18^\circ < \theta_r \leq 30^\circ$ $198^\circ < \theta_r \leq 210^\circ$	U-V	$V_{W1} < V_{W2}$ $V_{W1} > V_{W2}$	$18^\circ < \theta_r \leq 30^\circ$ $198^\circ < \theta_r \leq 210^\circ$	
		$ \Delta W  >  \Delta U $	$30^\circ < \theta_r \leq 42^\circ$ $210^\circ < \theta_r \leq 222^\circ$	W-U	$V_{U1} > V_{U2}$ $V_{U1} < V_{U2}$	$30^\circ < \theta_r \leq 42^\circ$ $210^\circ < \theta_r \leq 222^\circ$	
<b> \Delta W </b>		$\Delta U < 0$ $\Delta V > 0$	$ \Delta U  <  \Delta V $	$60^\circ < \theta_r \leq 78^\circ$ $240^\circ < \theta_r \leq 258^\circ$	W-U	$V_{V1} < V_{V2}$ $V_{V1} > V_{V2}$	$60^\circ < \theta_r \leq 78^\circ$ $240^\circ < \theta_r \leq 258^\circ$
			$ \Delta U  >  \Delta V $	$42^\circ < \theta_r \leq 60^\circ$ $222^\circ < \theta_r \leq 240^\circ$	W-U	$V_{V1} < V_{V2}$ $V_{V1} > V_{V2}$	$42^\circ < \theta_r \leq 60^\circ$ $222^\circ < \theta_r \leq 240^\circ$
	$\Delta U > 0$ $\Delta V < 0$	$ \Delta U  <  \Delta V $	$150^\circ < \theta_r \leq 162^\circ$ $330^\circ < \theta_r \leq 342^\circ$	U-V	$V_{W1} > V_{W2}$ $V_{W1} < V_{W2}$	$150^\circ < \theta_r \leq 162^\circ$ $330^\circ < \theta_r \leq 342^\circ$	
		$ \Delta U  >  \Delta V $	$138^\circ < \theta_r \leq 150^\circ$ $318^\circ < \theta_r \leq 330^\circ$	V-W	$V_{U1} < V_{U2}$ $V_{U1} > V_{U2}$	$138^\circ < \theta_r \leq 150^\circ$ $318^\circ < \theta_r \leq 330^\circ$	

Fig. 2.7 presents the basic flowchart of the proposed initial rotor position estimation method.

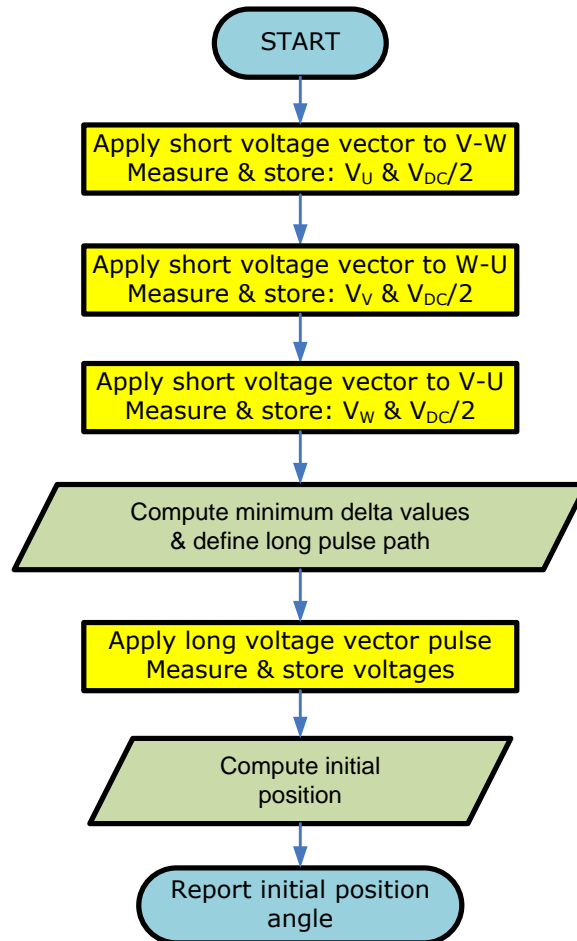


Fig. 2.7 Proposed initial position detection method flowchart

## 2.4 Experimental results

In Fig. 2.8 the sensorless drive system block schematic is shown which is used to implement and verify the proposed method. The driving of the power inverter and implicit the BLDC motor is done by the system microcontroller, S12X (HCS12XDP512) family, 16-bit [92]. The  $V_{DC}$  supply voltage of the power inverter is 14V. The control and monitor of the system is done via a PC application which communicates with the system microcontroller via USB communication interface.

The employed machine consists of a salient-pole brushless dc motor with concentrated windings connected in star configuration having the parameters presented in Table 2.1.

The short pulse-injecting time applied in this experiment was  $22\mu\text{s}$  followed by a freewheeling time. Thus the total time of the three short pulses is approximately  $140\mu\text{s}$ . The third freewheeling time is a little bit longer than the other because here the computation for the long pulse decision is done. The time needed to apply a

short pulse is not affected by the motor parameters, it is only dependent on the microcontroller ADC (Analog to Digital Converter) conversion time and the settle time of the floating terminal voltage. The battery and the phase voltages are sampled and recorded before the end of each pulse period.

The long pulse-injection time was  $350\mu\text{s}$ , followed by a freewheeling period. The long pulse time has to be chosen long enough to induce high enough phase currents for reaching the magnetic saturation of the stator core.

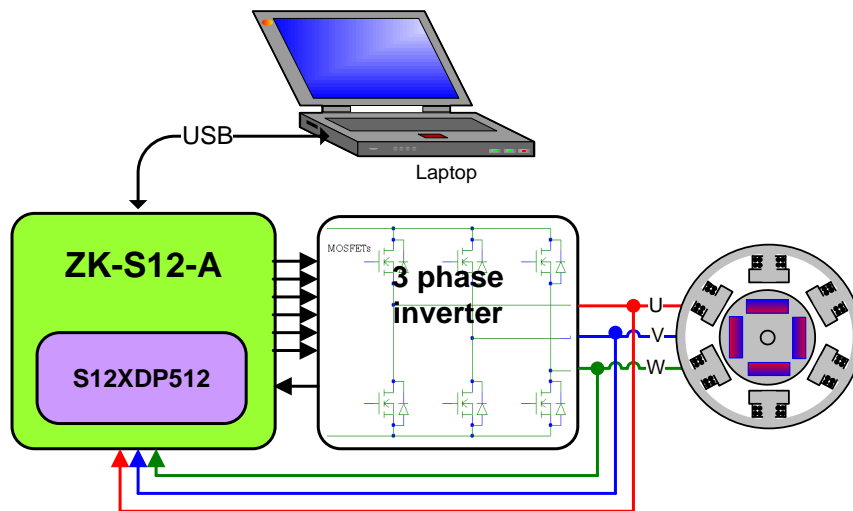


Fig. 2.8 Sensorless BLDC drive system block schematic

The *overall* initial rotor position estimation time for the used BLDC motor was around 0,8ms.

Fig. 2.9 presents the phase voltages for the short pulses injection period for the case when the rotor is aligned with  $d$ -axis to  $U$  phase. The calculated delta value amplitudes are  $\Delta V < 0$ ,  $\Delta W > 0$  and  $|\Delta V| < |\Delta W|$ . There are two possible position intervals which gives the same results  $0^\circ < \theta_r \leq 18^\circ$  and  $180^\circ < \theta_r \leq 198^\circ$ . The discrimination between these two position alignment possibilities is done by evaluation of the long pulse response. Fig. 10 shows the long pulse waveforms for North ((a)  $\Rightarrow 0^\circ < \theta_r \leq 18^\circ$ ) and South ((b)  $\Rightarrow 180^\circ < \theta_r \leq 198^\circ$ ) magnetic pole alignment. Note the increase (Fig. 2.10 (a) North Pole) and decrease (Fig. 2.10 (b) South Pole) of the floating terminal voltage during the long pulse.

This demonstrates that the proposed method is valid and an overall of  $18^\circ$  electrical rotor position estimation resolution is possible, for some rotor positions the estimation accuracy is even better,  $12^\circ$  electrical. Fig. 2.11 presents the estimated rotor position result over a complete electrical rotation of the rotor, Fig. 2.12 the estimation error of the proposed method.

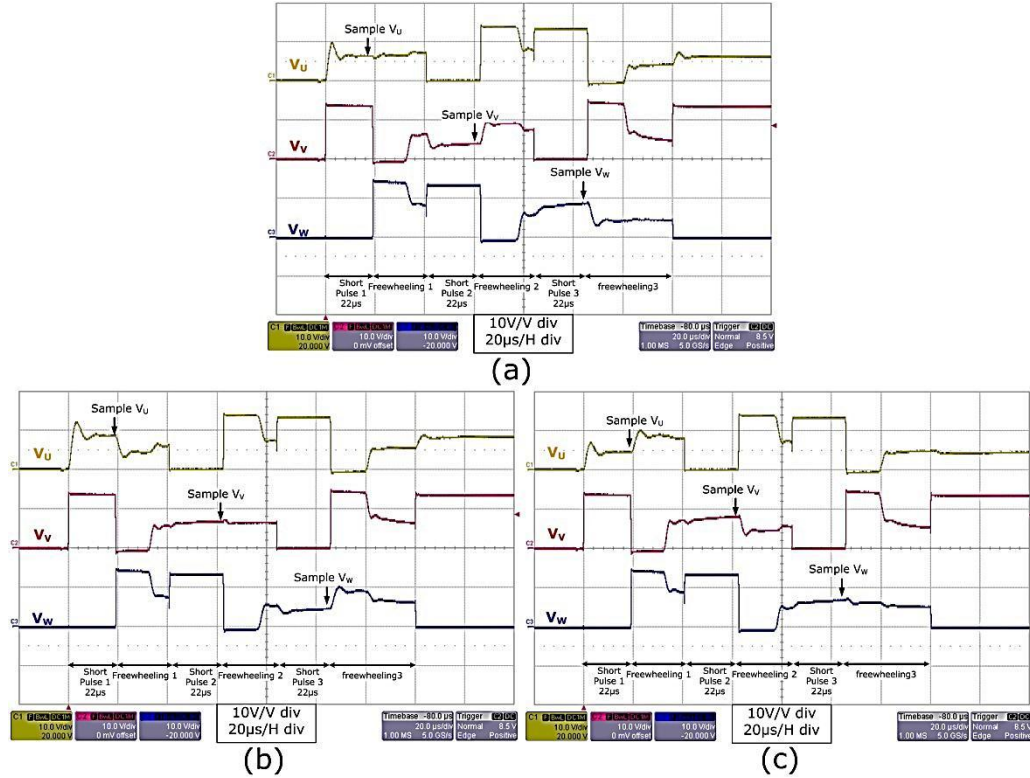


Fig. 2.9 Short pulses injection waveforms  
 (a) Rotor magnet aligned to phase  $U$ ,  $0^\circ < \theta_r \leq 18^\circ$  or  $180^\circ < \theta_r \leq 198^\circ$ ;  
 (b) Rotor magnet aligned to phase  $V$ ,  $90^\circ < \theta_r \leq 102^\circ$  or  $270^\circ < \theta_r \leq 282^\circ$ ;  
 (c) Rotor magnet aligned to phase  $W$ ,  $150^\circ < \theta_r \leq 162^\circ$  or  $330^\circ < \theta_r \leq 342^\circ$ ;

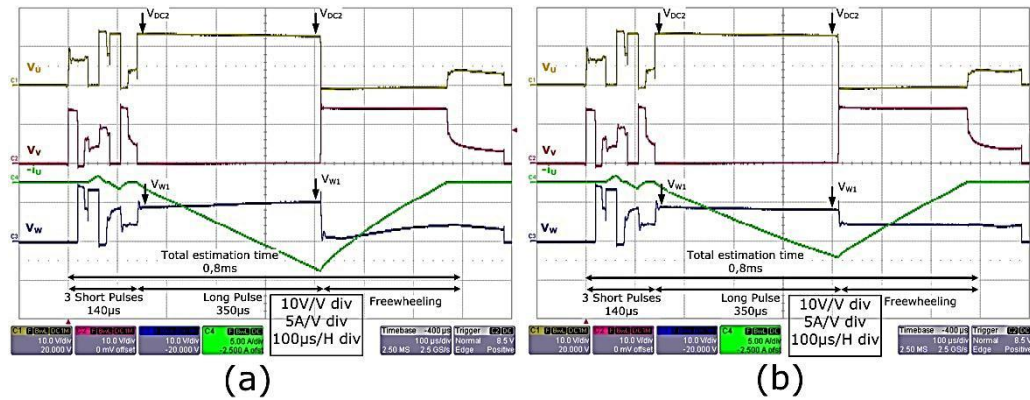


Fig. 2.10 Long pulse injection waveforms  
 (a) Rotor aligned with North magnetic pole;  
 (b) Rotor aligned with south magnetic pole;



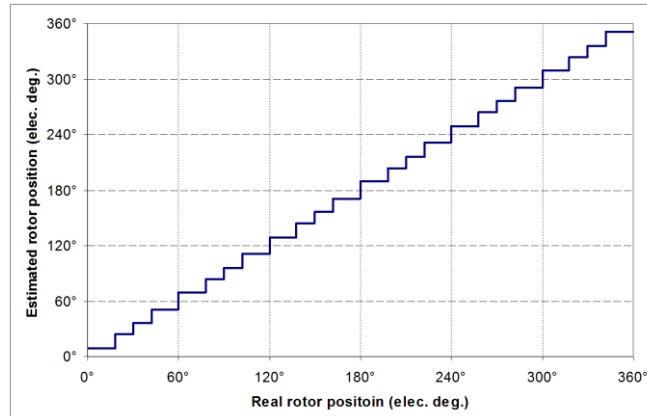


Fig. 2.11 Initial rotor-position estimation method result

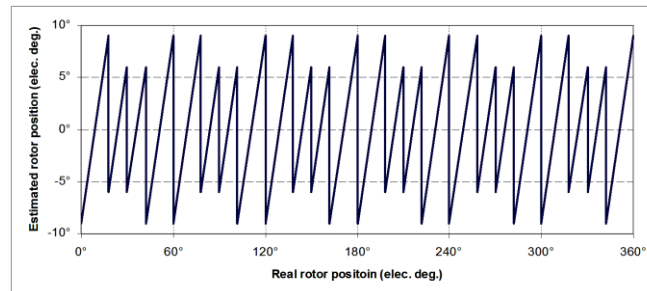


Fig. 2.12 Estimation error in electrical degrees of the proposed method

Due to the pulse application and the voltage measurement procedure, this method is the fastest known initial rotor position estimation method for salient pole BLDC motors. The following Table 2.4 presents a comparison between the most representative initial rotor position detection methods (presented in chapter 1). Table 2.4 presents a comparison between the most representative initial rotor position estimation methods highlighting the new proposed methods advantages [54]-[58], [82]-[87].

Table 2.4 Comparison of existing and proposed method

Special Feature	[54]	[56]	[57]	[58]	[82]	[85]	[86]	[87]	Proposed Method
Number of pulses	6	5	12	3	3	6	6	6	<b>4</b>
DC-link Current	1	1	1	-	1	-	1	-	<b>0</b>
Phase Currents	-	-	-	-	-	3	-	-	<b>-</b>
Terminal Voltage	-	-	-	3	3	-	-	3	<b>3</b>
Resolution of the estimated position	60°	30°	30°	60°	30°	24°	30°	30°	<b>18°</b>
Estimation time [ms] *	4.2	3.5	8.4	2.1	2.1	4.2	4.2	4.2	<b>0.8</b>

\* Considering the motor parameters shown in Table 2.1

### Experimental setup detailed description

The block schematic of the experimental setup is presented in Fig. 2.8. This is composed of:

- S12x family system microcontroller;
- Three phase power inverter and driver circuit;
- BLDC motor mounted on a KISTLER evaluation bench;
- PC GUI (Graphical User Interface);

The Freescale HC9S12XDP512MAL system microcontroller is equipped on a SofTec ZK-S12-A Starter kit, below the picture of the board (Fig. 2.13) [91][92].

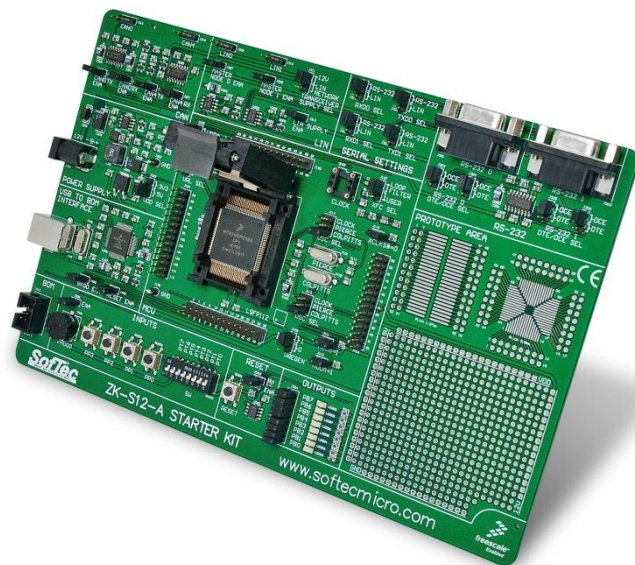


Fig. 2.13 SofTec ZK-S12-A starter kit board [91]

Using this microcontroller the software which controls the BLDC motor inverter and the proposed initial detection position method was implemented. The program was developed using Freescale CodeWarrior IDE Development Studio v5.9.0.

The three phased power inverter stage was developed specially to evaluate this proposed method and is composed of an Infineon three phase power bridge driver IC TLE6280GP type which drives the six power MOSFET's (BUK765R2-40 type from NXP) [93][94]. The schematic of the three phased inverter circuit is presented in ANNEX Fig. 9.1.

The employed BLDC motor is similar with the one presented in Fig. 1.12 manufactured by Brose, the mechanical drawings of the motor assembly are presented in Fig. 2.14.

The graphical user interface (GUI) used to control the BLDC motor control system and display its parameters, results has been developed using National Instrument LabWindows / CVI. The GUI application communicates with the system microcontroller via USB interface. Since the ZK-S12-A starter kit board has no USB interface a simple USB to serial converter circuit has been used FT232R from FDTI chip [95]. A screenshot of the developed GUI is presented in Fig. 2.15.

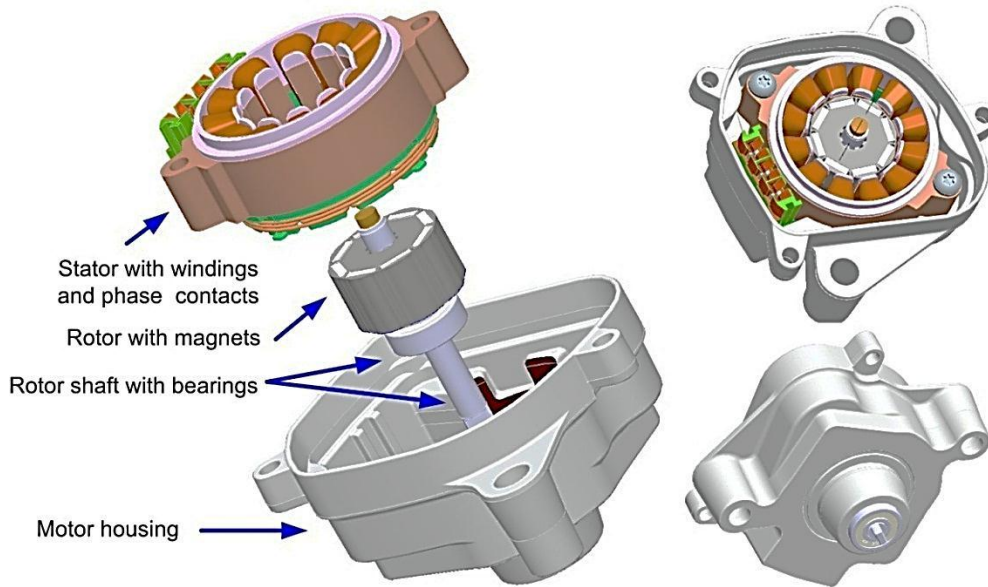


Fig. 2.14 Employed BLDC motor assembly drawings

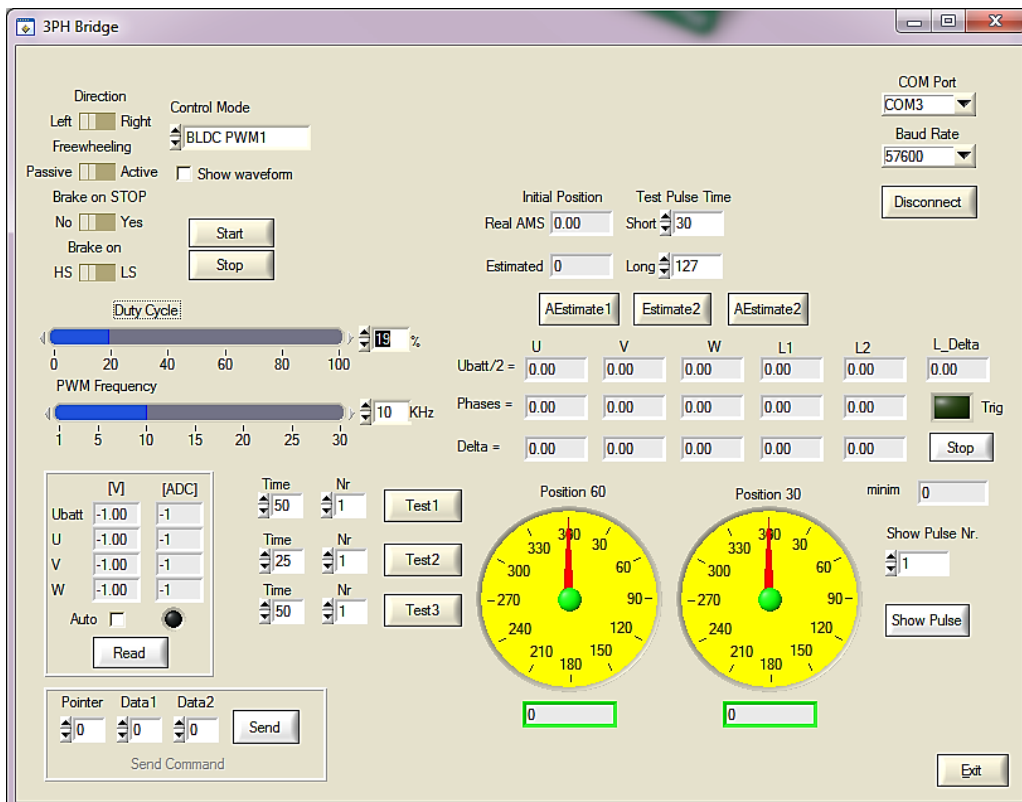


Fig. 2.15 Proposed initial position estimation method evaluation GUI screenshot

The experimental test bench picture is presented in the next picture (Fig. 2.16)

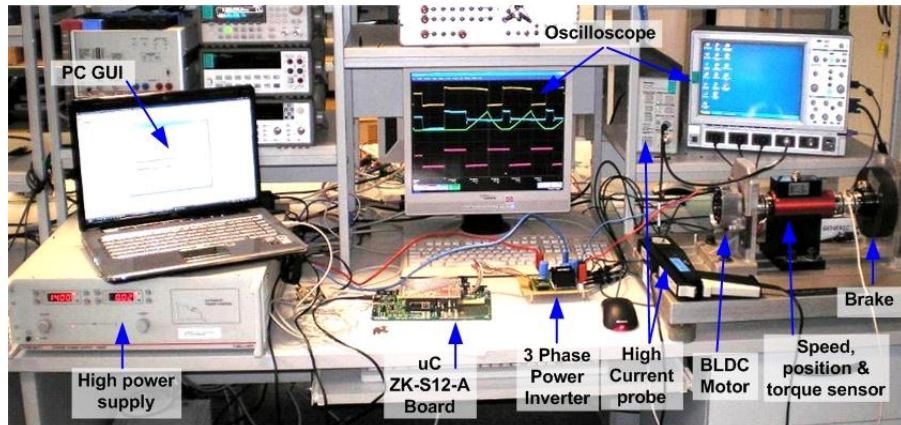


Fig. 2.16 Picture of the Experimental test-bench

## Summary

A novel initial rotor position estimation algorithm, for salient pole brushless dc motor drives, based only on voltage sensing at the motor terminals has been proposed and presented by the author. The overall estimation resolution of the proposed method is  $18^\circ$ . Great benefit is that no current measurement is needed for the initial-rotor position estimation and the time needed for the rotor position estimation is considerably shorter than the estimation time of the already proposed methods.

Once again, it is demonstrated that from initial rotor position detection point of view the rotor configuration with inset magnets had obvious advantages in comparison with the surface mounted magnets and the brushless dc motor for low performance applications such fans, coolers, pumps compressors; the motor should be designed with high saliency.

Temperature range requirement of some electronics in automotive applications is  $[-40^\circ \dots 150^\circ]$ . In such case the electrical time constant of the motor can double due to the stator phase resistance change over temperature. No temperature compensation algorithm is necessary with this technique, fact which must be taken into account for most of the already proposed solutions. This is one strong point of the proposed solution.

## 3 Automotive brushless DC motor control system

In the first part of this chapter a short overview of the automotive applications which employ BLDC motors as actuators is presented. On the second part an automotive BLDC motor control ASIC concept is presented based on existing state of the art technology, known methods and control algorithms and new ideas of the author presented in several scientific conferences, papers and proceedings [132]-[148], [151], [152], [154], [156]-[166], [171].

### 3.1 Overview of automotive brushless DC motor control systems

Recent evolution and innovations in the BLDC motor technology opened the possibility of implementation and development of high performance BLDC actuator systems for the automotive industry, in the same time benefitting from the increased reliability and robustness of this technology.

A broad overview of automotive electrification trends has been elaborated in the first chapter of the thesis elaborated by Dr. Coroban V. S. [106]. This chapter presents the most representative application for BLDC motors in an automobile:

- Double clutch transmission control unit, Fig. 3.2;
- Four wheel drive / transfer-case control unit, Fig. 3.4;
- Shift by wire;
- Active Turbocharger;
- Air intake throttle valve control, Fig. 3.1;
- General propose BLDC actuators (smart actuator) used for window lifting, active valve control, exhaust brake, etc., Fig. 3.1;
- Active suspension and roll stabilization systems, Fig. 3.3;
- Brake by wire system Fig. 3.5;
- Pump applications for: oil, cooling liquid, water, fuel, etc., Fig. 3.6;
- Fan applications for engine, passenger compartment ventilation, Fig. 3.8;
- Radar, range scanning actuator;
- Electronic adaptive steering assistance, automatic parking systems Fig. 3.7;



Fig. 3.1 Water cooled general propose BLDC actuator, Air intake, throttle control valve

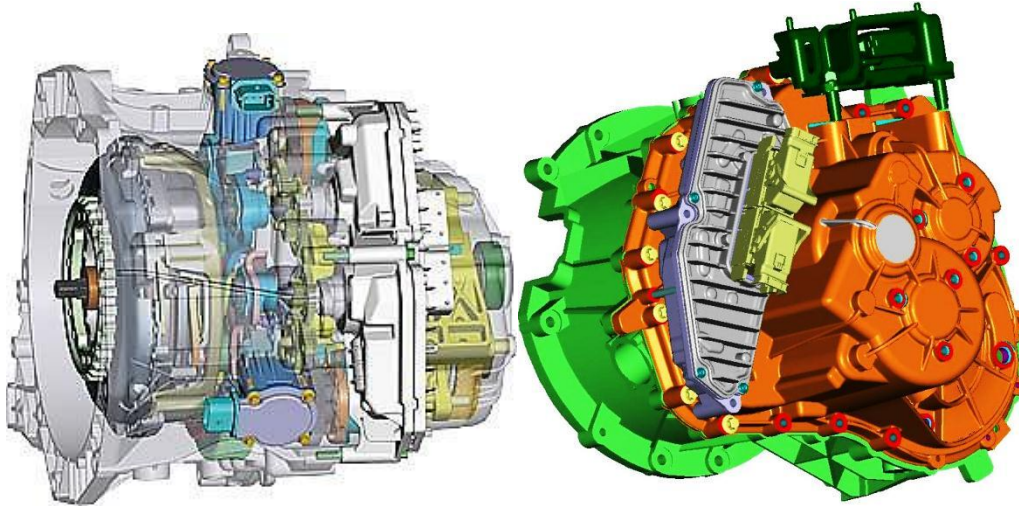


Fig. 3.2 Getrag double clutch PowerShift 6DCT250, using 4 BLDC motor actuators [109]

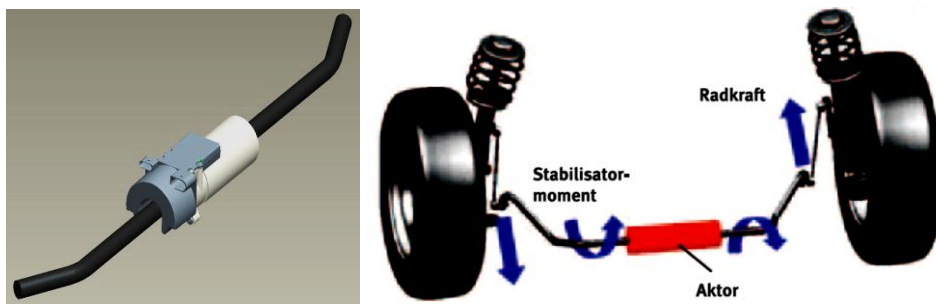


Fig. 3.3 Active suspension, roll stabilization system

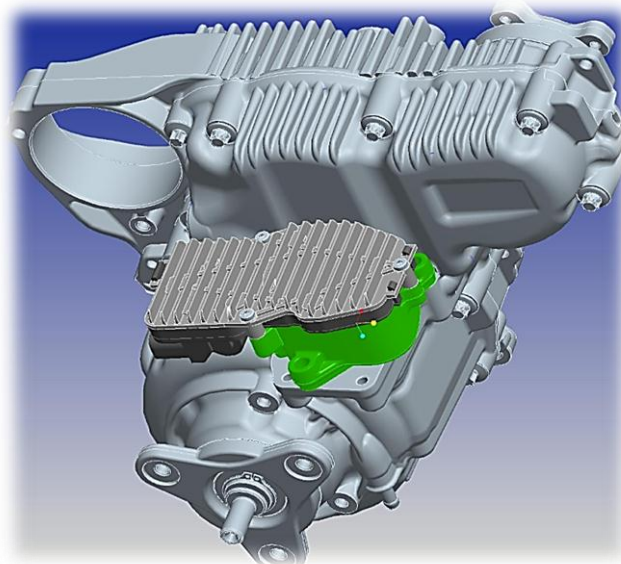


Fig. 3.4 Four wheel drive, transfer-case assembly

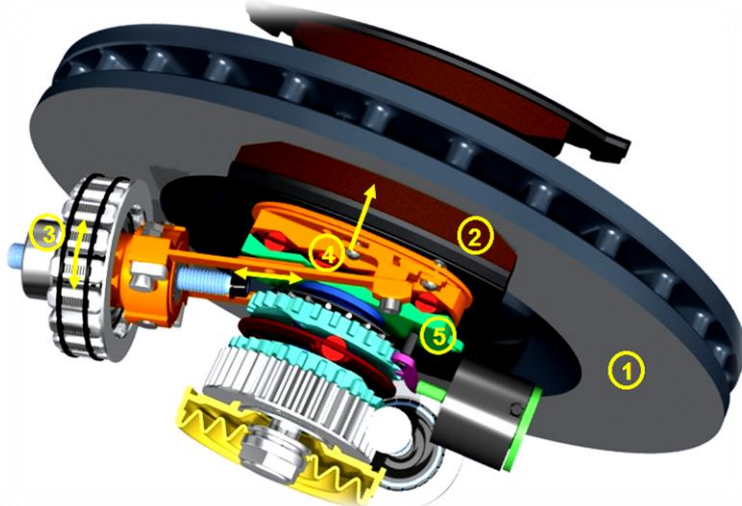


Fig. 3.5 Brake by wire system



Fig. 3.6 BLDC motor driven fuel pump [107]



Fig. 3.7 Adaptive electronic steering system using BLDC motor [110]



Fig. 3.8 BLDC blower and engine cooling fan application [110]

In most of the automotive applications like engine management control unit (ECU), transmission control unit (TCU), break by wire systems, or transfer-case control units, the system is connected to several input sensors, actuators and communication networks. The advanced driving/control of a BLDC motor requires considerable computing power (especially for sensorless drive) from the units' system microcontroller, which in most of the cases is not available. Therefore two implementation categories of the BLDC motor control exist, depending on the motor drive performance requirements in the particular application:

- Software implementation of the BLDC motor control;
- Hardware implementation of the BLDC motor control (using a specialized motor controller ASIC);

The software implemented high performance driving of the BLDC motor as mentioned requires significant computing power which is not available in all systems. Advanced drive of the BLDC motor can be implemented by pure software (using minimal HW only to adapt the switching elements control signal levels) using the computational power offered by a DSP or a microcontroller [46], [111]-[126]. Fig. 3.9 presents a block schematic of a DSP based electrical steering control system [118]. In this system the complete control of the BLDC motor is implemented in the software application running on the DSP. Such systems are very expensive to implement and most of the DSP computing power is occupied with the BLDC motor control.

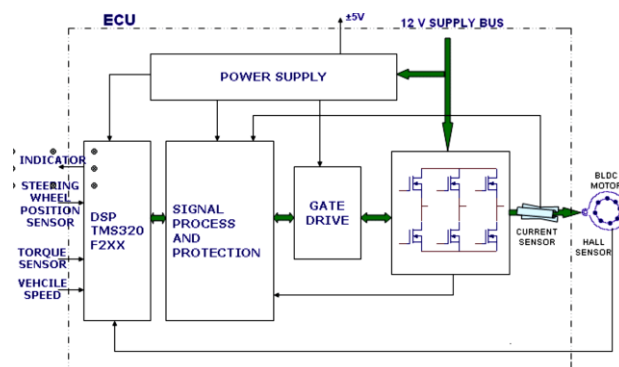


Fig. 3.9 DSP base BLDC motor control, steering assistance module [118]



Some microcontroller manufacturers have developed special microcontrollers for BLDC motor control. In these microcontrollers beside the standard ALU and IO interfaces, a BLDC motor controller block is also implemented. The BLDC motor control module interface is taking over a big part of the BLDC motor control task therefore, significantly reducing the overall required computing power [127]-[135]. The block schematic of such a BLDC motor driver system is presented in Fig. 3.10. However the main functionalities which can be implemented using such a technology are the control algorithm (using logic cells) of the BLDC motor. The analog high power MOSFETs gate driver, the failure monitoring circuits, current measurement circuits and so on cannot be implemented, because the BLDC motor specialized microcontrollers are manufactured using low voltage silicone chip technology. Therefore the BLDC motor control system must contain a power bridge driver unit as presented in Fig. 3.10 (APMOTOR56F80000).

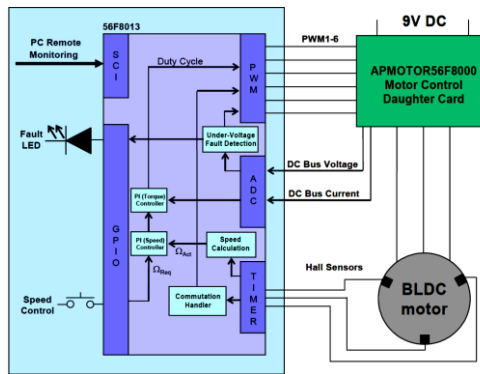


Fig. 3.10 BLDC motor control system using Freescale 16-bit hybrid controller [127]

In case of applications which require more than one BLDC motor, like an electro-mechanically actuated transmission control unit (as presented in Fig. 3.2) these systems present a major drawback. These BLDC driver microcontrollers usually have only one BLDC motor control module included. Therefore each motor needs its own microcontroller. However, mainly in prototype and industrial systems which control several BLDC motors, each of them can be controlled by a separate microcontroller or DSP, coordinated by a main or master microprocessor. The block schematic of such a system is presented below (Fig. 3.11).

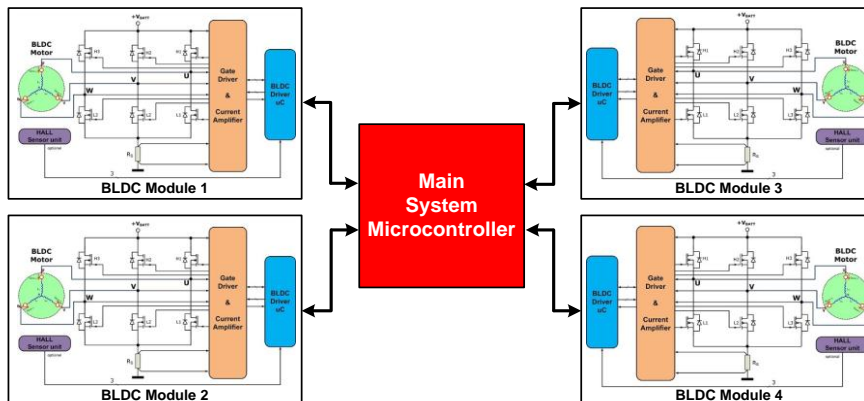


Fig. 3.11 Modular BLDC motor control system block schematic

The drawback of these systems is the overall costs of the implementation which is quite high compared to other systems. Nevertheless it's a good approach to modular based system design as mass production machines or equipment, control systems, used in industrial applications.

In the automotive industry the control systems have a tremendous cost control pressure, demanding very low priced units, with very high requirements in the same time. Such systems cannot be implemented using only specialized microcontroller solutions or DSPs because their high performance comes with a high price (especially for DSP driven systems). When the system performances are reduced (like a specialized microcontroller driven system) also the price is reduced but the overall system performance may not fit with all the application requirements. Solutions to this problem are systems, containing one single main microcontroller combined with specialized BLDC motor controller ASICs. Such systems can provide very high drive performances and having in the same time a low price. Several control functions of the BLDC motor being implemented in these ASIC's reduces significantly the computational power required to control the BLDC motor. In addition these ASIC's being developed in a mixed signal technology (digital and analog circuits on the same chip) permits several functions to be integrated on them, thus compacting the system, increasing its performances and reducing the costs. A block diagram of such a system dedicated for automotive applications is presented in the next Fig. 3.12. The concept can also be applied for single microcontroller systems, controlling several BLDC motors. An example of such a system using four BLDC motor control ASIC modules is presented in Fig. 3.13.

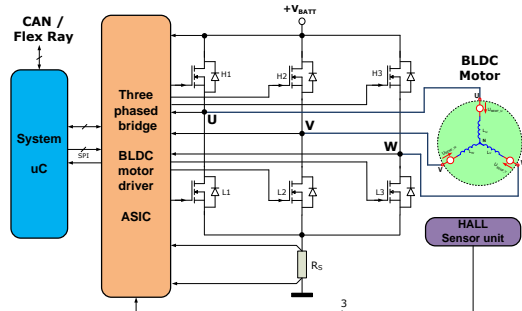


Fig. 3.12 ASIC driven BLDC motor control system block schematic

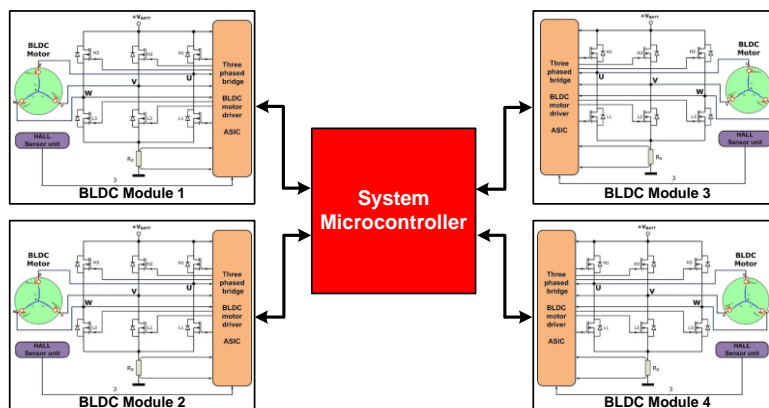


Fig. 3.13 Multi BLDC motor driver system diagram using specialized ASIC's

### 3.2 Automotive BLDC motor control ASIC

In this subchapter a complex architecture for a BLDC motor controller ASIC is proposed, designated to automotive applications, based on the existing state of the art technology and new ideas, concepts proposed by the author.

The block diagram presenting the internal modules of the proposed ASIC is presented in Fig. 3.14. It contains several units, each dealing with specific functions which shall be implemented inside the ASIC. These modules are the MOSFET gate driver block, the current measurement and amplifier unit, the diagnosis system for the BLDC motor and the control ASIC itself, the motor drive mode and commutation logic (including the look-up table for six step commutation and the sensorless zero crossing detection comparators) and a control interface including an IO communication interface (SPI) for communication with the system microcontroller and a disable unit for failure situations.

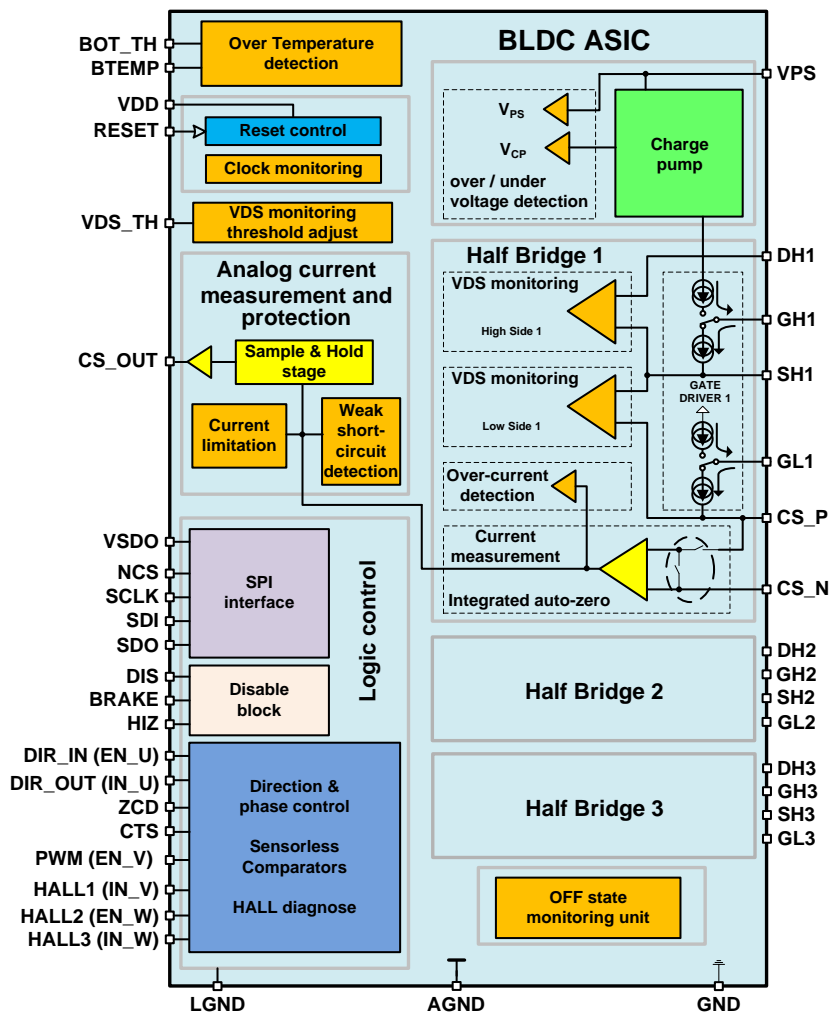


Fig. 3.14 Proposed BLDC driver ASIC block diagram

The following table detail the IO configuration of the proposed ASIC.

Table 3.1 IO configuration of the proposed BLDC driver ASIC

IO pin name	Function block	Details
DIR_IN	Motor control	Rotational direction control input signal
DIR_OUT	Motor control	Actual rotating direction of the motor
PWM	Motor control	PWM input for BLDC motor voltage control
ZCD	Motor control	Zero crossing detection signal
CTS	Motor control	Commutation trigger signal
HALL1, HALL2, HALL3	Motor control	Hall sensors position input signals
CS_OUT	Current measurement	Analog current measurement output
CS_P, CS_N	Current measurement	Current measurement input sense lines, connected to DC link shunt
DIS	ASIC control	Disable input of the ASIC
BRAKE	ASIC control	Brake mode entry
HIZ	ASIC control	High impedance control for the bridge
RESET	ASIC control	Reset input of the ASIC
VSDO	Logic supply	SPI IO logic level supply voltage
NCS	SPI	Chip select
SCLK	SPI	Serial communication clock
SDI	SPI	Serial communication input data
SDO	SPI	Serial communication output data
DH1, DH2, DH3	Diagnosis	Sense line for the HS external MOSFET's drain, for the $V_{DS}$ monitoring circuit
GH1, GH2, GH3	MOSFET driver	Gate control signals of HS MOSFET's
SH2, SH2, SH3	MOSFET driver	Phase terminals voltage sense lines
GL1, GL2, GH3	MOSFET driver	Gate control signals of LS MOSFET's
VPS	Power Supply	Battery voltage power supply input
VDD	Power Supply	Logic supply voltage
LGND	Power Supply	Logic supply ground connection
GND	Power Supply	Power supply ground connection
AGND	Power Supply	Analog supply ground connection
VDS_TH	Diagnosis	$V_{DS}$ monitoring threshold voltage
BOT_TH	Diagnosis	Bridge over-temperature detection threshold
BTEMP	Diagnosis	Bridge temperature sense input

### 3.2.1 Three phased power inverter MOSFET's gate driver

An advanced three phased power inverted is built using only N-channel MOSFET's for both HS and LS switches. Therefore a high voltage internal supply is needed to charge the HS MOSFET's gates, to voltages above the battery voltage. In a typical automotive applications the used MOSFET types has a gate threshold

voltage between 3-5V and the recommended  $V_{GS\_ON}$  voltage around 10V, this ensures the very low on resistance ( $R_{DS\_ON}$ ) of the MOSFET when is activated [148].

There are two common implementations of this high voltage generation circuit in the motor controller electronics. The most common implementation is the bootstrap circuit (bootstrap capacitor) which is charged up during the LS MOSFET conduction and its stored energy is used to supply the HS gate driver circuit [138]-[140]. The disadvantage of this method is that switching of the LS MOSFET must occur to generate the high voltage, this limit the maximum PWM duty cycle which can be used to drive the BLDC motor.

Another way to generate the internal high voltage is using a low power charge pump. This has a separate oscillator and generates the high voltage regardless of the bridge operation. Another advantage of such a system is that in low battery voltage conditions (below 10V) the full charge of the LS MOSFET's gate is still possible (from the charge pump voltage  $V_{CP}$ ) reducing its power consumption. The concept schematic of a two stage charge pump is presented in Fig. 3.15.

The two stage charge pump is capable to generate a voltage approximately three times higher than the input voltage. This is not needed for high battery voltages, therefore the second stage of the charge pump can be disabled via "EnableS2" signal. The complete disable of the charge pump can be done via the two "EnableS1" and "EnableS2" input signals.

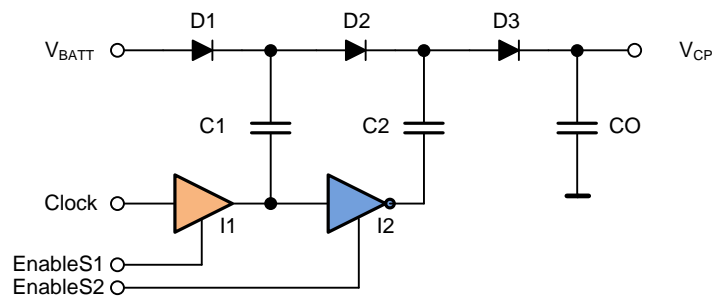


Fig. 3.15 Two stage charge pump concept schematic

Having this high voltage available on the chip all the power MOSFET's gates are charged from this charge pump voltage ( $V_{CP}$ ). The best technique for a good control of the MOSFET's switching behavior is to charge the gates using constant current sinks and sources. In the ASIC these current sources shall be controllable to several predefined current values, this ensures easy change of their switching times and adaptation of the circuit to different MOSFET types.

A much detailed operation of the gate driver unit operation mode which should be included in this proposed ASIC architecture is presented in chapter 4, Alternating freewheeling PWM technique for a better power distribution.

### 3.2.2 Load current measurement unit

The most commonly implemented BLDC motor current measurement concept is the measuring of the DC link current of the power inverter block.

The load current measurement shall be based on a differential input operational amplifier circuit with configurable gain, followed by a Sample & Hold (S&H) stage, configured to sample the average value of the current through the BLDC motor. This

S&H current measurement technique replaces the classical high order low pass filtering which causes long time delays in the current measurement path. Using the S&H stage combined with a good synchronization of the sampling points the current measurement output is updated to the actual value every PWM cycle. The next Fig. 3.16 presents the current measurement circuit block schematic. It contains the differential input amplifier circuits with SPI configurable gain, the output Sample & hold Stage, an offset voltage reference which is added to the output voltage for "Auto Zero" calibration possibility. The "Auto Zero" enables the precise measurement of the amplifiers offset voltage, improving the overall load current measurement accuracy. In addition the offset can be measured also "online", in the field, thus correcting the current measurement offset errors over temperature and lifetime of the final product. When the "Auto Zero" circuit is activated the current sense inputs of the input amplifier are disconnected from the shunt and shortened together. Therefore at the CS\_OUT terminal the internal  $V_{OFFSET}$  voltage can be measured.

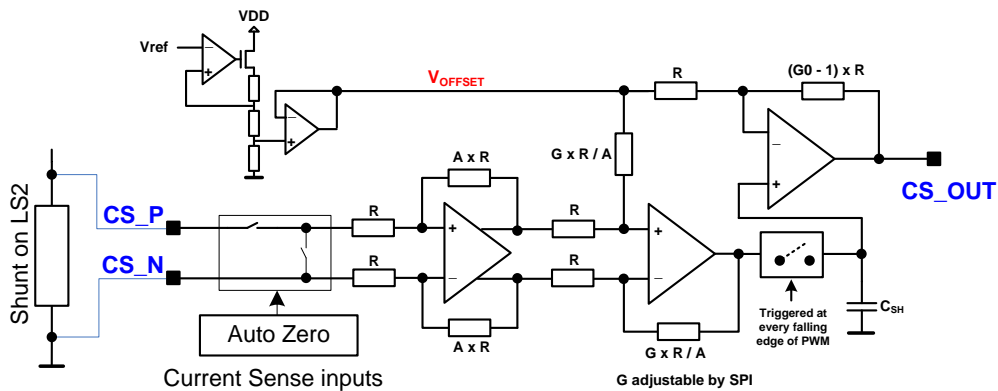


Fig. 3.16 Current measurement circuit block diagram

The overall amplification factor is determined by the configured gain value  $G$ . Therefore the output voltage of the circuit will be:

$$V_{CS\_OUT} = (V_{CS\_P} - V_{CS\_N}) \cdot G + V_{OFFSET} \quad (3.1)$$

In order that the above presented current measurement concept measure the input average current correctly, the S&H stage must be synchronized with the current flowing through the BLDC motor. This is achieved by the so called "Double PWM" technique. In this technique the input PWM from the microcontroller is doubled internally of the ASIC. Then the sampling of the load current is synchronized with the falling edge of the PWM input signal, edge which is in the middle point of the doubled PWM signal ON phase generated internally and used to drive the power MOSFET's. The signal flowchart is presented in the next Fig. 3.17.

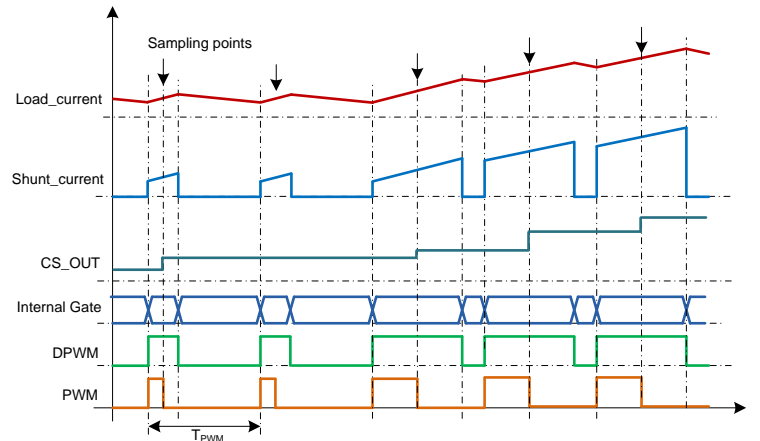


Fig. 3.17 S&H average current measurement synchronization procedure

The PWM generator unit should be capable of being configured into double PWM mode for average current measurement or for normal mode in which at the output PWM duty cycle is the same with the input PWM duty cycle, generated by the microcontroller, but the sampling of the load current shall still happen at the falling edge of the input PWM signal. With this mechanism the BLDC motor peak current is measured. This configuration is important for the initial position estimation methods implementation, based on peak current measurement, current generated by a voltage vector applied for a predefined time period (methods described in chapter 1.4 and 1.5).

Due to the fact that the actual current commutation at the motor terminals is delayed by the MOSFET's switching time. The ideal sample point presented in the Fig. 3.17 will be always before the middle point of the on phase of the current through the motor. To correct this problem the sample points shall be delayed with a pre-configurable delay time. Using the S&H\_DEL3..S&H\_DELO (Table 3.15) bits the sample point can be delayed with a predefined time period. This delay time shall be equal with the sum of the current switching and delay time through the power MOSFETs.

### 3.2.3 Diagnosis system of the ASIC

In all automotive applications, detection of fault conditions of the BLDC motor and the control electronics is mandatory. The control electronics must identify any fault conditions and then apply counter measures to protect the system and beyond, the automobile passengers. The detected fault condition is reported to the system microcontroller and it is accessible via the diagnosis interface of the automobile for further service investigations [19].

For a typical advanced automotive application the following diagnoses of the BLDC motor and control system are required:

- Short circuit to GND (SCG) at U, V or W;
- Short circuit to battery (SCB) at U, V or W;
- Short of the load (SCL);
- Open Load (OL);

- Weak short circuit (WSC);
- Supply voltages monitoring (battery supply, logic supply, ASIC internal charge pump over and under voltage failure condition detection);
- ASIC internal logic clock;
- HALL sensors;
- BLDC controller power MOSFET bridge and ASIC over temperature;

The diagnosis block is a subpart of this ASIC dealing with the fault condition detection only. Fig. 3.18 presents the block diagram of the proposed ASIC with focus on the diagnosis functions. These diagnosis functions are combined methods based on the existing state of the art technology in BLDC motor control ASIC's [137]-[146], [158]-[160] and new diagnosis methods-circuits introduced by the author, presented in several papers [6], [7].

According to Fig. 3.18 the proposed BLDC motor controller ASIC includes the following diagnosis units:

- BLDC motor ON state monitoring;
  - Short detection units;
  - Load current monitoring;
- BLDC motor Off state monitoring;
- Supply voltages supervising;
- Hall signal error detection;
- Internal clock monitoring;
- Over-temperature sensing;

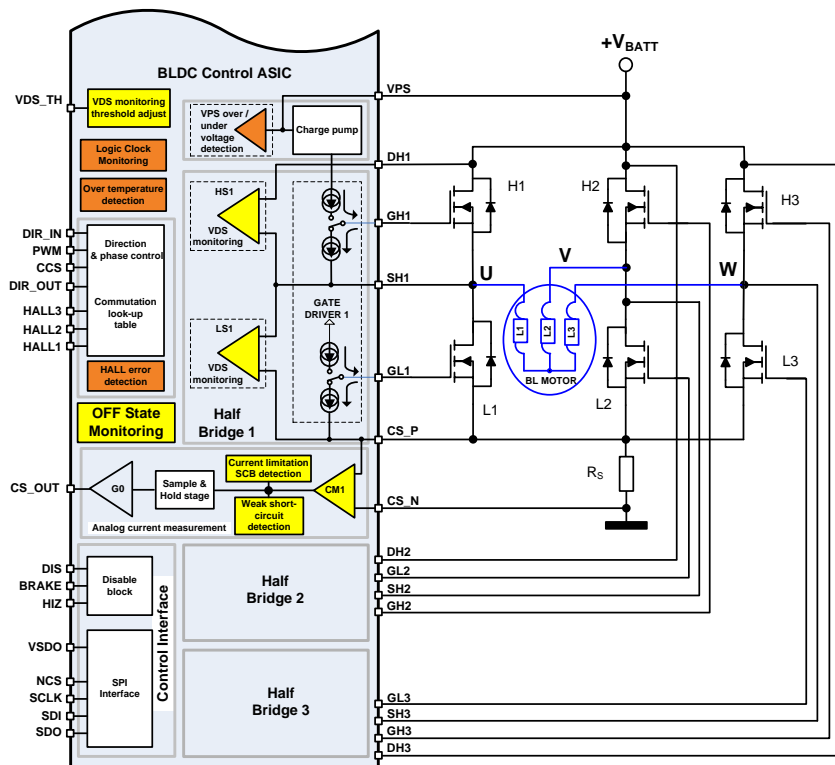


Fig. 3.18 BLDC motor control ASIC diagnosis units



For the BLDC motor monitoring itself, two monitoring modules are implemented. One is active during the BLDC motor operation, module called "ON State Monitoring" (OSM) and the other is active when the BLDC motor is OFF and the control bridge is deactivated, module named "OFF State Monitoring" (OFSM). The next three subchapters (3.2.3.1, 3.2.3.2 and 3.2.3.3) present the proposed implementation for these two units.

**3.2.3.1 BLDC motor ON state diagnosis unit**

During the motor operation, for automotive applications the detection of short conditions is mandatory. There are several short circuit conditions which must be considered (SCB, SCG, SCL and WSC), each of them being detected using different methods as described in the next sections.

**A. Short to ground (SCG) detection mechanism during ON-State**

Short circuits to GND conditions are detected monitoring the voltage drop across the high side MOSFET drain to source terminals (the classic  $V_{DS}$  monitoring) [143]. Fig. 3.19 presents the short circuit current path and the detection mechanism. The voltage drop across the high side MOSFET drain to source is applied to a voltage reference shifter, which provides the HS (High Side)  $V_{DS}$  drop voltage regarded to GND, then this voltage is compared to a threshold voltage ( $V_{DS\_TH}$ ) using a comparator circuitry. In case the MOSFET  $V_{DS}$  voltage exceeds this threshold the short condition is detected and the default reaction of the ASIC is to shut down the power MOSFET's to avoid further damage to the system due to the high short current. The SCG detection current threshold can be expressed as follows:

$$I_{SC} \geq \frac{V_{DS\_TH}}{R_{DS\_ON}} \quad (3.2)$$

- where with  $I_{SC}$  denoting the short detection threshold,  $V_{DS\_TH}$  the comparator input threshold voltage and  $R_{DS\_ON}$  the MOSFET drain to source ON resistance.

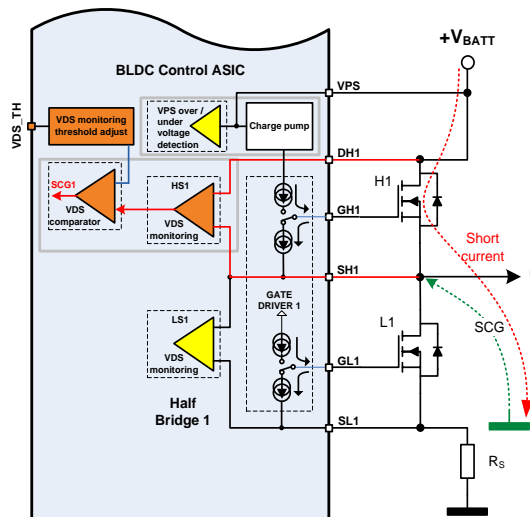


Fig. 3.19 SCG detection method

\*with red color the failure detection circuit blocks are highlighted

The disadvantage of this method is that the  $R_{DS\_ON}$  of a MOSFET has a very large dependency on various parameters as the gate voltage  $V_{GS}$ , drain current and operating temperature etc. Having high enough gate voltage which ensures the full open of the MOSFET the  $R_{DS\_ON}$  is mainly temperature and initial tolerance dependent. It changes from 0,75 (at  $-40^{\circ}\text{C}$ ) to 1,8 (at  $+175^{\circ}\text{C}$ ) normalized value of the  $R_{DS\_ON}$  referenced to  $25^{\circ}\text{C}$  [147][148]. According to eq. (3.2) the short detection threshold will also change, Fig. 3.20 presents the normalized short detection threshold over temperature (considering the  $R_{DS\_ON}$  tolerance and 2% tolerance for the detection reference voltage accuracy) where it can be seen that the detection threshold decreases with the increase of the MOSFET die temperature due to the increase of its  $R_{DS\_ON}$ . To cope with this issue the short detection threshold current should be calculated for  $R_{DS\_ON}$  of the MOSFET at high temperatures. In case we have a SCG condition combined with low die temperature, we can have the situation that the actual short current does not exceeds the short detection threshold due to the low  $R_{DS\_ON}$ . However the short current will cause the MOSFET die temperature to increase due to the increased power dissipation then the  $R_{DS\_ON}$  and  $V_{DS}$  voltage will exceed the SCG detection threshold and the failure will be detected.

The second and third half bridges are protected with the same concept, therefore the circuit is implemented three times inside the ASIC.

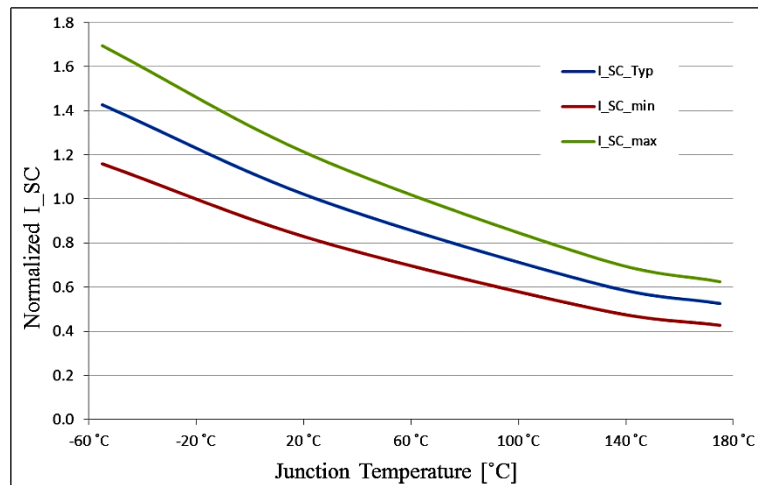


Fig. 3.20 Normalized VDS monitoring threshold over temperature

### B. Short to Battery (SCB) detection mechanism during ON-state

There are two possible ways to detect SCB (Short Circuit to Battery) conditions based on the block schematic presented in Fig. 3.18.

The first method is by using the  $V_{DS}$  monitoring of the low side (LS) MOSFETs, similar to the HS MOSFET  $V_{DS}$  monitoring for SCG condition detection (concept presented in Fig. 3.21). The LS (Low Side)  $V_{DS}$  monitoring suffers the same temperature and tolerance limitation as the HS  $V_{DS}$  monitoring.

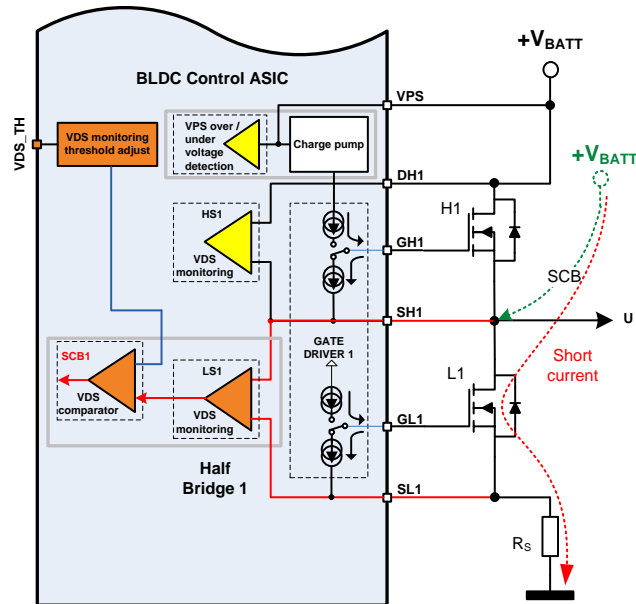


Fig. 3.21 SCB detection method using VDS monitoring of LS MOSFET's

In case of SCB conditions another more accurate detection method can be also applied, using the drop voltage on the current measurement shunt resistor. This SCB failure detection concept is presented in Fig. 3.22. The voltage across the shunt resistor is applied to a repeater amplifier with differential input (to eliminate any internal ASIC GND and external GND shift effect), the output voltage of this is then compared to a threshold voltage ( $SCB\_TH$ ). In case the drop voltage on the shunt exceeds the  $SCB\_TH$  failure condition is detected and the ASIC default reaction is to disable all the power MOSFET's and signal the error to the system microcontroller. The SCB detection threshold of this concept is much more accurate, it depends only on the tolerance of the shunt resistor, the comparator and its threshold voltage, as expressed in the following equation:

$$I_{SCB} \geq \frac{SCB\_TH}{R_S} \quad (3.3)$$

- where with  $I_{SCB}$  denoting the short detection threshold,  $R_{DS\_ON}$  the MOSFET drain to source ON resistance and  $R_S$  the shunt resistance.

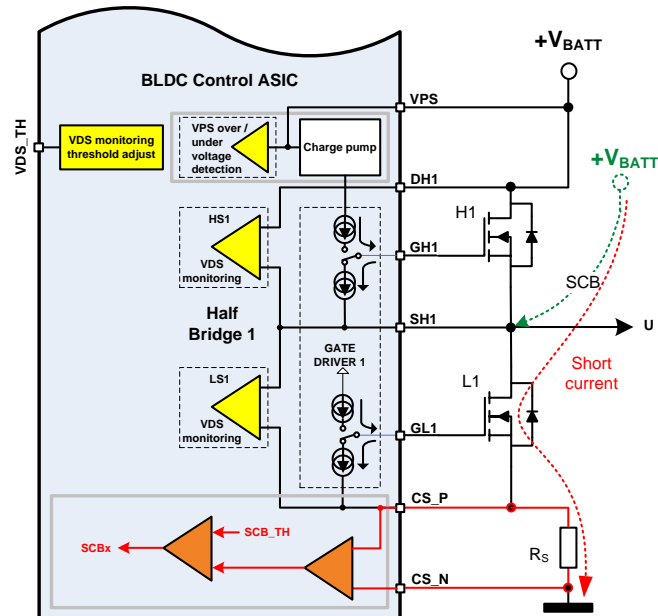


Fig. 3.22 SCB detection method using the current measurement path

Another advantage of this concept is that it needs to be implemented only once. The discrimination between SCB\_U (Short to battery at phase U of the motor), SCG\_V or SCB\_W is done knowing the active LS MOSFET in the moment of the failure.

An advanced BLDC motor driver ASIC shall contain both SCB detection circuits to increase its versatility, since not all of the applications require the BLDC current measurement. In applications where the BLDC motor current measurement is implemented, the active SCB failure detection mechanism shall be based on the current measurement path, due its better detection threshold accuracy.

### C. Short of the load (SCL) detection mechanism during ON-State

In SCL condition, the current flow among a HS and a LS MOSFET, from different half bridges. Fig. 3.23 presents an example SCL between U and V phases and the implied detection circuit block schematic. The short circuit causes high drop voltage on both H1 and L2 MOSFET'S triggering the short detection by their  $V_{DS}$  monitoring circuits, resulting SCG\_U and SCB\_V to be detected in the same time. The error signals are fed into an AND logic circuit which indicates the SCL condition. In the same manner shorts between V-W and U-W phases are detected. The default reaction of the ASIC would be to disable all the output MOSFET'S and report the error to the system microcontroller.

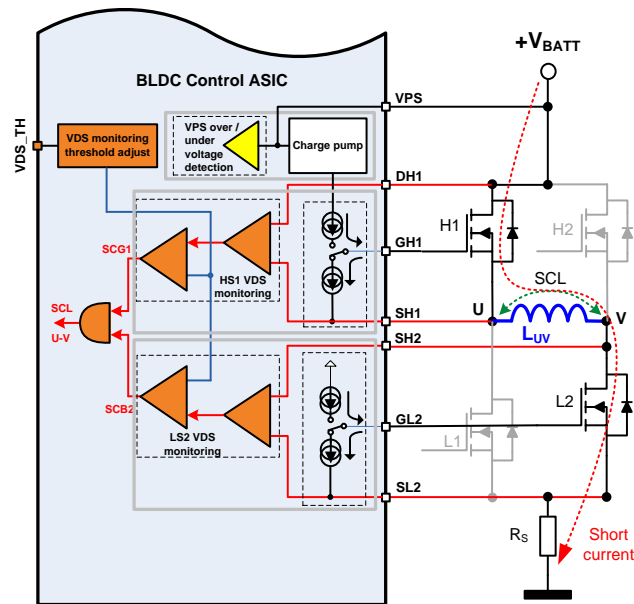


Fig. 3.23 SCL detection method using VDS monitoring

The main drawback of this classic method is the fact that the actual short circuit current detection is very dependent on the MOSFET die temperature as shown in Fig. 3.20. It has been demonstrated that the bridge MOSFET's has no equal power dissipation, resulting a different die temperature of the MOSFET's [4]. In a real application the thermal resistance to the cooling area may not be equal for all six MOSFET's, contributing to the die temperature differences. So there are short conditions in which only a SCB or SCG is detected because the other MOSFET die temperature is lower and its  $V_{DS}$  monitoring circuit needs a higher short current to detect the failure.

In the next subchapter 3.2.3.3 a combined ON and OFF state monitoring solution for the SCL detection method is proposed, which overcome these limitations.

#### D. Weak short circuit (WSC) detection mechanism during ON-State

For an advanced automotive BLDC motor application it is very important to have a weak short circuit detection mechanism. The intention of this WSC detection is the detection of leakage currents which are in the normal operating range of the motor current which are not detectable by the  $V_{DS}$  monitoring or current measurement units.

In normal operation having one shunt current measurement in the DC line, as presented in Fig. 3.18, the freewheeling current during the OFF phase of the control PWM flows via two LS or via two HS MOSFET's. Fig. 3.24 c) presents the current path during OFF phase (freewheeling) of the PWM, phase U and V are activated, phase W is in high impedance [16]. During the freewheeling period no current flows via the shunt resistor  $R_s$ , therefore any current flow, must come from a weak short circuit (WSC). The detection threshold can be set actually much lower than the maximum nominal load current of the BLDC motor itself. In a practical application the WSC detection threshold is set to around 10% of the maximum nominal motor

current. The failure detection method block circuit is similar with the one presented in Fig. 3.22 with the different threshold voltage ( $WSC\_TH$  instead of  $SCB\_TH$ ). Actually this WSC detection circuit can be combined with the SCB detection circuit using the same comparator circuitry with a multiplexed threshold voltage. During ON phase of the PWM the circuit threshold voltage should be  $SCB\_TH$ , detecting SCB failure conditions and during the OFF phase of the PWM,  $WSC\_TH$ , detecting WSC failure conditions. Therefore the WSC detection threshold can be expressed as follows:

$$I_{WSC} \geq \frac{WSC\_TH}{R_S} \quad (3.4)$$

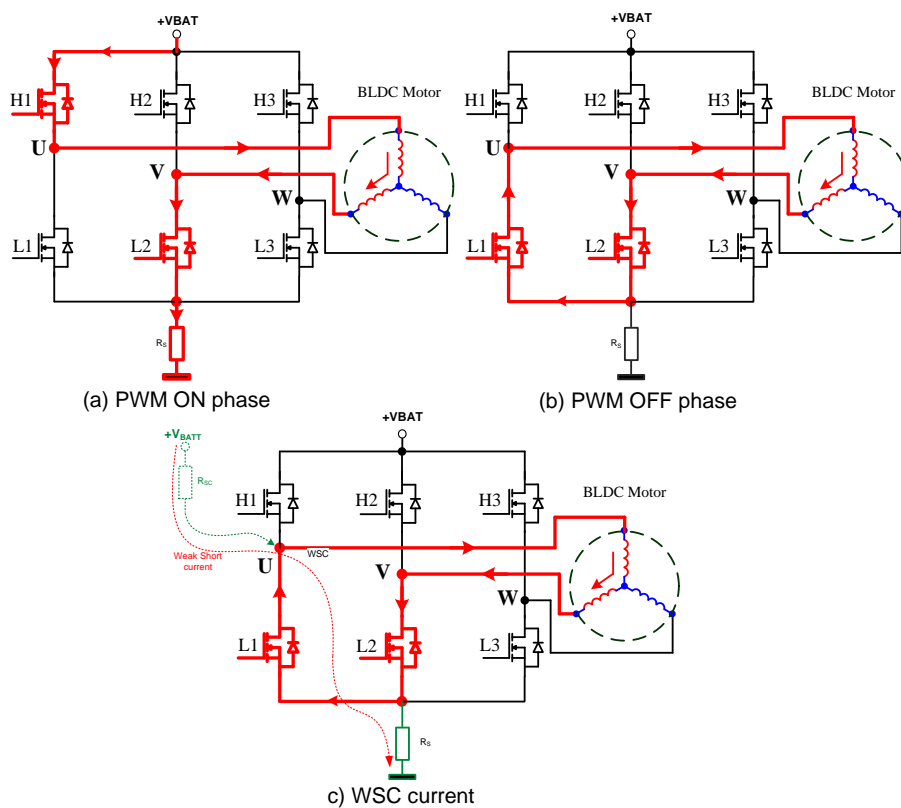


Fig. 3.24 Weak short circuit current path

As a minus of this method is that the WSC to GND is not possible to detect and also not possible to identify exactly at which output the failure has occurred.

### 3.2.3.2 BLDC motor OFF-state diagnosis unit

#### A. OFF state monitoring concept proposal

When the motor is inactive, the bridge outputs have to be monitored to avoid the starting of the bridge in case of failure conditions, which may lead to malfunction of the system or even permanent damage.

With the proposed OFF state monitoring concept SCG, SCB and OL failure conditions are possible to detect.

The OFF-state monitoring mechanism block diagram is presented in Fig. 3.25. The circuit consists of current source at V phase output and pull down resistances at U and W phases. The resulted voltage at the phase terminals are compared to two thresholds, one for SCB and second for SCG condition detection. The circuit shall be active only during OFF phase of the bridge when all MOSFET's are turned OFF, the activation is done closing sw1, sw2 and sw3 switches. The diodes in the concept schematics are protecting the internal circuits against shorts to voltages above Vint or below GND.

In normal mode when the BLDC motor (in star connection) is connected to the bridge outputs its internal low resistance shortens all the three terminals together resulting the same voltage at each of the phases set by the current source and pull down resistances. The equivalent circuit is presented in Fig. 3.26. The resulting voltage at the phase terminals will be (ignoring the motor windings low resistance):

$$V_{U\_OSM} = V_{V\_OSM} = V_{W\_OSM} = \frac{R_{OSM} \cdot I_{OSM}}{2} + V_D \quad (3.5)$$

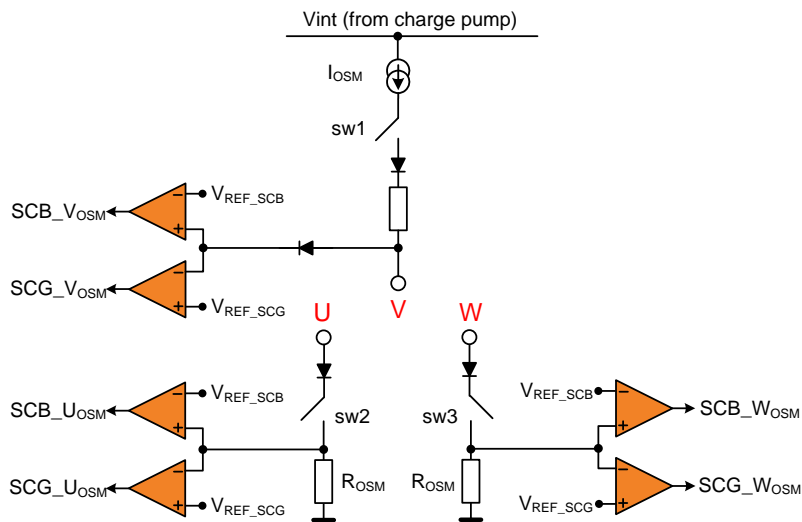


Fig. 3.25 OFF state monitoring circuit concept

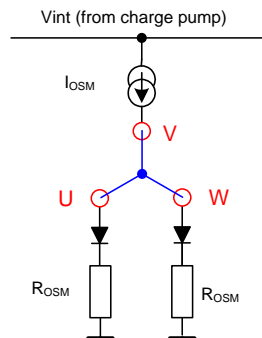


Fig. 3.26 OFF state monitoring equivalent circuit with BLDC motor connected

For a 12V battery voltage automotive application this voltage is set around 3,5V. The SCB threshold voltage ( $V_{REF\_SCB}$ ) has to be over this value (e.g. 4,5V) and the SCG detection threshold ( $V_{REF\_SCG}$ ) has to be below this value (e.g. 2,5V) having around 1V headroom for the short detection. When a SCB at one of the phases occurs all the phase voltages will be equal with the battery voltage, triggering a  $SCB\_X_{OFSM}$  to be detected at each output. In case of SCG conditions all the phase terminals will be at GND level triggering a  $SCG\_X_{OSM}$  to be detected at each of the outputs. In case of open load (OL) condition the motor windings will not shorten all three phases ending up with SCG detection at one phase and SCB at the other phase. Table 3.2 summarizes the OSM diagnosis result according to the failure indication.

Table 3.2 OFF state monitoring diagnosis interpretation

Nr.	Failure	Final OFSM diagnosis
1	$SCB\_U_{OFSM}$ $SCB\_V_{OFSM}$ $SCB\_W_{OFSM}$	SCB at one of the phases
2	$SCG\_U_{OFSM}$ $SCG\_V_{OFSM}$ $SCG\_W_{OFSM}$	SCG at one of the phases
3	$SCG\_U_{OFSM}$ $SCB\_V_{OFSM}$ $SCB\_W_{OFSM}$	Open Load at U phase
4	$SCG\_U_{OFSM}$ $SCB\_V_{OFSM}$ $SCG\_W_{OFSM}$	Open Load at V phase
5	$SCB\_U_{OFSM}$ $SCB\_V_{OFSM}$ $SCG\_W_{OFSM}$	Open Load at W phase

### B. OFF state monitoring circuit proposal and simulation

The simulation results (performed using OrCad PSpice v16.0) for the OFSM circuit based on the concept presented in Fig. 3.25 are shown in Fig. 3.27, having the circuit parameters:  $I_{OSM} = 1\text{mA}$ ;  $R_{OSM} = 7\text{k}\Omega$  (R6 and R9);  $V_{int} = 10\text{V}$ ;  $V_{REF\_SCB} = 4,5\text{V}$ ;  $V_{REF\_SCG} = 2,5\text{V}$ ;  $V_d = 0,5\text{V}$ . The schematic of the used circuit for the simulations is presented in Fig. 3.27. The simulation results are presented in Fig. 3.28 where the failures are applied consecutively with a short time difference between. First open load conditions has been generated at phase U, V and then phase W followed by a SCG and SCB failure condition applied to phase U.

The circuit used for the OL failure condition generation is presented in Fig. 3.29 only for phase U for the other phases the circuit is identical, L1 and R13 simulates the U phase winding connected in star configuration with the other two phase windings. It uses relay switches controlled by pulse generators with different pulse delay times. Fig. 3.30 presents the short to ground and short to battery simulation circuit used in the simulations. The figure presents only for one phase U, for the other two phases the implemented circuit is the same.



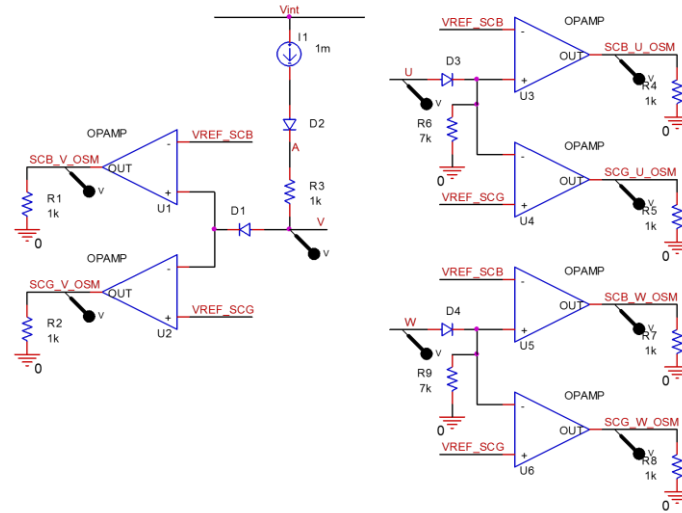


Fig. 3.27 OFF state monitoring circuit use in simulations

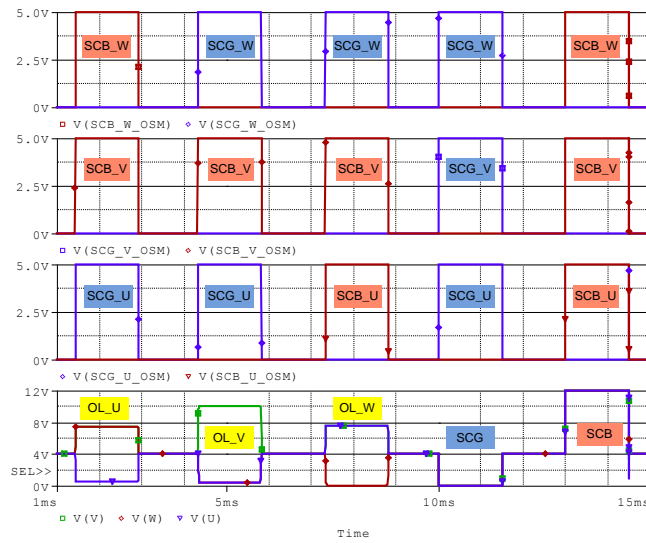


Fig. 3.28 OFF state monitoring (OSM) circuit simulation results

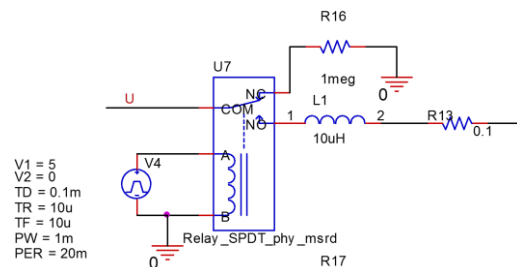


Fig. 3.29 Open Load (OL) failure simulation circuit

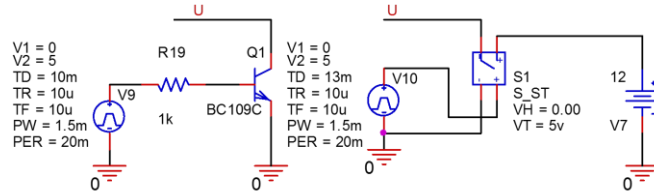


Fig. 3.30 Short to ground and battery simulation circuits

**3.2.3.3 OFF and ON state motor diagnosis combined interpretation**

As it can be observed none of the above described monitoring methods (ON and OFF state) can provide a full diagnosis of the BLDC motor. Combining the results from the two monitoring blocks we can have a much complete diagnosis. Fig. 3.31 presents the flow chart of the diagnosis using the two monitoring concepts.

Table 3.3 summarizes the fault conditions and the final diagnosis combining the results from ONSM and OFSM.

In the final concept the failures shall be identified using Table 3.3 and the default reaction of the ASIC has to be the disabling of the motor control (by turning OFF all power MOSFET's of the bridge) and reporting the failure via the communication interface to the system microcontroller. The failure register shall have 23 latched bits, to store the diagnosis result of the BLDC motor. The re-enabling of the bridge after the failure has been removed and must be conditioned to an error read and erase command.

The combination of the already existing and proposed diagnosis methods delivers a much comprehensive diagnosis report compared to existing solutions and implementations.

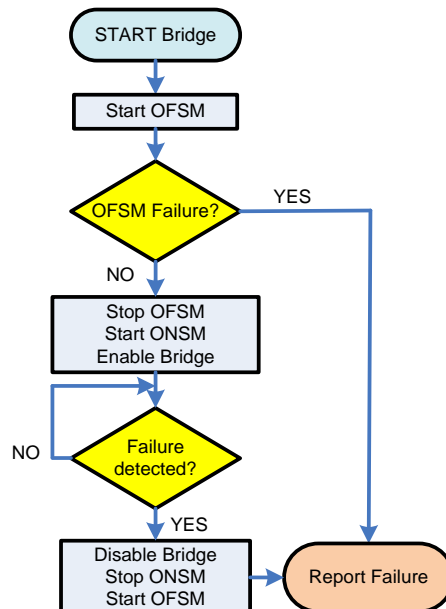


Fig. 3.31 Diagnosis flow chart

Table 3.3 ONSM + OFSM diagnosis interpretation

Nr.	ONSM	OFSM	Final diagnosis	Comments
1	SCB_U	SCB_U <sub>OFSM</sub> SCB_V <sub>OFSM</sub> SCB_W <sub>OFSM</sub>	SCB_U	short to battery at phase U.
2	SCB_V	SCB_U <sub>OFSM</sub> SCB_V <sub>OFSM</sub> SCB_W <sub>OFSM</sub>	SCB_V	short to battery at phase V.
3	SCB_W	SCB_U <sub>OFSM</sub> SCB_V <sub>OFSM</sub> SCB_W <sub>OFSM</sub>	SCB_W	short to battery at phase W.
4	SCG_U	SCG_U <sub>OFSM</sub> SCG_V <sub>OFSM</sub> SCG_W <sub>OFSM</sub>	SCG_U	short to GND at phase U.
5	SCG_V	SCG_U <sub>OFSM</sub> SCG_V <sub>OFSM</sub> SCG_W <sub>OFSM</sub>	SCG_V	short to GND at phase V.
6	SCG_W	SCG_U <sub>OFSM</sub> SCG_V <sub>OFSM</sub> SCG_W <sub>OFSM</sub>	SCG_W	short to GND at phase W.
7	WSC	SCB_U <sub>OFSM</sub> SCB_V <sub>OFSM</sub> SCB_W <sub>OFSM</sub>	WSC	to battery at one of the phases
8	SCB_U	No failure	SCL_U	Load short at U phase
9	SCB_V	No failure	SCL_V	Load short at V phase
10	SCB_W	No failure	SCL_W	Load short at W phase
11	SCG_U	No failure	SCL_U	Load short at U phase
12	SCG_V	No failure	SCL_V	Load short at V phase
13	SCG_W	No failure	SCL_W	Load short at W phase
14	SCB_U SCG_V	No failure	SCL_UV	Load short between phases U and V
15	SCB_V SCG_U			
16	SCB_U SCG_W	No failure	SCL_UW	Load short between phases U and W
17	SCB_W SCG_U			
18	SCB_V SCG_W	No failure	SCL_VW	Load short between phases V and W
19	SCB_W SCG_V			
20	No failure	SCG_U <sub>OFSM</sub> SCB_V <sub>OFSM</sub> SCB_W <sub>OFSM</sub>	OL_U	Open Load at U phase
21	No failure	SCG_U <sub>OFSM</sub> SCB_V <sub>OFSM</sub> SCG_W <sub>OFSM</sub>	OL_V	Open Load at V phase
23	No failure	SCB_U <sub>OFSM</sub> SCB_V <sub>OFSM</sub> SCG_W <sub>OFSM</sub>	OL_W	Open Load at W phase

#### 3.2.3.4 Brushless motor hall signals monitoring unit

To drive BLDC motors, using three phased inverter rotor position information is needed. This can be achieved using rotor position sensors [208]-[211], so called

sensored drive and sensorless estimating the rotor position evaluating the phase voltages and currents. In sensored drive mode in most of the applications hall sensors are used. The most common BLDC drive implementation is the six step, or 120° electrical commutation method which requires three hall sensor units. The displacement of these hall sensors is presented in Fig. 1.18. The three hall cells generate digital signal which represents the rotor electrical position with a 60° electrical resolution. The position is encoded using grey code as presented in Fig. 3.32.

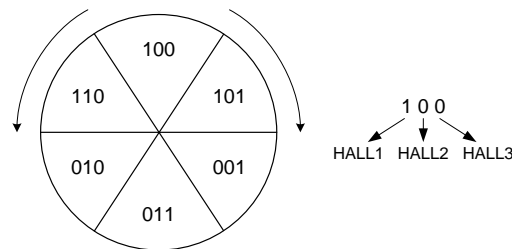


Fig. 3.32 Six commutation steps grey code

Without correct hall signals the BLDC motor cannot be driven correctly. Therefore it is a necessity to detect failure conditions of these hall signals and eventually correct them [149], [150], [208]-[210].

There are several failure conditions which can be detected using very simple principles:

- Hall pattern error;
- Hall sequence error;
- Hall jitter failure detection and filtering;

In addition to the above presented failure condition detection the hall sensors supply voltages are also mandatory to be supervised. This can be achieved using a circuit based on the battery voltage monitoring concept presented in the next subchapter, or by simple software monitoring measuring the hall supply voltage via the system microcontroller ADC converter.

### 3.2.3.5 Hall signals pattern error detection method

The encoding of the six steps of the 120° electrical commutation method is done using grey code as shown in Table 3.4. Having three halls sensors eight position combination can be encoded, two of these combinations '000' and '111' are not used for position encoding, these are invalid combinations. In case the control electronics detects that all hall sensors are stuck to '111' or '000' it considers it as hall pattern error.

Table 3.4 Six step block commutation encoding

HALL1	HALL2	HALL3	Sequence
0	0	0	<b>Invalid!</b>
1	0	0	Sequence 1
1	0	1	Sequence 2
0	0	1	Sequence 3
0	1	1	Sequence 4
0	1	0	Sequence 5
1	1	0	Sequence 6
1	1	1	<b>Invalid!</b>

This failure is frequently caused by the missing power supply of the hall cells or if one or more of the hall cells are damaged. For example if one hall cell is damaged and is stuck at one level (0 or 1 logic) there are combinations of the hall pattern when the other two hall cells are at the same level as the damaged hall cell causing a hall pattern error to be detected.

The detection concept is very simple, Fig. 3.33 presents the basic implementation circuit for the hall pattern error detection. It uses two logic gates, AND respectively a NAND gate with three inputs. The outputs of these are fed into an OR circuit who's output is connected to a latching circuit. This latching circuit then provides the hall pattern failure signal "FLBL\_PAT". The error flag is maintained until the D Latch circuit is cleared via the "CLR\_ERROR" signal. This mechanism ensures that the application software can detect also not permanent pattern failures of the hall signals.

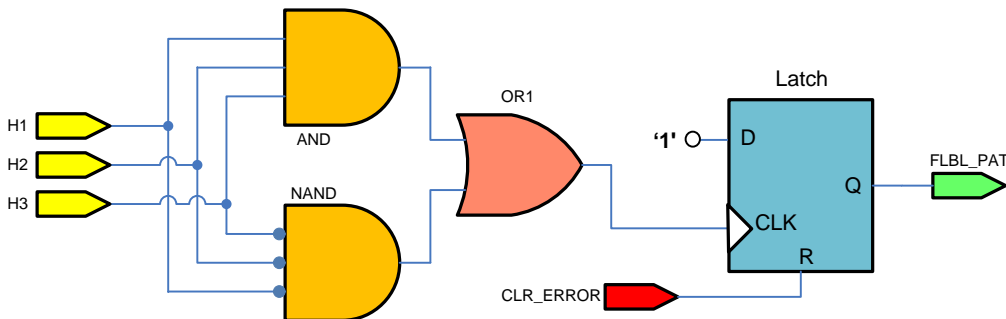


Fig. 3.33 Hall signals pattern error detection concept

**Pattern error detector implementation proposal and simulation results**

The hall signals pattern failure detection schematic circuit is presented in Fig. 3.34. A screenshot of the simulation result is presented in Fig. 3.35.

In the simulation we can observe that in the 2<sup>nd</sup> μs of the simulation all hall signals (H1, H2 and H3) are at '0' logic level consequently the circuit detects the failure and sets "LVL\_ERR\_OUT" signal to high logic level. The error is still kept by the output latch circuit until it is cleared by the "CLR\_LVL\_ERR" signal. The "CLR\_LVL\_ERR" signal is controlled by the system microcontroller. At the 8<sup>th</sup> μs time of the simulation all the hall signals are at high logic level '1', we can observe that the failure is detected by the circuit and afterwards is cleared by the "CLR\_LVL\_ERR" signal.

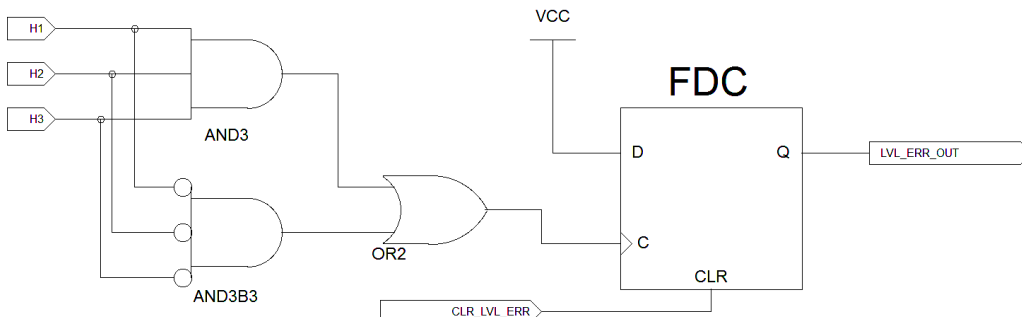


Fig. 3.34 Hall signals pattern failure detection circuit schematic

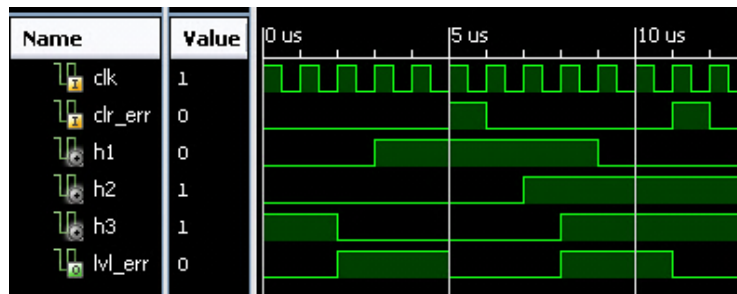


Fig. 3.35 Hall signals pattern failure detection circuit simulation results

### 3.2.3.6 Hall signals sequence error detection method

When the hall sequence pattern is not consistent with the previous step, hall sequence code, the failure must be detected in the control system. The grey code method ensures that from one hall sequence (pattern) to the next or previous only one hall signal changes its level. When two hall signal levels are changing in the same time or with a very short time difference between them, sequence error shall be detected.

The hall sequence error detection concept is presented in Fig. 3.36. It uses three transition detection units (TD1, TD2 and TD3) for each hall signal. These transition detector units generate a short pulse for each transitions of their input hall signal. The generated pulse width establishes the time interval in which two hall sensor changes is considered as sequence error. The outputs of these are fed into three AND circuits which will detect the combinations of simultaneous hall transitions, the outputs of these are fed into an OR circuit which provides the hall sequence error signal, which is stored by the latch circuit. The output of this latch provides the "FLBL\_SEQ" flag. If sequence failures occur, this latch keeps the error flag (FLBL\_SEQ) until cleared by the "CLR\_ERROR" signal.

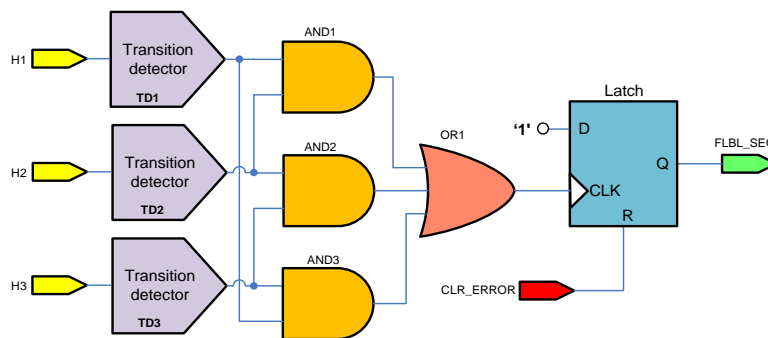


Fig. 3.36 Hall sequence error detection concept

Fig. 3.37 presents a signal flow diagram example of the hall sequence error detection circuit. During time interval  $t_1$  we have a transition at H1 hall signal, the TD1 transition detector generates a pulse with a predefined length  $t_p$  (see TD1\_OUT). During time interval  $t_2$  we see that the second hall signal H2 also has a transition, the TD2 transition detector generates the pulse (see TD2\_OUT), the two pulses do not overlap therefore no error is been detected. Now during time interval  $t_3$  there is a transition at both hall signals H1 and H2 with a very short time

difference between them, which leads to the transition detectors pulses to overlap, causing sequence error detection (FLBL\_SEQ signal). During t4 time interval the system microcontroller is reading the error after which it can clear it and restart the BLDC motor, or disable the system due to permanent failure of the Hall cells. The error is maintained by the output latch (from Fig. 3.36) till it is cleared via CLR\_ERROR signal, which is exemplified in Fig. 3.37 at the end of t4 time interval.

The hall sequence error mainly happens in case of short circuits between two hall signals, mostly caused by damage in the wiring harness of the BLDC motor or damage of the hall sensors itself.

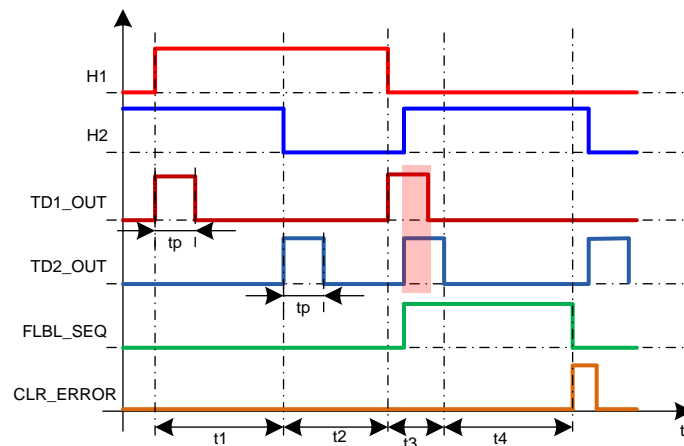


Fig. 3.37 Hall sequence error detection signal flow diagram

**Sequence error detector implementation proposal and simulation results**

The sequence error detection schematic circuit is presented in Fig. 3.38. A screenshot of the simulation results of the circuit is presented in Fig. 3.39.

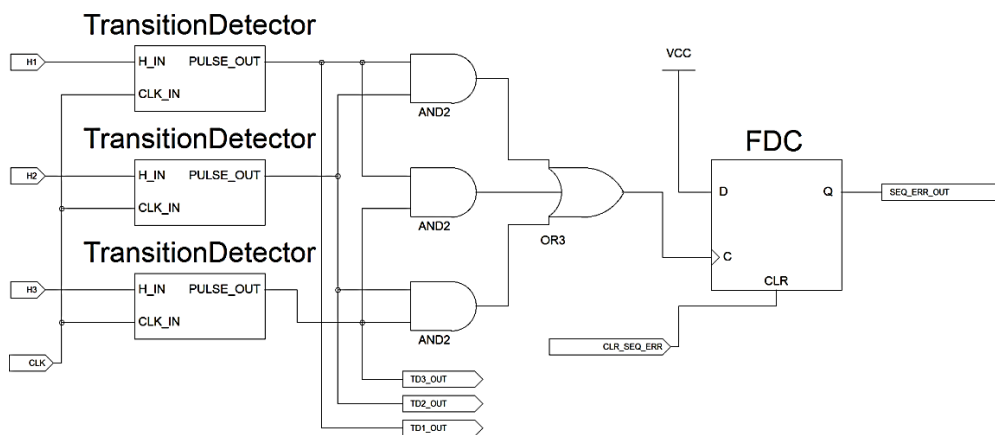


Fig. 3.38 Hall signals sequence failure detection circuit schematic

In the simulations we can observe that at every input hall signal transition (H1, H2 and H3) the corresponding transition detector (td1\_out, td2\_out and td3\_out) generates a predefined pulse equal with four clock cycles ("clk"). If the two pulses

overlap, as we can observe at 9 $\mu$ s time point, the sequence error is detected, "seq\_err" signal goes to high level. The error is generated because of the too close level change of H1 and H3 hall signals.

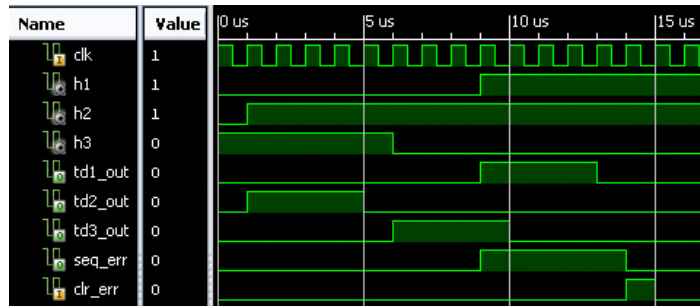


Fig. 3.39 Hall signals sequence failure detection circuit simulation results

The transition detector circuit is presented in Fig. 3.40. It is composed of two separate blocks one for rising and second for falling transition detection of the input hall signal. The transition detection is done via the input D latches, and the output pulse is generated using a four bit counter. When the counter reaches four, the counter is cleared and the output signal is toggled to '0' logic level. The generated pulse length can be adjusted by the max counter value at which the circuit is cleared. The hall input signal is applied to "H\_IN" input and the pulse is provided at "PULSE\_OUT" output.

The logic circuits clock frequency has been set to 1Mhz (CLK\_IN signal), therefore the actual sequence error detection time is 4 $\mu$ s. This timing is defined by the transition detector output pulse time. Different timing can be obtained by changing the time at which the transition detector is cleared.

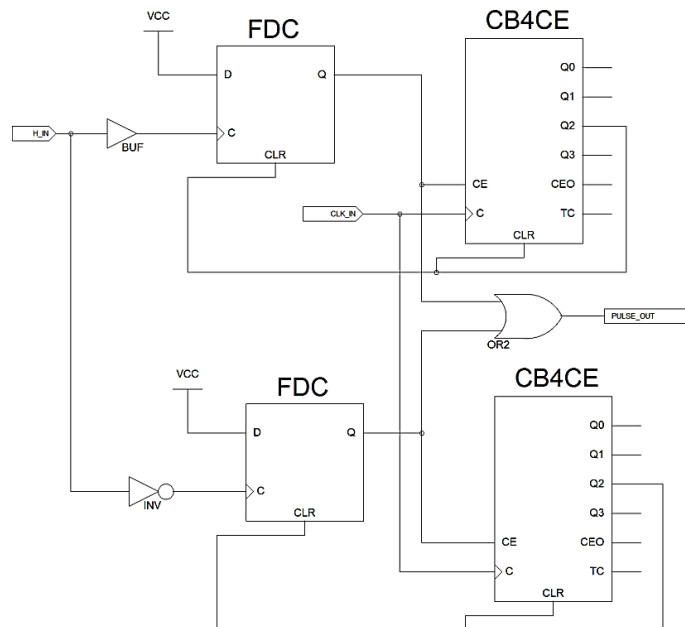


Fig. 3.40 Transition detector circuit schematic



### 3.2.3.7 Hall signals jitter detection and filtering method

A particular failure type of the hall sensors is the jitter, which causes instability of the hall signal level, constantly jumps from high to low level. In automotive systems there are several root causes for this jitter. One root cause is the small hysteresis of the hall sensor itself. In case the rotor is stopped exactly at the commutation points of the hall signals, due to EMC disturbances over the hall cell or mechanical vibrations the hall cell output can jitter between high and low level. Other possibilities are noises induced into the wiring harness of the hall sensor output signal, considering that the BLDC motor is connected to the electronic control unit via a wiring harness. All these negative effects can cause stall of the BLDC motor. Because of the fast change of one hall signal the output vector applied to the motor will constantly be changed, causing high mechanical vibrations and failure in the control system. For example the HALL signal is used to determine the actual speed of the motor. In case we have jitter on the hall signals the control algorithm will sense a higher speed than the actual motor speed. A hardware or software filtering of these jitter via a low pass filter is not possible because it will delay the actual switching of the hall signals which will lead to a late commutation of the phases ending up in decayed performance of the BLDC motor, which will generate less torque as proven in a paper elaborated by the author [5].

This section of the paper presents an innovated concept introduced by the author (patent pending) which is able to detect and filter the jitter of the hall cells without delaying the hall signals. The diagram of the proposed concept is presented in Fig. 3.41. The idea is based on two transition detectors of the input hall signal which generate a predefined pulse width. One of the transition detector TD1 is active only on raising edges and the second transition detector TD2 is active only on falling edges of the input hall signal.

When there is no transition detected the clock signal is fed into the first Latch1, this feeding the HALL\_IN signal to the HALL\_OUT. When transition occurs, the HALL\_OUT signal will load the HALL\_IN level and in the next moment the transition is detected and further load of the HALL\_OUT signal is prohibited until the transition detectors outputs are back to their initial low logic level. Therefore any input hall signal jitter during the transition detectors output pulse is filtered out by this mechanism. In case the input signal presents a jitter, positive and negative transitions will be detected. The output pulses of the two transition detectors will overlap loading into Latch2 a '1' logic level representing the jitter error (JIT\_ERR\_OUT). The JIT\_ERR\_OUT signal can be cleared via the CLR\_JIT\_ERR signal. The flowchart of the signals is presented in Fig. 3.42.

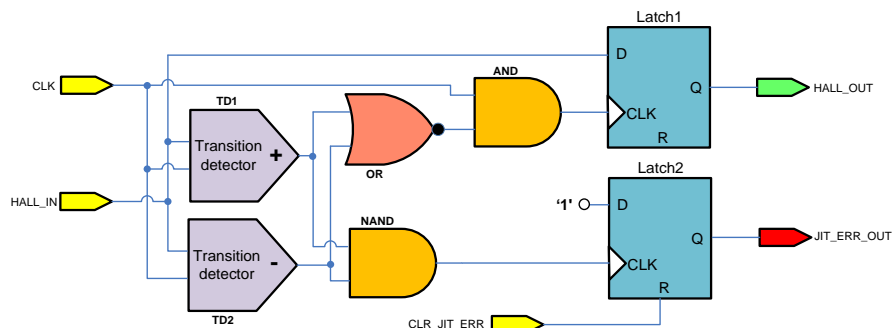


Fig. 3.41 Hall jitter error detection and filtering circuit

During  $t1$  period (of the signal flow from Fig. 3.42) we have a positive transition at the input hall signal which is immediately loaded at the HALL\_OUT signal and is also detected by the TD1 unit which generates the predefined pulse with pulse time  $tp$ . During time period  $t2$  we have a negative transition of the input hall signal which is loaded to the output and this time TD2 generates a pulse. The two pulses do not overlap, therefore the JIT\_ERR\_OUT signal stays at low level. During time interval  $t3$  there is a jitter present on the input hall signal, both transition detectors generate a pulse. The hall output Latch1 (HALL\_OUT) is loaded with the input hall signal level after the first transition, afterward the latch clock is disabled (see OR\_OUT signal in Fig. 3.42) until the input jitter disappears and the transition detectors outputs returns to '0' logic level (time interval  $t4$ ). At the beginning of  $t5$  the jitter failure indicator signal is cleared via the CLR\_JIT\_ERR signal provided by the system microcontroller.

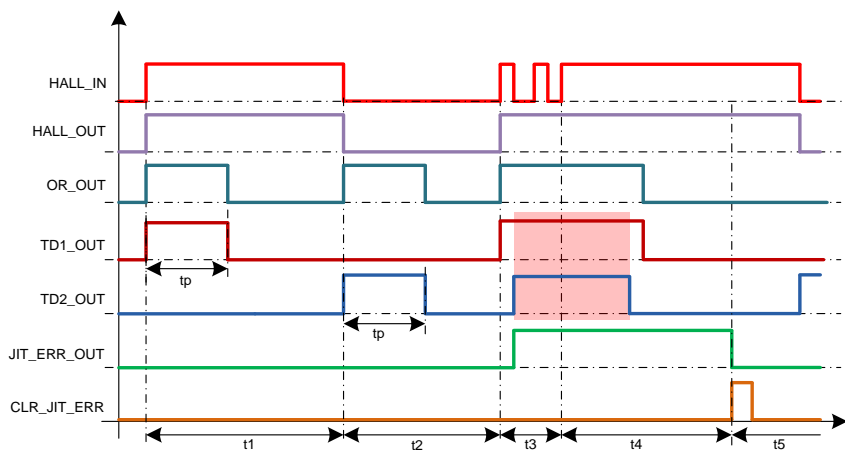


Fig. 3.42 Hall jitter filtering and detection signal flow

### ***Jitter error detector implementation proposal and simulation results***

The jitter error detection and filter implementation circuit is presented in Fig. 3.45. In the figure we can observe the transition detector circuits made with the input FDC latch circuits, the pulse time delay is generated using the two CB8CE counter circuits (one for each transition detector). The HALL\_OUT signal is loaded in the FD latch type, below which the jitter detection output latch (FDC type) is placed.

The simulation result of the implemented logic circuit is presented in Fig. 3.43. During the second microsecond of the simulation we have a rising transition at the hall input signal (hall\_in), which is reflected at the output (hall\_out) after one clock cycle. The transition detector TD1 active on rising edge of the input signal generates a pulse with a predefined time period of 20 clock pulses. At the 26<sup>th</sup> microsecond time of the simulation we have a falling edge at the hall\_in signal, which this time is detected by TD2 transition detector and reflected at the output signal (hall\_out). At the 49<sup>th</sup>  $\mu$ s time of the simulation we have a second rising edge of the input hall signal immediately followed by several other negative and positive transitions caused by jitter of the hall input signal. This case both transition detectors will have a pulse generated at the output which overlap, consequently jitter error is detected. As it can be seen the hall\_out signal reflects only the first rising transition level and is kept constant during the input signal disturbance proving the proposed filtering concept validity.

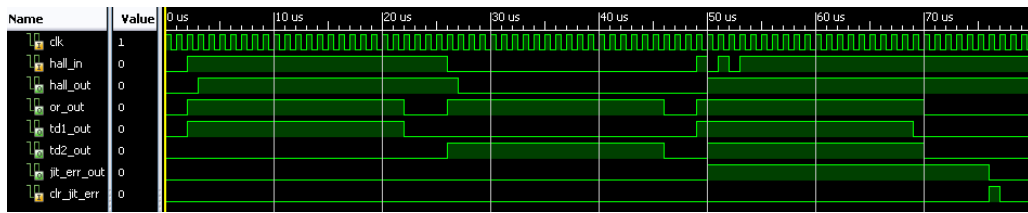


Fig. 3.43 Hall jitter detection and filtering circuit simulation result, jitter at rising edge

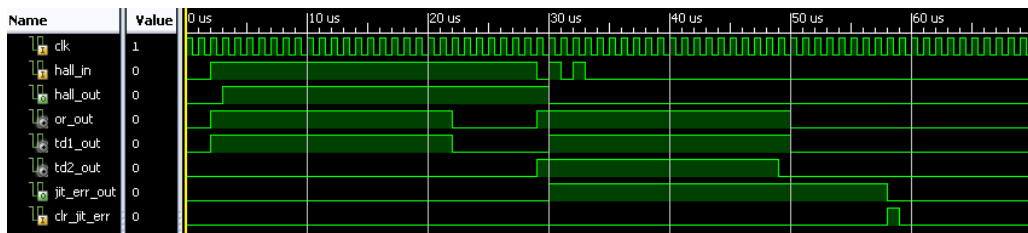


Fig. 3.44 Hall jitter detection and filtering circuit simulation result, jitter at falling edge

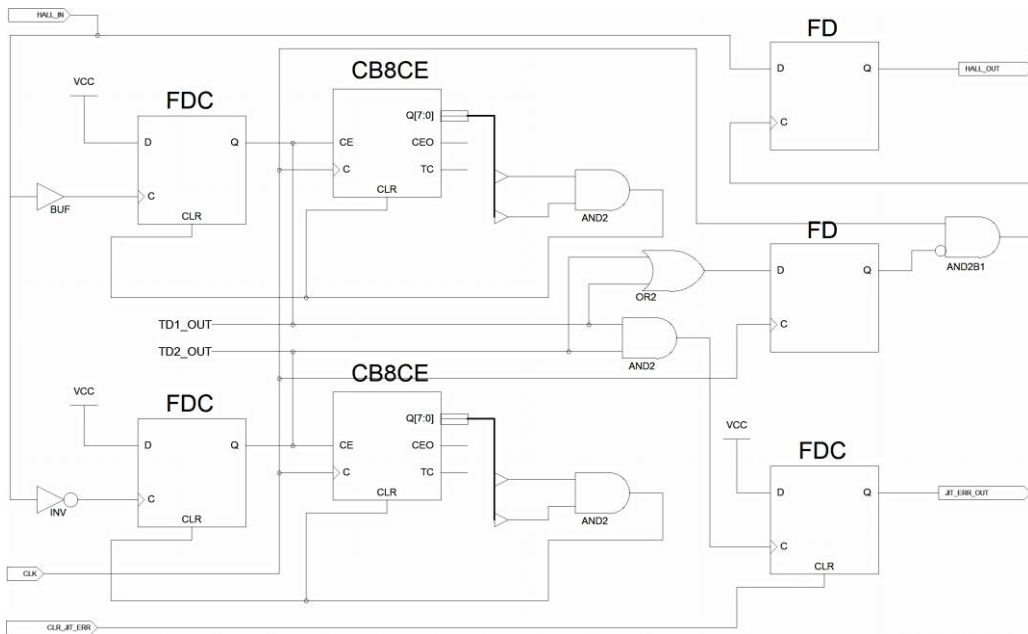


Fig. 3.45 Hall jitter detection and filtering logic schematic circuit

The output signal, hall\_out is delayed with one clock cycle which may influence the BLDC motor performance, nevertheless by using high enough input clock frequency for the circuit the delay will be insignificant.

To prove this fact, let's consider the following example: we have a BLDC motor with four pole pairs, and a clock frequency of the circuit about 20MHz. Having these inputs we can calculate the hall signals delay in electrical angles for different revolutions of the BLDC motor.

The time period of one clock cycle is the following:

$$t_{CLK} = \frac{1}{f_{CLK}} = \frac{1}{20 \cdot 10^6} = 50ns \quad (3.6)$$

With 50ns time delay, the electrical angle delay for a BLDC motor with four pole pairs at 5000RPM will be:

$$ElecDelay = f_{CLK} \cdot 360 \cdot \frac{RPM \cdot polpairs}{60} = 50 \cdot 10^{-9} \cdot 360 \cdot \frac{5000 \cdot 4}{60} = 0.006^\circ(\text{electrical}) \quad (3.7)$$

If we repeat the calculation at 10k RPM using a BLDC motor with six pole pairs the electrical delay would be 0.018° electrical degrees. In conclusion a 20MHz clock gives very low electrical angle delay without a noticeable decay of the BLDC motor performance. Note that typical hall sensors used in the BLDC motors has 1° electrical degree accuracy or even worse mainly due to mechanical positioning accuracy of the hall cells.

**3.2.3.8 Hall diagnosis circuits experimental setup**

All the above described hall diagnosis logic circuits has been implemented using a Xilinx Cool Runner II CPLD (Complex Programmable Logic Device) circuit XC2C256-TQ144 equipped on a Digilent X-board. The logic circuit design has been developed using Xilinx ISE WebPack v12.4 and simulated using Mentor Graphics ModelSim Xilinx edition III. The top level of the hall input signals diagnosis circuits is presented in the next Fig. 3.46.

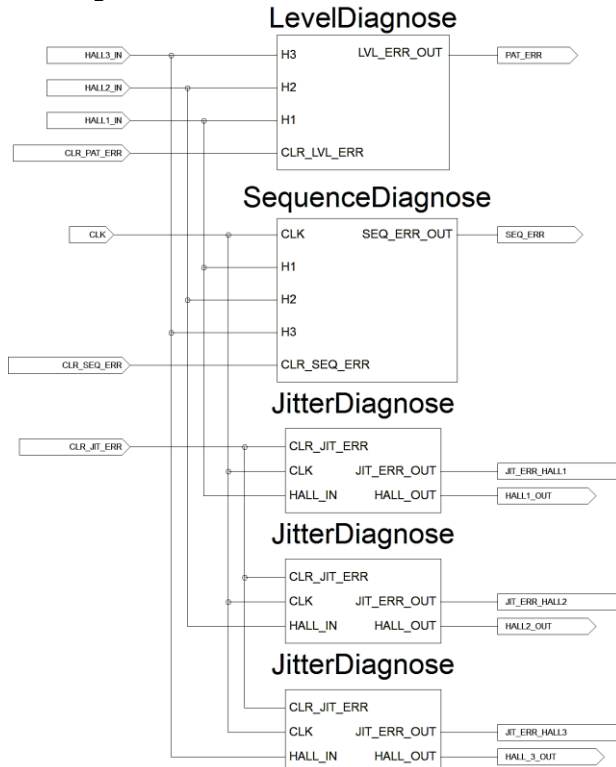


Fig. 3.46 Hall signals diagnose top level circuit

The circuit contains the pattern error detection block (LevelDiagnose), the sequence error detection unit (SequenceDiagnose) and the three jitter detection, filtering units (JitterDiagnose), one for each hall signal. The unit has as input signals the three hall sensor signals HALL1\_IN, HALL2\_IN and HALL3\_IN, the clock input CLK and the three error clear signals one for each error type. CLR\_PAT\_ERR is for the pattern error signal (PAT\_ERR) clear, CLR\_SEQ\_ERR for the sequence error output signal (SEQ\_ERR) and finally CLR\_JIT\_ERR for the jitter error output signals JIT\_ERR\_HALL1, JIT\_ERR\_HALL2 and JIT\_ERR\_HALL3. The jitter detection and filtering block provides at the output the jitter free hall signals HALL1\_OUT, HALL2\_OUT and HALL3\_OUT.

### **3.2.3.9 Diagnosis implementation of the BLDC motor driver ASIC**

A safe and correct operation of a system which employs a BLDC motor cannot be ensured only by monitoring the BLDC motor failures as presented in the last subchapters. The key functions and operating conditions of the BLDC motor controller ASIC must also be monitored.

In this subchapter the monitoring circuits of vital functions and operating conditions of the BLDC motor controller ASIC are presented, including:

- External and internal supply voltages monitoring units;
- The ASIC internal clock monitoring concept;
- Over-temperature condition detection units;

### **3.2.3.10 Battery voltage monitoring system**

The most important voltage in an automotive system is the battery supply voltage. Since this is the supply voltage of the BLDC motor control system it has to be monitored for over and under-voltage conditions. If the battery voltage is too low, the BLDC motor cannot be driven up to its full power, if it's below the logic supply voltage the motor controller ASIC is not able to drive the motor, therefore it is necessary to sense battery under-voltage conditions. In case the battery voltage is too high the BLDC motor can be driven over its rated power which can lead to destruction of the BLDC motor, or if the battery voltage exceeds the control circuit components maximum voltage ratings, it can lead to destruction (electrical overstress) of the control electronics. Detection of these failure conditions at the battery line can be provided using two comparators (as shown in Fig. 3.47), one for under-voltage and second for overvoltage monitoring. The battery voltage is fed into the two comparators via a voltage divider circuit realized with R1 and R2. The comparators outputs are fed into the enable logic of the bridge, disabling it in case the battery voltage is out of its limits.

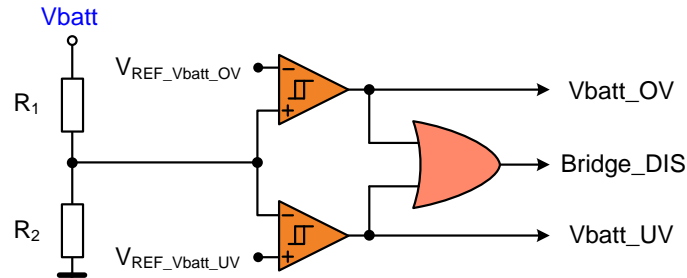


Fig. 3.47 Battery voltage monitoring circuit concept

Of course the battery over-voltage detection circuit cannot provide protection against very high voltages over the maximum ratings of the electronic circuits. This protection has to be done via external voltage limiter circuits or suppressor diodes which can protect the circuit for short over-voltages. This technique is very often used in the automotive applications, for load-dump protections [19].

#### **Simulation of the proposed circuit concept**

This section demonstrates using PSpice simulations the proper operation of the concept circuit proposed for the BLDC motor controller system voltages monitoring. The simulations are only presented for the battery voltage monitoring circuit the other logic supply and charge pump monitoring units having similar configuration with different failure detection threshold voltages (described in the next sections). The circuit used for the simulation is presented in Fig. 3.48.

Fig. 3.49 presents the time simulations results where the battery voltage has been raised from 0V to 30V. It can be clearly observed that in case of under or over voltage conditions the "Bridge\_DIS" signal is at high logic level. The circuit is designed to detect battery under-voltage below 6V and overvoltage over 27V.

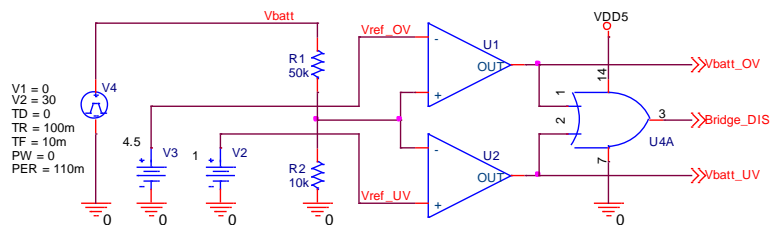


Fig. 3.48 Battery voltage monitoring circuit

The circuit is designed to be supplied from a typical 5V supply (the logic supply of the BLDC motor controller ASIC) therefore the battery voltage must be divided with a factor of six, divider realized with R1 and R2 (from Fig. 25). Therefore the resulting voltage references must also be divided with a factor of six to keep the reference and battery voltage ratio to one, resulting battery overvoltage detection threshold ( $V_{ref\_OV}$ ) of 4,5V and under-voltage detection threshold ( $V_{ref\_UV}$ ) of 1V.

In order to improve the stability of the comparator circuit, it can be designed with a small hysteresis which would prevent the failure indicator output to jitter due to noises at the input voltage.

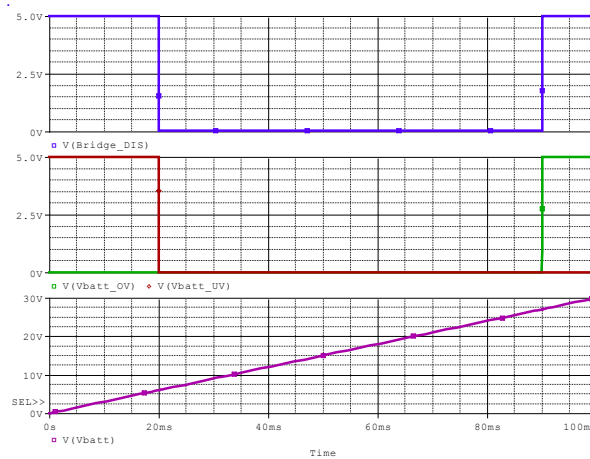


Fig. 3.49 Battery voltage monitoring circuit simulation results

### 3.2.3.11 Logic supply monitoring system

Almost all BLDC motor control ASIC's have at least two power supplies. One is the battery voltage and second is the low voltage logic supply. To ensure the correct operation of the BLDC motor controller ASIC this logic supply voltage must be between its limits. Therefore it is necessary to supervise this voltage and in case it is out of limits, the control of the BLDC motor shall be disabled.

The supervising circuit should be realized in the same way as the battery voltage supervisor circuit (Fig. 3.47) just with different over and under voltage detection thresholds according to the internal logic circuit operational voltage limits.

### 3.2.3.12 Charge pump output voltage monitoring system

This internal charge pump voltage as described in 3.2.1 is very important for a proper functioning of the bridge inverter, therefore any failure of it, under or over voltages must be sensed and the bridge shall be disabled to prevent further damage. The fault detection circuit is again very simple, it is similar with the battery voltage supervising circuit presented in Fig. 3.47 just with different threshold voltages.

### 3.2.3.13 Logic clock monitoring unit

All internal processes (e.g. dead time generator, SPI communication, failure detection filter times etc.) of an advanced BLDC motor driver ASIC are timed via the internal clock and PLL (Phase Locked Loop) module. In case this clock module time base fail all internal processes timing are compromised, therefore the BLDC motor cannot be controlled correctly. It can even cause damage to external components, as example if the internal clock goes to higher frequency, the dead time between HS and LS MOSFET switch (generated by the ASIC) will be shorten, causing their switching period to overlap which leads to high cross currents, damaging the power inverter. Therefore it is very important to make sure that this clock is in its limits. In case there is a PLL unit inside the ASIC, it must be guaranteed that the ASIC does not start up until the PLL is locked, in case it fails to lock than the ASIC shall remain disabled.

The detection of such failure cases is very easy to implement using a separate low frequency oscillator [153][167], than the main clock of the ASIC is compared to this low frequency oscillator clock. The comparison can be made using a simple frequency counter with the measurement period defined by the low frequency oscillator. In case one of the oscillators gets out of its limits, the measured frequency will also be out of limits and the failure can be detected by a simple digital comparator.

The block schematic of such a clock monitoring system is presented in Fig. 3.50. The two generated clock sources the "Main Clock" and the low frequency LF Oscillator outputs are fed into a counter circuit with the time base set by the low frequency oscillator. The resulted count number is then compared with two thresholds, "CLOCK\_MAX" and "CLOCK\_MIN". The outputs of these are set to one logic in case the number fed into the 'A' input is higher than the number fed into the 'B' input. The two outputs of the comparators are combined together using an OR circuit, at which output the "CLOCK\_FAIL" signal is provided.

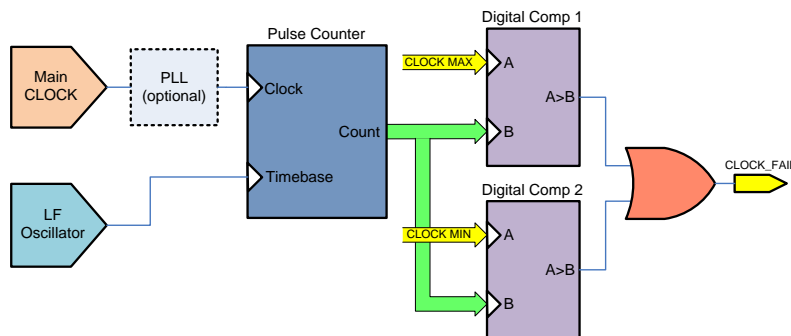


Fig. 3.50 Clock monitoring concept

### 3.2.3.14 ASIC over-temperature sensing

Over temperature conditions are damaging for any electronic systems. Therefore it's very important to detect and protect the BLDC motor control circuit in these conditions. Basically two temperature sensors are needed in the system. One for the power inverter MOSFET block and second, for the BLDC motor controller ASIC.

Solutions for these circuits exist in many applications and proposed in several papers. In this paper two example circuits are presented which fulfill the requirements of temperature monitoring of such BLDC motor control units designed for automotive applications.

The BLDC motor controller ASIC die temperature influences the correct operation of the system. Since there is no need to sense-it with high accuracy and disable the ASIC at a certain die temperature a very simple circuit proposal can be used, as presented in Fig. 3.51 [155], [156].



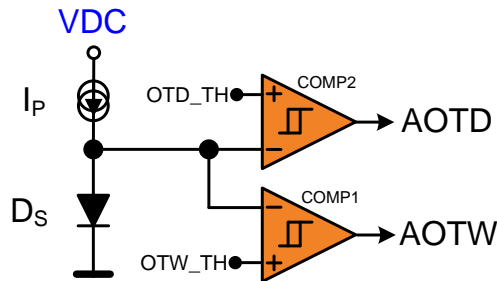


Fig. 3.51 ASIC over-temperature sensing circuit

The circuit is based on the forward voltage change over temperature of a diode  $D_S$  which is polarized via a constant current source  $I_p$ . The voltage drop on the diode is then compared with two temperature thresholds. The first comparator (COMP1) provides a warning signal, the ASIC chip temperature is very close to its maximum operating temperature indicated by the level of the AOTW (ASIC Over-temperature Warning) signal. The second comparator is for over-temperature detection with its threshold voltage defined by OT\_TH. The comparators shall be designed with a small hysteresis. The output of the second comparator COMP2 provides the over-temperature error signal (AOTD) which disables the ASIC.

### 3.2.3.15 Bridge over-temperature sensing

Depending on the application needs, the bridge temperature measurement can be done in several ways and it doesn't necessarily have to be implemented inside the BLDC controller ASIC.

The simplest way is to use a voltage divider circuit composed of a thermistor and a linear resistor as presented in Fig. 3.52. The output voltage will change over temperature, which is fed into the system microcontroller ADC (Analog to Digital Converter) input, then the microcontroller can calculate the bridge temperature and disable it in case of over-temperature conditions. The disadvantage of this method is that the accuracy of the temperature measurement is quite poor and may not fit to every application, nevertheless it's one of the cheapest solutions.

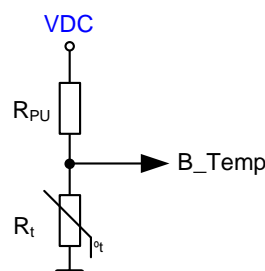


Fig. 3.52 Bridge temperature measurement using a thermistor

Another more accurate temperature measurement can be realized as example using digital temperature sensor as in [154], [157].

The above presented temperature protection method based on the microcontroller SW application has the drawback that the over-temperature protection can be compromised by failures of the microcontroller operation. To

overcome this drawback the BLDC controller ASIC should be equipped with a bridge over-temperature comparator circuit. The concept of this circuit is presented in Fig. 3.53.

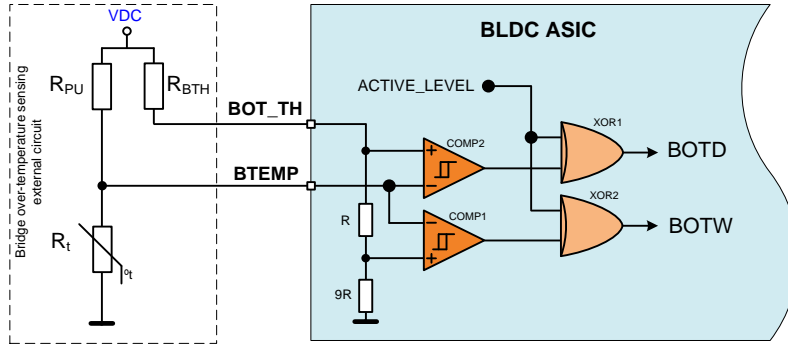


Fig. 3.53 Bridge over-temperature detector implementation, inside the BLDC ASIC

The bridge temperature monitoring is based on two comparator circuits, one for a warning temperature level and second for over-temperature detection. The circuit is designed in a way that the warning level detection threshold is 10% below the over-temperature detection threshold. The two thresholds are set by the external pull-up resistor value  $R_{BTH}$ . To make the circuit compatible with a large type of temperature sensors having positive or negative temperature coefficients, the over-temperature detection signals must have configurable active level. This active level selection is implemented using two XOR circuits (one for each comparator). The selection between over-temperature detection active high or low is selected by "ACTIVE\_LEVEL" signal.

**Proposed diagnosis units summary**

Table 3.5 presents a comparison between the most representatives BLDC motor control ASIC's and the proposed one in this thesis.

Table 3.5 BLDC motor driver ASIC's diagnostics comparison

Diagnose	MCZ33937	A4935	TMC603A	MTD6501	TLE7189	L6235	UC3625	ECN30207	TB6633	ATA6833	Proposed
	[137]	[138]	[140]	[142]	[143]	[145]	[146]	[158]	[159]	[160]	-
SCB	Yes	Yes	Yes	Yes	Yes	Yes	Yes	no	Yes	Yes	Yes
SCG	Yes	Yes	Yes	Yes	Yes	Yes	Yes	no	Yes	Yes	Yes
OL	Yes	no	no	no	no	no	no	no	no	no	Yes
SCL	no	Yes	no	no	no	Yes	no	no	no	no	Yes
WSC	no	no	no	no	no	no	no	no	no	no	Yes
Over-current	Yes	Yes	Yes	Yes	Yes	Yes	no	Yes	Yes	Yes	Yes
Vbatt OV	no	no	no	no	Yes	no	Yes	Yes	no	Yes	Yes
Vbatt UV	Yes	Yes	Yes	no	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Logic OV	no	no	no	no	Yes	no	no	no	no	no	Yes
Logic UV	Yes	Yes	no	no	Yes	no	Yes	no	no	no	Yes
CP OV	no	no	no	no	no	no	no	no	no	Yes	Yes
CP UV	no	Yes	Yes	no	Yes	no	no	no	no	Yes	Yes
Over Temp.	Yes	Yes	no	Yes	Yes	Yes	no	no	Yes	Yes	Yes
Hall Pattern	no	no	no	-*	no	no	no	no	-*	no	Yes
Hall Sequence	no	no	no	-*	no	no	no	no	-*	no	Yes
Hall Jitter	no	no	no	-*	no	no	no	no	-*	no	Yes
Logic clock	no	no	no	no	no	no	no	no	no	no	Yes

\*sensorless BLDC motor driver ASIC therefore does not require hall sensors.

### 3.2.4 Sensored control module

The BLDC motor controller ASIC shall contain a sensored control module. This module is actually containing the look-up table for the six step ( $120^\circ$  block commutation) BLDC motor control based on the three HALL sensor signals. In the alternating freewheeling method evaluation chapter 4, the implementation method of such a look-up table is presented (Fig. 4.16) and demonstrated.

The sensored drive block schematic is presented in Fig. 3.54, the ASIC drives the power MOSFET's inverter block. The applied vector to the motor is dependent on the input hall signals and the DIR\_IN control signal from the microcontroller. The speed or current control is done via the PWM input signal which determines the voltage applied to the BLDC motor. The controller ASIC has three major output signals, one which represents the actual rotational direction of the BLDC motor (DIR\_OUT), second which generates a transition at each input hall signal change, therefore measuring the frequency of the CCS (Cycle Count Signal) the exact speed of the BLDC motor can be measured by the system microcontroller and finally the CS\_OUT representing the load current.

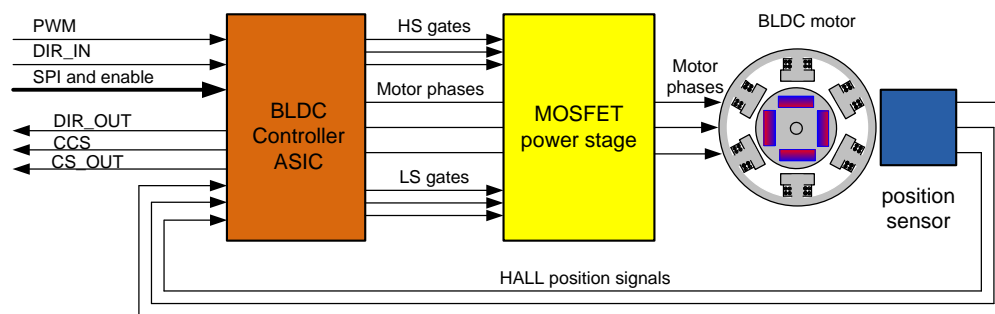


Fig. 3.54 BLDC control ASIC sensored drive configuration

### 3.2.5 Sensorless control module

The sensorless control module shall be based on the ZCD (Zero Crossing Detector) at the floating terminal, methods presented in chapter 1.4.3 Commutation detection methods using the floating terminal voltage [44]-[45], [128]-[135]. The implemented circuit shall be able to detect zero crossings at half of the battery voltage and at GND level. The principle diagram of the sensorless ZCD comparator is presented in Fig. 3.55. All the voltages are additionally divided with  $1/3$ , this enables the implementation of the circuit using lower rated voltage components with much shorter response time.

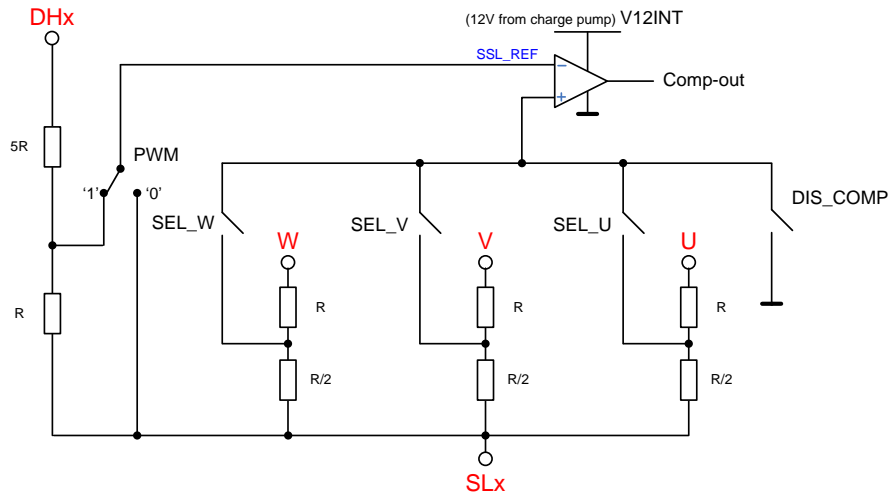


Fig. 3.55 Principle diagram of the sensorless ZCD comparator circuit

Basically the circuit is composed of one comparator circuit which input is connected to the phase voltage dividers via a multiplexer circuit. This switch selects the floating phase and connects it to the comparator circuit. The input battery voltage reference is taken from the drain terminals of the HS transistors, this voltage is closest to the motor phase terminal (which is commutated to the battery). The battery reference voltage during the ON phase of the PWM is connected to the ZCD comparator reference input (SSL\_REF). During PWM OFF time the reference voltage of the comparator is connected to GND for ZCD at GND level. Therefore the reference voltage multiplexer switch as it shown in the figure is controlled by the PWM amplitude. The ground reference of the circuit shall be the source terminals of the LS MOSFET's. Using this connection the actual circuit GND shift effects upon the ZCD is eliminated.

In order to make the circuit more robust the ZCD must have some filtering implemented. Fig. 3.56 presents the filtering mechanism.

When the PWM signal switches ON the ZCD circuit is masked for a short time period ( $t_M$ ) to enable the input signal to settle otherwise the ringing on the input signal could create fake ZCD's. So the ZCD is enabled after this  $t_M$  time period until the PWM signal changes its level. When the input voltage crosses the ZCD comparator threshold voltage for a longer period than  $t_F$  the comparator will detect a zero crossing. After this the ZCD comparator circuit is disabled until the next commutation phase. At the beginning of each commutation phase the ZCD circuit shall be disabled due to the demagnetization pulse (see Fig. 1.39 and Fig. 1.40) which would create a fake ZCD pulse.

Fig. 3.56 presents a positive ZCD at the half of the battery voltage level. The other ZCD cases (negative transition at half of the battery voltage or crossings at GND level) are filtered using the same mechanism as presented.

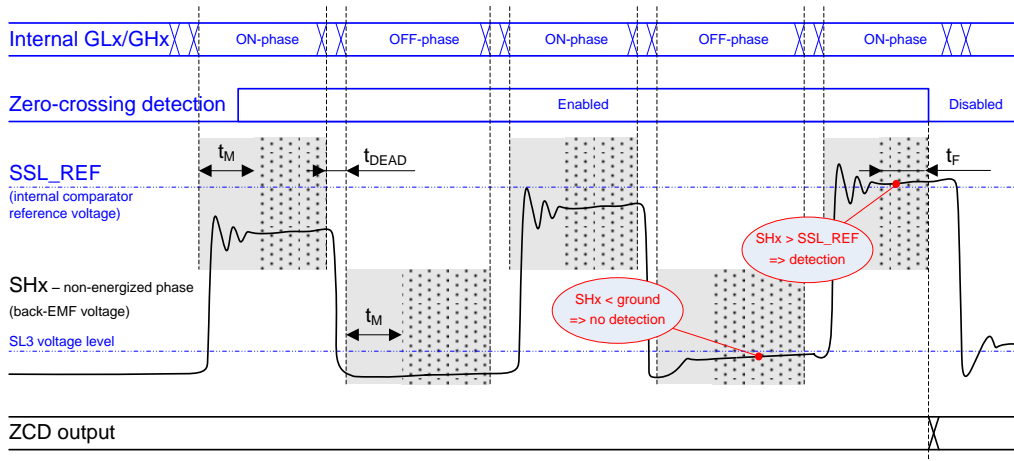


Fig. 3.56 ZCD filtering mechanism

From the above circuits it is obvious that the ZCD pulses are not generated when the phase commutations should happen. Therefore the system microcontroller has to trigger the phase commutations. The commutation table is implemented inside the ASIC. The following diagram presents the sensorless BLDC motor control concept. The BLDC controller ASIC provides to the microcontroller the ZCD signal, based on this, the actual speed and acceleration of the BLDC motor is calculated, then the microcontroller has to compute when the next phase commutation shall happen. This is communicated to the BLDC motor controller ASIC via transitions at the CTS (Commutation Trigger Signal) which triggers the commutation of the outputs to the next commutation phase according to the current commutation phase, direction input and commutation table of the ASIC.

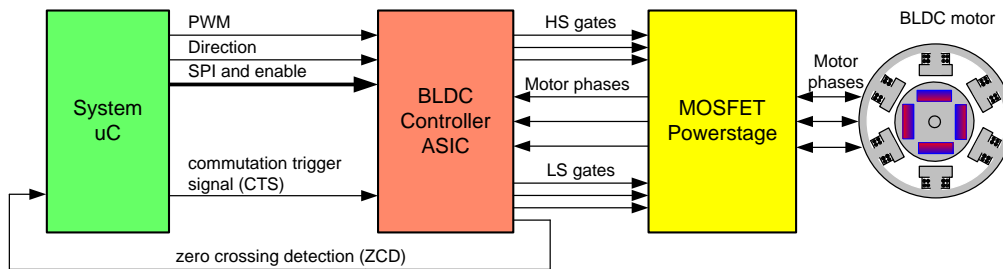


Fig. 3.57 BLDC control ASIC sensorless drive configuration

The sensorless operation requires initial rotor position detection method for startup. This is very difficult to integrate into an ASIC because the initial position estimation method is very dependent on the BLDC motor construction. Therefore the best approach would be to implement this via SW supported with some HW circuits as the method proposed by the author in Chapter 2.

### 3.2.6 Software controlled operation mode

The integrated hardware features of the BLDC ASIC are not optimized for every kind of brushless motors which are controllable using a three phased power inverter circuit. To extend the application portfolio in which this proposed ASIC can be implemented, a separate software controlled mode should be implemented. In this mode each of the three half-bridges are separately controlled via six input signals (two for each half-bridge), connected to the system microcontroller. The six control input pins are multiplexed with the other inactive pins of the sensed control mode to reduce the total pin number of the chip. See alternative pin functions put in brackets in the ASIC block diagram from Fig. 3.14. One of these signals shall be the enable signal (ENU, ENV and ENW) of the particular half-bridge and the other shall define which switch of the half-bridge is active (LS or HS, INU, INV, INW) as presented in Table 3.6 for U half bridge.

Table 3.6 Half-bridge input signals truth table

ENU	INU	Output
0	x	High impedance, LS and HS MOSFET's OFF
1	0	Low Side (LS) MOSFET ON (HS MOSFET OFF)
1	1	High Side (HS) MOSFET ON (LS MOSFET OFF)

Using this operation mode a multitude of different control strategies can be implemented as the twelve step commutation mode or 60° block commutation method, 180° block commutation method or even high sophisticated sine-wave or FOC (Field Oriented Control) strategies for PMSM's (Permanent Magnet Synchronous Motor).

The switching between the implemented HW control modes and this software controlled mode should be done via a SPI configurable bit in the BLDC ASIC configuration registers (Bit HB3 from the proposed CF1 SPI register, see subchapter 3.2.7).

### 3.2.7 BLDC ASIC serial control interface

The BLDC motor controller ASIC is controlled by the system microcontroller via SPI (Serial Peripheral Interface) bus [168]-[170]. Via this interface the BLDC motor controller ASIC operation mode is configured and the status of the operation mode, diagnosis is read back.

Due to the high number of status and configuration bits the SPI interface shall be configured to 24 bit length. Therefore one SPI communication cycle produces an exchange of three data bytes (including instruction codes and parity bit) between the system microcontroller and the BLDC controller ASIC.

The first 4 bits of the communication word are reserved for the instruction coding followed by 19 data bits and one last parity bit (LSB) as presented in Fig. 3.58. Therefore fourteen instruction codes are possible, excluding the instruction codes with all bits "0000" and "1111" which shall be avoided. The following Table 3.7 summarizes the instruction codes of the ASIC. The undefined remaining instruction codes are reserved for future use.

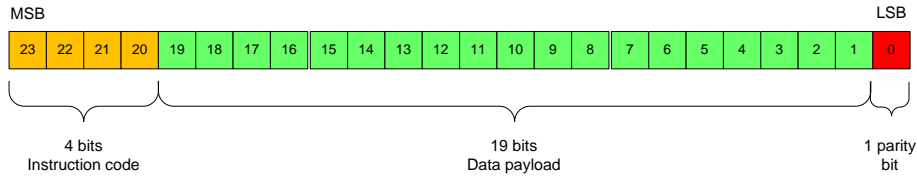


Fig. 3.58 SPI data configuration

Table 3.7 Instruction codes of the BLDC controller ASIC

Instruction code (bin)	Description
0000	Error, wrong instruction code
0001	ASIC Identification and version code
0010	Write configuration register CR0
0011	Write configuration register CR1
0100	Write configuration register CR2
0101	Reserved
0110	Reserved
0111	Reserved
1000	Reserved
1001	Read status register SR0
1010	Read status register SR1
1101	Read & Write status register SR0
1110	Read & Write status register SR1
1111	Error, wrong instruction code

Table 3.8 presents the first configuration register content (CR0), Table 3.9 the second (CR1) and Table 3.16 the third (CR2) configuration register of the proposed ASIC.

Table 3.8 CR0 Configuration register 0 bits description

Bit	Name	Description
20-23	Instr. code	"0010"
19	VPS_OV_DIS	Disables the bridge deactivation in case of battery overvoltage conditions
18	WSC_DIS	Disables the bridge deactivation in case of WSC
17	DIS_HSEQ	Disables the bridge deactivation in case of hall signals sequence error
16	DIS_HJIT	Disables the bridge deactivation in case of hall signals jitter error
15	DIS_HPAT	Disables the bridge deactivation in case of hall signals pattern error
14	OC_DIS	Over current detection disable
13	WSC_DIS	Disables the weak short circuit detection
12	SSL	Activate sensorless control mode
11	AFW	Set alternating freewheeling control mode
10	Gain	Current measurement path amplifying factor

Bit	Name	Description
9	S&H_DIS	Disable S&H stage (sample switch permanently closed)
8	AZ	Auto zero mode entry
7	CM	Current measurement enable
6	VDS_DIS	Disable VDS monitoring on LS MOSFET's
5	HB3	Control the three half bridges separately
4	FBRAKE	Brake in case of failure
3	DPWM	Double PWM mode enable
2	OFSM	Enables the Off-state monitoring unit
1	BE	Bridge Enable
0	P	Parity bit

The FBRAKE bit configures the ASIC reaction in case a failure is detected. According to this bit there are two possible reaction modes of the ASIC. If FBRAKE='0' then in case of a failure detection all power MOSFET's are switched OFF putting the bridge outputs into high impedance. If FBRAKE='1' in case of failure detection the ASIC should brake the motor by opening all LS MOSFET's or in case of SCB failure all HS MOSFET's.

Table 3.9 CR1 Configuration register 1 bits description

Bit	Name	Description
20-23	Instr. code	"0011"
19	DT2	Dead time configuration bit 2
18	DT1	Dead time configuration bit 1
17	DT0	Dead time configuration bit 0
16	GC2	MOSFET's gate charge current configuration bit 2
15	GC1	MOSFET's gate charge current configuration bit 2
14	GC0	MOSFET's gate charge current configuration bit 2
13	TM2	ZCD detection mask time ( $t_M$ ) select bit 2
12	TM1	ZCD detection mask time ( $t_M$ ) select bit 1
11	TM0	ZCD detection mask time ( $t_M$ ) select bit 0
10	TF2	ZCD filter time ( $t_F$ ) selection bit 2
9	TF1	ZCD filter time ( $t_F$ ) selection bit 1
8	TF0	ZCD filter time ( $t_F$ ) selection bit 0
7	DEG2	ZCD and S&H disable time, degauss pulse time bit 2
6	DEG1	ZCD and S&H disable time, degauss pulse time bit 1
5	DEG0	ZCD and S&H disable time, degauss pulse time bit 0
4	S&H_DEL3	Sample delay time bit 3
3	S&H_DEL2	Sample delay time bit 2
2	S&H_DEL1	Sample delay time bit 1
1	S&H_DELO	Sample delay time bit 0
0	P	Parity bit

DT2..DT0 bits define the generated dead time to avoid the simultaneous conduction of the HS and LS MOSFET's. The following Table 3.10 presents the actual dead time setting, according to the configuration bits.



GC2..GC0 configures the external power MOSFET's gate charge and discharge currents as detailed in Table 3.11. The combinations are obtained using five current sources (25mA, 50mA, 100mA, 75mA and 250mA) activated separately to obtain the desired values.

Table 3.12 and Table 3.13 presents the zero crossing detector comparator masking and filter time configuration possibilities needed for a proper ZCD.

Table 3.10 Dead time bit configurations

DT2	DT1	DT0	Dead time	DT2	DT1	DT0	Dead time
0	0	0	1 $\mu$ s	1	0	0	6 $\mu$ s
0	0	1	1.5 $\mu$ s	1	0	1	8 $\mu$ s
0	1	0	2 $\mu$ s	1	1	0	12 $\mu$ s
0	1	1	4 $\mu$ s	1	1	1	16 $\mu$ s

Table 3.11 Power MOSFET's gate charge currents configuration

GC2	GC1	GC0	I <sub>GATE</sub>	GC2	GC1	GC0	I <sub>GATE</sub>
0	0	0	25 mA	1	0	0	125 mA
0	0	1	50 mA	1	0	1	175 mA
0	1	0	75 mA	1	1	0	250 mA
0	1	1	100 mA	1	1	1	500 mA

Table 3.12 ZCD mask time configuration bits

TM2	TM1	TM0	Mask time	TM2	TM1	TM0	Mask time
0	0	0	0.2 $\mu$ s	1	0	0	2 $\mu$ s
0	0	1	0.5 $\mu$ s	1	0	1	2.5 $\mu$ s
0	1	0	1 $\mu$ s	1	1	0	3 $\mu$ s
0	1	1	1.5 $\mu$ s	1	1	1	4 $\mu$ s

Table 3.13 ZCD comparator filter time

TF2	TF1	TF0	SSL filter	TF2	TF1	TF0	SSL filter
0	0	0	0.2 $\mu$ s	1	0	0	2 $\mu$ s
0	0	1	0.5 $\mu$ s	1	0	1	2.5 $\mu$ s
0	1	0	1 $\mu$ s	1	1	0	3 $\mu$ s
0	1	1	1.5 $\mu$ s	1	1	1	4 $\mu$ s

At the phase commutations the commutated phase energy is discharged into the battery causing disturbances in the sensorless ZCD module and the current measurement path. To avoid this problem the two blocks should be disabled during the degauss time, Table 3.14 presents the disable time possible configurations defined by DEG2..DEG0 bits. The configuration used in the application has to be chosen according to the BLDC motor windings inductance and the supply voltage.

Table 3.14 ZCD and S&amp;H current measurement disable time setting during degauss pulse

DEG2	DEG1	DEG0	DEG time	DEG2	DEG1	DEG0	DEG time
0	0	0	0.2 $\mu$ s	1	0	0	3 $\mu$ s
0	0	1	0.5 $\mu$ s	1	0	1	4 $\mu$ s
0	1	0	1 $\mu$ s	1	1	0	6 $\mu$ s
0	1	1	2 $\mu$ s	1	1	1	12 $\mu$ s

Delay time configuration of the sampling point is controlled by S&H\_DEL3..S&H\_DELO bits as presented in the next Table 3.15.

Table 3.15 S&amp;H delay time configuration table

S&H DEL3	S&H DEL2	S&H DEL1	S&H DELO	Delay time	S&H DEL3	S&H DEL3	S&H DEL3	S&H DEL3	Delay time
0	0	0	0	50 ns	1	0	0	0	500 ns
0	0	0	1	100 ns	1	0	0	1	600 ns
0	0	1	0	150 ns	1	0	1	0	800 ns
0	0	1	0	200 ns	1	0	1	0	1 $\mu$ s
0	1	0	0	250 ns	1	1	0	0	1.5 $\mu$ s
0	1	0	1	300 ns	1	1	0	1	2 $\mu$ s
0	1	1	0	350 ns	1	1	1	0	3 $\mu$ s
0	1	1	1	400 ns	1	1	1	1	4 $\mu$ s

Table 3.16 CR2 Configuration register 2 bits description

Bit	Name	Description
<b>20-23</b>	Instr. code	<b>"0100"</b>
<b>19</b>	CP_UV_DIS	Disable bridge deactivation in case of charge pump under-voltage
<b>18</b>	CP_OV_DIS	Disable bridge deactivation in case of charge pump over-voltage
<b>17</b>	BOTD_DIS	Bridge disable in case of bridge over-temperature
<b>16</b>	BOT_DIS	Bridge over-temperature comparator circuit enable
<b>15</b>	BOT_LEV	Bridge over-temperature active level selection
<b>14</b>	OC2	Overcurrent detection bit 2
<b>13</b>	OC1	Overcurrent detection bit 1
<b>12</b>	OC0	Overcurrent detection bit 0
<b>11</b>	VDS2	VDS monitoring threshold divider bit 2
<b>10</b>	VDS1	VDS monitoring threshold divider bit 1
<b>9</b>	VDS0	VDS monitoring threshold divider bit 0
<b>8</b>	HJIT1	Hall jitter filter time selection bit 1
<b>7</b>	HJIT0	Hall jitter filter time selection bit 0
<b>6</b>	FLBL_DIS	Disable bridge operation in case of hall error
<b>5</b>	WSC1	Weak short detection threshold bit 1
<b>4</b>	WSC0	Weak short detection threshold bit 0
<b>3..1</b>	0	Reserved
<b>0</b>	P	Parity bit

The following Table 3.17 presents the overcurrent detection thresholds, voltage measured on the shunt resistor. Table 3.18 presents the VDS monitoring threshold adjustment table, using these configuration bits the VDS monitoring threshold change over temperature can be corrected.

Table 3.17 Overcurrent detection configuration bits

OC2	OC1	OC0	OC limit	OC2	OC1	OC0	OC limit
0	0	0	40 mV	1	0	0	80 mV
0	0	1	50 mV	1	0	1	120 mV
0	1	0	60 mV	1	1	0	180 mV
0	1	1	70 mV	1	1	1	240 mV

Table 3.18 VDS monitoring divider configuration bits

VDS2	VDS1	VDS0	VDS limit	VDS2	VDS1	VDS0	OC limit
0	0	0	1 -> (25°C)	1	0	0	1.3 -> (80°C)
0	0	1	0.8 -> (-30°C)	1	0	1	1.4 -> (100°C)
0	1	0	0.9 -> (0°C)	1	1	0	1.55->(130°C)
0	1	1	1.2 -> (50°C)	1	1	1	1.7 -> (160°C)

Table 3.19 presents the hall jitter detection and filter time configuration bits. Table 3.20 presents the weak short circuit threshold values configurable by WSC1 and WSC0 bits of CR2 configuration register of the BLDC ASIC.

Table 3.19 Hall jitter filtering time configuration

HJIT1	HJIT0	Jitter filter time
0	0	10 $\mu$ s
0	1	15 $\mu$ s
1	1	20 $\mu$ s
1	1	40 $\mu$ s

Table 3.20 Weak short circuit detection threshold configuration bits

WSC1	WSC0	WSC detection threshold
0	0	10 mV
0	1	20 mV
1	1	30 mV
1	1	40 mV

The following two tables present the status registers content of the BLDC ASIC (Table 3.21 presents the SR0 and Table 3.22 presents the SR1). There are two accessing instruction codes for each register SR0 and SR1.

The first two instructions encoded with "1001" and "1010" enables only the reading of the status registers. This ensures that the failure bits are not cleared accidentally. Based on the failure indications the SW application can decide to clear the failure bits or not. When the application SW clears all the failure bits, the BLDC controller bridge is automatically re-enabled. In case the failure is still present, the BLDC ASIC diagnosis unit will redetect the failure disabling the bridge and setting the failure bits back.

Table 3.21 SR0 Status register 0 bit description

Bit	Name	Description
19	BRAKE	Brake input pin level
18	DIS	Disable input pin level
17	DIR	Direction input pin level
16	HIZ	High impedance set input pin level
15	VPS_OV	Battery supply over-voltage
14	VPS_UV	Battery supply under-voltage
13	VDD_OV	Logic supply over-voltage
12	VDD_UV	Logic supply under-voltage
11	VCP_OV	Charge pump over-voltage
10	VCP_UV	Charge pump under-voltage
9	CLKF	Logic clock failure
8	AOTW	ASIC over temperature warning
7	AOTD	ASIC over temperature disable
6	BOTW	Bridge over temperature warning
5	BOTD	Bridge over temperature disable
4	WSC	Weak short circuit detection
3..1	0	Reserved
0	P	Parity bit

Table 3.22 SR1 Status register 1 bits description

Bit	Name	Description
19	SCB_U_ONSM	Short to battery at phase U by On-state monitoring
18	SCG_U_ONSM	Short to ground at phase U by On-state monitoring
17	SCB_V_ONSM	Short to battery at phase V by On-state monitoring
16	SCG_V_ONSM	Short to ground at phase V by On-state monitoring
15	SCB_W_ONSM	Short to battery at phase W by On-state monitoring
14	SCG_W_ONSM	Short to ground at phase W by On-state monitoring
13	WSC_ONSM	Weak short circuit detected by On-state monitoring
12	SCL_ONSM	Short of the load detected by the ONSM
11	SCB_OFSM	Short to battery detection by Off-state monitoring
10	SCG_OFSM	Short to ground detection by Off-state monitoring
9	OL_U_OFSM	Open load at phase U
8	OL_V_OFSM	Open load at phase V
7	OL_W_OFSM	Open load at phase W
6	HALL_PAT	Hall pattern error
5	HALL_SEQ	Hall sequence error
4	HALL_JIT	Hall jitter error
3	HALL1	Internal Hall1 signal level
2	HALL2	Internal Hall2 signal level
1	HALL3	Internal Hall3 signal level
0	P	Parity bit

Clearing the status bits can be done only using instruction codes "1101" for SR0 or "1110" for SR1 register and in the data field setting the corresponding bit of the desired flag to be cleared to "1".

Sending a command with read and clear instruction with all data field set to "1" will clear all status bits from that status register.

As example "1101 1111 1111 1111 1111 1110" (0xDFFFFE) will clear all error bits from SR0 register.

## Summary

This chapter of the thesis is considered by the author as being the most important chapter of the thesis presenting an innovative architecture for a BLDC motor controller ASIC.

The first subchapter 3.1, presents a short overview of the BLDC motor applications in the automotive industry followed by an overview of BLDC motor controller system architectures.

The second subchapter 3.2 presents the proposed architecture of the BLDC ASIC describing several internal blocks based on the existing state of the art in the BLDC motor controller circuits technology and new ideas, methods introduced by the author as the current measurement circuit architecture; the OFF state monitoring diagnosis and combined diagnosis interpretation, the Hall signal jitter detection and filter method (patent pending) the Bridge temperature monitoring unit implementation in the ASIC, communication interface protocol definition.



## 4 Alternating freewheeling PWM technique for a better power distribution

The automotive electronics has very high operating temperature requirements, up to 150°C or more especially for automatic transmission control units. Therefore the power consumption balance between the electronic control unit components is very important, especially for the power inverters or H-bridges using mostly MOSFET transistors as switching elements (see Fig. 4.1 for DC and Fig. 4.3 for BLDC).

In the literature we find several papers and books relating different driving strategies of the power MOSFET's gates, improving its switching characteristics and reducing losses [172]-[175]. The paper in [176] presents an evaluation of the MOSFET parameters, tolerance and its influence on the total power consumption. The overall power consumption of BLDC driving electronics is dependent also on the chosen driving strategy of the BLDC motor itself, improving its efficiency and performances, [173]-[179] thus reducing the total power consumption and losses as well. The method presented in this chapter does not propose to reduce the overall power consumption of the bridge switching elements. The aim of the principle is to distribute the total power consumption more equally between the switching elements thus reducing the maximum power consumption per switching element, increasing its lifetime [4], [180], [212] and the maximum output power deliverable by the bridge in the same operating conditions.

### 4.1 Bridge power consumption estimation

The conventional driving method of a DC motor H-Bridge is driving its switching elements (e.g. MOSFET transistors) with a PWM signal [174], [177]. During the ON time of the PWM signal the current flows via one high-side (HS) and one opposite low-side (LS) transistor depending on the rotating direction (Fig. 4.1 (a),(c)), followed by a freewheeling period. The freewheeling current depending on the driving method can flow via the other two transistors antiparallel diode back to the power supply, when no active freewheeling is used.

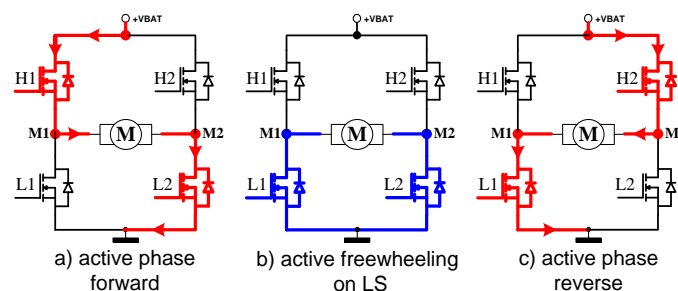


Fig. 4.1 H-Bridge driving method

To reduce the power consumption of the switching MOSFET's the freewheeling current is forced actively to flow via the two LS or HS transistors (see Fig. 4.2)

depending on the driving method by turning ON the MOSFET's during this freewheeling period. Usually active LS freewheeling is applied (Fig. 4.1 (b)).

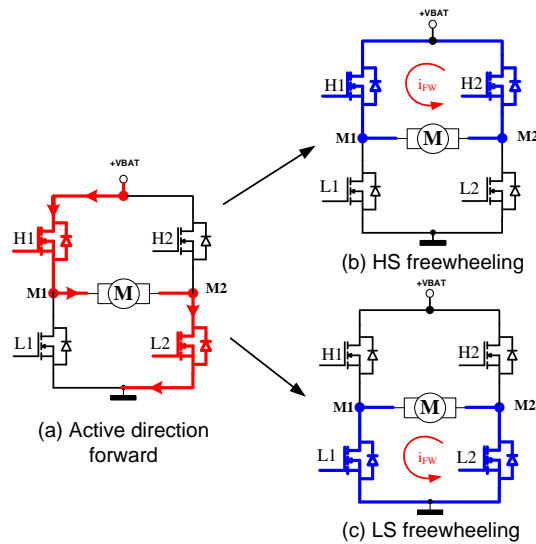


Fig. 4.2 H-bridge freewheeling paths

The control of the BLDC (Brushless DC) motors with permanent magnets is done using three phased Bridge (see Fig. 4.3). For the six step commutation method at one given moment only two of the half bridges are activated in accordance to rotor position [177], the third being OFF. Each of the six control sequences can be simplified to an H-bridge drive mode.

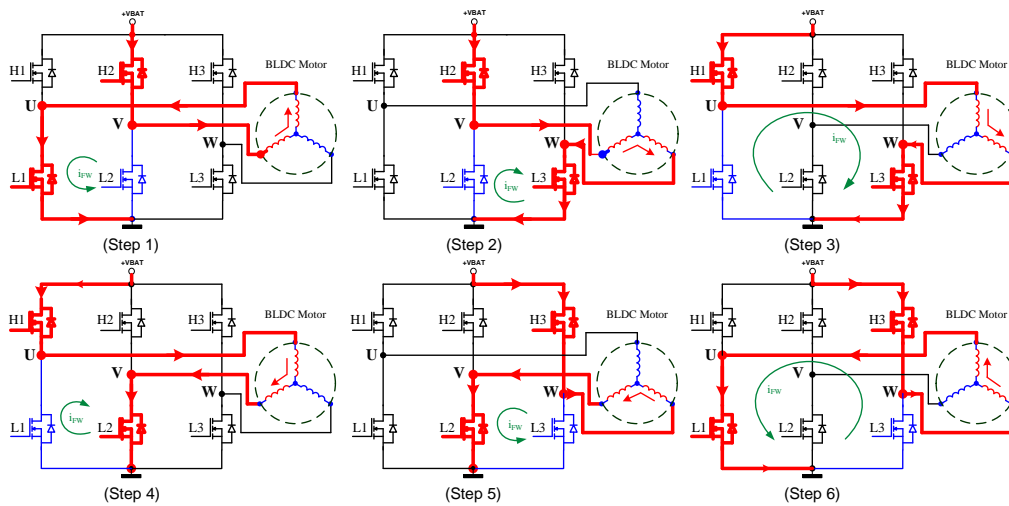


Fig. 4.3 BLDC motor - three phased bridge driving method, commutation steps

At a particular control sequence only three of the switching elements are active. In the case shown in Fig. 4.1 (a) the  $H1$ ,  $L1$  and  $L2$  switches are activated, therefore



only these elements contribute to the total power consumption of the H-Bridge. The total power dissipation  $P_t$  of these elements can be split into two components [174]:

- static power consumption  $P_{on}$ ;
- switching losses  $P_{sw}$ ;

Therefore the total power consumption will be:

$$P_t = P_{sw} + P_{on} \quad (4.1)$$

The static power dissipation  $P_{on}$  represents the amount of power dissipated during the ON time of the MOSFET. In the case shown in Fig. 4.1 (a) the *H1* static power dissipation  $P_{ON_{H1}}$  can be expressed as follows:

$$P_{ON_{H1}} = R_{dsON} \cdot i_l^2 \cdot (DC - t_{DT} \cdot F_{PWM}) \quad (4.2)$$

The static power consumption of *L1* ( $P_{ON_{L1}}$ ) and *L2* ( $P_{ON_{L2}}$ ):

$$P_{ON_{L1}} = R_{dsON} \cdot i_l^2 \cdot (1 - DC - t_{DT} \cdot F_{PWM}) \quad (4.3)$$

$$P_{ON_{L2}} = R_{dsON} \cdot i_l^2 \quad (4.4)$$

- with  $R_{dsON}$  denoting the ON resistance of the switching MOSFET;  $I_l$  – average load current;  $DC$  – Duty Cycle (1 representing 100%);  $F_{PWM}$  – the PWM frequency;  $t_{DT}$  – dead time (time delay between LS and HS switching).

*H2* transistor has no power consumption being off in this case.

In the method proposed in this chapter the MOSFET's are driven with a constant gate current, thus making the gate charging and switching characteristics very close to linear [175]. The switching losses  $P_{sw}$  are dependent on the MOSFET drain-source voltage, drain current and gate driving method, all these parameters influence it's switching time. In the literature we find several papers relating methods to calculate MOSFET transistors switching times and power losses according to different driving methods and operating conditions [172][174][175]. In our case having a constant gate charge current a good approximation of the switching losses is given by the following simplified expressions:

$$P_{sw} = i_l \cdot V_{DC} \cdot F_{PWM} \cdot t_{sw} \quad (4.5)$$

$$t_{sw} = \frac{Q_{gd} + (C_{gd\_ext} \cdot V_{DC})}{i_g} \quad (4.6)$$

- with  $V_{DC}$  denoting the power supply voltage;  $t_{sw}$  – switching time of the MOSFET;  $Q_{gd}$  – gate-drain (Miller) charge;  $C_{gd\_ext}$  – external gate-drain capacitance (if it's the case);  $i_g$  – gate charge current.

In the case presented in Fig. 4.1 (a) the switching loss appears only at the *H1* MOSFET (assuming the motor is not in generator mode), because this drives the switching at the motor terminal output. At the *L1* MOSFET the switching loss is

resumed to the losses during the switching from  $-V_{D\_FW}$  (MOSFET substrate diode voltage) to GND, which is negligible, plus the power consumption of the substrate diode  $P_{sw\_dt}$  during  $t_{DT}$  (4.7).

$$P_{sw\_dt} = 2 \cdot F_{PWM} \cdot V_{D\_FW} \cdot i_l \cdot t_{DT} \quad (4.7)$$

As a summary for the case from Fig. 4.1 (a) based on (4.1)–(4.7) we can conclude the following power consumptions for the H-Bridge MOSFET's:

$$\begin{aligned} P_{H1} &= R_{dsON} \cdot i_l^2 \cdot (DC - t_{DT} \cdot F_{PWM}) + i_l \cdot V_{DC} \cdot F_{PWM} \cdot t_{sw} \\ P_{H2} &= 0 \\ P_{L1} &= R_{dsON} \cdot i_l^2 \cdot (1 - DC - t_{DT} \cdot F_{PWM}) + 2 \cdot F_{PWM} \cdot V_{D\_FW} \cdot i_l \cdot t_{DT} \\ P_{L2} &= R_{dsON} \cdot i_l^2 \end{aligned} \quad (4.8)$$

From these equations we can conclude that the power consumption of the bridge MOSFET's are not equal, *H1* and *L2* having the highest power consumption, *H2* having no power consumption at all, being turned off for this operating mode.

For BLDC motor driving three phased bridge the same power consumption basics can be applied as to the H-Bridge. The conducting MOSFET's depend on the current phase commutation step. Considering that the motor rotates, each of the *Hx* MOSFET's are going through commutation steps where they are switched with the PWM signal or turned off (see Fig. 4.3). The same fact for the *Lx* MOSFET's which are according to the commutation step in full conduction, conducting during PWM-OFF time or switched off. Therefore the total power consumption of these MOSFET's is the average power consumed during the six commutation steps (4.9).

$$\begin{aligned} P_{Hx} &= \frac{1}{3} \cdot \left[ R_{dsON} \cdot i_l^2 \cdot (DC - t_{DT} \cdot F_{PWM}) + i_l \cdot V_{DC} \cdot F_{PWM} \cdot t_{sw} \right] \\ P_{Lx} &= \frac{1}{3} \cdot \left[ R_{dsON} \cdot i_l^2 \cdot (1 - DC - t_{DT} \cdot F_{PWM}) + 2 \cdot F_{PWM} \cdot V_{D\_FW} \cdot i_l \cdot t_{DT} \right] + \frac{1}{3} \cdot R_{dsON} \cdot i_l^2 \end{aligned} \quad (4.9)$$

## 4.2 Proposed power distribution method

The proposed driving method of the bridge MOSFET's has its aim of better power distribution among the switching MOSFET's in order to transfer a part of the power consumption from the most dissipating to less dissipating MOSFET's.

This can be achieved by a very simple driving technique, alternating the usual LS freewheeling with HS freewheeling for each consecutive PWM period. Fig. 4.4 presents the current paths for H-Bridge control, where Fig. 4.4 (a) and (c) are the PWM on periods and Fig. 4.4 (b) and (d) are the respective LS and HS freewheeling periods. Fig. 4.5 presents the gate and the output signals at the motor terminals for forward driving direction. Note that the gate driving signals (GH1, GH2, GL1 and GL2) and motor terminal signals (M1 and M2) frequency is half of the PWM frequency.

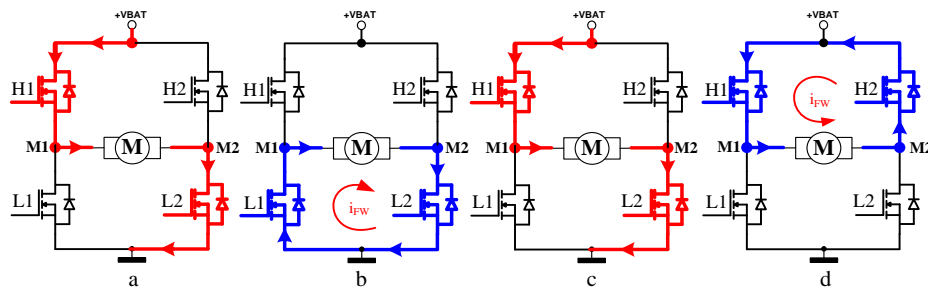


Fig. 4.4 Alternating freewheeling current paths

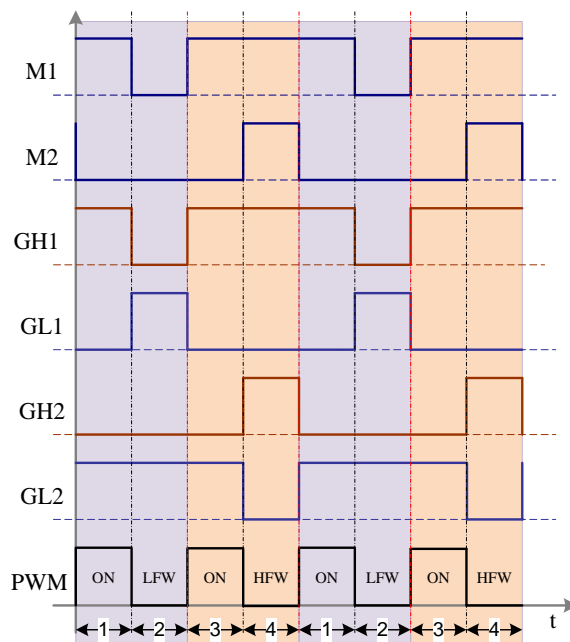


Fig. 4.5 Alternating freewheeling gate control and motor terminal signals

With this method the switching loss appears for one PWM cycle at the LS MOSFET and second at the HS MOSFET, alternatively. In the same way the substrate diode power consumption during the dead time once appears at the LS and second at the HS MOSFET, alternatively.

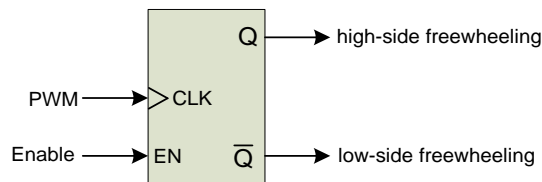


Fig. 4.6 Implementation of low/high side freewheeling path control

In case of H-bridge the switching MOSFET's power consumption can be estimated using the following equations:

$$P_{H1} = P_{L2} = \frac{1}{2} \left[ R_{dsON} \cdot i_l^2 \cdot (1 + DC - t_{DT} \cdot F_{PWM}) + (i_l \cdot V_{DC} \cdot F_{PWM} \cdot t_{sw}) \right] \quad (4.10)$$

$$P_{H2} = P_{L1} = \frac{1}{2} \left[ R_{dsON} \cdot i_l^2 \cdot (1 - DC - t_{DT} \cdot F_{PWM}) \right] + (F_{PWM} \cdot V_{D\_FW} \cdot i_l \cdot t_{DT})$$

Good power consumption estimation for the BLDC three phased bridge MOSFET's can be obtained using:

$$P_{Hx} = P_{Lx} = \frac{1}{3} \left[ R_{dsON} \cdot i_l^2 \cdot (1 + t_{DT} \cdot F_{PWM}) \right] + \frac{1}{6} F_{PWM} \cdot i_l \cdot (V_{D\_FW} \cdot t_{DT} + V_{DC} \cdot t_{sw}) \quad (4.11)$$

According to (4.10)(4.11) we can conclude that the power consumption of the most consuming switching elements is less compared to the classical LS or HS freewheeling methods, with an increase of the power consumption of the less consuming MOSFET's.

The great benefit of the better power distribution is that the maximum temperature of the switching elements is reduced offering the possibility to even further increase the output power of the bridge without overloading the switching elements. On the other hand decreasing the MOSFET's operating temperature by decreasing the max power dissipation leads to a longer lifetime of the switching components [4], [180].

## 4.3 Experimental results

### 4.3.1 Simulation of the alternating freewheeling concept

The simulations of the alternating freewheeling concept have been done using a simplified circuit presented in Fig. 4.7. For comparison in parallel the conventional LS freewheeling circuit was also simulated using the circuit presented in Fig. 4.8. The gates of the switching MOSFET's are charged from a constant pulse current source ( $\pm 75\text{mA}$ ) with a PWM frequency of 10 KHz. The simulation results of the alternative freewheeling (AFW\_Hx and AFW\_Lx) are presented in comparison to the classical LS freewheeling method (LSFW\_Lx and LSFW\_Hx) for three phased bridge in Fig. 4.9 (64A max load current) and for H-Bridges in Fig. 4.10 (maximum load current of 26A).

The simulation results clearly demonstrate that the alternating freewheeling method leads to a better power distribution among the bridge MOSFET's in both cases, BLDC motor driving three phased bridge or DC motor driving H-bridge.

In order to obtain very accurate simulation results, the used power MOSFET (BUK765R2-40B) PSpice model has been requested and received from NXP Semiconductors, the model parameters are presented in the second page of the ANNEX section.

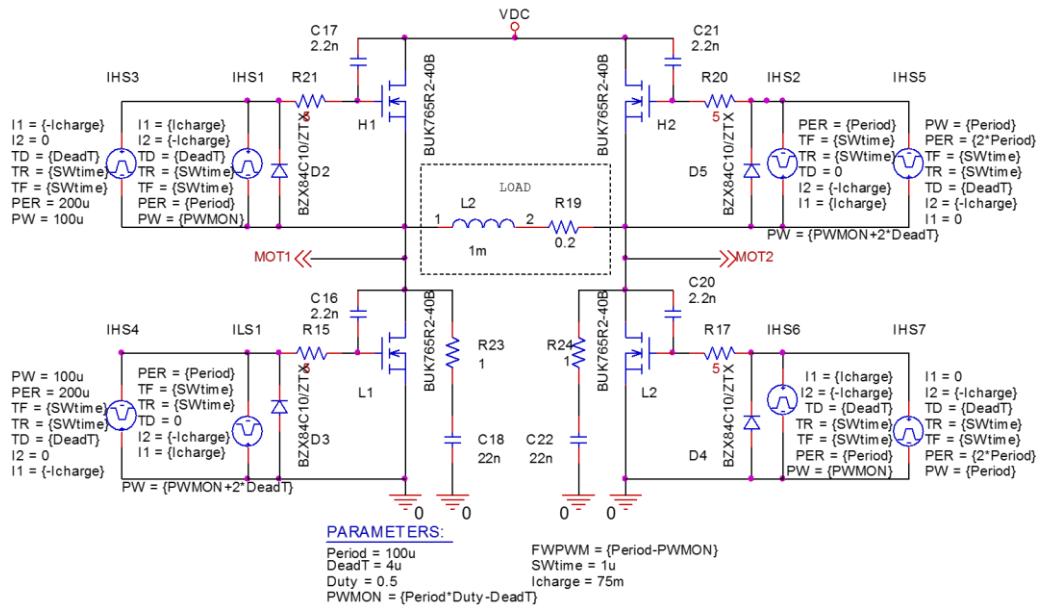


Fig. 4.7 Schematics of the alternating freewheeling implementation used in the simulations

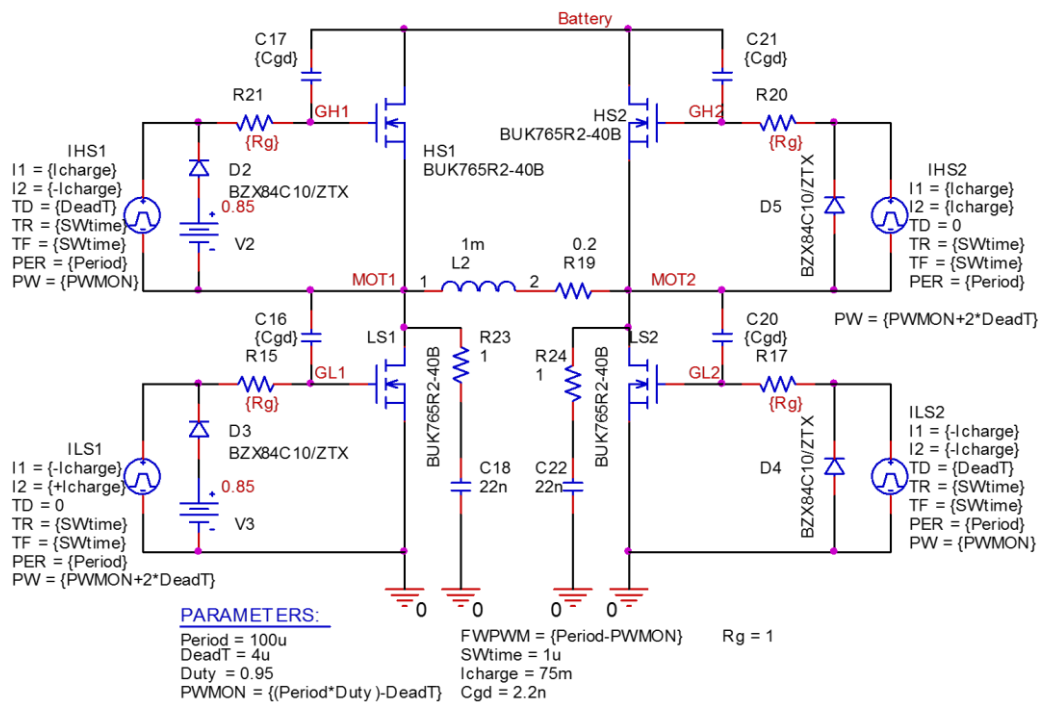


Fig. 4.8 Schematics of the classical LS freewheeling implementation used in the simulations

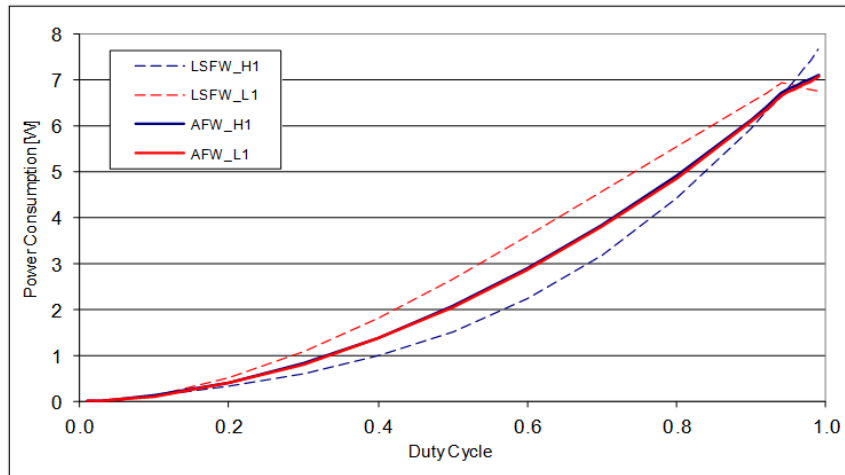


Fig. 4.9 3ph bridge power consumption (dotted line - LS freewheeling)

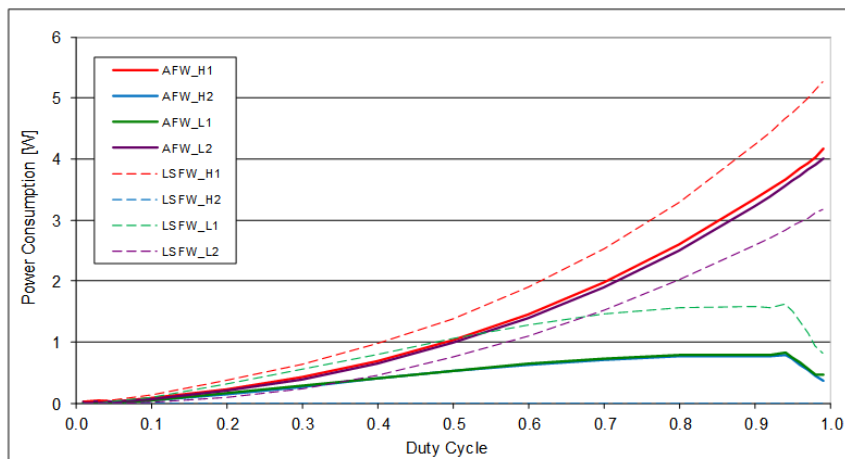


Fig. 4.10 H-Bridge power consumption (dotted line - LS freewheeling)

### 4.3.2 Calculation VS simulation comparison

To demonstrate the correctness of the elaborated theoretical formulas, the circuit parameters have been calculated using formulas (4.1)-(4.11) and results compared with the PSpice simulation having same operating conditions. Fig. 4.11 presents the comparison for DC motor driving H-Bridge.

Fig. 4.12 presents the comparison results for BLDC motor driving three phased bridge. With dotted lines the simulation results are presented and with solid lines the calculation results. The chosen calculation points are the same as the simulation points of the circuit defined by the input PWM signal duty cycle. The following duty cycle points have been used: 0.01; 0.03; 0.05; 0.1; 0.2; 0.3; 0.4; 0.5; 0.6; 0.7; 0.8; 0.9; 0.92; 0.94; 0.95; 0.96; 0.97; 0.98; 0.99; (out of the results, the graphs in Fig. 4.11 and Fig. 4.12 have been generated).

The results of the simulations and calculations we can clearly conclude that the proposed calculation formulas are giving very close to reality power consumption estimation.

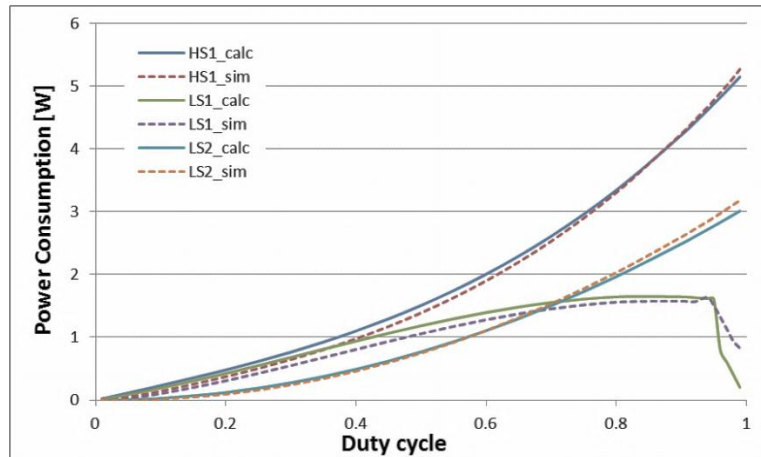


Fig. 4.11 Simulation VS calculation power dissipation results for H-Bridge

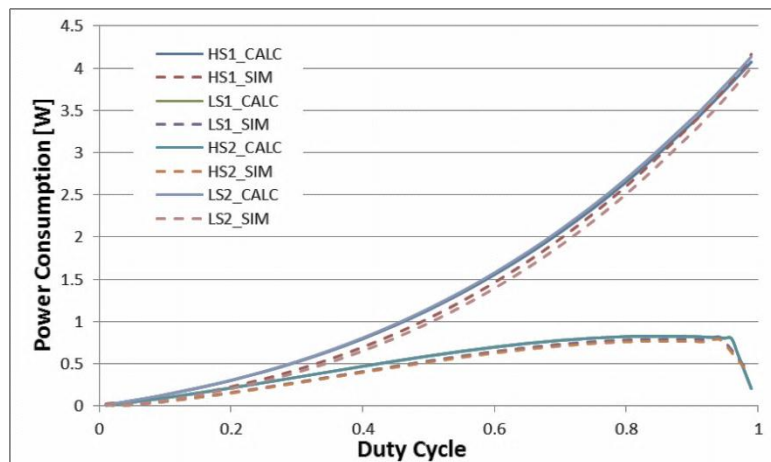


Fig. 4.12 Simulation VS calculation power dissipation results for 3ph Bridge

### 4.3.3 Experimental evaluation of the alternating freewheeling concept

The experimental circuit block schematic used for the lab evaluation is presented in Fig. 4.13. It consists of a main microcontroller using Freescale S12XF384, which is the interface to the PC application via USB (Universal Serial Bus). The implementation of the bridge MOSFET's switching strategy, logics is implemented using a Xilinx CoolRunner II, CPLD (Complex Programmable Logic Device) XC2C256.

For the DC motor control H-Bridge drive logic circuit is presented in Fig. 4.14. The switching from LS to HS freewheeling is done using a counter circuit whose output is toggled by each rising edge of the PWM. From the Q0 output of this

counter (CB2CE) the APWM (alternating PWM) and AFW (alternating freewheeling) signals are generated. These APWM and AFW are the control signals of the MOSFET driver input. The MOSFET driver has two separate inputs for each half bridge, INx and INHx, Table 4.1 presents the truth table for the half bridges.

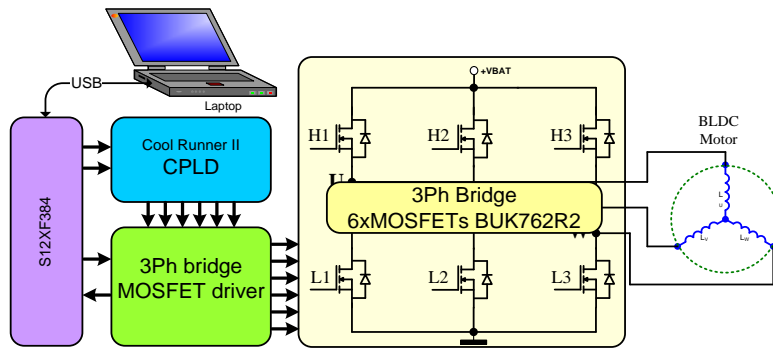


Fig. 4.13 Test bench setup and configuration

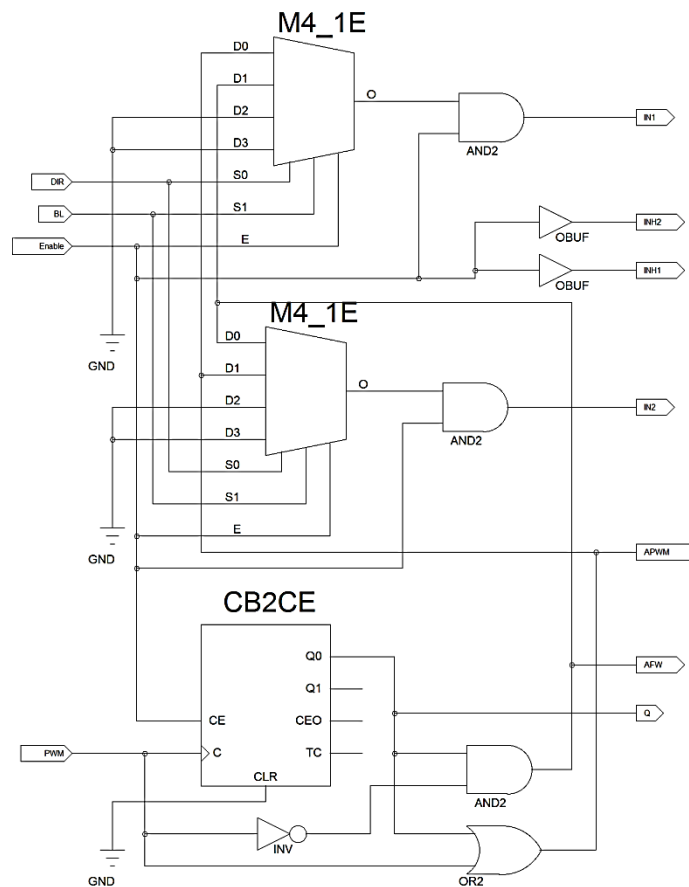


Fig. 4.14 Alternating freewheeling implementation for DC motor control H-Bridge



Table 4.1 Half bridge input VS output truth table

INx	INHx	HSx	LSx	OUTx
0	0	OFF	OFF	HZ
1	0	OFF	OFF	HZ
0	1	OFF	ON	LOW - GND
1	1	ON	OFF	HI - Vbatt

Table 4.2 presents the IO configuration of the alternating freewheeling control circuit for DC motors (based on Fig. 4.14).

Table 4.2 DC motor control logic circuit IO signals

IO port name	Port direction	Port signal meaning
DIR	Input	Motor rotation direction control
BL	Input	Switch to BLDC mode (implementation not shown in schematic from Fig. 4.14)
Enable	Input	Enable (high) input signal
PWM	Input	PWM signal from the microcontroller
IN1	Output	Input of 1 <sup>st</sup> half bridge*
INH1	Output	Enable of 1 <sup>st</sup> half bridge*
IN2	Output	Input of 2 <sup>nd</sup> half bridge*
INH2	Output	Enable of 2 <sup>nd</sup> half bridge*
APWM	Output	Alternating PWM
AFW	Output	Alternating freewheeling
Q	Output	Counter Q0 output, debugging only

Table 4.3 presents the IO configuration of the alternating freewheeling control circuit for BLDC motors (based on Fig. 4.15 and Fig. 4.16).

Table 4.3 BLDC motor control logic circuit IO signals

IO port name	Port direction	Port signal meaning
DIR	Input	Motor rotation direction control
BL	Input	Switch to BLDC mode
Enable	Input	Enable (high) input signal
PWM	Input	PWM signal from the microcontroller
H1, H2, H3	Input	Hall sensor input signals
IN1	Output	Input of 1 <sup>st</sup> half bridge*
INH1	Output	Enable of 1 <sup>st</sup> half bridge*
IN2	Output	Input of 2 <sup>nd</sup> half bridge*
INH2	Output	Enable of 2 <sup>nd</sup> half bridge*
IN3	Output	Input of 3 <sup>rd</sup> half bridge*
INH3	Output	Enable of 3 <sup>rd</sup> half bridge*
APWM	Output	Alternating PWM, debug only
AFW	Output	Alternating freewheeling, debug only
Q	Output	Counter Q0 output, debug only

\* According to Table 4.1

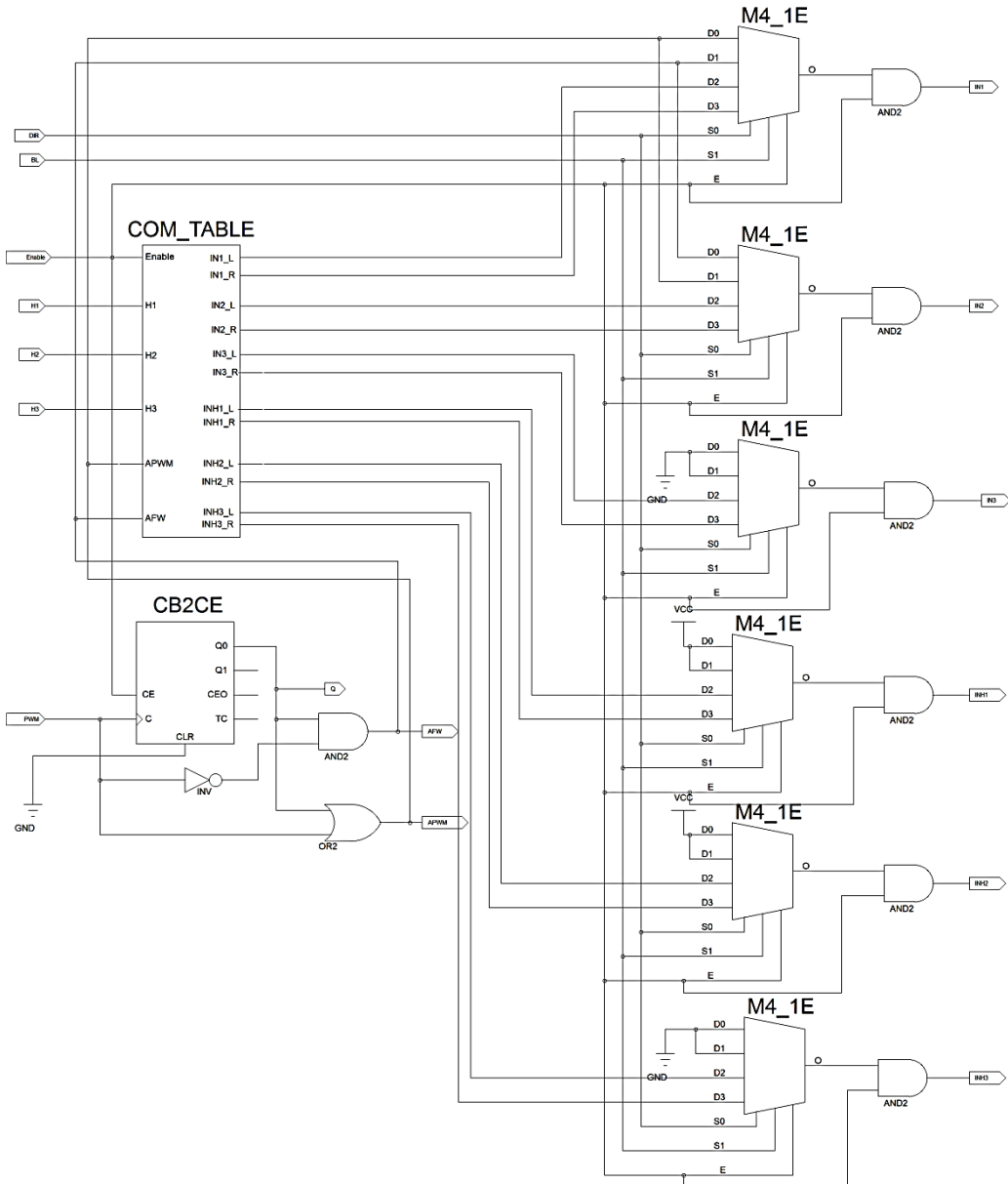


Fig. 4.15 Alternating freewheeling implementation for BLDC motor control 3 phased Bridge

The alternating freewheeling command signals for BLDC driving three phased bridge are again obtained using the CB2CE counter unit. The BLDC motor phases are commutated using the COM\_TABLE unit which sets the output vector according to the hall sensor inputs (H1, H2 and H3) and the direction input (DIR). The schematic of the commutation table is presented in the next Fig. 4.16. Basically the circuit contains two look-up tables implemented with six M8\_1E mux circuits. The upper six MUX circuits are for the counter-clockwise rotation direction and the bottom MUX circuits are for clockwise rotation direction. The output phase drive

input signals then are selected from this two look-up table outputs based on the direction DIR input signal.

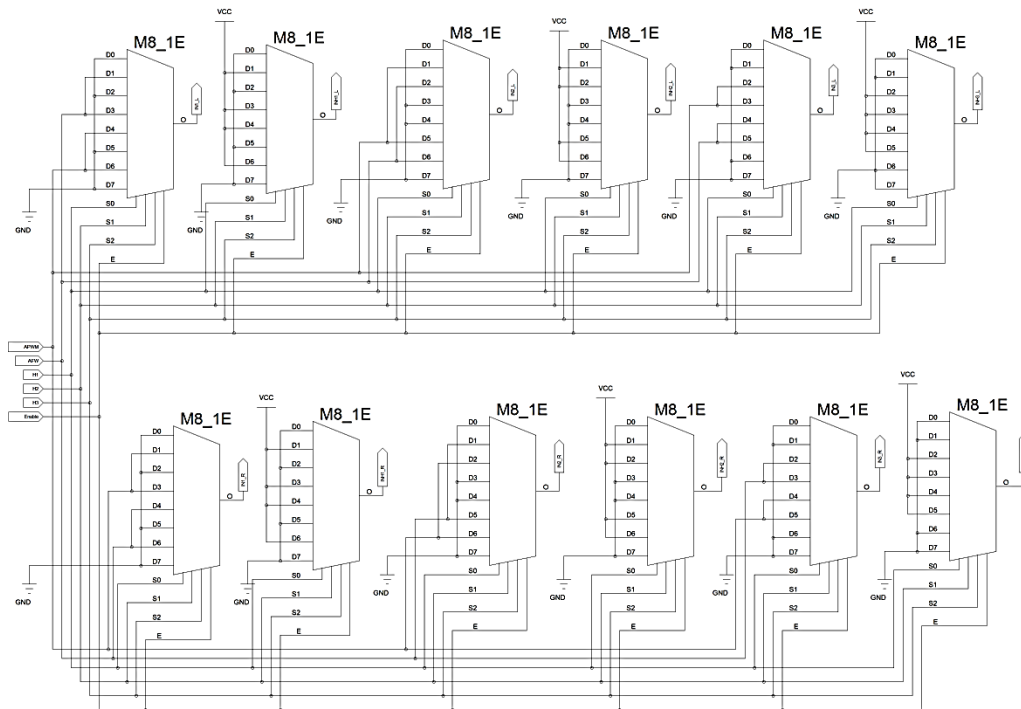


Fig. 4.16 Commutation look-up table implementation schematic

The following picture (from Fig. 4.17) presents the actual experimental setup based on the block schematic principle presented in Fig. 4.13. It can be seen on the left side of the picture the evaluation board with the CPLD and on the right side the BLDC motor evaluation board containing the microcontroller, the MOSFET gate driver circuit and the six power MOSFET's of the three phased inverter. The inverter driver can be configured to use only the first two half bridges for DC motor control H-Bridge.

During the evaluations instead of real motor, spare loads have been used (resistor and coil circuit in series connection). This helps to avoid the change of the load current due to heating of the motor windings, mechanical load changes etc. The DC motor H-Bridge evaluation spare load has the following parameters:  $150\text{m}\Omega + 250\mu\text{H}$ . The BLDC motor simulation was done using three spare loads connected in delta configuration (for maximum possible load currents) with the following parameters for each winding:  $250\text{m}\Omega + 180\mu\text{H}$ .

For BLDC motor driver bridge the phase commutation needs to be done according to the input hall signals, as it would do when driving a real BLDC motor. Therefore the hall signals have been simulated using three digital output ports of the microcontroller. The hall sequence commutation frequency was set to 1KHz.

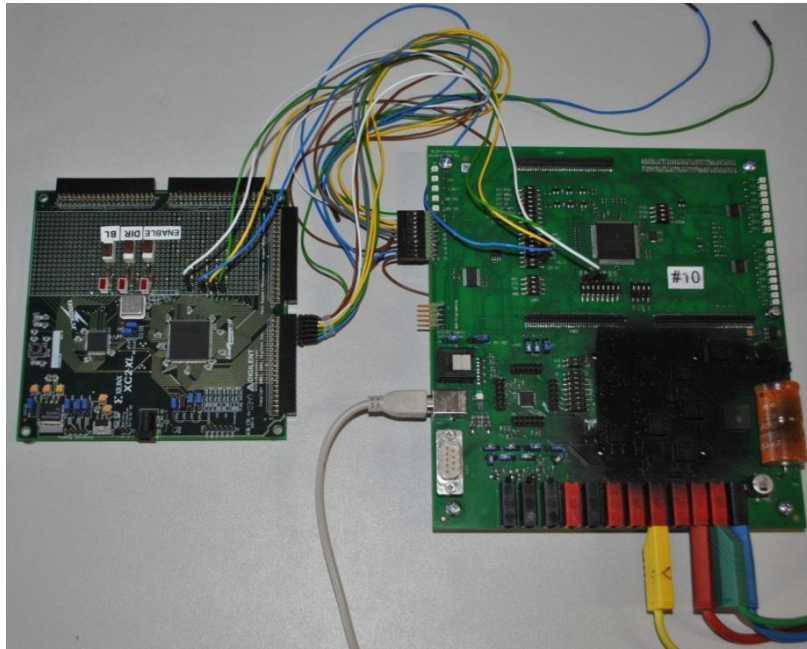


Fig. 4.17 Alternating freewheeling experimental bench setup

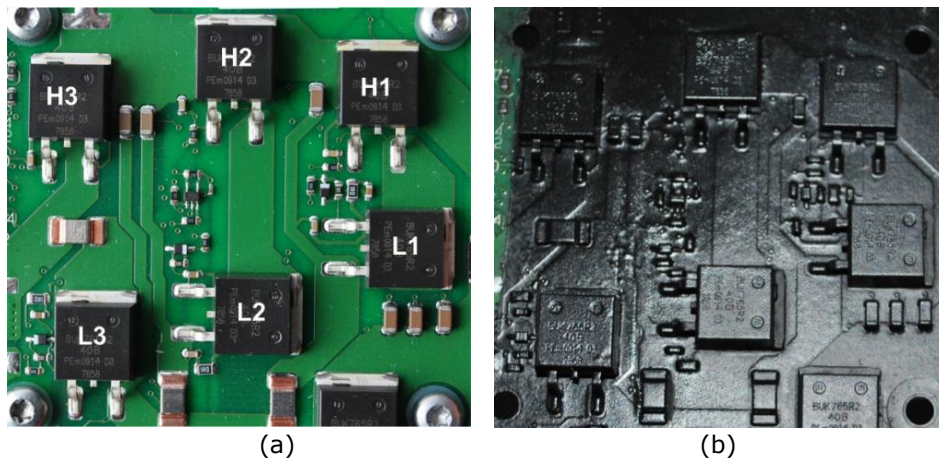


Fig. 4.18 Three phased bridge MOSFET's displacement

The temperature measurements were conducted using a FLIR T365 thermal camera. The measurements were done using the experimental board having no heat-sink mounted on the power MOSFET's, making the thermal differences more visible. The placement of the MOSFET's can be seen in Fig. 4.18 (a). Before the thermal imaging measurements the power MOSFET's area of the evaluation board has been painted black. This ensures a homogenous thermal radiation property over the board surface obtaining very accurate thermal imaging results.

Before thermal imaging the alternating freewheeling test circuit has been evaluated for correct operation. The three phase bridge signals are presented in Fig. 4.19 and Fig. 4.20.

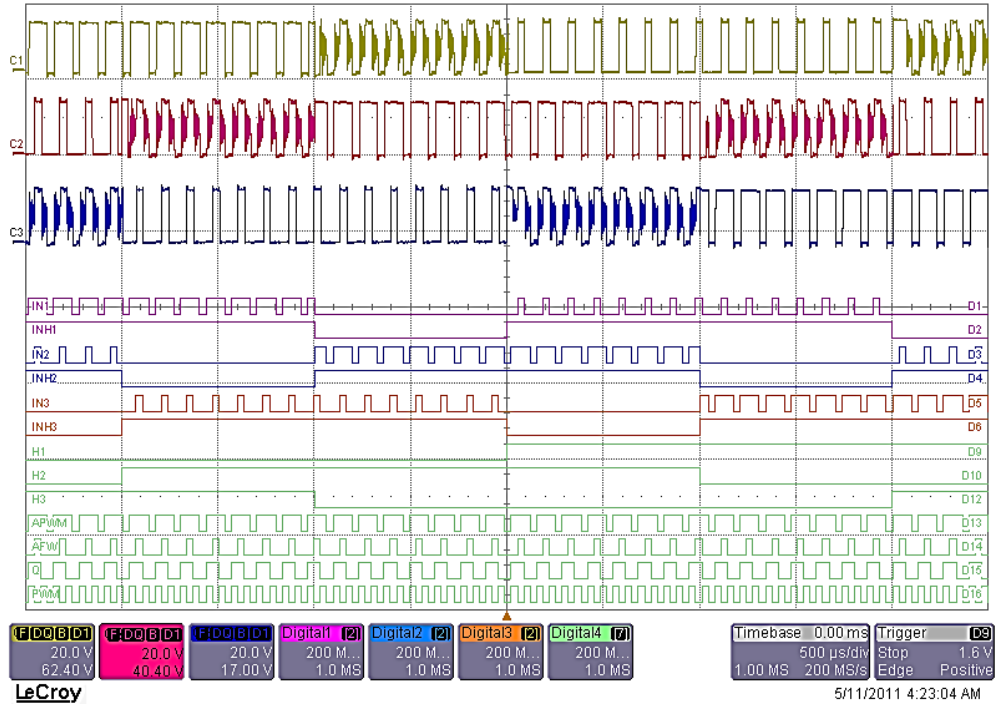


Fig. 4.19 BLDC Alternating freewheeling signal measurement\*

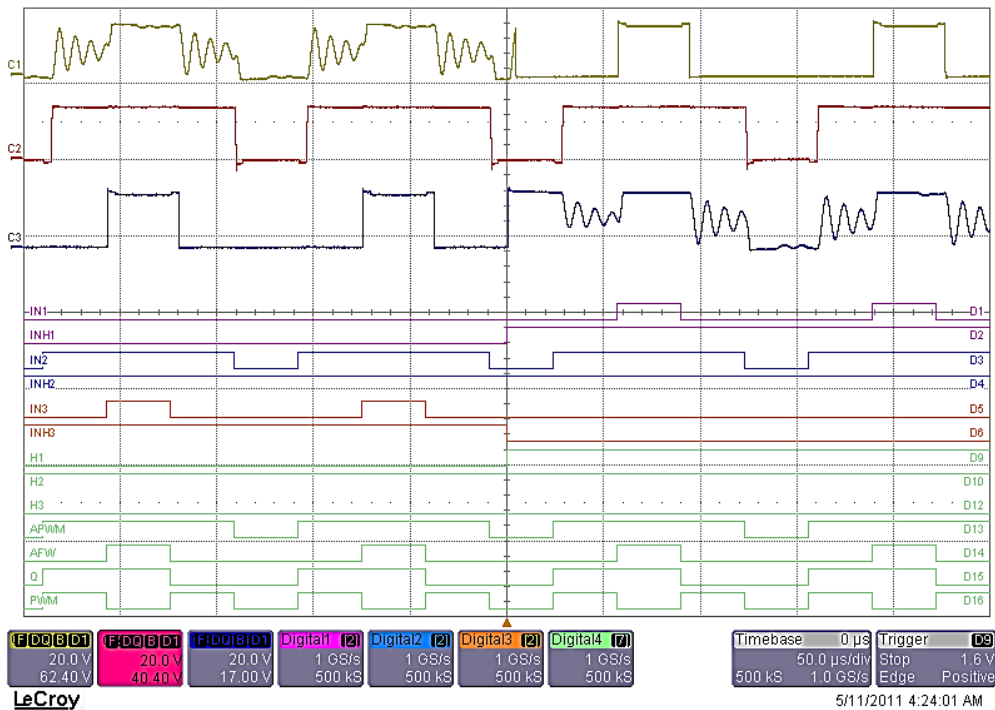


Fig. 4.20 BLDC Alternating freewheeling signal measurements zoomed\*

\*Legend CH1 – Phase U, CH2 – phase V, CH3 – Phase W; digitals named in the picture

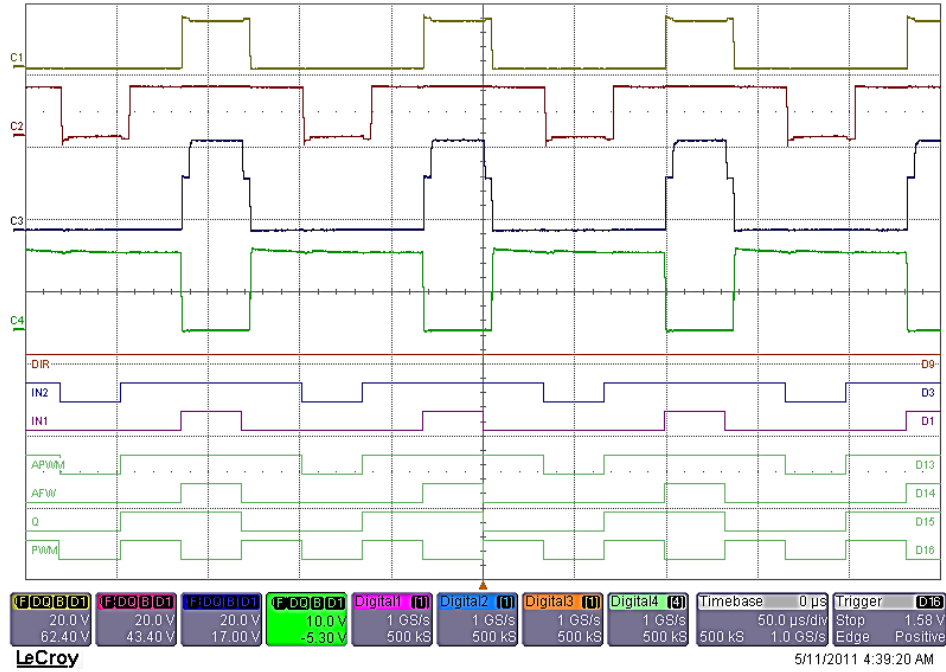


Fig. 4.21 H-Bridge alternating freewheeling signal measurements

Legend: CH1 – Motor A, CH2 – Motor B, CH3 – Gate H1, CH4 - Gate L1; digital signals labeled in the picture

In the next two graphs, the thermal imaging evaluation results are presented in a graphic form, for BLDC motor driver configuration in Fig. 4.22 and for DC in Fig. 4.23. The continuous lines show the alternating freewheeling measurement results, with dotted lines (for comparison) the classical LS freewheeling method measurement results are presented.

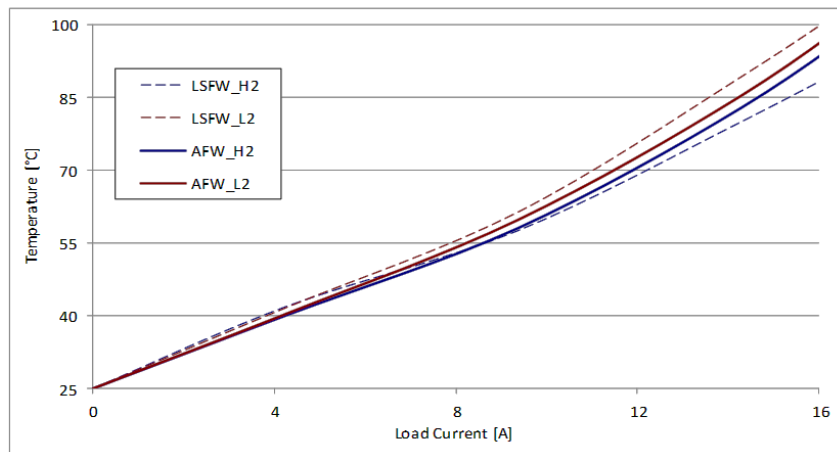


Fig. 4.22 Thermal analysis results for BLDC motor driving bridge (dotted line - classical LS freewheeling)

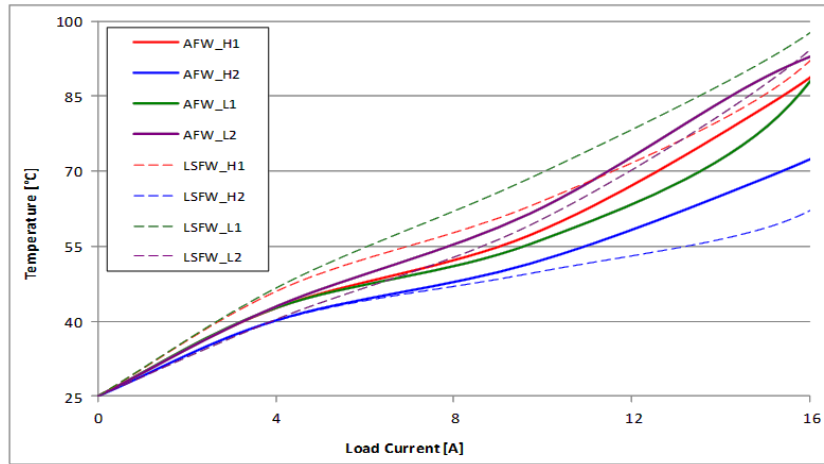


Fig. 4.23 Thermal analysis results for DC motor driving bridge (dotted line - classical LS freewheeling)

The next two figures present thermal imaging pictures taken during the evaluation at different PWM duty cycles. Fig. 4.24 presents the thermal images of the three phased bridge and Fig. 4.25 for H-Bridge configuration. The measurements have been done using 14V battery voltage and 15KHz PWM frequency.

A disadvantage of the method is that at high duty cycles (typically over 90-95%) combined with high switching losses the method has no benefit at all, because the static power saved at the active LS transistor (which is conducting during the PWM ON) is smaller than the added switching loss, ending up with a higher power consumption as for the classical LS freewheeling method. Nevertheless considering that in most of the applications the bridge is not driven continuously at high duty cycles (over 90%) the method still has the benefit of better power distribution for the system typical operating conditions. The method has considerable benefit only if the bridge MOSFET's are isolated thermally, otherwise a common heat sink mounted on the power MOSFET's with low thermal resistance leads to insignificant power distribution improvement.

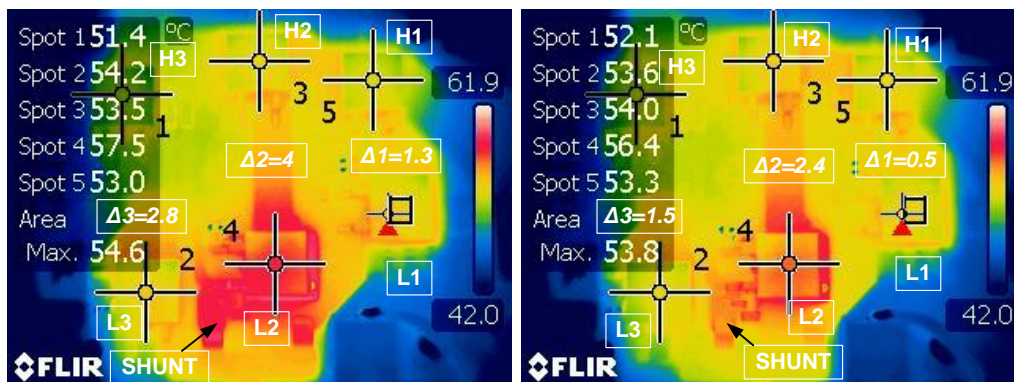


Fig. 4.24 Thermal analysis results –at 10A, 14V battery voltage, BLDC drive configuration

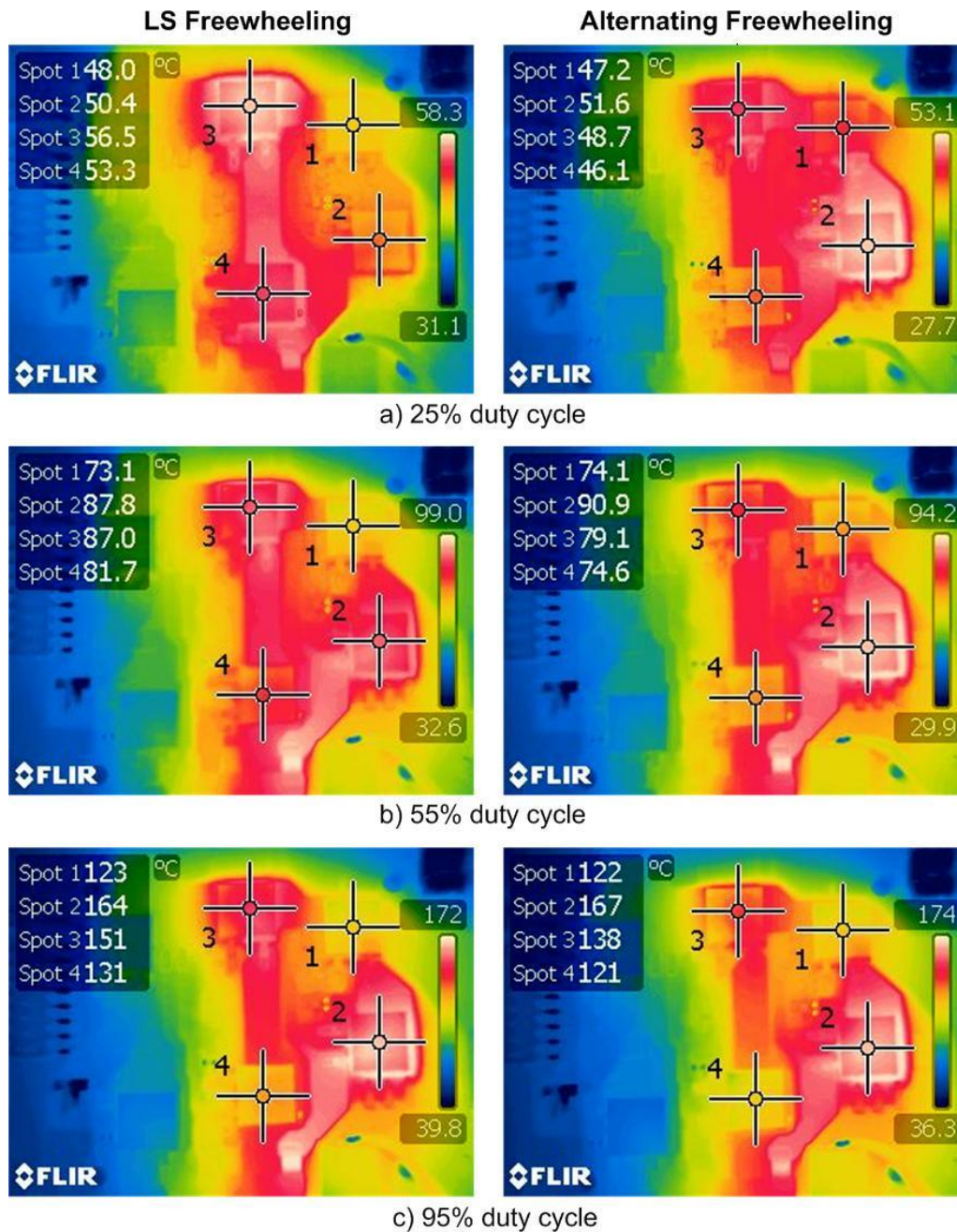


Fig. 4.25 Thermal measurement pictures for DC mode



## Summary

This chapter presents an implementation of an advanced gate driving method for three phased BLDC motor driver power inverter circuits, called "alternating freewheeling" method. The basic idea used in the proposed method is the alternation of the freewheeling path (high and low side) for each consecutive PWM period. A similar idea has been suggested in [212] for DC motor driver H-bridges. Nevertheless the method has not been fully developed and evaluated for DC motor driving H-Bridges, in addition the author extends the alternating freewheeling concept for BLDC motor driving three phased power inverter circuits.

The second subchapter briefly presents the proposed concept. The author proposes a calculation method (equations) for the MOSFET's power consumption, with very good estimation accuracy, demonstrated by comparison with simulation results presented in the third subchapter.

As mentioned the third subchapter presents the simulation and experimental (using thermal imaging) results, in comparison to the classical low side freewheeling method, for both DC motor driver H-Bridge and BLDC motor driver three phased power inverter.

The great advantage of the method is the lifetime extension of the switching elements and the increase of the maximum output power due to better power distribution. The method is demonstrated using MOSFET's as switching component, nevertheless it can also be applied to similar motor driving bridges using bipolar transistors, thyristors, IGBT's or other active switch types.



## 5 Hardware implemented field-weakening BLDC motor control

This chapter presents a new advanced field weakening implementation method proposed by the author. The method has been presented during the 15<sup>th</sup> WSEAS conference of 2011 on circuits and systems held in Corfu, Greece, with the paper "Hardware Implementation of Field-Weakening BLDC Motor Control" [5].

### 5.1 Field weakening operation

The torque output of a brushless motor is constant over a speed range limited by the power electronic converter ability to maintain the demanded phase currents at the required level. Fast and accurate control of the phase winding current is only possible if the supply voltage is larger than the back-EMF voltage amplitude. The speed at which the back-EMF voltage effective amplitude is equal to the supply voltage is referred as the maximum normal operating speed or base speed. Fig. 5.1 presents the torque versus speed characteristics of a BLDC motor. The motor can run over its base speed in the field-weakening mode, in which a component of the phase winding current produces a magnetic field opposing the permanent magnet field and reducing the effective back-EMF voltage amplitude. Field weakening can be accomplished by increasing the phase angle by which the current leads the back-EMF voltage [16]. This method is also called phase-advanced drive. Fig. 5.2 shows the vector representation of the field weakening. The graph from Fig. 5.3 presents the normalized speed output of a BLDC motor in respect to its base speed versus the phase advance angle under no load conditions [181], [183]-[187], [190]-[193] [207].

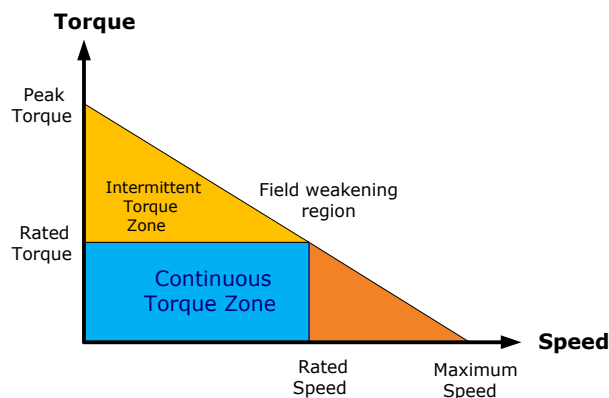


Fig. 5.1 Torque VS speed characteristic of a BLDC motor

This phase advance allows fast current rise before the "occurrence" of the back-EMF. (assuming a  $PM$  span angle  $a_{PM} < 150^\circ - 160^\circ$ ) An approximate way to estimate the advance angle required  $a_{ar}$ , for  $120^\circ$  conduction, may be based on linear current rise to the value  $I$ :

$$(a_a)_{120^\circ} = \omega_r \frac{L_s \cdot I}{V_{dc}}; \quad \omega_r = 2 \cdot p \cdot n \cdot \pi \quad (5.1)$$

- where with  $n$  denoting the rotor speed in revolutions per second (rps),  $V_{DC}$  the supply voltage,  $L_s$  the phase inductance and  $p$  the number of magnetic pole pairs of the rotor;

The phase advance is usually implemented using software resources of the system microcontroller. The motor control algorithm commands the power inverter to switch to the next commutation step with a pre-defined time before the actual next commutation point, indicated by the hall signals. In order to achieve this, the control algorithm must estimate the time when the next hall signal commutation will occur, according to the rotor speed, acceleration/deceleration and calculate the phase pre-commutation time which will give the desired phase angle advance [182]. The implementation of these phase advance methods on microcontrollers requires significant computational power which is not available in most of automotive ECU's (Electronic Control Unit) which control BLDC actuators. As an example some double clutch automatic transmission control unit uses four BLDC motor actuators to control the automatic gearbox. Beside the control of the BLDC motors, the system microcontroller has several other tasks assigned to, like the shifting algorithm, diagnosis of the system, read and interpret signals from several different sensors, communication with the rest of the automobile ECUs etc. Therefore in most of the systems the computational power required for a high performance field weakening algorithm implementation is not available.

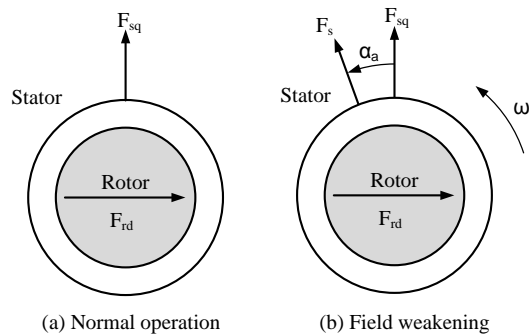


Fig. 5.2 Field weakening vector representation

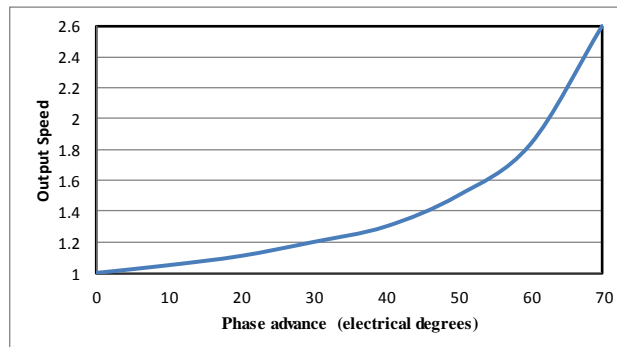


Fig. 5.3 Normalized speed output in respect to base speed for a BLDC motor

## 5.2 Phase advance implementation using rotary encoder

The sensed rotor position detecting methods and driving algorithms are detailed in chapter 1.3.1. The phase advance or field weakening method presented in this chapter is based on advanced rotary encoder ASIC, using hall position sensing technology developed specially for BLDC motor drive purpose [188], [205].

The rotor position is sensed by the rotary encoder circuit placed exactly beneath the rotor shaft Fig. 5.4 (a). A small magnet is attached to this shaft, with the magnetic field poles configuration as shown in Fig. 5.4 (b) (one pole pair magnet).

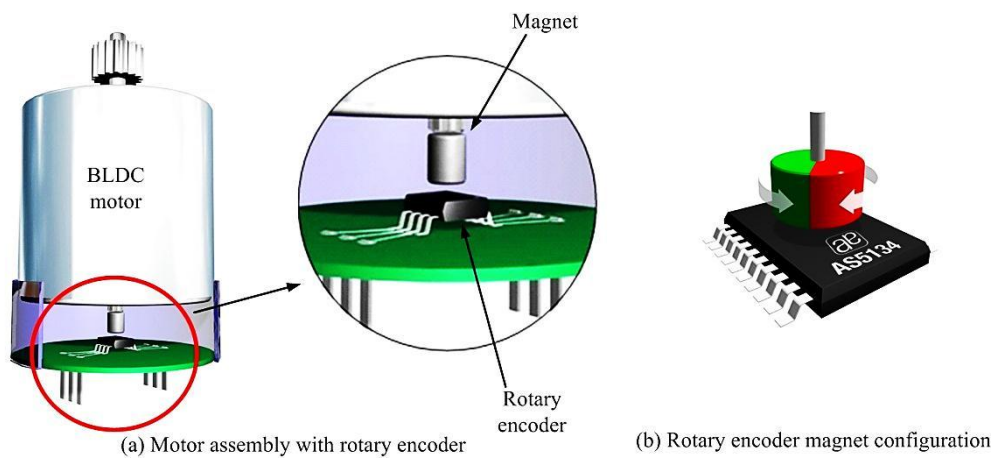


Fig. 5.4 Assembly of rotary position encoder

The BLDC optimized rotary encoder provides three output hall position signals (U, V, W outputs, from Fig. 5.5) simulating three separate halls cells. Fig. 5.5 presents the internal block schematic of such a rotary encoder developed by Austria Micro Systems, the AS5134. The small magnet used for the position sense has one pole pair, therefore the encoding period of the internal hall cells is a complete 360° mechanical. The internal logic of the sensor divides this complete mechanical period to several complete electrical periods (configurable 1 to 6) according to the number of magnetic pole pairs of the employed BLDC motor.

Before this encoder can be used as rotor position sensor and provide correct hall signals the following steps must be followed:

- Configure the number of rotor magnetic pole pairs;
- Calibrate the "zero position" of the encoder;

The initial "zero position" must be calibrated together with the BLDC motor in order to align the BLDC motor zero position and with the rotary encoder zero position. Fig. 5.6 presents the zero position calibration procedure. First the rotor of the BLDC motor is aligned with the "zero position", by applying a voltage vector which will move the rotor in the desired position. The rotary encoder angle indication is read out from the sensor and stored. Then the application software can set the rotary encoder zero position via SPI command. There is also a possibility to program this zero angle position in the chip OTP memory, in case no further change is done by the application over the stored initial zero position.

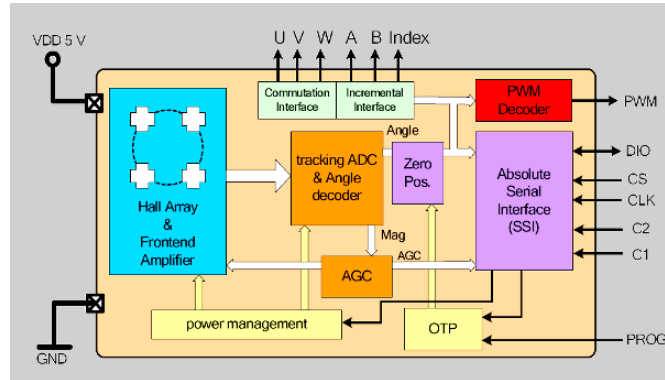


Fig. 5.5 Magnetic rotary encoder ASIC block diagram [188]

The original intention of this programmable zero angle is the calibration of the sensor itself, to match the zero position angle of the BLDC motor rotor.

This programmable zero position of the rotary encoder gives the possibility of the implementation of a hardware phase advanced drive. In case the initial position is programmed with a certain angle offset the rotary encoder will generate the three hall signals with a pre-advanced angle. Therefore the software application task is only the set of the phase advanced zero angle position and the sensor itself will generate the hall signals with a constant advance in phase with the desired angle. Via this method no considerable computational power is needed for the phase advance, now done very precisely by the rotary encoder regardless of rotor speed or acceleration, the phase advance is in every case equal with the predefined angle.

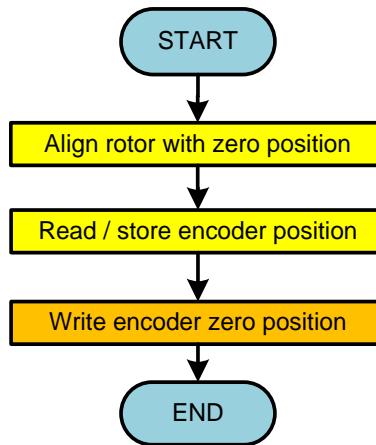


Fig. 5.6 Flowchart of zero position calibration

As example if the zero position of the rotor corresponds to  $a_0 = 50^\circ$  (mechanical) of the encoder, the encoder will always subtract from his measured position angle  $a_e$  the  $50^\circ$ . This can be described as follows:

$$a_r = a_e - a_0 \quad (5.2)$$

- where  $a_r$  represents the current rotor position,  $a_0$  the zero angle correction,  $a_e$  the measured angle by the rotary encoder;  
Based on this equation (5.2) and considering the number of pole pairs of the rotor the phase advanced rotor position can be expressed as follows:

$$a_r = a_e - \left( a_0 + \frac{a_{advance}}{polepairs} \right) \quad (5.3)$$

- where  $a_{advance}$  represents the desired phase advance electrical angle.  
From this equation we can derive the zero position command  $a_0$  to the encoder which advances the hall signals with the desired angle:

$$a'_0 = a_0 + \frac{a_{advance}}{polepairs} \quad (5.4)$$

### 5.3 Field weakening implementation experimental results and setup

To demonstrate and validate the concept a test setup was built, the block diagram is presented in Fig. 5.7.

The BLDC motor used is equipped with a magnetic rotary encoder AS5134, the three hall output signals of this sensor are used as rotor position information for the three phased inverter controller ASIC.

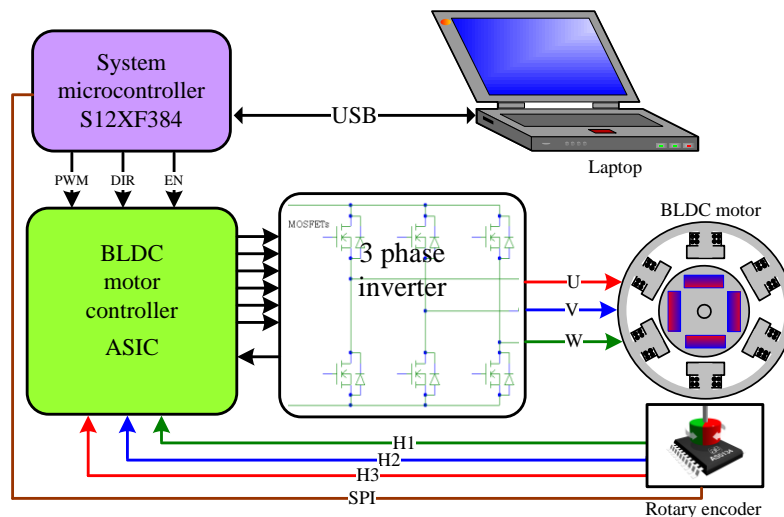


Fig. 5.7 Field weakening implementation experimental setup

The BLDC motor controller ASIC has its input signal from the system microcontroller PWM, DIR (direction), EN (enable) and the rotary encoder hall

signals. The six step commutation table is implemented inside the ASIC and provides the six gate signals for the inverter MOSFET's.

The system microcontroller is connected via USB interface to a PC application from which the system operational parameters are set (like activate motor, set PWM duty cycle, motor direction, read and write the rotary encoder registers, etc.). The parameters of the employed BLDC motor are presented in Table 5.1.

To evaluate the motor performance change according to the applied phase advance, the motor was evaluated using a motor evaluation bench. The picture of this, Kistler 4503A2L00 type [189], is presented in Fig. 5.8.

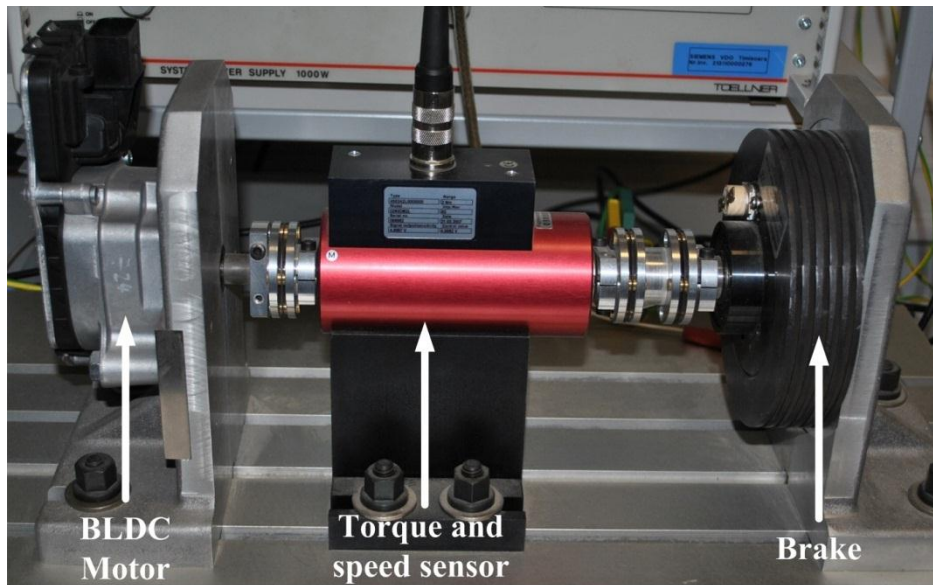


Fig. 5.8 BLDC Motor evaluation bench setup

Table 5.1 Parameters of the BLDC motor used for field weakening evaluation

Number of stator poles	12
Number of rotor poles	8
Rated DC voltage	12V
Max phase current	50A
Back-EMF	$k_E = 3,7V/krpm$ ( $E_{10k}/krpm$ )

During the laboratory evaluation the motor was set with different zero angle programmed for the rotary encoder resulting in  $-40^\circ$ ,  $-20^\circ$ ,  $0^\circ$ ,  $20^\circ$  and  $40^\circ$  electrical angle phase advance ( $\pm 5^\circ$ ,  $\pm 10^\circ$  and  $0^\circ$  mechanical angle advance). The battery voltage used for this evaluation was set to 14V, the applied duty cycle of the PWM driving signal was set to 100%. The speed versus torque characteristic of the motor was evaluated for each case, the results are presented in Fig. 5.9. It can be observed that the phase advance causes increase in the maximum speed and torque for the same operating conditions like battery voltage and applied PWM duty cycle.

To be able to perform the evaluation of the proposed method using the Kistler motor evaluation bench an automatic test system has been set up, presented in Fig. 5.10.



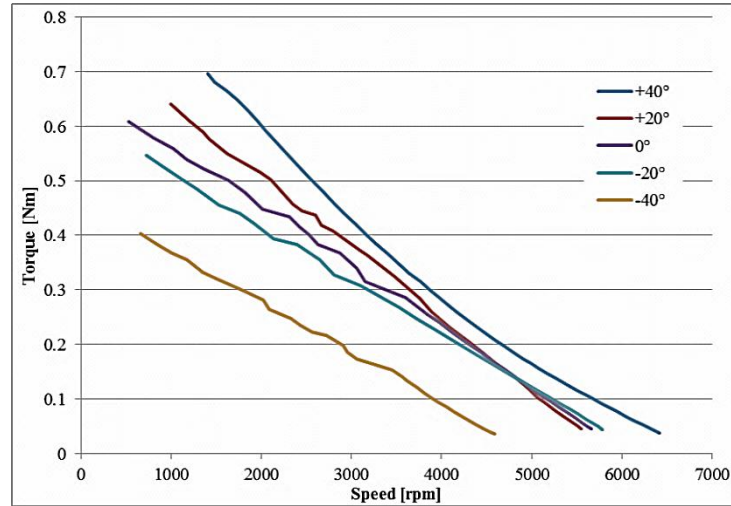


Fig. 5.9 Torque VS Speed for different phase advance angle

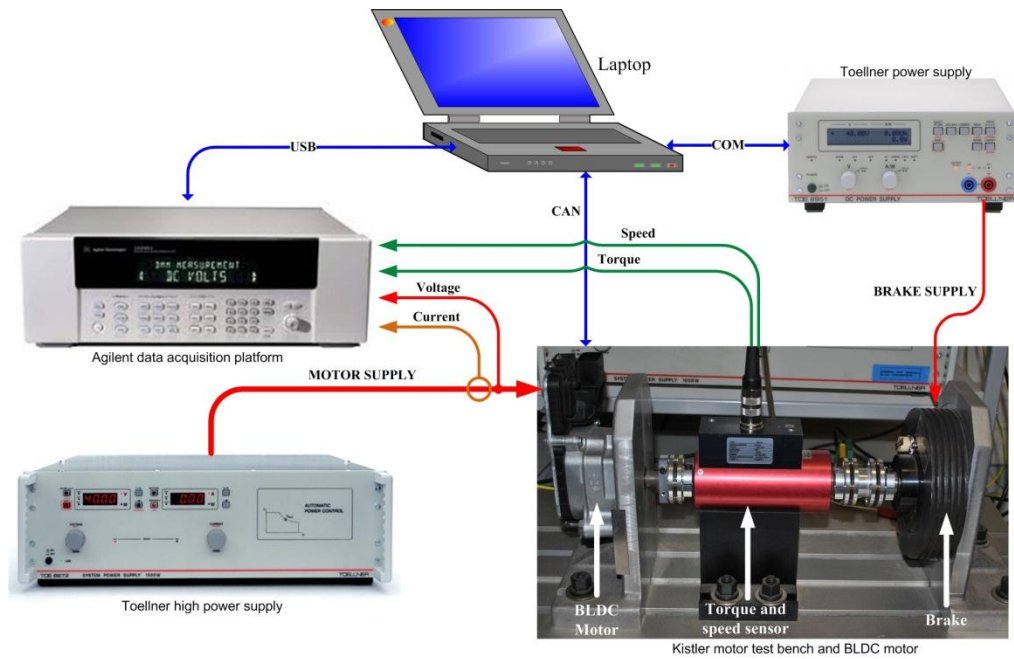


Fig. 5.10 Automatic motor evaluation test system

- The motor evaluation bench has the following main components:
- Kistler Motor test bench
    - BROSE, BLDC motor;
    - Torque and Speed sensor;
    - Electromagnetic brake;
  - TOE8872-40 programmable high power supply – used to supply the BLDC motor three phased power inverter;

- TOE8951 programmable power supply – used to control the electromagnetic brake;
- Agilent 34980A data logger;
- PC application to control the instruments (developed by the author);

For this motor evaluation test system a PC application has been developed using LabWindows/CVI v8.5 development environment. The application can control the motor operational parameters (set supply voltage, brake strength) and measure/store the BLDC and control electronics operational parameters (generated speed, torque, load current and supply voltage). The instrument communication and setup panel is shown in Fig. 5.11. On this interface panel, the communication parameters with the programmable power supply communication can be configured (used to set the voltage applied to the electromagnetic brake – control the brake power) and the used input channels of the Agilent data logger to which the torque, speed, load current and voltage signals are connected.

The motor parameter evaluation can be done in two modes manually and automatically. In the manual mode (panel presented in Fig. 5.12) the user can set brake voltage level and measure the actual torque, generated by the BLDC motor, the rotational speed, the power inverter electronics supply voltage and load current. There is also a possibility to extract from the total supply current the motor control electronics quiescent current (when the motor is stopped), subtracting this value the current consumed by the BLDC motor and the power MOSFET's can be calculated. Using this data the application can automatically calculate the generated mechanical power, the consumed electrical power and the efficiency of the BLDC motor for the given operating point.

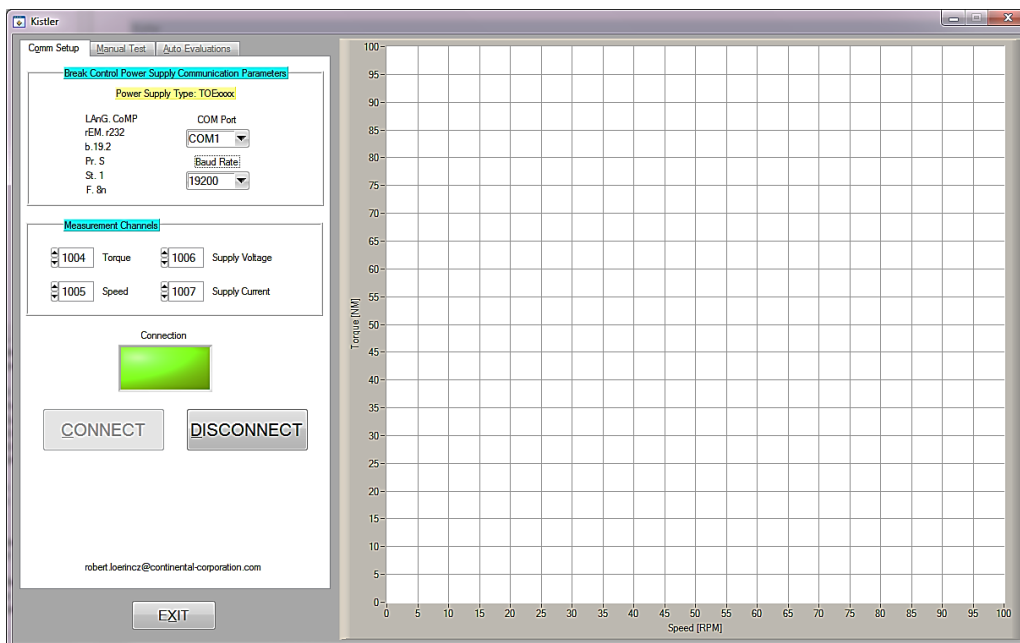


Fig. 5.11 Kistler motor test bench control application setup panel

### 5.3 - Field weakening implementation experimental results and setup 171

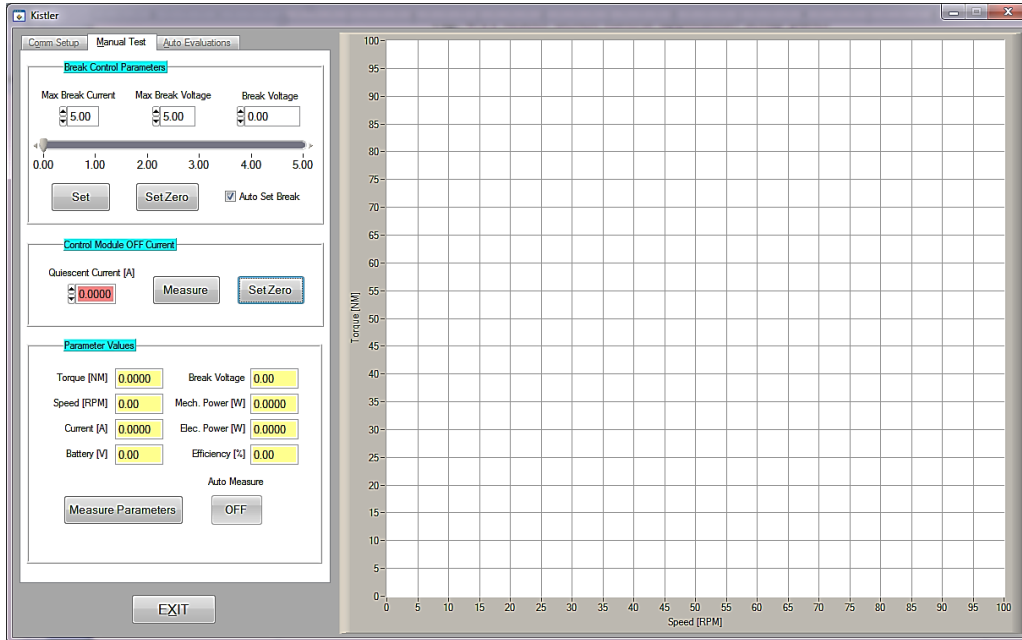


Fig. 5.12 Kistler motor test bench control application manual evaluation panel

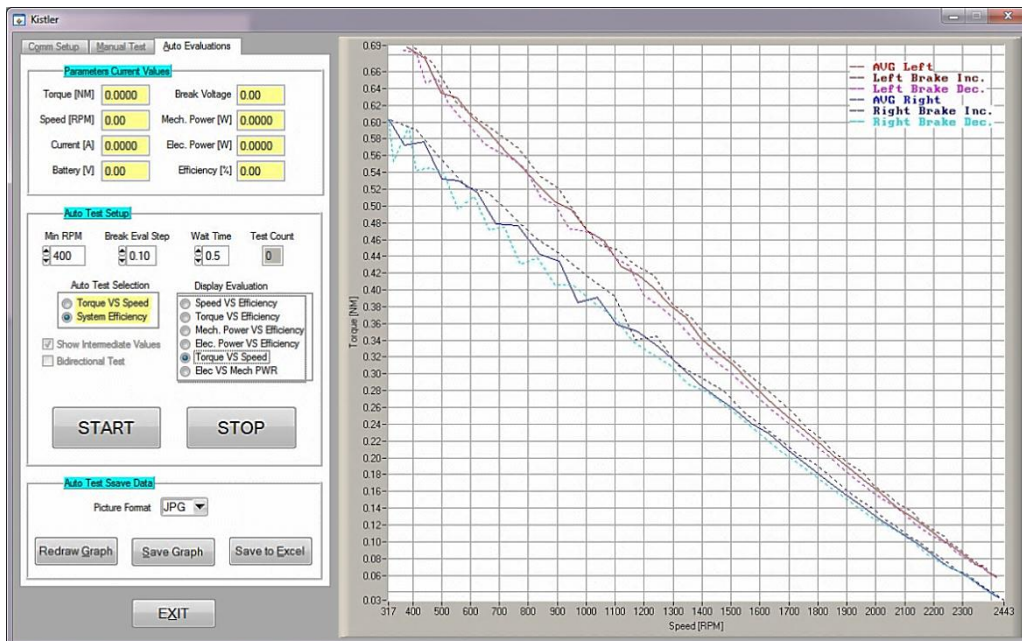


Fig. 5.13 Kistler motor test bench control application auto evaluation panel

In automatic evaluation mode (interface panel presented in Fig. 5.13) the application increases the brake power until the motor is at 10% of its maximum measured speed (without any brake) after which the brake power decreased until the braking is completely stopped. During the evaluation the operating parameters

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of the BLDC motor (speed & torque) and control electronics (supply voltage & load current) are acquisitioned. The collected measurements are than used to calculate and graphically present the BLDC motor and control electronics operational curves like:

- Torque VS Speed;
- Speed VS Efficiency;
- Mechanical Power VS Efficiency;
- Electrical Power VS Efficiency;
- Electrical power VS Mechanical Power;

The application can repeat the evaluation up to ten different operating points of the BLDC motor, presenting the result on the same graph for comparison proposes. The resulted graph picture can be saved or the measurement data can be exported into a Microsoft excel file for further evaluation and analysis. An example of the generated file is presented in the next Fig. 5.14.

Efficiency Evaluation Measurement Results															
Report created by KISTLER Auto tester															
Report date: 2011.4.21 - 15h:2m:4.8s															
Meas.	Motor Speed [RPM]			Motor Torque [NM]			Battery Voltage [V]			DC Current [A]			Elec. PWR. [W]	Mech. PWR [W]	Efficiency [%]
Nr.	Brake +	Brake -	Average	Brake +	Brake -	Average	Brake +	Brake -	Average	Brake +	Brake -	Average	PWR. [W]	PWR [W]	[%]
1	6336.2	6310.2	6323.2	0.0308	0.0336	0.0322	13.82	13.82	13.82	4.395	4.468	4.432	61.24	21.3	34.78
2	6308.6	6257.7	6283.2	0.0327	0.0377	0.0352	13.82	13.81	13.81	4.491	4.624	4.558	62.95	23.16	36.78
3	6283.9	6202.2	6243	0.035	0.0425	0.0388	13.81	13.8	13.81	4.588	4.833	4.71	65.04	25.34	38.96
4	6256	6153.1	6204.6	0.038	0.047	0.0425	13.81	13.79	13.8	4.709	5.033	4.871	67.23	27.63	41.09
5	6217.9	6102	6159.9	0.0411	0.0524	0.0467	13.8	13.79	13.79	4.869	5.225	5.047	69.62	30.15	43.3
6	6176	6026.7	6101.3	0.045	0.0594	0.0522	13.79	13.78	13.78	5.056	5.524	5.29	72.92	33.36	45.75
7	6124.4	5933.5	6029	0.0495	0.0687	0.0591	13.78	13.76	13.77	5.293	5.828	5.561	76.59	37.32	48.73
8	6053.4	5785.1	5919.3	0.056	0.0816	0.0688	13.77	13.74	13.76	5.596	6.347	5.972	82.16	42.66	51.93
9	5955.8	5633.2	5794.5	0.0652	0.0957	0.0804	13.76	13.72	13.74	5.995	6.992	6.493	89.2	48.81	54.72
10	5858.4	5510.5	5684.4	0.0743	0.1071	0.0907	13.74	13.7	13.72	6.347	7.495	6.921	94.95	54.01	56.88
11	5753.5	5407.5	5580.5	0.0843	0.1167	0.1005	13.72	13.68	13.7	6.8	7.943	7.372	101	58.72	58.14
12	5643.3	5330	5486.6	0.095	0.1238	0.1094	13.7	13.67	13.68	7.289	8.218	7.754	106.1	62.86	59.25
13	5519.5	5242.4	5381	0.1077	0.1322	0.1199	13.68	13.65	13.67	7.803	8.57	8.187	111.9	67.59	60.4
14	5401.7	5187.4	5294.5	0.1195	0.1376	0.1286	13.66	13.64	13.65	8.323	8.839	8.581	117.13	71.29	60.86
15	5293.9	5142.4	5218.1	0.1317	0.1416	0.1366	13.64	13.63	13.64	8.824	9	8.912	121.53	74.66	61.43
16	5158	5072.1	5115.1	0.1455	0.1485	0.147	13.62	13.62	13.62	9.368	9.255	9.312	126.85	78.74	62.07
17	5182.2	4962	5072.1	0.1431	0.1595	0.1513	13.63	13.61	13.62	9.166	9.667	9.417	128.25	80.36	62.66
18	5180.2	4819.4	4999.8	0.1434	0.1745	0.1589	13.63	13.59	13.61	9.177	10.232	9.704	132.07	83.22	63.01
19	5180	4625	4902.5	0.1434	0.1958	0.1696	13.63	13.55	13.59	9.187	11.11	10.149	137.95	87.07	63.11
20	5189.4	4383.7	4786.6	0.1426	0.2237	0.1832	13.63	13.51	13.57	9.177	12.101	10.639	144.4	91.81	63.58
21	5161.4	3976.1	4568.8	0.1452	0.2749	0.2101	13.63	13.44	13.54	9.328	14.057	11.692	158.26	100.51	63.51
22	5121.8	3752.8	4437.3	0.15	0.3058	0.2279	13.61	13.38	13.5	9.519	15.455	12.487	168.52	105.89	62.84
23	5053.1	3595.2	4324.2	0.1578	0.3281	0.2429	13.6	13.34	13.47	9.836	16.307	13.072	176.1	110	62.46
24	4960.5	3455.2	4207.8	0.1683	0.3489	0.2586	13.59	13.3	13.44	10.238	17.22	13.729	184.57	113.96	61.74

Fig. 5.14 Kistler test bench control SW excel report example

## Summary

A hardware implementation of phase advanced drive method of BLDC motors is presented in this chapter. In contrast to the classical software implementation of the phase advanced driving, this hardware implemented method requires significantly reduced computational power while maintaining the advanced angle accuracy even better than most of the existing software algorithms can perform. In addition the price difference of these rotary encoders for BLDC motor applications compared to the three separate hall sensors solution is insignificant or even cheaper.

A disadvantage of the current encoder technology is that there is no possibility to change the phase advance during the motor operation, because the encoder has to be set into configuration mode which disables the position signal generation. Nevertheless the future version of this encoder type (already under development) will be able to change the offset of the zero angle position during the motor operation.

For the proposed field weakening method performance demonstration and the BLDC motor characterization the author has defined an automatic test system and developed a powerful PC based control application for it.

Based on the developed method a scientific paper was elaborated and presented in the 17<sup>th</sup> WSEAS International Conference on Circuits and Systems, held in Corfu islands, Greece 2011 [5].



## 6 A new hall effect based speed sensor interface circuit

This chapter presents a Hall Effect based rotational and speed sensor interface circuit proposed by the author. The new concept was demonstrated via PSpice simulations and laboratory experiments. The proposed concept has been presented first time during the 14<sup>th</sup> WSEAS international conference on circuits in 2010. The paper with the title "A new Rotational Speed Sensor Interface Circuit with Improved EMC Immunity" has been published in the conference proceedings [3].

### 6.1 Review of rotational speed sensors

Today's modern cars are equipped with several driver assisting units creating a more comfortable and safer driving experience. Among these electronic units are the: ABS (Anti-lock Braking System), TCU (Transmission Control Unit), XCU (4 wheel drive Control Unit), ECU (Engine Control Unit), TCS (Traction Control System), ESP (Electronic Stability Program) etc. These systems are connected to several external or internal sensors which provide continuous information about the car parameters, driving conditions, inputs from the driver etc. Among the most important sensors for these systems are the position and speed sensors. These provide vital information about actuators position, rotational speed of different wheels/shafts of the car, based on which the electronic control units assist the driver.

There are several types of speed and position sensors developed in the last years, mainly based on the following technologies:

- Optical speed sensors;
- Inductive speed sensors;
- Magnetic (hall effect) speed sensors;

The optical sensors are based on a light sensitive unit (photodiode or phototransistor) which is masked from a light source (e.g. infrared LED) by a slotted disk [197]. The inductive speed sensors are based on a pick up coil excited by magnets placed on the rotating wheel [19] [198].

Fig. 6.1 presents a concept drawing of such an inductive speed sensor, where:

- 1 - Shielded cable;
- 2 - Permanent magnet;
- 3 - Sensor housing;
- 4 - Housing block;
- 5 - Soft-iron core;
- 6 - Coil;
- 7 - Air gap;
- 8 - Toothed pulse ring – for example the crankshaft of an automobile.

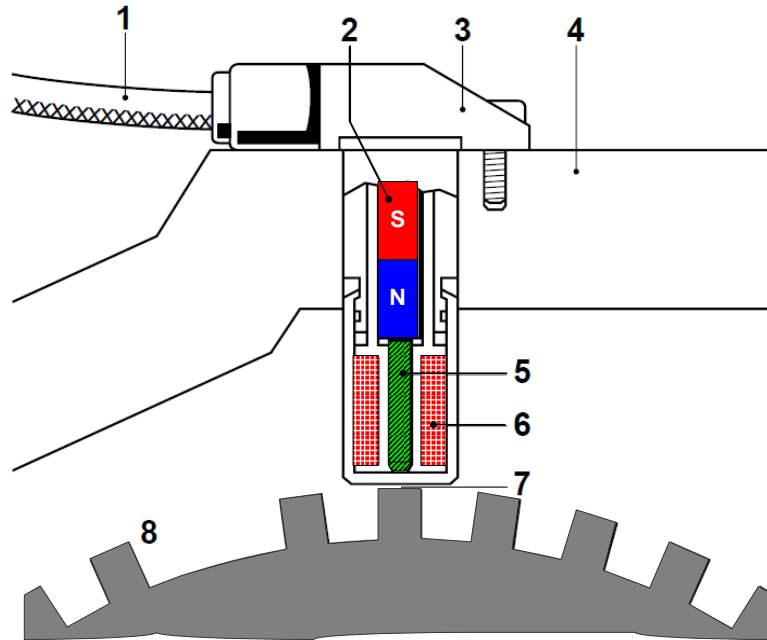


Fig. 6.1 Inductive speed sensor concept

The magnetic speed and position sensors based on Hall cell technology are the highest performance sensors [199]-[202], the detailed operating concept of such sensors is presented in the next subchapters.

## 6.2 Classical interface circuit

Today most of the wheel speed sensors used in new designs are Hall Effect based, which give the speed information encoded in the supply current of the sensor itself. In this way the wiring connections to the sensor is minimized to two wires [200], [203], [204]. Fig. 6.2 presents a connection scheme example of these sensor types. The speed information is encoded as current pulses in the sensor power supply line, using 7-14mA current levels. This current is fed into a shunt resistor at the receiver unit, which then compares the voltage drop on this shunt resistor with a reference voltage to detect the pulses. The Infineon TLE4953 series differential two-wire Hall Effect sensor IC (Integrated Circuit) using active target wheel generates a current pulse on its supply line each time a magnetic field transition occurs (see Fig. 6.3) [201]. In other sensor constructions the magnet is integrated inside the speed sensor and the magnetic circuit is closed by the external tooth wheel made of a ferromagnetic material (as in case of inductive speed sensors presented in Fig. 6.1) In addition some sensors can sense the rotational direction, information encoded in the generated pulse duration (see Fig. 6.4).

The pulses duration for the employed sensor type are:

- 60 $\mu$ s for left rotational direction;
- 120 $\mu$ s for right rotational direction;



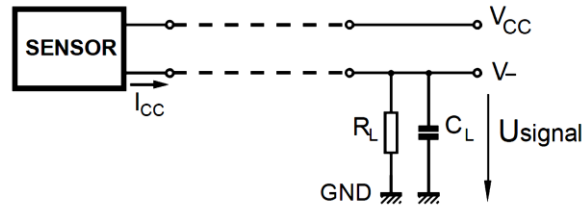


Fig. 6.2 Two wire speed sensor interconnecting diagram

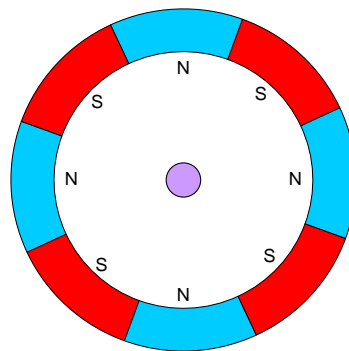


Fig. 6.3 Hall Effect speed sensing concept

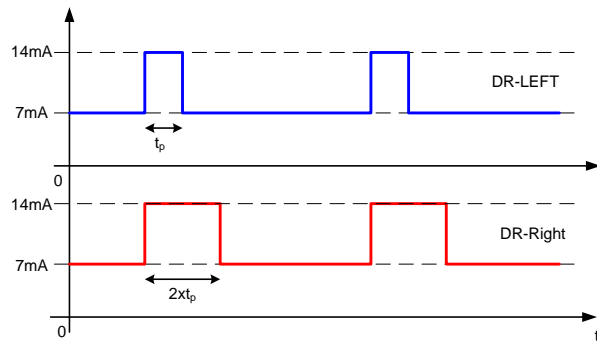


Fig. 6.4 Output signal and direction encoding

### 6.2.1 Typical speed sensor interface circuit

In Table 6.1 are listed the sensor supply current limits, according to its supplier specification [201].

The speed measurement itself is done by the system microcontroller, counting the number of pulses during a defined time period or measuring the time interval between two consecutive pulses. The rotation direction is detected in a separate evaluation process which employs the measurement of the pulse duration generated by the sensor.

In order that the microcontroller can count these pulses, an interfacing circuit is necessary, which converts the input current signal levels to TTL or CMOS logic levels

compatible with the microcontroller digital inputs. The basic circuit for this is using the voltage drop on the input shunt resistor fed to a voltage comparator circuit input which has a threshold voltage in the middle of the input voltage range.

The optimum threshold voltage can be expressed as follows:

$$V_{TH} = \frac{(I_{LO} + I_{HI}) \cdot R_S}{2} \quad (6.12)$$

- Where with  $V_{TH}$  denoting the optimal threshold voltage;  $I_{LO}$ ,  $I_{HI}$  – current high and low levels;  $R_S$  – shunt resistor;

Fig. 6.5 presents a typical application circuit example for the interface circuit between the speed sensor and the microcontroller digital input [200].

Table 6.1 Typical speed sensor worst-case supply current limits [201]

Parameter	Symbol	Limit Values			Unit
		Min.	Typ.	Max.	
Supply current	$I_{LO}$	5.9	7	8.4	mA
Supply current	$I_{HI}$	11.8	14	16.8	mA
Supply current ratio	$I_{HI}/I_{LO}$	1.9	-	-	-

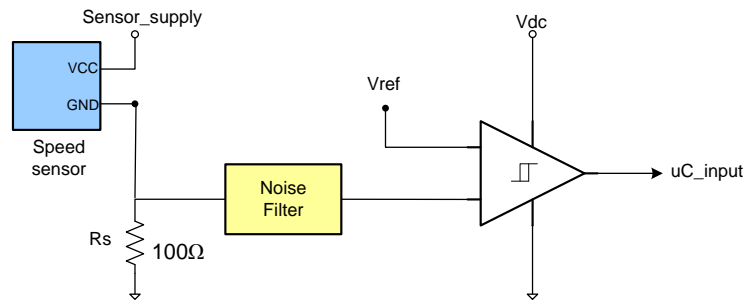


Fig. 6.5 Typical speed sensor microcontroller input interface circuit block diagram example

The voltage drop on the shunt resistor  $R_S$  filtered by a low pass filter circuit (usually RC filter) is fed into a voltage comparator which has its reference voltage given by equation (5.1). Fig. 6.6 presents the circuit behavior in typical conditions. Fig. 6.7 presents the circuit behavior for sensor supply current limits of a typical speed sensor. It can be observed that at the sensor supply current limit extremes the static threshold voltage  $V_{th}$  is very close to the drop voltage amplitude on the shunt resistance thus making the circuit very sensitive to input signal noises. The worst case limits of the sensor supply current presented in Fig. 6.7 are simulated using a simple current pulse generator connected in parallel with a sine wave offset current generator.

For automotive application the EMC performance of these circuits is very important, especially because these sensors are often placed far away from the electronic control unit and the connecting wire harness can act as an antenna picking up a lot of electro-magnetic disturbances, noises.

From this EMC point of view the performance of the typical application circuit is quite poor. To improve the immunity of the circuit, the comparator should be designed with hysteresis. The amount of hysteresis that can be applied is limited by the threshold voltage  $V_{th}$  accuracy, the shunt resistor accuracy  $R_S$  and the  $I_{HI}$ ,  $I_{LO}$  limits of the currents given by the speed sensor.

The typical hysteresis that can be applied can be expressed as follows:

$$V_{hyst\_TYP} = (I_{HI} - I_{LO}) \cdot R_S \quad (6.13)$$

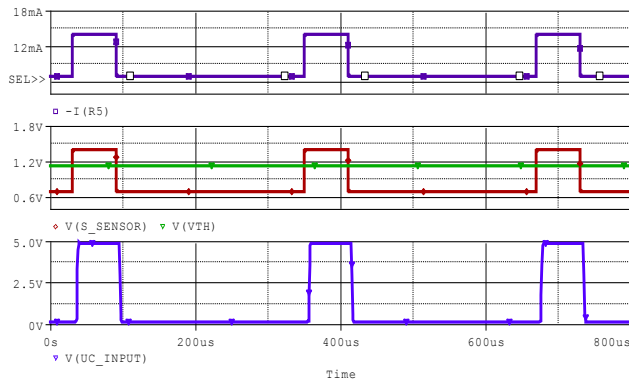


Fig. 6.6 Typical speed sensor interface circuit behavior

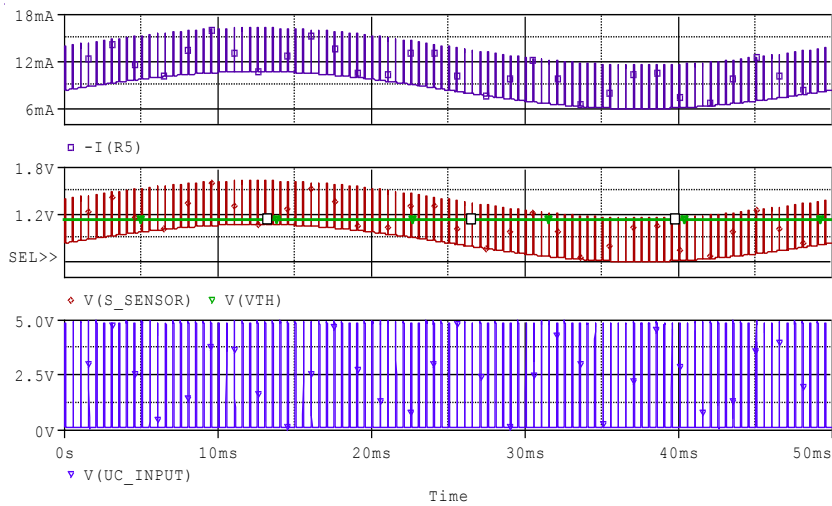


Fig. 6.7 Typical circuit behavior, at sensor supply current limit ranges

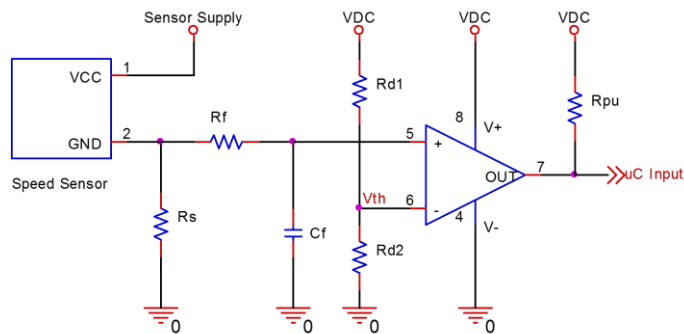


Fig. 6.8 Typical speed sensor to microcontroller input, interface circuit example \*without hysteresis

As example, if we use a shunt resistor with a typical value of  $R_S=100\Omega$ , a threshold voltage for the comparator  $V_{th}=1,05V$  (resulted from equation (6.1) using limits from Table 6.1) and taking into account the speed sensor typical supply current limits presented in Fig. 6.6, the maximum hysteresis than can be applied according to equation (6.2) will be:

$$\mathbf{V_{hyst\_TYP} < 700mV}$$

If we take into account the speed sensor supply current worst case limits, listed in Table 6.1, the hysteresis limits for the comparator according to equation (6.3) will be much less:

$$V_{hyst} = (I_{HI\_MIN} - I_{LO\_MAX}) \cdot R_S \quad (6.14)$$

$$\mathbf{V_{hyst} < 340mV}$$

Considering the other components tolerance of the interface circuit, like 1% precision for the shunt resistor and the threshold voltage divider resistors, 1% accuracy of the supply voltage ( $V_{DC} = 5V$ ), using equations (6.4 and 6.5) the resulted worst case maximum hysteresis will be:

$$V_{hystWC} = (I_{HI\_MIN} - I_{LO\_MAX}) \cdot R_{S\_MIN} - \Delta V_{th} \quad (6.15)$$

$$\Delta V_{th} = \frac{R_{d2MAX}}{R_{d2MAX} + R_{d1MIN}} \cdot V_{DCMAX} - \frac{R_{d2MIN}}{R_{d2MIN} + R_{d1MAX}} \cdot V_{DCMIN} \quad (6.16)$$

$$\mathbf{V_{hystWC} < 336,5mV.}$$

In case of a real automotive application even this resulted  $V_{hystWC}$  is not feasible, because the temperature and aging effect of the components is not taken into consideration. However these parameters depend on the quality and performance of the chosen components. Nevertheless out of the above calculations we can conclude that the main restriction for the comparator hysteresis and the input circuitry performance limitation is given by the speed sensor supply current limits itself.

Fig. 6.9 summarizes all the above assumptions in a graphic form. It can be clearly seen the small distance between the input signal worst-case limits and the comparator threshold. In a real application this threshold is also influenced by the components initial tolerance temperature and aging. In graph a typical 5% overall tolerance for this threshold voltage is considered. This percentage is given considering a 2% overall accuracy (initial + temperature + aging drift) of the reference voltage  $V_{ref}$  and 3% for the voltage divider circuit resistors (1% initial +2% temperature and aging drift) used to obtain out of the reference voltage de desired threshold voltage.

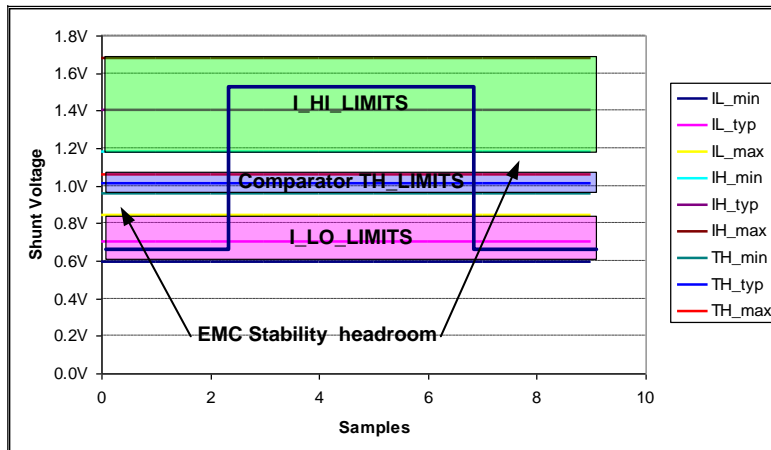


Fig. 6.9 EMC stability headroom of the classical speed sensor interface circuitry

### 6.2.2 Improved classical interface circuit

A good improvement from EMC point of view can be obtained for the typical interface circuit, using a comparator circuitry with dynamic hysteresis. The concept circuit is presented in Fig. 6.9. The dynamic behavior of the comparator threshold voltage is given by R5 and C4. When the comparator output level changes, for a short time a small voltage is added in addition to the hysteresis making the circuit less sensitive to noises around the commutation points (speed sensor current level change points). The time while the dynamic hysteresis acts, has to be shorter than the actual pulse time generated by the sensor (see Fig. 6.4), otherwise the output pulse time will not be equal with the pulse time from the input and the rotation direction detection will be affected.

As already mentioned the circuit presented in Fig. 6.10 has its comparator stage designed with a static plus a dynamic hysteresis. The static hysteresis is achieved by the positive reaction path realized with R4. The dynamic hysteresis is generated by R5 and C4 where R5 determines the amplitude of the dynamic hysteresis and C4 the time for which the dynamic is active. Now for a typical circuit supplied from 5V ( $V_{DC} = 5V$ ) and with the threshold voltage set to 1,05V (according to equation 1 and Table 6.1) the positive and negative hysteresis regarding to the typical  $V_{th}$  value are not equal. This is because the  $V_{th} \neq V_{DD}/2$ .

The following equations express the max and min thresholds given by the static hysteresis:

$$V_{TH\_LO} = \frac{R4 \parallel R6}{R4 \parallel R6 + R1} \cdot V_{DC} \quad (6.17)$$

$$V_{TH\_HI} = \frac{(R4 + R2) \parallel R6}{(R4 + R2) \parallel R6 + R1} \cdot V_{DC} + \frac{R1 \parallel R6}{R1 \parallel R6 + R4 + R2} \cdot V_{DC\_O} \quad (6.18)$$

- Where  $V_{DC\_O}$  represents the voltage to which the comparator output pull up resistor is connected (this case R2).

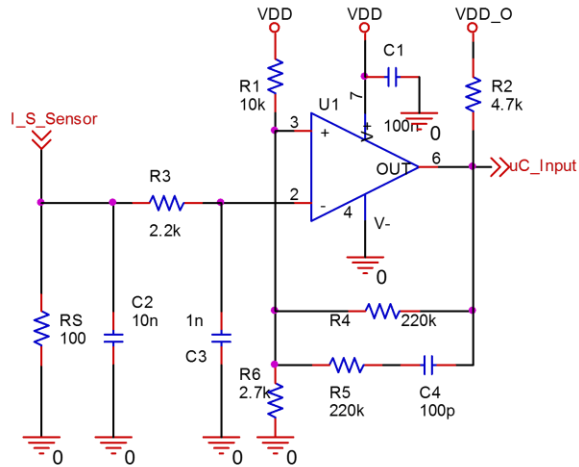


Fig. 6.10 Improved classical interface circuit with dynamic hysteresis

The VDD\_O might be different voltage level than the supply voltage of the circuit because of output voltage level compatibility achievement. Fig. 6.11 presents the typical behavior of the improved circuit. Note that because of the inverting comparator configuration the output signal fed to the microcontroller is inverted. This can easily be corrected by the application software by setting the input ports to react on negative input signal transition instead of positive. Fig. 6.12 presents the dynamic hysteresis behavior at switching points of the output signal. Note that the circuit used for simulations is optimized for 3.3V logic level output signal (output pull-up resistor R2 is connected to 3.3V).

The circuit immunity is improved for a short time after the input signal commutation fronts, however the EMC vulnerability during the time intervals between the pulses still remains (when the dynamic in the hysteresis disappears).

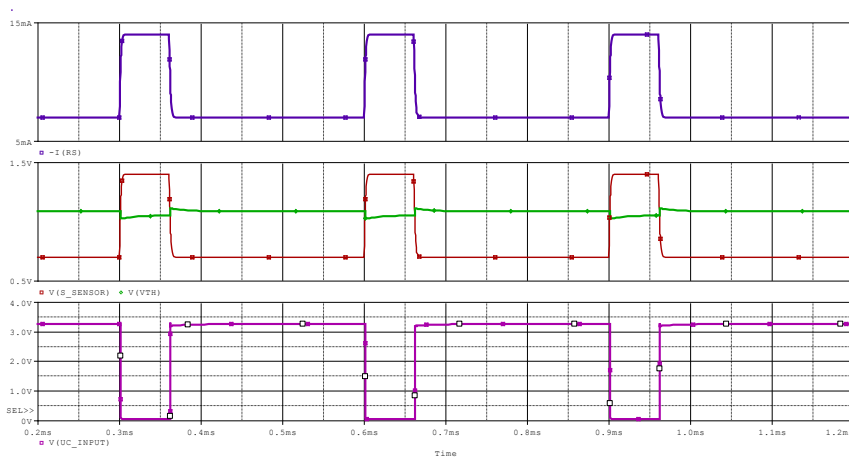


Fig. 6.11 Typical behavior of the classical interface circuit with dynamic hysteresis

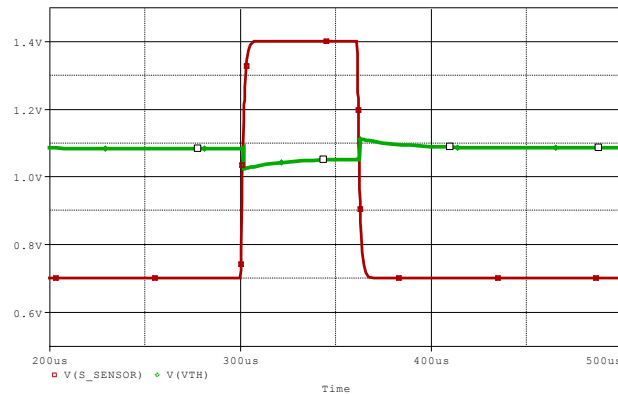


Fig. 6.12 Dynamic hysteresis signal behavior

### 6.3 Proposed interface circuit

The interface circuit comparator threshold voltage and hysteresis amplitude is mainly dependent on the speed sensor supply current limits as demonstrated in the last subchapter. The worst case supply current limits given by the sensor suppliers are quite large, however a minimum ratio between  $I_{HI}$  and  $I_{LO}$  is guaranteed. This means that if the  $I_{LO}$  limit goes to higher values also  $I_{HI}$  goes to higher values to keep the minimum  $I_{HI}/I_{LO}$  ratio of 1.9 (listed in Table 6.1). The proposed circuit is based on this supply current ratio, setting the comparator threshold voltage dynamically according to the actual  $I_{LO}$  current value. Fig. 6.13 presents the block diagram of the proposed circuit.

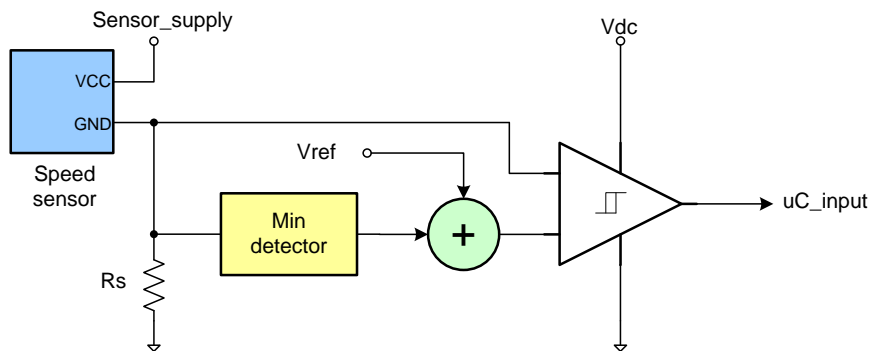


Fig. 6.13 Proposed speed sensor interface block diagram

In addition to the classical method this circuit contains a minimum value detector block which detects the input signal minimum value. To this minimum value a reference voltage is added. The typical reference voltage required can be expressed with the following formula:

$$V_{ref_{TYP}} = \frac{(I_{HI} - I_{LO}) \cdot R_S}{2} \quad (6.19)$$

Taking into consideration the worst case supply current limits of the speed sensor, which should be used in the implemented application circuit, the equation will be:

$$V_{ref} = \frac{(I_{HI_{MIN}} - I_{LO_{MIN}}) \cdot R_S}{2} \quad (6. 20)$$

The amount of hysteresis for this new concept circuit that can be applied to the comparator in order to increase the input noise immunity of the interface circuit will be:

$$V_{hyst\_enh} = (I_{HI_{MIN}} - I_{LO_{MIN}}) \cdot R_S \quad (6. 21)$$

Under the conditions within the example from the last subchapter the amount of hysteresis according to equation (6.21) will be:

$$V_{hyst\_enh} = 590mV.$$

Comparing the maximum applicable hysteresis of the classical interface circuit ( $V_{hyst} = 340mV$ ) with this concept the resulted maximum applicable hysteresis can be increased with **250mV**.

The above concept calculations are summarized in a graph from Fig. 6.14, where  $I_{LO}$  and  $I_{HI}$  limits are representing the worst case supply current limits of the speed sensor.

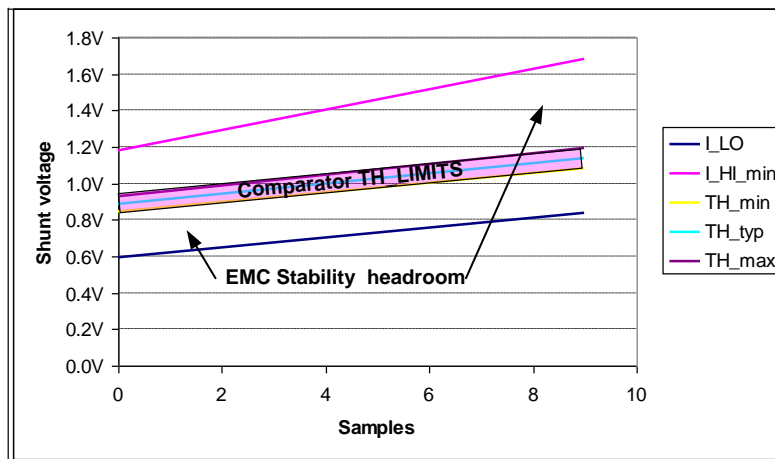


Fig. 6.14 EMC stability headroom of the proposed speed sensor interface circuitry  
 \*for  $I_{LO}$  and  $I_{HI}$  in the diagram their worst case limits are considered

Another important advantage of this concept is that the comparator threshold voltage never gets too close to the input voltage limits. Compared with the behavior of the typical circuit presented in Fig. 6.7, the threshold voltage of the proposed circuit is always with at least a  $V_{ref}$  (= 295mV worst case) voltage difference from the input voltage levels.



## 6.4 Simulation and experimental results

To validate the proposed concept the circuit was designed, simulated then built up for experimental evaluation. This subchapter presents the simulation and experimental measurement results.

For the simulations and experimental laboratory measurements as input parameters the Infineon speed sensor TLE4953 series supply current limits were applied [201].

### 6.4.1 Simulation of the proposed circuit

The simulation of the circuit was performed using OrCad PSpice V16.0. The evaluation of the proposed concept was done using the circuit schematic presented in Fig. 6.15.

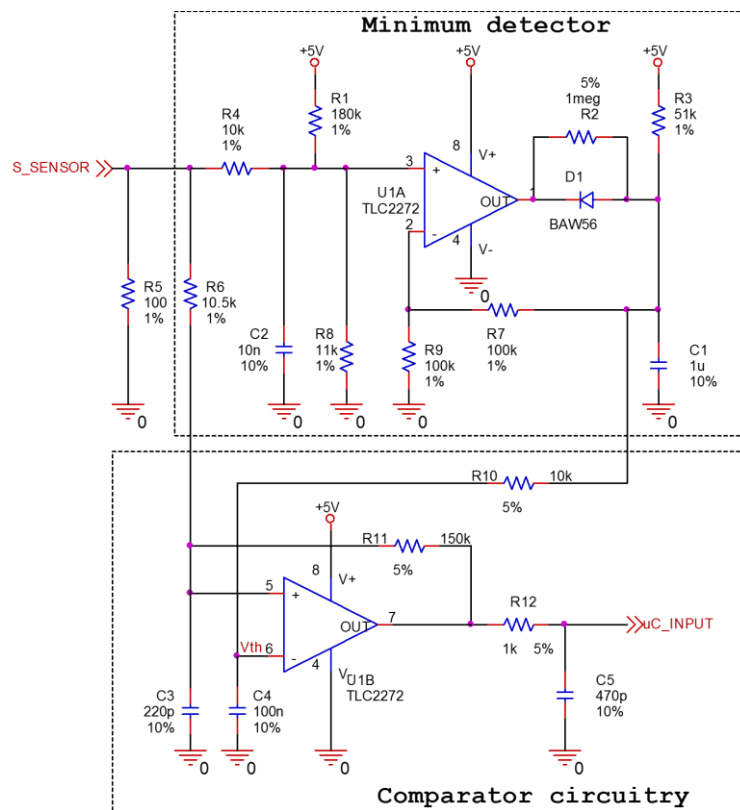


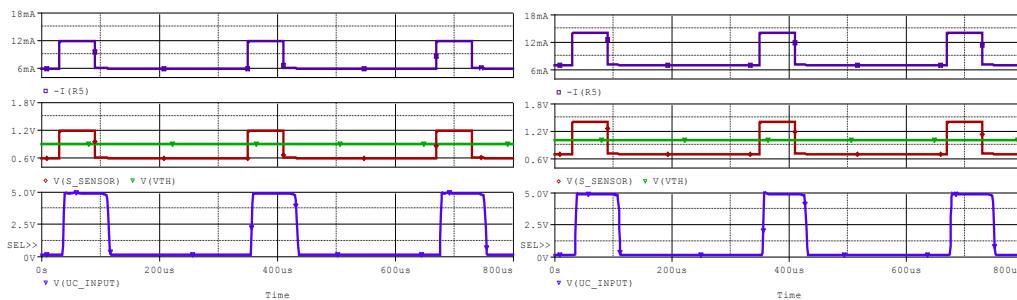
Fig. 6.15 Proposed speed sensor interface circuit schematic

The speed sensor GND pin is connected to the S\_SENSOR input signal which is connected to the shunt resistor R5. The signal from the shunt resistor is applied to the minimum detector circuit via an RC low pass filter composed by R4 and C2. The minimum voltage detector circuit is composed by U1A operational amplifier and the surrounding components. With R1 and R8 an offset voltage is added to the minimum detector circuit ( $V_{ref}$  from Fig. 6.13). With R7 and R9 the amplifying factor

of the minimum detector circuit is set to one. The minimum detector circuit provides the adaptive threshold voltage at C1 capacitor terminal ( $V_{th}$  net). This capacitor is charged via R3 and discharged via the U1A output and D1. The voltage comparator with the hysteresis is implemented with U1B operational amplifier and the surrounding components. The input signal from the shunt resistor is applied to the comparator non-inverting input via a low pass filtering network (R6 and C3). This filter increases the immunity of the circuit for high frequency disturbances, induced in the sensor connecting wiring harness. The reference voltage for this comparator stage (minimum input voltage +  $V_{ref}$ ) is fed via a low pass circuit implemented using R10 and C4. This low pass filter eliminates the ripple from the minimum detector output given by the time constant of the circuit. The positive feedback in the comparator circuit creates a small hysteresis (given by R11), this further improves the circuit immunity against input signal noises.

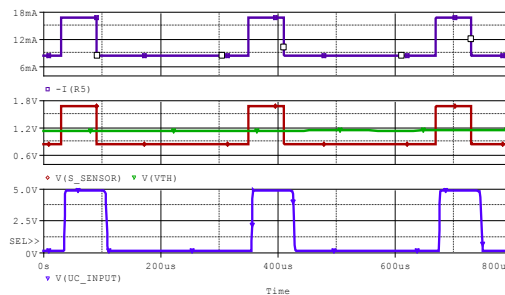
Fig. 6.16 presents the simulation results for different supply current limits of the speed sensor as follows:

- simulation at minimum supply current limits;
- simulation for typical supply currents;
- simulation at maximum supply current limits;



(a)  $I_{LO} = 5,9\text{mA}$ ;  $I_{HI} = 11,8\text{mA}$ ;  
 $V_{th} = 994\text{mV}$

(b)  $I_{LO} = 7\text{mA}$ ;  $I_{HI} = 14\text{mA}$ ;  
 $V_{th} = 882\text{mV}$



(c)  $I_{LO} = 8,4\text{mA}$ ;  $I_{HI} = 16,8\text{mA}$ ;  $V_{th} = 1,135\text{V}$

Fig. 6.16 Proposed method sensor supply current limit simulation results

To simulate the speed sensor supply current limits change over temperature and lifetime, under worst case conditions (according to the sensor supplier datasheet) and the dynamic threshold behavior, a sinusoidal offset current with 20Hz frequency is added to the signal, generated by the speed sensor. The speed sensor simulation itself is done using a current pulse generator. Fig. 6.17 presents the speed sensor

simulation circuit used in the simulations. The speed sensor is supplied by V1 voltage source of 7V.

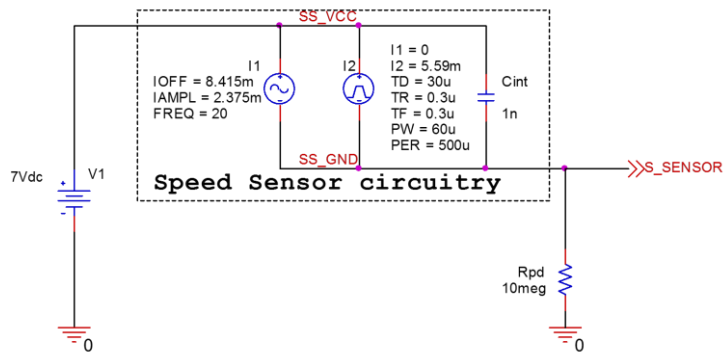


Fig. 6.17 Circuit used to simulate the speed sensor

The speed sensor itself is simulated via  $I2$  current source and  $I1$  is the sine wave current source which helps to simulate the worst cases of the supply current limits.  $Cint$  simulates the internal capacitance of the speed sensor.

The simulation results are presented in the next Fig. 6.18.

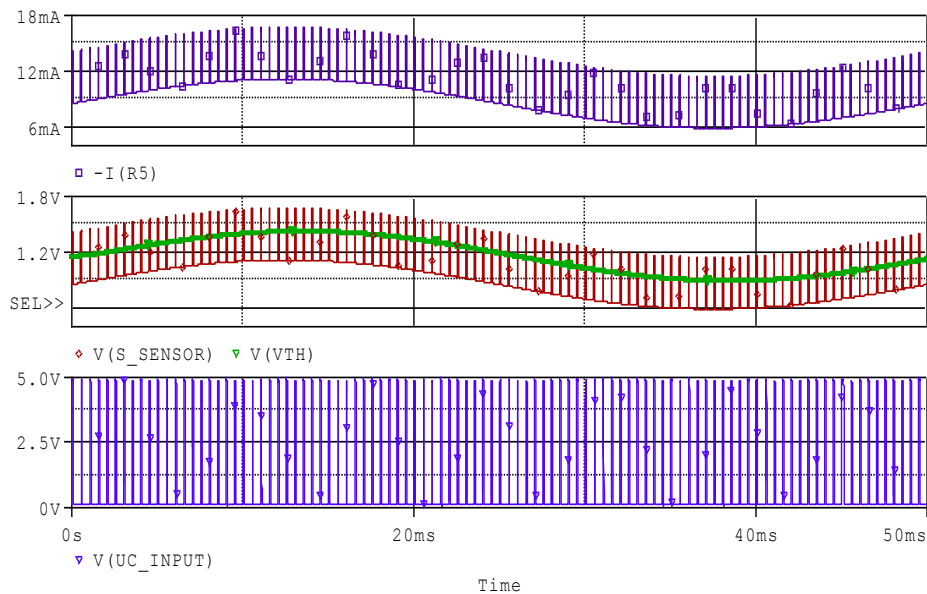


Fig. 6.18 Adaptive threshold simulation result

### 6.4.2 Noise immunity simulation

In order to prove and evaluate the better immunity against input noise signals of the proposed method, its performance is compared to the performance of the classical comparator circuit with hysteresis. The classical interface circuit schematic

used for the comparison in the simulations is presented in Fig. 6.19. For the proposed method the circuit from Fig. 6.15 is used.

The evaluation is done by adding a high frequency noise to the input signal from the speed sensor. The amplitude of this noise is ramped up to values where both circuits fail. The noise amplitude where each particular circuit fails is then measured and compared. Table 6.2 presents the summary of the EMC immunity evaluation results. The values from the table, represent the noise signal amplitude measured at the circuit input shunt resistor (R5 from Fig. 6.15 and R15 from Fig. 6.19) at which the circuits fail to generate the correct output signals. The input current limits used are those defined in Table 6.1. The input noise simulation results are presented in Fig. 6.20 for typical input signal current limits, Fig. 6.21 for the minimum and Fig. 6.22 for the maximum limits. During the simulation noise signal has been added to the input of the circuit (in parallel with the speed sensor input) with ramped up amplitude (see the red trace in the simulation pictures from Fig. 6.20 to Fig. 6.22) and the output signal correct generation failing point has been observed. Point at which the input noise amplitude has been measured and considered as the input noise at which the circuit fails to generate correct speed signals to the microcontroller. In these figures the better noise immunity of the circuit based on the proposed concept can be clearly observed (green top signal represents the classical circuit output signal from Fig. 6.19 and the blue signal the output of the proposed circuit presented in Fig. 6.15).

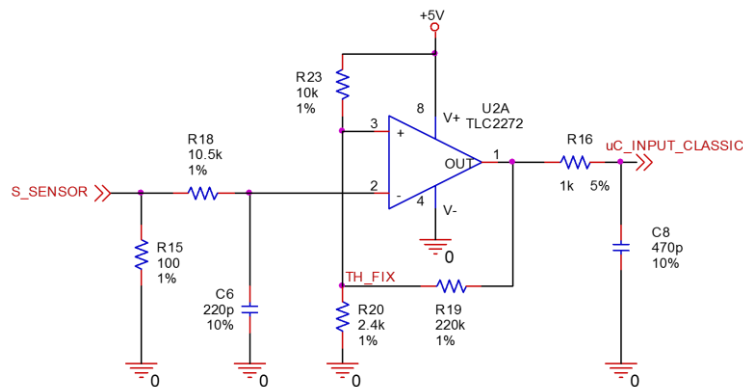


Fig. 6.19 Typical speed sensor to microcontroller input, circuit schematic with hysteresis

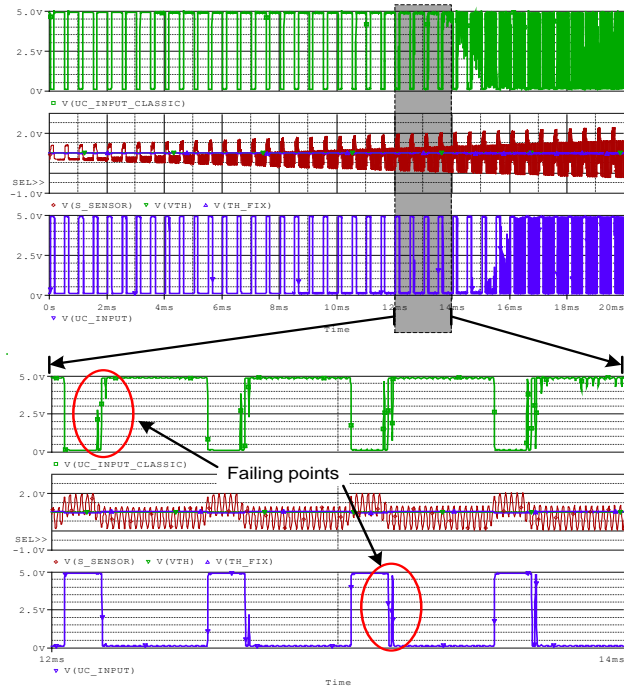


Fig. 6.20 Noise injecting simulation results for typical input current limits  
 $I_{LO} = 7\text{mA}$ ;  $I_{HI} = 14\text{mA}$ ;

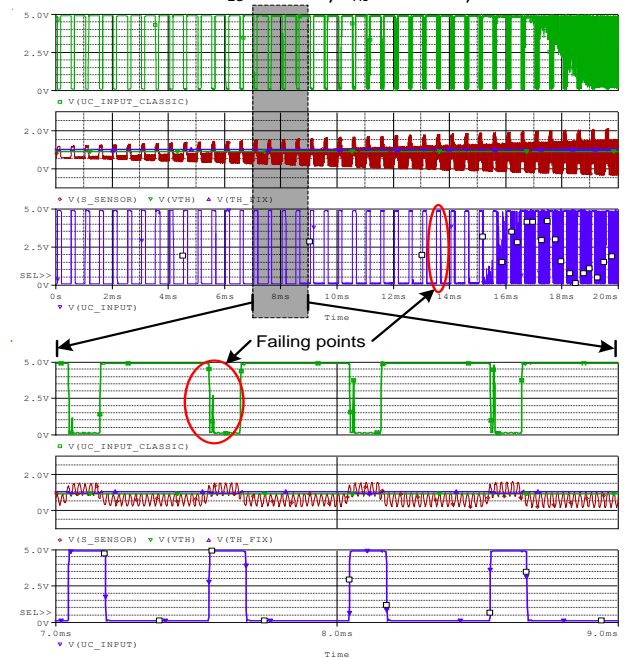


Fig. 6.21 Noise injecting simulation results for minimum input current limits  
 $I_{LO} = 5,9\text{mA}$ ;  $I_{HI} = 11,8\text{mA}$

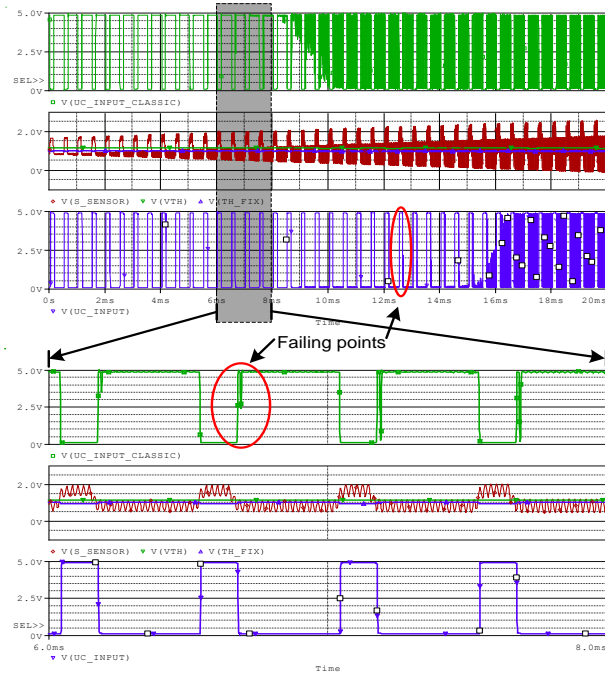


Fig. 6.22 Noise injecting simulation results for typical input current limits  $I_{LO} = 8,4\text{mA}$ ;  $I_{HI} = 16,8\text{mA}$ ;

Table 6.2 Noise immunity limits simulation results.

$I_{LO}, I_{HI}$ limits	Classic Circuit	Proposed Circuit
Min.	0.72 V	1.22 V
Typ.	1.23 V	1.28 V
Max.	0.62 V	1.24 V

Table 6.2 concludes the EMC simulation results for the two circuits.

This proposed method presents some disadvantages in case the sensor signal does have for a short time a DC shift. The situation is presented in Fig. 6.23, with a positive 15mA shift for 35ms. It can be seen that at the moment of the shift both circuits fails to provide the output signal, after a few milliseconds the new proposed method (green trace) threshold adapts itself and the circuit starts to provide correct speed signals at the output. At the moment when the DC shift disappears the classic circuit immediately start to generate correct speed signals to the microcontroller, but the proposed method still need some time to adapt its threshold and generate correct signals (this case around 2ms, missing four input pulses). So in either case (at the beginning and after the DC shift), the proposed method does not generate correct speed signals, while the classic method fails to generate the correct speed signals only during the DC shift. In case of a negative DC shift the situation is even worse, because the rise time of the adaptive threshold voltage is much longer than the fall time, due to the different charge and discharge currents of the adaptive threshold circuit output capacitor (C1 from Fig. 6.15). The situation is presented in Fig. 6.24 for a -15mA DC shift, with thirteen missing pulses.

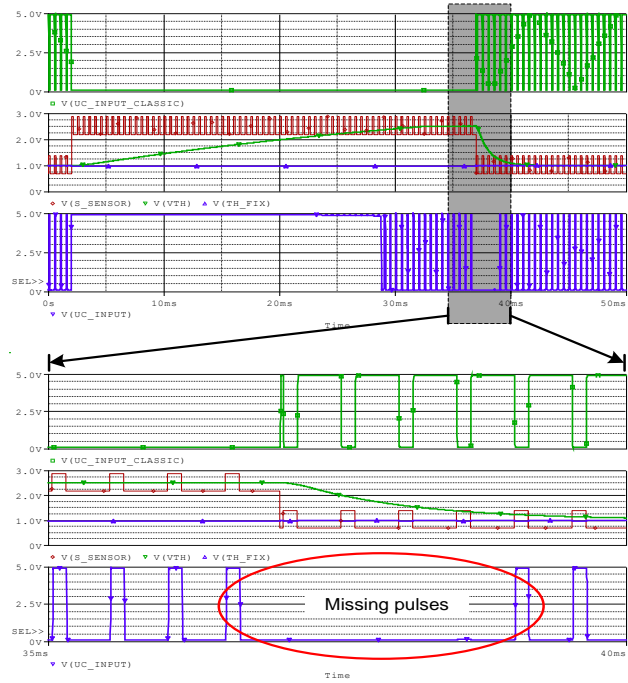


Fig. 6.23 Circuit behavior for a short positive DC shift

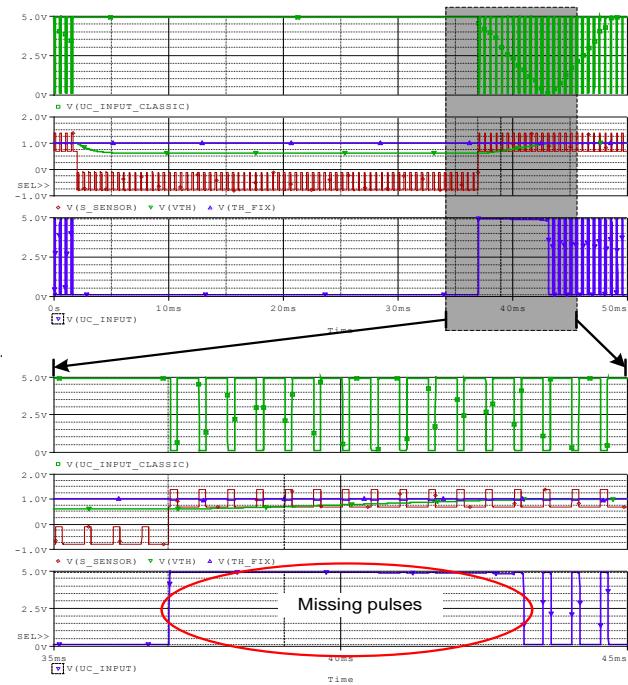


Fig. 6.24 Circuit behavior for a short negative DC shift

### 6.4.3 Laboratory evaluation results

In Fig. 6.25 the measurement results for different speed sensor supply current limits are presented, evaluated at room temperature. For the measurements the Infineon TLE4953 speed sensor current limits were applied to the circuit sensor input. The input signals were supplied from a programmable signal generator, Agilent 33220A type.

This circuit being designed for automotive applications, it has to work properly in a wide temperature range. For most of the TCU (Transmission Control Unit) applications the required functional temperature range is between  $-40^{\circ}\text{C}$  to  $+140^{\circ}\text{C}$ . Therefore the circuit performance was evaluated also at low ( $-40^{\circ}\text{C}$  Fig. 6.26) and high temperatures (Fig. 6.27  $+140^{\circ}\text{C}$ ).

In the presented experimental measurement results the maximum pulse frequency was used (around 12Khz for left rotating direction and 6Khz for right rotating direction). These are the most critical operational frequencies of the circuit, but it does not prove that the circuit can operate also at low rotation speeds resulting in low frequency of the current pulses. Therefore experiments were conducted to prove the proper circuit operation also at low pulse frequencies, the results are shown in Fig. 6.28. These measurements were done at room temperature for two different pulse frequencies at 100Hz, presented in Fig. 6.28 a) and 1KHz, presented in Fig. 6.28b).

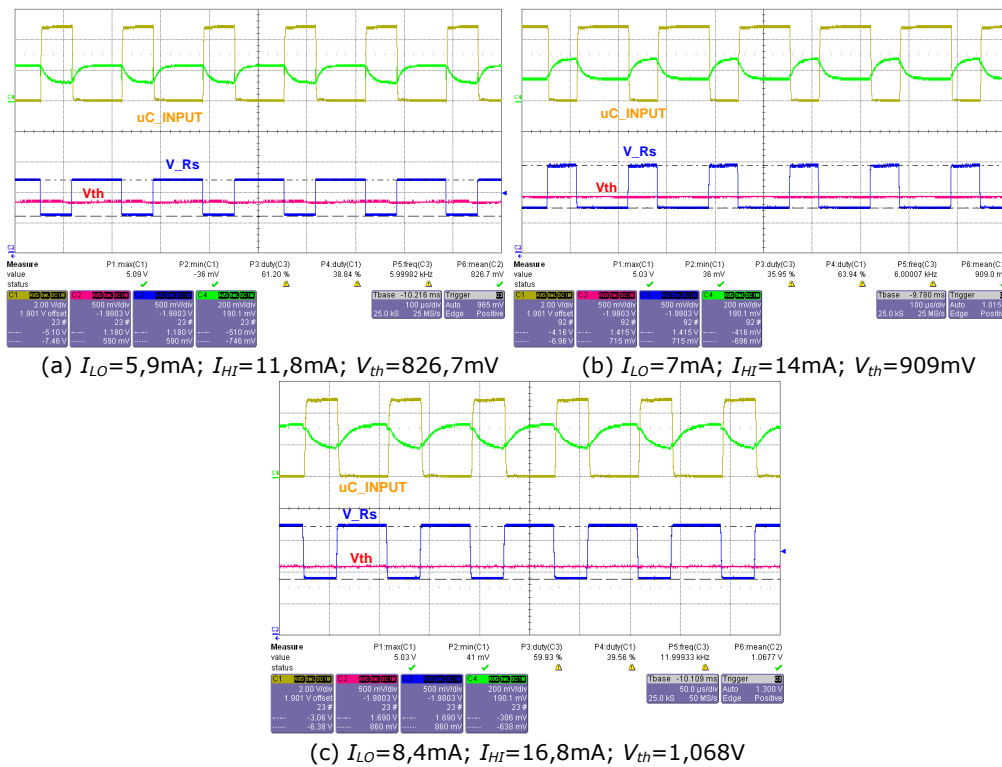
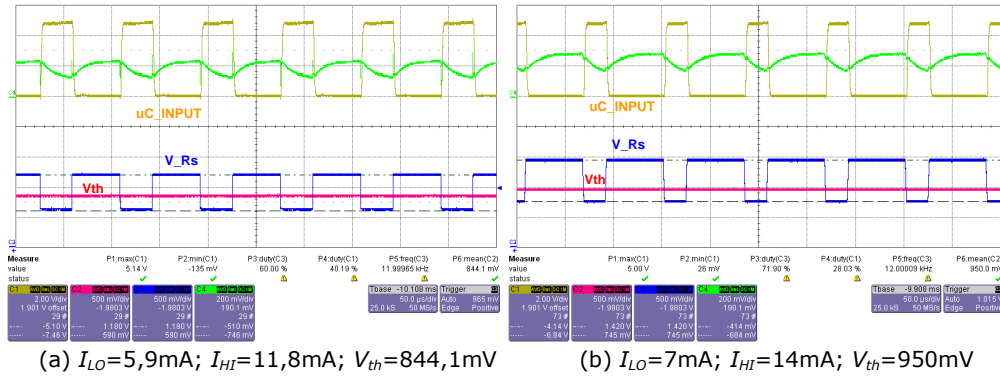


Fig. 6.25 Sensor supply current limit measurement results

\* Note: CH1 is in inverted mode; conditions: room temperature, right rotation direction;





\* Note: CH1 is in inverted mode;  
 \*\*Conditions:  $-40^\circ$  ambient temperature, right rotation direction;

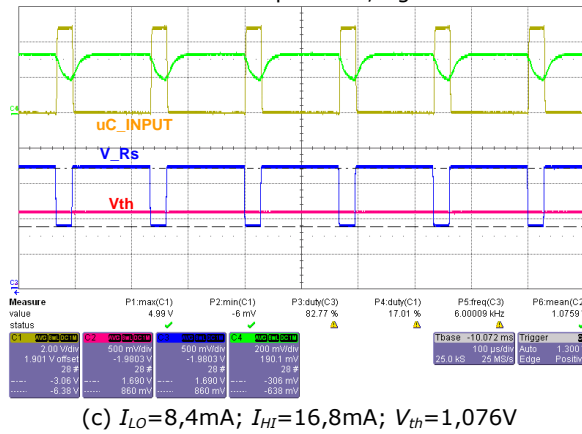
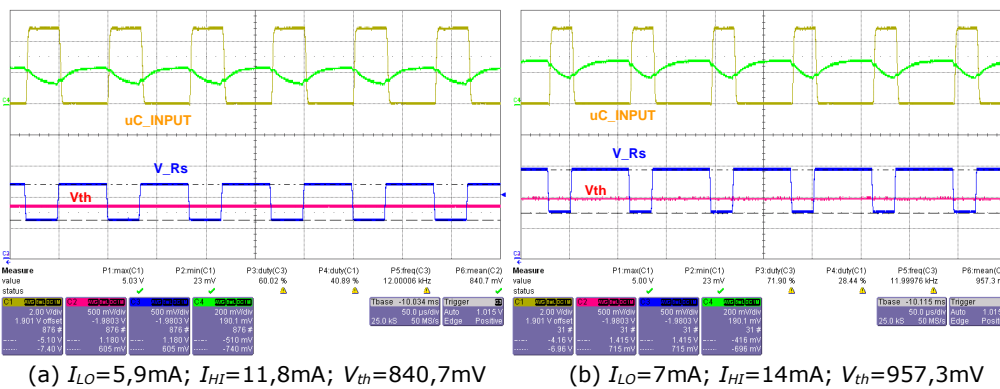
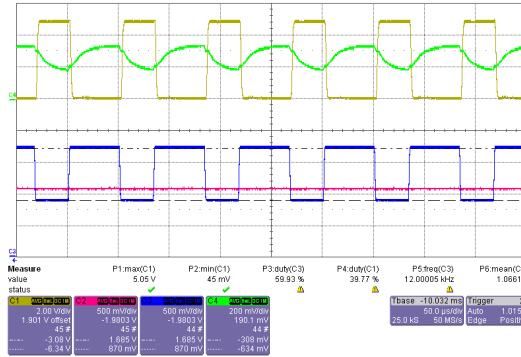


Fig. 6.26 Sensor supply current limit measurement results at low temperature ( $-40^\circ\text{C}$ )

\* Note: CH1 is in inverted mode;  
 \*\*Conditions:  $-40^\circ$  ambient temperature, right rotation direction;



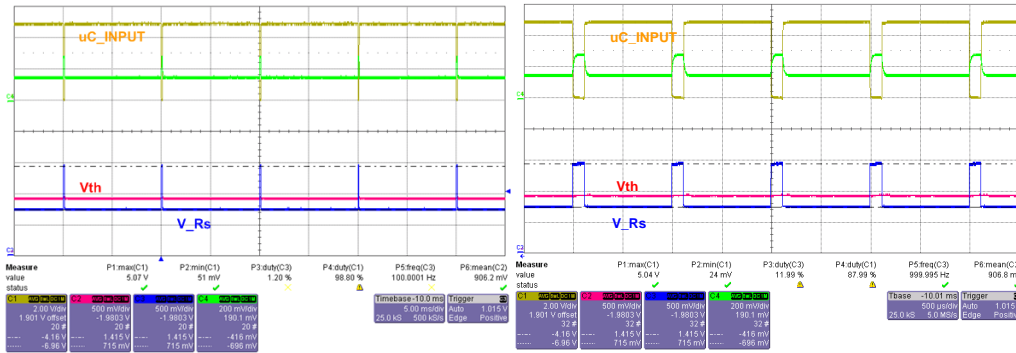


(c)  $I_{LO}=8,4\text{mA}$ ;  $I_{HI}=16,8\text{mA}$ ;  $V_{th}=1,066\text{V}$

Fig. 6.27 Sensor supply current limit measurement results at high temperature (+140°C)

\* Note: CH1 is in inverted mode;

\*\*Conditions: +140° ambient temperature, right rotation direction;



(a) 100Hz pulse frequency

(b) 1KHz pulse frequency

Fig. 6.28 Speed sensor input circuit operation at different pulse frequencies

\*Note: CH1 is in inverted mode.

The measurements show similar results with the simulations, proving the concept validity and good performance. The experiments over temperature show no considerable temperature dependency of the circuit proving its applicability in wide operational temperature range of the automotive applications. Table 6.3 summarizes the measured adaptive threshold values over temperature and input signal limits (from Table 6.1).

Table 6.3 Measured adaptive threshold values over temperature

$I_{LO}$ , $I_{HI}$ limits	Temperature		
	-40°C	25°C	140°C
<b>Min.</b>	0.844V	0.827V	0.841V
<b>Typ.</b>	0.950V	0.909V	0.957V
<b>Max.</b>	1.076V	1.068V	1.066V

## Summary

This chapter presents a new concept for rotational speed sensor interface circuit with an adaptive threshold voltage proposed by the author.

This threshold voltage automatically adapts to the changes in the sensor supply current limit parameters over initial tolerance, temperature and aging, in order to obtain better performances and higher immunity against input signal noises, disturbances.

The validity of the concept is first proven by PSpice simulations, including functional simulations and EMC performance comparison with the classical method. Second an experimental circuit was built up and its performance was evaluated over the input signal current limits range and over temperature. The result proves its applicability in high performance wide temperature range automotive applications.



## 7 Conclusions and personal contributions

### 7.1 Conclusions

The present work is dedicated to the advanced BLDC motor control systems integrated in automotive applications, especially focusing on hardware solutions implemented inside an application specific integrated circuit (ASIC) thus increasing the control system performances and in the same time reducing the computational power required from the system microcontroller.

Based on the ideas and results presented in the thesis, the main conclusions are summarized as follows:

- ❖ The number of automotive applications that integrate a BLDC motor, instead of conventional DC motors, hydraulic systems or pneumatic actuators has increased significantly in the last few years. The actuator systems, pumps or fans based on BLDC technology have a very big potential in the future and it's expected to witness considerable growth in the next years. At the moment the biggest trend is the implementation of pumps and fans using sensorless control of the BLDC motor due to the less complexity and higher robustness of the sensorless BLDC motor itself. Nevertheless it is a very big challenge for the automotive industry to develop such sensorless control solutions which are reliable enough and can operate safely in all the harsh conditions and environments to which an automotive system must fully comply and being in the same time economically reasonable and safe.
- ❖ In applications in which sensorless drive of the BLDC motor is desired, best control performances can be obtained if the BLDC motor is designed with significant saliency. As demonstrated in the thesis based on the saliency effect the initial rotor position can be estimated very fast with a good accuracy. The saliency effect helps in the generation of zero crossing detection at low rotational speeds, even if the back-EMF amplitude is not detectable extending the sensorless operation speed range of the BLDC motor.
- ❖ Using the alternating freewheeling method to drive a three phased power inverter, equalizes to power consumption among its switching elements. This extends the lifetime and maximum possible output power of the inverter circuit. The conducted theoretical analysis (mathematical calculations and simulations) of the PWM strategy proves its advantages over the classical low side or high side freewheeling methods, however results of the laboratory experiments do not presents so significant thermal differences between the two methods. This is mainly due to the thermal contact between the switching elements which transfers heat from the most to the less dissipating elements. Still the concept is a very good approach for three phased power inverters in which there is a big thermal resistance between the switching elements as example when they are mounted on separate heat sinks.

- ❖ The fifth chapter of the thesis presents a new a hardware implemented field weakening drive concept for BLDC motors. The concept is proven to be among the best methods for the phase advanced operation of a sensed BLDC motor control system. This is achieved using an advanced rotor position sensing circuit with a programmable zero rotor position, based on which the three position hall signals are generated. Programming this zero position with a predefined offset, representing the desired phase advance, the position hall signals will be generated with the predefined phase advance eliminating the high computational power required to implement such phase advance using software solutions.
- ❖ Based on the existing state of the art in BLDC motor control methods, BLDC motor control systems, motor driver ASIC architectures, requirements for the future BLDC motor control systems in the automotive industry an advanced BLDC motor controller ASIC architecture is proposed. This includes power MOSFET's gate driver circuit concept, synchronized sample and hold current measurement unit, a sensed or sensorless control module for the BLDC motor and an advanced diagnosis module for the whole BLDC motor control system. For the configuration of the ASIC and check of the operational status of the system a serial communication protocol is proposed (using SPI). All configurations and diagnosis reports of the ASIC are grouped in 24 bit registers accessible via this serial interface.
- ❖ The proposed Hall Effect based speed sensor input interface circuit with adaptive threshold is proven to have considerably higher immunity against input signal noises and tolerances of the input signal current levels provided by the speed sensor. The "EMC Stability Headroom" concept as performance indicator has been introduced to evaluate the input noise immunity of such interface circuits. A drawback of the proposed method is that its implementation requires a higher complexity circuit compared to classical methods increasing its implementation cost.

### **Future research and development directions**

Technologies based on Brushless motors are ever evolving ones. The author wishes to continue his research and development in this field evaluating new unexplored ideas as:

- ❖ Sensorless startup methods based on saliency;
- ❖ Advanced Brushless motor drive methods using advanced multicore microcontrollers for automotive applications;
- ❖ Advanced power MOSFET gate drive circuits, based on configurable constant current sources for individual control of the gate charge phases and commutation;
- ❖ Optimization methods for the DC link filter components calculation according to required EMC performance and lifetime.

## **7.2 Original contributions**

This section of the thesis presents the original contributions, from the author point of view.

**Theoretical Contributions:**

- ❖ A novel algorithm for initial rotor position estimation of salient pole BLDC motors, the algorithm being the fastest of all existing ones for salient pole BLDC motor types;
- ❖ A MOSFET's power consumption calculation and simulation method for the alternating freewheeling concept, applied for six step BLDC motor driver three phased power inverter;
- ❖ Hall position signal jitter detection and filter method – patented idea;
- ❖ A new hardware implemented solution for field weakening operation of BLDC motors;
- ❖ A new concept for Hall Effect based rotational speed sensor interface circuit, with improved EMC performance;
- ❖ Introduction of "EMC Stability Headroom" as an EMC performance indicator for Hall Effect based rotational speed sensor input circuits.

**Applicative Contributions:**

- ❖ An overview of the BLDC motor drive methods and strategies, including sensed and sensorless methods;
- ❖ An overview of BLDC motor controller systems;
- ❖ Development and implementation of an alternating freewheeling method for a better power distribution among the three phased power inverter switching elements;
- ❖ Development and implementation of an automated evaluation software for the BLDC motor test bench (Kistler);
- ❖ Proposal and implementation of a BLDC motor advanced diagnosis system;
- ❖ Proposal and implementation of BLDC motor rotor position hall sensors diagnosis system;
- ❖ Implementation proposal of a diagnosis system for the BLDC motor controller ASIC itself;
- ❖ Three phased power inverter bridge, temperature monitoring concept and circuit implementation proposal in the BLDC motor controller ASIC, using an external temperature sensing device (PTC or NTC) with configurable warning and over-temperature detection thresholds;
- ❖ Proposal of a BLDC motor control ASIC architecture based on the state of the art of the existing BLDC motor control ASIC's and new proposed and demonstrated ideas, methods introduced by the author and presented in this thesis;
- ❖ Development and implementation of a three phased power inverter board controlled by a microcontroller evaluation board (ZK-S12X-A), plus application software (microcontroller monitor software and PC graphical user interface) for BLDC motors used for the proposed initial position detection method evaluation;
- ❖ Development and implementation of an evaluation board for BLDC motors (hardware schematic, microcontroller monitor software, PC graphical user interface and digital logic circuit), used for the evaluation of the proposed methods in this thesis: alternating freewheeling, diagnose circuit and hardware phase advance;
- ❖ Overview of automotive rotational speed measurement methods;





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This paper presents a new initial rotor position estimation method for brushless dc motors (BLDC). It consists in injection of four short voltage pulses at the motor terminals and then based on the evaluation of the voltage measured at the terminal of the non-energized (floating) stator phase, the position is estimated. The first three pulses are applied for a very short time to evaluate the rotor position while the fourth (last) pulse is used only for detection of magnet polarity. The estimation time of the position with an uncertainty of 1800 is independent of the motor electrical time constant, being less than 140 μs, while the detection of magnet polarity could last longer (up to few milliseconds) until the iron core is saturated. The proposed method is proved only for salient pole BLDC motors (L<sub>d</sub> ≠ L<sub>q</sub>). The advantages of the proposed method are taught to be: quickness, simplicity, accuracy, low computation effort, and the most important: insensitive to the high voltage disturbances specific to the battery voltage in the vehicles. No current sensor is used for the proposed setup. Experimental results are provided to prove the concept and validate the solution.

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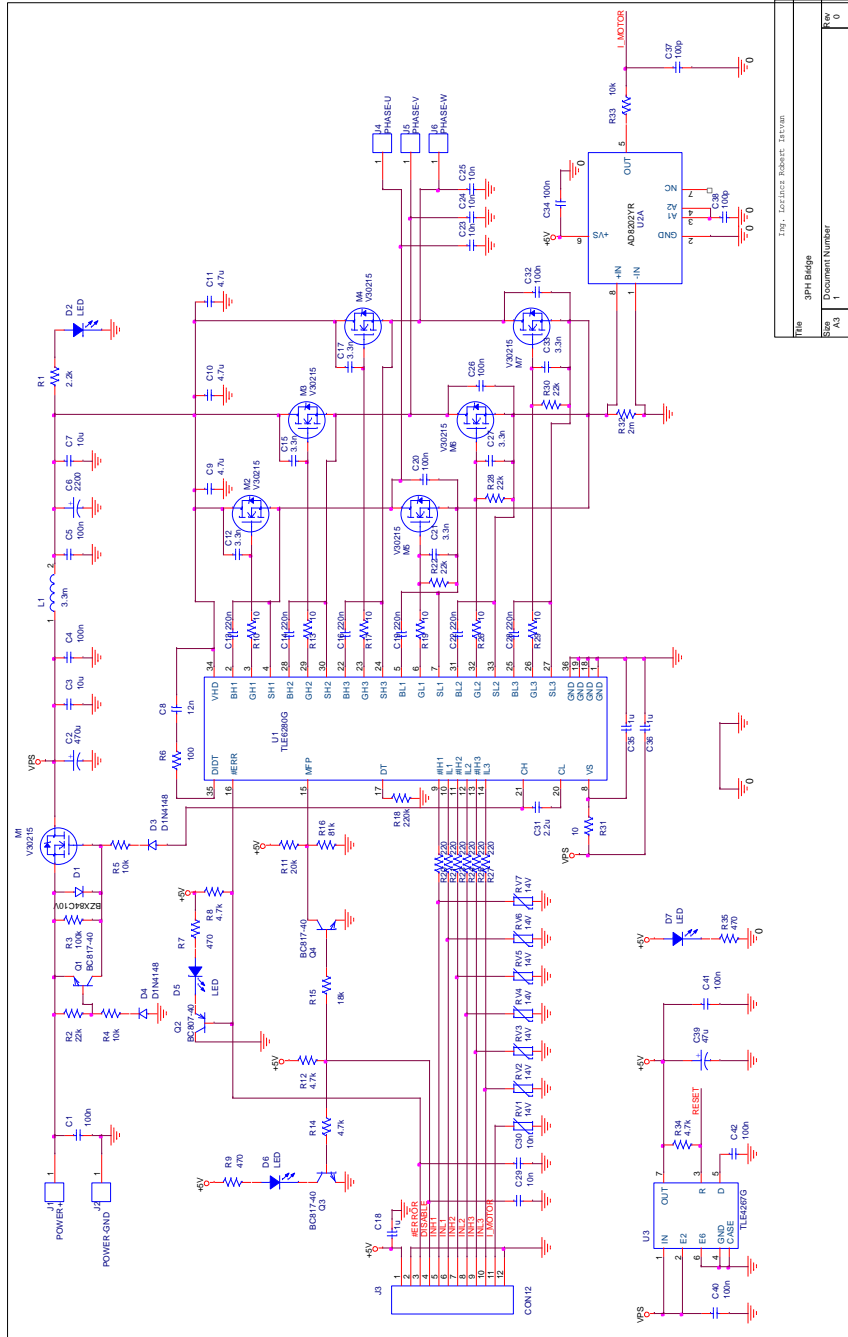


Fig 9.1 Three phased Bridge schematic diagram using TLE6280G

Title	3PH Bridge
Size	Document Number
Rev	1
Date	Surabaya, November 09, 2008

**BUK765R2-40B PSpice model parameter list**

```

*Model BUK765R2-40B
*N.B prepared by MC 23/8/04 assumes 2 source wires and 1 gate wire, wires are
made of aluminum.
*$
.SUBCKT BUK765R2-40B D G S
X1 S 5 bondwire params: length=4m dia=350u
X2 S 5 bondwire params: length=4m dia=350u
X4 G 1 bondwire params: length=4m dia=125u
Rg 1 4 0.7
Rdgd 2 3 1e9
Rcgd 3 4 1e9
Rcgs 4 5 1e8
Dgd 3 2 Dgd
Cgd 3 4 1.98E-09
Cgs 4 5 2.4E-09
M1 2 4 5 5 Mint
M2 4 2 3 3 Mdg
Rd 2 D Rtemp1 0.1e-3
Dsd 5 6 Dsd
Rdsd 6 D Rtemp1 0.1e-3
Rlsd 5 D Rtemp2 2.20E+11
.MODEL Mint NMOS(Vto=3.515 Kp=38 Nfs=1e11 Eta=1e3
+ Level=3 L=1e-4 W=1e-4 Gamma=0 Phi=0.6 Lambda=0 Is=1e-24
+ Js=0 Pb=0.8 Pbsw=0.8 Cj=0 Cjsw=0 Cgso=0 Cgdo=0 Cgbo=0
+ Tox=1e-7 Xj=0 Ucrit=1e4 Diomod=1 Vfb=0 Leta=0 Weta=0
+ U0=0 Temp=0 Vdd=0 Xpart=0)
.MODEL Dsd D(Bv=46 Ibv=250e-6 Rs=2.4e-3 Is=1.02e-11
+ N=1 M=0.5 VJ=1 Fc=0.5 Cjo=2.12e-09 Tt=33e-9)
.MODEL Dgd D(Cjo=7.5e-10 Rs=1e-3
+ Is=1e-14 M=0.4 N=1 VJ=1 Fc=0.5)
.MODEL Mdg NMOS(Vto=1e-3 Kp=10 Nfs=0 Eta=0
+ Level=3 L=1e-4 W=1e-4 Gamma=0 Phi=0.6 Lambda=0 Is=1e-24
+ Js=0 Pb=0.8 Pbsw=0.9 Cj=0 Cjsw=0 Cgso=0 Cgdo=0 Cgbo=0
+ Tox=1e-7 Xj=0 Ucrit=1e4 Diomod=1 Vfb=0 Leta=0 Weta=0
+ U0=0 Temp=0 Vdd=0 Xpart=0)
.MODEL Rtemp1 RES(TC1=5.16e-3)
.MODEL Rtemp2 RES(TC1=-0.05)
.ENDS
*$
.SUBCKT bondwire 1 3 params: length=1m dia=1u
L1 1 2 {2*length*(log(4*length/dia)-1)*1e-7}
R1 2 3 {length*2.8e-8/(3.1415*(dia/2)^2)}
R2 1 2 {(2*length*(log(4*length/dia)-1)*1e-7)*2*3.1415*50e6}
.ENDS
*$

```

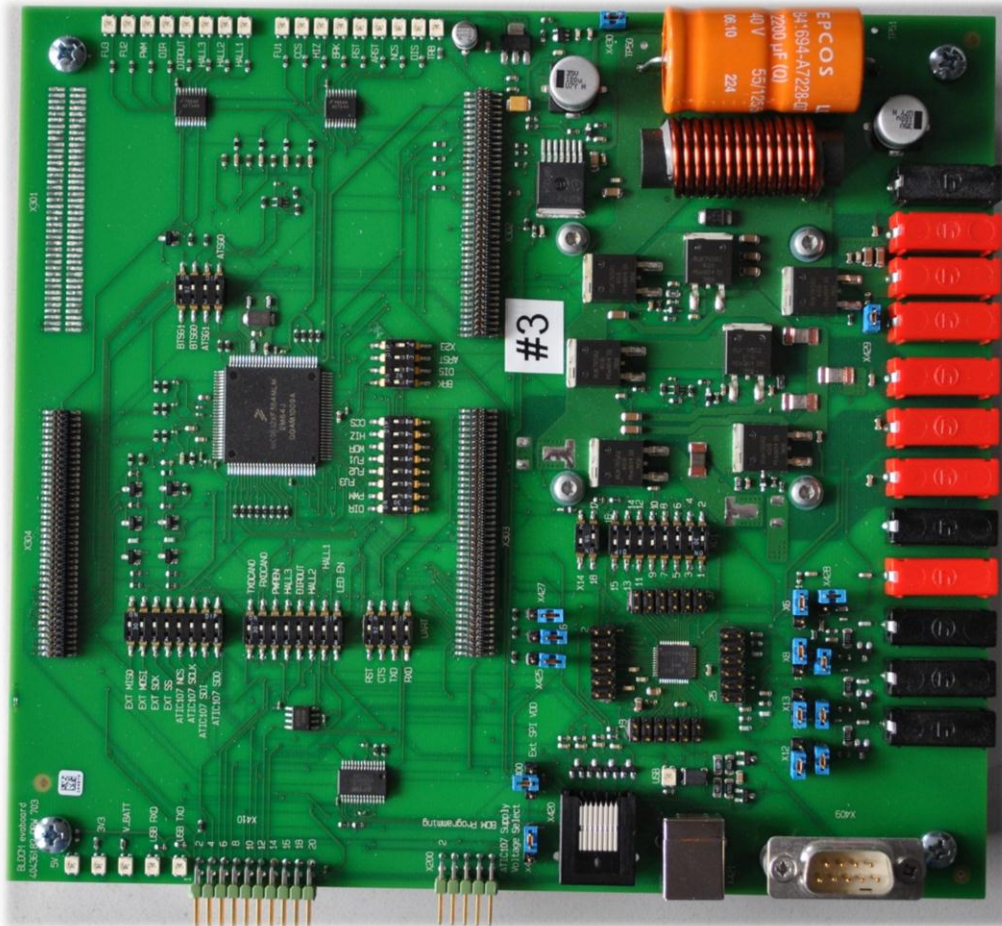


Fig. 9.2 BLDC Evaluation board (second generation) picture, developed by the author