Design and Experiment A Modified Clock Gated Dual Edge Triggered Sense Amplified Flip Flops for Low Power and High-Performance Applications

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Abstract: *In this paper, a Modified Clock Gated Dual Edge Triggered–Sense Amplified (MCGDET-SA) Flip-Flop (FF) is used to improve the performance by reducing the power consumption. The power consumption obtained by decreasing the clock switching power, reducing the delay and avoids power leakage. Unlike various earlier gated FF, the proposed MCGDET-SA FF involves retention property to lower the consumption and to change the modes of the switch circuits from idle to active and active to idle. The power dissipation is obtained using feedback path improvement. In the clock gating method, less number of transistors is used to reduce the area of the silicon. The proposed sense amplifier FF minimizes the delay and increases the speed where it leads to decrease the power consumption more. This paper aimed to combine all above-said features and proposed a modified clock gated amplified flip-flop for low and high-performance application in VLSI. The proposed FF is simulated, and the results verified for various supply voltages. The experimental result shows more improvements regarding power consumption, delay performance comparing with the other FF architectures.*
Keywords: *Flip Flops, VLSI, Low Power, Dual Edge Triggered, Sense Amplified.*

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DSP	-	Digital Signal Processing
DET	-	Dual Edge Trigger
VLSI	-	Very Large-Scale Integration
FF	-	Flip Flop
SAFF	-	Sense Amplifier Flip Flop
MCG	-	Modified Clock Gated
MCGDET-SAFF	-	Modified Clock Gated Dual Edge Triggered Sense Amplifier Flip Flop

1. Introduction

In the recent development of VLSI (Very Large-Scale Integration) circuits design, the power consumption is an essential factor to consider particularly for low power applications. Because of increasing demand for small power applications, it is necessary to design the low power circuit with reduced heat [1, 2] by using low powered latches and flip-flops. The most power consumption components of Clock Distribution Network (CDN) and flip-flops used in this design. These components consume 30% to 60% of the total system power flip-flops are absorbing 90% of power [3]. Now a day, the micro processor's power consumption is growing by just about 20% per year [4]. Due to the frequency scaling and deep pipelining the clocking system consumes more power, so it is necessary to reduce the power consumption both in clock distribution networks and flip-flops. And also, the hard time cost at high-frequency operation the latency of the flip-flops should be reduced [5, 6].

In 3-D VLSI circuits, Multi-plane synchronization causes more power consumption, and these are at the high levels [7]. Due to the dynamic power, the supply voltage has a quadratic effect and also leads to scale down when decreasing the power [2]. Automatically, the system protection decreases if the supply voltage reduces. And if the transistor threshold voltage drops, leakage power increases [2, 8]. So the power consumption techniques needed with reduced latency by without affecting the supply. Dual-edge triggering is one of the methods to reduce the power in CDN. Dual-Edge Triggered Flip-Flops (DETFFs) are used to reduce the frequency of the CDN by decreasing the power to 50% without affecting throughput [9-13]. Here the flip-flops are used to sample the data on both rising, and falling edges and half the clock frequency is required to get the same data throughput of Single Edge-Triggered Flip-Flops (SETFFs) [14]. Dual-Edge Sense Amplifier Flip-Flop (DE-SAFF) uses a clocking scheme which can be extended to enable dual-edge triggering in any dynamic CMOS logic circuit described in [12]. But this method modifies the single-edge dynamic logic and causes an increase in area. So far introduced all dual-edge triggering schemes designed by changing the circuit of the single-edge triggered flip-flop [9-18].

This method can use for enabling the dual-edge triggering in any dynamic CMOS logic circuit by considering the factors of power consumption and by reducing the area. At the same time, it is no need to alter the structure of the single-edge triggered dynamic logic circuit. Because of the problems faced in the existing flip-flop architecture, a new proposed method introduced in which new sense- amplifier based flip-flop circuits (SAFF) used due to its differential

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characteristics, fast operation speed, and low-power consumption. The sense amplified flip-flop measured as an agent of high-performance flip-flops [5], [14-16]. It has the similar operating concept of dynamic CMOS logic circuits. It has pre-charge and evaluation phases, to examine the feasibility of the new improved dual-edge triggering scheme. It is implemented in various methods within digital channels such as microprocessors and signal processing units. By using the dual edge triggering the flip-flop can sample data on both rising and falling edges of the clock. In this paper, a new Modified Clock Gated – Dual Edge Triggered Sense Amplifier flip-flop proposed.

2. **Related Works**

Z Chen et al. (1999) discussed the reduction of leakage current using transistor stacking. An algorithm presented in this paper, for selecting and assigning an optimal high-threshold voltage to achieve the best leakage power saving under target performance constraints. The author described that because of stacking subthreshold current decreases very much, DIBL effect also reduces that causes further reduction in subthreshold leakage [19]. A.G.M. Strollo and D. De Caro (2000) presented a new flip-flop to minimize power dissipation on both the master and slave latches when there are no data transitions. Clock gating is used to reduce power consumption and also to avoid unnecessary switching of circuit node. In this paper, it described that when the input and output of D-FF are same, then the small circuit scheme is used to control the clock of D-FF that control the triggering of D-FF[24]. N. Nedovic et al. (2001) presented a novel timing characterization for dual-edge triggered flip-flops. The clock period is very crucial to any sequential circuit. Similarly, term setup time and hold decide the input data. Clock period must be higher than the propagation delay of the device; there is more specification about clock period and data time limitation discussed in this paper [10]. N. Nedovic et al. (2002) proposed anew dual edge-triggered flip-flop that saves power by inhibiting transitions of the nodes. The proposed flip-flop is 12% faster with 10 %lower energy-delay product for 50% data activity, as compared to the previously published dual edge-triggered storage elements [4]. Koichi Nose et al. (2002) proposed a threshold voltage hopping (TH-hopping) scheme where the threshold voltage dynamically controlled through software depending on a workload. A control signal which sends from software guided the voltage supply connected to the body of MOS device that results in low Vth or Vth high required for different operation [25].

W.M. Chung et al. (2003) have researched low power, and low voltage in VLSI circuits and also the use and implementation of the dual edge-triggered flip-flop (DETFF). The main advantage of using DETFF is, it allows maintaining a constant throughput while operating at only half the clock frequency. The author compared previously published papers on static dual edge triggered flip-flops (DETFFs) together for their design, performance, power dissipation, low voltage and low power applications which seem the DETFF is the best one for digital operation when comparing with others. [21]. N.Nedovic and V. G. Oklobdzija (2005) proposed the design of the dual-edge-triggered storage elements (DETSE) which describes the classification, detailed timing characterization, evaluation, etc. The author described the effect of clocking at halved clock frequency and impact of load on the clock distribution network of DETSE. They presented a seminar on dual-edge triggered flip-flops with clock load, delay, and internal power consumption compared with the fastest single-edge unleashed storage elements (SETSE) [9]. M.H. Ghadiri (2005) presented two simple structures of low-power dual-edge triggered static pulsed flip-flops (DSPFF). They composed a dual-edge pulse generator and a static flip-flop with equal toggling delays. The static feature of DSPFF avoids the unnecessary internal node transitions to reduce power consumption. The simple structure of pulse generator with double-edge triggering proposed which results, low power dissipation in clock distribution networks [15]. Y.-T.Liu et al. (2006) suggested two new dual edge-triggered flip-flops. One of the flip-flops eliminates redundant transitions of internal nodes when current data is same as the previous one. It has the least power delay product compared to other dual edge-triggered flip-flops in all range of possible data switching activity, and its delay is also the smallest. The other proposed flip-flop disabled internal clocked transistors [1].

L.Y. Chiouand S.C. Lou (2007) proposed a dual-edge triggered and dual-Vth level converting flip-flop (LCFF). The LCFF utilizes energy-saving features that can use in a multi-V dd and multi-Vth system. The author described a novel power-aware latch structure, to eliminate the internal power during the transition. It shows that when operated in sleep mode, the power-aware latch switched to the low-leakage mode and still retained its data [12]. Y. Hu (2007) proposed a new type of pulse-triggered exact single-phase clock (TSPC) flip-flop with low threshold voltage clock transistor and its several improved structures for high-performance low-power applications. They described estimation of reduced power consumption of the CDN with low clock-swing and double-edge triggering [16]. S. E. Esmaeili et al. (2009) proposed a dual-edge triggered Differential Conditional Capturing Energy Recovery (DE-DCCER) flip-flop allows the clock frequency reduced by the factor 2. They described the resonant clocking techniques, to achieve significant power reduction compared to square wave clocking [13].

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3. **Problem Statement**

In this paper, the comprehensive study tells about the various existing FF architectures, analyzed the limitations and planned a new Modified Clock Gated Sense Amplifier (MCG-SA) based FF circuit based on the compelling advantages, speed in operation, less area utilization and less power consumption. The proposed MCGDET-SAFF circuit is designed and simulated by different methods within digital channels like DSP. The first MCG-SAFF is used to obtain a considerable power lessening by integrating DET mechanism and conditional pre-charging. Also by exhausting haste symmetrical latch, the MCGDET-SAFF cab able to accomplish lower power dissipation and delay. The proposed design has considered the baseline circuit, it developed a novel CGFF to decrease the power dissipation further at low switching activity, and the second proposed FF design gives more power savings additionally.

4. **Motivation**

The integration of average delay and power is energy consumption. Power is directly proportional to the square of the voltage. One of the ways to obtained power consumption is by reducing the voltage usage. It also helps to diminish the logic speed. In various digital filters under DSP it is necessary to preserve the computation and throughput at a determined threshold. To maintain, the performance, parallel architectures are used as a low-level voltage supply. DET flip-flop devices are used to realize these concepts. Also, to reduce the delay, sense amplifier FF is integrated. But new VLSI circuit system demands low power for high-performance applications. Hence this paper motivated to design a novel modified clock gated dual edge triggered sense amplifier flip-flop for reducing the power utilization, power dissipation, delay to increase the performance of the system which used for any low power and high-performance applications.

In this paper, it is studied comprehensively about the various existing FF architectures, analyzed the limitations and planned a new Modified Clock Gated Sense Amplifier (MCG-SA) based FF circuit based on the compelling advantages, speed in operation, less area utilization and low-power consumption. The proposed MCGDET-SAFF circuit is designed and simulated by different methods within digital channels like DSP, μP and the like. The first MCG-SAFF is used to obtain a considerable power lessening by integrating DET mechanism and conditional pre-charging. Also by exhausting haste symmetrical latch, the MCGDET-SAFF cab able to accomplish lower power dissipation and delay. The proposed design has considered the baseline circuit, it developed a novel CGFF to decrease the power dissipation further and at low switching activity, the second proposed FF design gives more power savings additionally.

5.Existing Flip Flop Design

A novel explicit-pulsed dual-edge triggered sense-amplifier flip-flop for low-power, and high-performance applications presented in this paper. By incorporating the dual-edge triggering mechanism in the new fast latch and employing conditional pre-charging, the DET-SAFF can achieve low-power consumption that has the small delay. To further reduce the power consumption at low switching activities, a clock-gated sense-amplifier is engaged. Extensive post-layout simulations proved that the proposed DET-SAFF exhibits both the low-power and high-speed properties, with delay and power reduction up to 43.3% and 33.5% of those the prior art, respectively. When the switching activity is less than 0.5, the proposed CG-SAFF demonstrates its superiority regarding power reduction. During zero input switching activity, CG-SAFF can realize up to 86% in power saving. This paper motivated to design MCGDET-SAFF to increase the percentage of power and delay reduction.

6. **Dual-Edge Triggered Sense-Amplifier Flip-Flop (DET-SAFF)**

To eliminate the unneeded transitions in the pulse generator, CG-SAFF introduced. It used the DET-SAFF circuit as the base circuit and integrated with the clock gating technique. This technique is mainly utilized to diminish the active power indulgence in synchronous circuits. This circuit called a digital circuit, and a clock signal synchronizes the components of it. Here the clock gating considered an event. The timing diagram and simulated waveform are shown in Figure 2 (a), (b) respectively. The schematic diagrams of CG-SAFF, sensing stage, and latching stage are shown in Figure 3 (a), (b), (c) respectively.

Meanwhile, to pull up transistor by turning on and charges the output node Q to a high state by setting up the node SB as low. To pull-up, the output nodes, a high-speed symmetric latch is introduced to make use of SB and RB. The pull-down path is modified further. It includes PULS controlled NMOS pass transistor, during which D (DB) straightforwardly fed to the Q(QB) node. It is to increase the speed from low to high output since the high-speed symmetric latch circuit instantly captures the input signal once the PULS generated. Here the low-to-high latency will also be enhanced.

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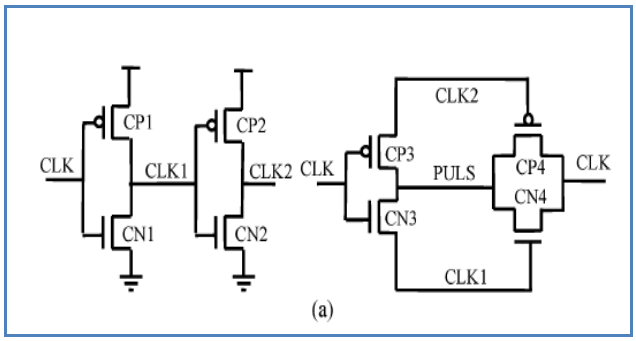


Fig.1(a)Dual Edge triggered Sense Amplifier Flip-Flop

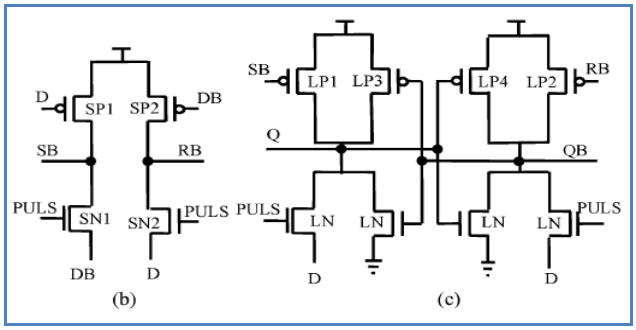


Fig .1.(b) . Dual Pulse Generator Sensing Stage

Fig. 1.(c) Symmetric Latch

The output node will not be charged only by pull-up transistors (LP1 & LP2) and also accused by the pass transistors (LN1 & LN2). Pass transistors may not load fully, but it can help with the pull-up transistors. LP3, LP4, LN3, and LN4 are the minimum size internal transistors designed for the point of maintaining the output state when the flip-flop is stable. In the proposed method the power reduction methods are only applicable for the latch part of the flip-flops. The pulse generator for all time is operating even when the input invokes no output changes for the switching activity of the clock signal is 1. This unwanted transition makes the power to be wasted particularly for low power applications. Conditional precharging is applied here to avoid this power wastage. The main benefit of DET-SAFF is high speed and low power. But the redundant transitions, particularly at low switching activities, lead a lot of energy to be wasted.

7.Clock-Gated Sense-Amplifier Flip-Flop (CG-SAFF)

To eliminate the unneeded transitions in the pulse generator, CG-SAFF introduced. It used the DET-SAFF circuit as the base circuit and integrated with the clock gating technique. This technique is mainly utilized to diminish the active power indulgence in synchronous circuits. This circuit called a digital circuit, and a clock signal synchronizes the components of it. Here the clock gating considered an event. The timing diagram and simulated waveform are shown in Figure 2 (a), (b) respectively. The schematic diagrams of CG-SAFF, sensing stage, and latching stage are shown in Figure 3 (a), (b), (c) respectively.

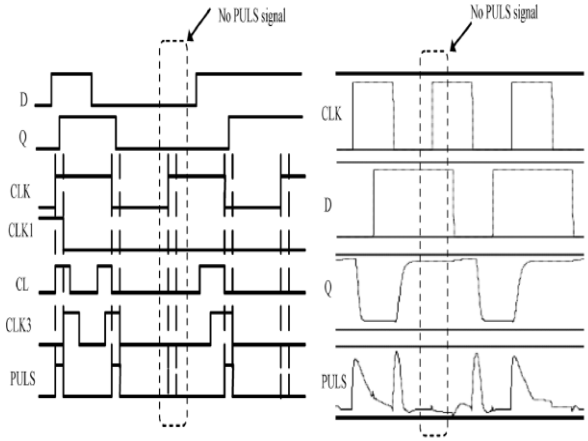
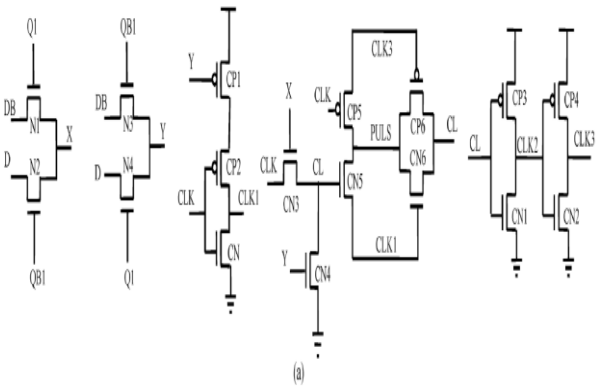


Fig.2 (a) CG-SAFF Timing Diagram (b) CG-SAFF Simulated Waveform

In this design, two comparators are used to match up to the prior and present input values. And also it is used to produce X, Y signals using different inputs D and DB and to the outputs Q1, QB1 which used as power signals. If D found as varied in Q1 of Q, then X is set up as high, and Y is set up as low. At the same time, the transistor N3 turned on for allowing the clock signal to go through as CL (Gated clock). And also, P1 is set to on and to force the CLK1 signal to high before the getting more upper edge of the clock. Hence to pull-up, the PULS signal to high, transistor N5 and the transmission gate are Switched ON. When the CLK1 is down to low, then the transparent window blocked after a specific stage, and CLK3 is pulled up.



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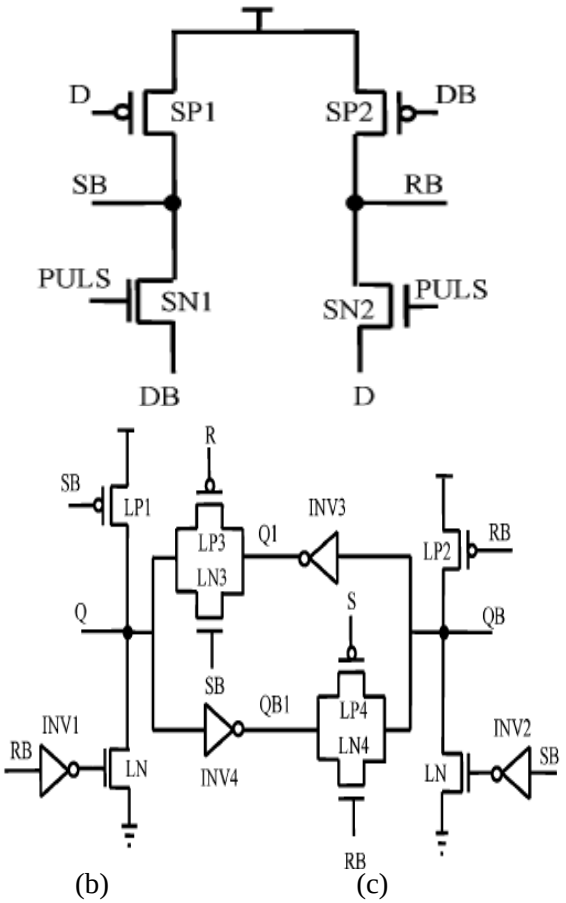


Fig. 3 Clock Gated Sense Amplifier Flip-Flop (a) – Schematic Diagram
(b) Sensing Stage (c) Latching Stage

Likewise, a short transparent period created at the rising edge of the clock. Here CLK1 is used for pulse generation and not CLK2. It is to ensure that thereby preventing race problems, and the flip-flop only gets the data at the triggering boundary of the clock. CL is little, and CLK3 elevated at the falling edge. While the CLK3 is low, then the sampling window will be closed. D remains in the same state for successive clock cycles and same as that X is small and Y is high. At low switching activity, CL has forced down; as a result, the flip-flop takes the advantage in power dissipation, and at the same time, the area of the design is considerably more. The sensing stage is similar to the DET-SAFF, and it has modified Nikolic's latch to hold buffered and differential outputs. The output Q1 and QB1 as an alternative of Q and QB are used in pulse generator to get the PULS signal. This CG-SAFF has the advantage to low switching activity.

8.Modified Clock Gated Sense Amplifier Flip-flop (MCG-SAFF)

The working principle of the MCG-SAFF is same as that of CG-SAFF. Also, with the principle of CG-SAFF, MCG-SAFF includes the additional circuit in X to avoid asynchronous data sampling.
In CG-SGFF, for the input on D transitions, there may be occurring of asynchronous pulse generation on the internal clock during global clock CLK=0. In a small period node X will be going from charge to discharge before the switch turns off.
The asynchronous transition happens at the output if the value of X is powerful enough to flip the nodes to the production. If it not happens and also the first activate of the inferior pathway has not efficiently conceded the input D to the output, then the higher path serves as a support that will trigger at the subsequent falling edge of internal clock C.
There are various sets of transistor sizing that can cause the asynchronous data sampling to fully appear, partially appear or may hide while adjusting the transistor sizes around Node X. The circumstance that creates the asynchronous transition occurs when the voltage of Node X attains the critical value to flip the output.
The circuit‘s parameters such as transistor size are personalized to remove Asynchronous Data Sampling which is shown in Figure 4.
1. Balanced sized
2. Modified I
3. Modified II

9.Method to avoid Asynchronous data sampling

In this method the CLK is restricted by the evaluation of D and Q. If D has distorted because the final clock move and is dissimilar from Q, then CLK will go by to the second comparator to match up with the C. This CLK and C comparator reins the switch T2 between the CLK and C.

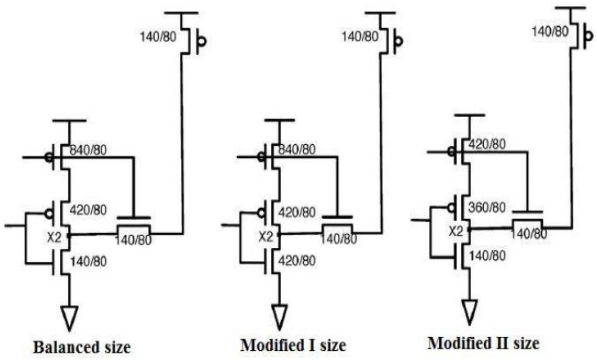


Fig. 4 . Modified Circuits on X

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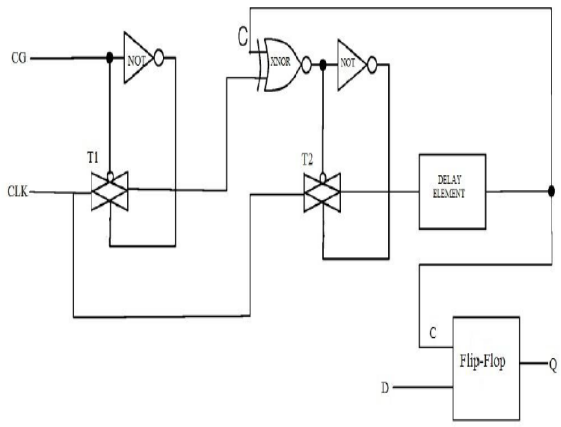
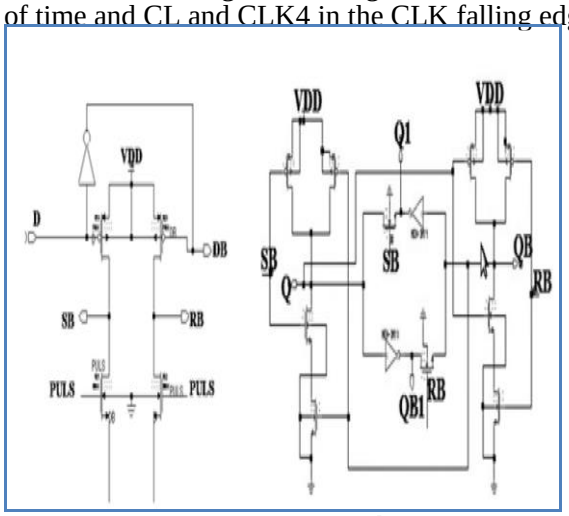


Fig.5. Method to avoid Asynchronous data sampling

At the moment of changing D CLK differs from C there is an occurring of Asynchronous sampling. Though with the second CLK & C comparator in Figure 5, the knob T2 will stay OFF when CLK ≠ C and C match with CLK. In the succeeding half cycle, the knob T2 turns ON, where CLK = C, but because they are equal, the flip-flop will not trigger until C changes, which follows CLK when is ON. Here, the modified II circuit gives the better power consumption when compared to another adjusted size.

10.Modified Clock Gated – Dual Edge Triggered Sense Amplifier Flip-Flops

The proposed sense amplifier flip-flops include three stages like the pulse generating stage, sensing step and the latching stage. The first two stages are similar to the Dual Edge triggered Sense Amplifier Flip-Flop (DET-SAFF) which is shown in Figure 1. The proposed MCG-DET SAFF is shown in Figure 6. Based upon sense-amplifier flip-flop (SAFF), the pulse generator samples the dataset. In the CLK rising edge, CLK and CLK3 together are high for a small duration of time and CL and CLK4 in the CLK falling edge.



(a) (b)

Fig. 6 . Proposed Modified Clock Gated – Dual Edge Triggered Sense Amplifier Flip-Flops
(a) Sensing Stage (b) Latching Stage

To pull-up, the output nodes, a high-speed symmetric latch is introduced to make use of SB and RB. RB is put in a high state if the input of D is high and at the same time transistors involved is in the state of pull-down network. It will make the quick discharge path recognized from QB to Ground. And if D is low, SB will set too high. Meanwhile, to pull up transistor by turning on and charges the output node Q to a high state by setting up the node SB as low. The internal set up is modified to get buffered differential outputs Q1 and QB1. It is to increase the speed from low to high output since the high-speed symmetric latch circuit instantly captures the input signal once the PULS generated.

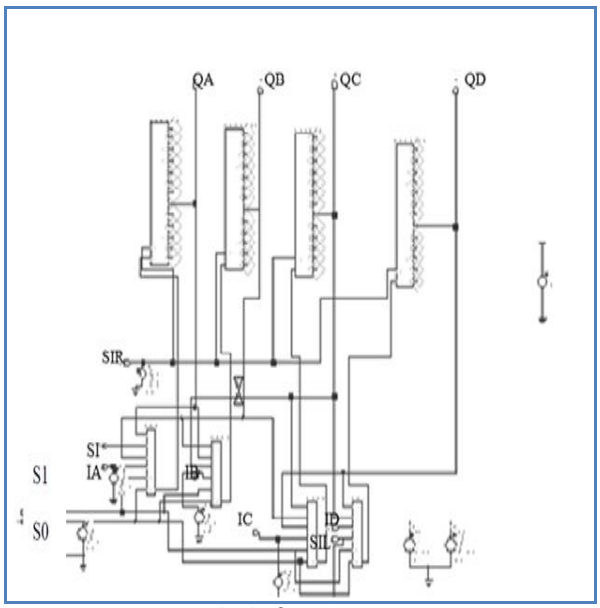


Fig.7. Universal Shift Register

In the proposed flip-flops, we introduce a universal shift register to hold up the previous state which is shown in Figure 7. If the input selected to the global shift register, S1=0, and S0=0 then the shift register holds the former state. If S1=0 and S0=1 then the entry performs shift right operation by taking a serial input (SIR), and in reverse, if S1= 1 and S0 = 0 then shift left activity will be performed. And at last if for the input S1=1 and S0=1 parallel input and parallel output operation will be performed.

11.Experimental Results and Discussion

The proposed MCGDET-SAFF was intended using chartered semiconductor Limited's CMOS 0.13μm process technology. The following Table-1 shows the set of all parameters used in the experimental setup and the experiment is carried out.

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Table-1: Experimental Setup Parameter and its Values

Parameter	Value
CMOS	0.13μm
Operating Temperature	27°C
Supply Voltage	1.0V
Tool	Mentor Graphics tool
Clock Frequency	0.8 GHz
Load Capacitance	100fF

The obtained results of the proposed MCGDET-SAFF are verified regarding consumed power and delay. The performance of the MCGDET-SAFF evaluated by comparing the obtained results of various flip-flops offered in earlier research works. The complete performance analysis of the multiple flip-flops is given in Table-2 and Table-3.

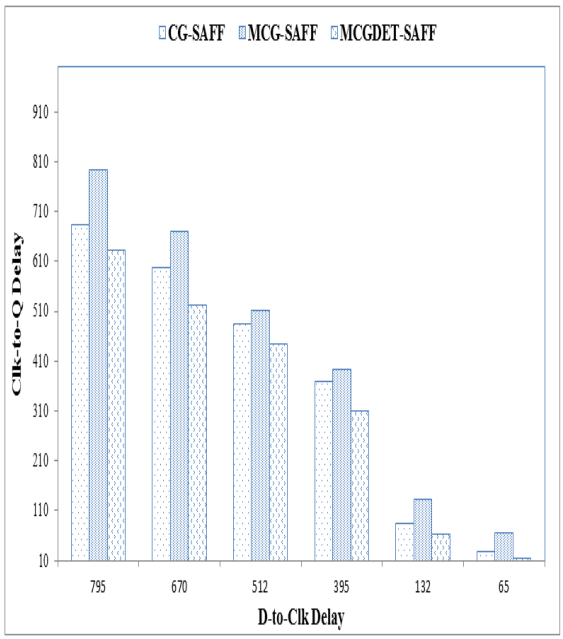


Fig. 8.CLK-to-Q delay as a function of D-to-CLK delay

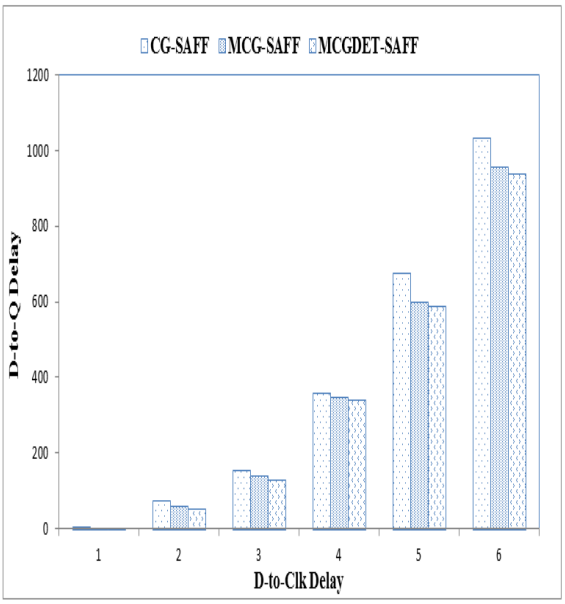


Fig. 9.D-to-Q delay as a function of D-to-CLK delay

Table-2: Performance Analysis of CG-SAFF @1.8v at Different Operating Frequencies for Different Switching Activity

Switching Activity	MOCF(GHz)	D-Q-Delay (ps)	Clk-to-Q Delay (ps)	RISE Time (ps)	Total Power Dissipation (nw)
25%	0.83	2646.88	642.01	1226.26	33.0154
	1	2547.87	542.91	1027.06	33.0154
	1.25	2050.97	445.96	829.15	33.0153
50%	0.83	2246.57	641.55	1225.66	33.0154
	1	2547.87	542.89	1027.16	33.0154
	1.25	2050.97	446.68	829.16	33.0154
75%	0.83	2646.97	642.01	1226.26	33.0154
	1	2547.87	542.9	1027.16	33.0154
	1.25	2050.97	445.97	829.16	33.0154
100%	0.83	2246.57	641.57	1225.66	33.0152
	1	2547.87	542.9	1027.16	33.0154
	1.25	1653.07	448.08	829.85	33.0154

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Table-3: Feature comparison of different FFs.

FF Design	CG-SAFF	MCG-SAFF	MCGDET-SAFF
Layout Area (mm^2)	69.13	64.23	63.12
Min D-to-Q Delay (ps)	120.23	90.17	84.35
Average power (0% all-0) µW	10.25	12.07	7.55
Average power (0% all-1) µW	10.35	12.76	7.45
Average power (12.5% activity) µW	12.68	13.11	12.11
Average power (25% activity)µW	14.95	15.95	14.95
Average power (50% activity)µW	19.87	18.46	19.43
Average power (100% activity)µW	26.15	24.15	24.15
Optimal PDP (25% activity) pJ	4.08	1.58	1.58

From the results, it obtained that the proposed MCGDET-SAFF has the lowest delay than the other FFs. It received 78% of the reduction in delay. There are various test patterns can be used for simulating the FF designs. In this paper, six models considered for multiple situations. The various probabilities are 25%, 50%, 75% and 100% for all 0's and 1's in data transition probabilities. The obtained results are given in Table-2. From the results presented in Table-3, the proposed MCGDET-SAFF architecture concluded as a better architecture in all the ways. The MCGDET-SAFF architecture utilizes the least number of transistors related to the architecture; the layout area reduced in the design. For example, the 10% of leakage power cut, and about 20% enhances the best PDP in 25% of activity.

Table-4: Comparison Results of CG-SAFF and MCGDET-SAFF

Designs	MCG-SAFF	MCGDET-SAFF
Clk-to-Q delay(ps)	187.03	152.04
Min D-to-Q delay(ps)	592.03	307
Rise Time (ps)	79.809	90
Fall Time (ps)	800	199
MOCF (GHZ)	1.25	1.25
Number of Transistors	38	22

Table-1 demonstrates the performance study of CG-SAFF and MCG-SAFF with MCGDET-SAFF.

The proposed MCGDET-SAFF obtained the least Clk-to-Q delay between the flip-flops. It earned more than 80% of the decrease in backlog. Finally, the Table-4 shows the comparison results of CG-AFF, MCG-SAFF, and MCGDET-SAFF flip flops. Also, from the experimental results, the power dissipation for various input switching activates for different FF designs, the proposed MCGDET-SAFF obtained better results. Concerned with PDP, the MCG-SAFF utilizes 6.5% more PDP compared with the MCGDET-SAFF. Though, the proposed MCGDET-SAFF outperforms than the other FF designs.

12.Conclusion

The primary objective of this paper is to design an experiment novel flip-flop architecture for low power and high-performance applications. To do that, this paper, proposed a modified clock gated dual edge triggered sense amplified flip-flop where it uses various significant features integrated from several types of flip-flops. Less power consumption, less area, power leakage reduction and delay reduction are the main features utilized by multiple FFs. The proposed MCGDET-SAFF comprises of CG circuit in the pulse generator design which acquires more delay in the Clk-to-Q and D-to-Q mechanism in MCGDET-SAFF. The proposed MCGDET-SAFF circuit obtained 79% less delay than existing architectures. The proposed design obtained substantial power reduction by integrating DET and conditional precharging. It also diminishes latency by using a fast latch. This new design is established to decrease the power dissipation and delay when associated with the clock gated sense amplifier flip-flop up to 26.1% and 86.5% respectively.

References

1. Y.-T. Liu, L.-Y. Chiou, and S.-J.Chang, "Energy-efficient adaptive clocking dual edge sense-amplifier flip-flop," *IEEE International Symposium on Circuits and Systems*, pp. 4329- 4332, 2006.
2. S. Kim, C. H. Ziesler, and M. C.Papaefthymiou "Charge-recovery computing on silicon," *IEEE Transactions on Computers*, vol.54, no.6, pp.651 – 659, June 2005.
3. H. Kawaguchi and T. Sakurai, "A reduced clock-swing flip-flop (RCSFF) for 63% power reduction," IEEE J. Solid-State Circuits, vol. 33, no. 5, pp. 807–811, May 1998.
4. N. Nedovic, W. W. Walker, V. G. Oklobdzija, and M. Aleksic, "A low power symmetrically pulsed dual edge-triggered flip-flop," *Proceedings of the 28th European Solid-State Circuits Conferenc*e, pp. 399 – 402, September 2002.
5. M. Cooke, H. Mahmoodi-Meimand,

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and K. Roy, “Energy recovery clocking scheme and flip-flops for ultra-low energy applications," *Proceedings of the 2003 International Symposium on Low Power Electronics and Design*, pp. 54 – 59, August 2003.

6. P. Hofstee, N. Aoki, D. Boerstler, P. Colman, S. Dhong, B. Flachs, N. Kojima, O. Kwon, K. Lee, D. Meltzer, K. Nowka, J. Park, J. Peter, S. Posluszny, M. Shapiro, J. Silberman, O. Takahashi, and B. Weinberger, “1 GHz single-issue 64 b PowerPC processor”, *IEEE Solid-State Circuits Conference*, pp. 92 – 93, February 2000.
7. V. F. Pavlidis, I. Savidis, and E. G. Friedman, “Clock distribution networks in 3-D integrated systems”, *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, pp. 1-11, 2010.
8. K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, “Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," *Proc. of the IEEE*, vol. 91, no. 2, pp. 305 – 327, February 2003.
9. N. Nedovic, V. G. Oklobdzija, "Dual-edge triggered storage elements and clocking strategy for low-power systems,"*IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 13, no. 5, pp.577 –590, May 2005.
10. N. Nedovic, M. Aleksic, and V. G. Oklobdzija, "Timing characterization of dual-edge triggered flip-flops," *Proceedings 2001, International Conference on Computer Design*, pp. 538 – 541, September 2001.
11. S. E. Esmaeili, A. J. Al-Khalili, and G. E. R. Cowan, “Dual-edge triggered energy recovery DCCER flip-flop for low energy applications’, *European Conference on Circuit Theory and Design*, *ECCTD*, pp. 57-60, August 2009.
12. L.-Y. Chiou, S.-C. Lou, "An energy-efficient dual-edge triggered level-converting flip-flop," *IEEE International Symposium on Circuits and Systems*, pp. 1157 – 1160, May 2007.
13. S. E. Esmaeili, A. J. Al-Khalili, and G. E. R. Cowan, "Dual-edge triggered sense amplifier flip-flop for resonant clock distribution networks," *IET Computers and Digital Techniques*, vol. 4, Iss. 6, pp. 499-514, 2010.
14. N. Nedovic, M. Aleksic, and V. G. Oklobdzija, “Conditional precharge techniques for power-efficient dual-edge clocking,” in Proc. 2002 Int. Symp. Low Power Electronics Design (ISPLED 2002), 2002, pp. 56–59.
15. M. H. Ghadiri, "Dual-edge triggered static pulsed flip-flops," *18th International Conference on VLSI Design*, pp. 846 – 849, 2005.
16. Y. Hu, Z. Li, R. Zhou, "A new type of high-performance low-power low clock-swing TSPC flip-flop," *7th International Conference on ASIC*, pp.130 – 133, October 2007.
17. V. Stojanovic, V. G. Oklobdzija, "Comparative analysis of master-slave latches and flip-flops for high-performance and low-power systems," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 4, pp. 536 – 548, April 1999.
18. C. Kim, S. M. Kang, "A low-swing clock doubled-edge triggered flipflop," *Symposium on VLSI circuits*, pp.183-186, June 2001.
19. Z Chen, M Johnson, L Wei, and K Roy, “Estimation of Standby Leakage Power in CMOS Circuits Considering Accurate Modeling of Transistor Stacks,” Proceedings of the 1998 international symposium on Low power electronics and design, pp. 239-224.
20. Y. Tsividis, Operation, and Modeling of MOS Transistor, McGraw-Hill, New York, 1987.
21. W.M. Chung, T. Lo, and M. Sachdev, “A comparative analysis of low-power low voltage dual-edge-triggered flip-flops," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2001 (accepted).
22. M. Pedram, Q. Wu, and X. Wu, "A New Design of Double Edge-Triggered Flip-Flops," 1998 Proceedings of the Asian and South Pacific Design Automation Conference (ASPDAC'98), pp. 417-421, 1998.
23. S. E. Esmaeili, R. Islam, A. J. Al-Khalili, and G. E. R. Cowan, “Dual-Edge Triggered Sense Amplifier Flip-Flop Utilizing an Improved Scheme to Reduce Area, Power, and Complexity," 19th IEEE International Conference on Electronics, Circuits, and Systems (ICECS), 2012.

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