DESIGN AND IMPLEMENTATION OF NEW ASYMMETRIC FIFTEEN LEVEL INVERTER WITH MINIMUM NUMBER OF SWITCHING DEVICES

V. Thiyagarajan[1], P. Somasundaram[2]
[1]Assistant Professor, Department of EEE, SSN College of Engineering, Kalavakkam, Tamilnadu, India.
[2]Associate Professor, Department of EEE, CEG, Anna University, Chennai, Tamilnadu, India.
Email: thiyagarajanv@ssn.edu.in

Abstract: *This paper proposes a new asymmetrical type fifteen level inverter with minimum number of power electronic switches to reduce THD. The proposed inverter consist of three DC voltage sources, seven main switches and four switches of H-bridge inverter to generate fifteen level output. The proposed multilevel inverter is very simple to construct and is suitable for medium voltage and high power applications. Different methods of calculating the switching angles are presented and the results are compared. The performance of the proposed fifteen level inverter is compared with other topologies. The simulation is performed using MATLAB/SIMULINK software to verify the function of the proposed inverter.*

Key words: *Multilevel inverter, Switching angle, Gate pulse, Asymmetric, THD.*

1. Introduction

Inverters plays an important role in modern power system. The various applications of inverters includes variable frequency drives, active filters, air conditioning, uninterruptible power supplies, high-voltage dc transmission system and flexible ac transmission systems [1-3]. The major classification of inverters includes: square wave inverters, quasi-square wave inverters and multilevel inverters (MLI) [3-4]. Among these, the multilevel inverters has an attractive solution in the medium voltage and high power applications [5]. The significant qualities of multilevel inverter includes low dv/dt stress, low distortion, high power quality, lesser common mode voltage, minimum switching losses, minimum electromagnetic interference, better control and use of renewable energy resources [6]. The multilevel inverter synthesize the staircase output voltage from the several independent DC voltage sources. The power electronic switches were controlled such that it aggregate these multiple DC voltage levels to achieve high output voltage. The rated voltage of the power electronic switches depends on the rating of the DC voltage. Therefore, the voltage stress on a power electronic switch is much lower than the operating voltage. The conventional topologies of multilevel inverters includes diode-clamped, flying capacitor and cascaded H-bridge inverters[6-9]. The multilevel inverter can be symmetric or asymmetric. In a symmetric inverter, all voltage sources have same magnitude. However, in an asymmetric inverter, each voltage sources have different magnitude.

Modern-day research has focused on developing new topologies of multilevel inverters with reduced number of components and novel pulse-width modulation (PWM) techniques. A selective harmonic mitigation pulse-width modulation (SHM-PWM) technique for the multilevel inverter is presented in [10]. In [11], the modified SHM-PWM technique is proposed. It employs the use of variable DC-link voltages. It will increases the range of modulation indices, reduces the number of switching transitions and minimizes the harmonics. A cascaded H-bridge multilevel inverter consisting of five level transistor clamped H-bridge power units is presented in [12]. It uses multicarrier phase-shifted PWM technique to achieve balanced power distribution among the power units. A modified cascaded multilevel inverter is proposed in [13]. This inverter consists of active input rectifier and H-bridge inverter. This inverter have the capability to control the input current and output voltage during the motoring and regenerative mode of operation. A symmetrical single phase seven level inverter is proposed in [14]. It uses three voltage sources and six switches to generate seven level output voltage. In this paper, the carrier based PWM techniques are used to generate the switching pulses.

This paper proposes a modified asymmetrical fifteen level inverter with reduced number of power electronic switches. The proposed inverter produces fifteen level output voltage with minimum THD using seven main switches, four switches of H-bridge inverter and three DC Voltage sources. Section-2 describes the proposed fifteen level inverter and its different modes of operation. Section-3 explains the different methods of calculating the switching angles. The simulation results are presented in Section-4 and hardware result is shown in Section-5. The conclusions are presented in Section-6.

2. Proposed Asymmetric Multilevel Inverter

The proposed "asymmetric" fifteen level inverter is shown in Fig. 1. The magnitude of each DC voltage sources are different and hence the term "asymmetric" is used. The proposed multilevel inverter consists of two sections, namely, level creator section and polarity changing section. The mail level creator section consist of 3 DC voltage sources and 7 main switches. This level creator part helps to produce unidirectional output voltage with various voltage levels such as 0, V_{dc}, $2V_{dc}$, $3V_{dc}$, $4V_{dc}$,

$5V_{dc}$, $6V_{dc}$ and $7V_{dc}$.

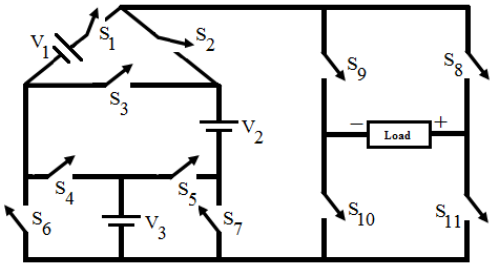
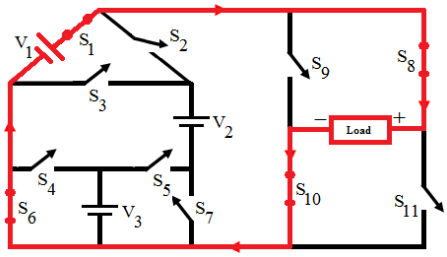
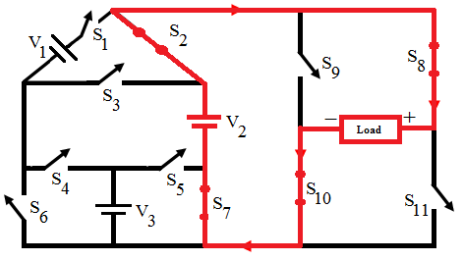


Fig. 1. Proposed topology of Multilevel Inverter

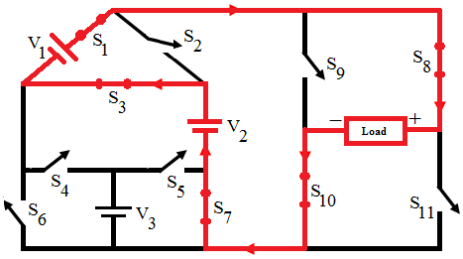
The conventional H-bridge inverter acts as a polarity changing section. This section helps to convert the unidirectional output voltage into bidirectional output voltage. When the switches S_8 and S_{10} are ON, positive levels of voltages are obtained and when the switches S_9 and S_{11} are ON, the negative levels of voltages are obtained.



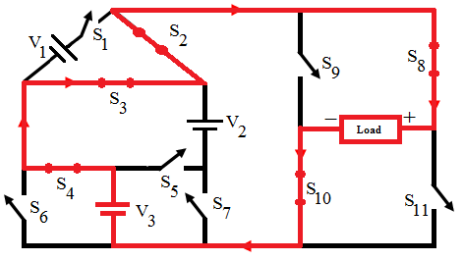
(a) Mode -1



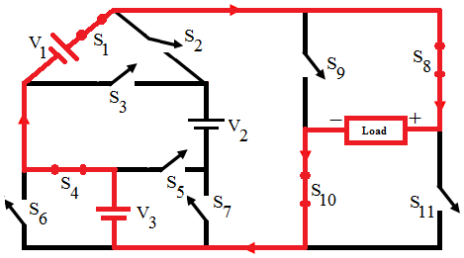
(b) Mode - 2



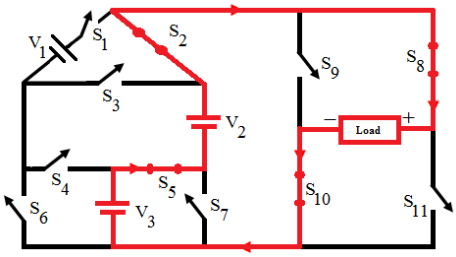
(c) Mode - 3



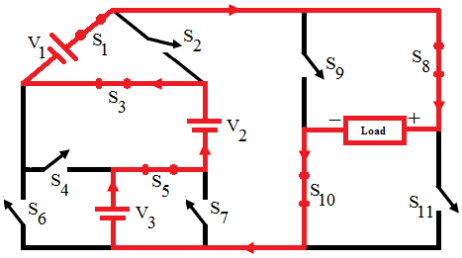
(d) Mode - 4



(e) Mode - 5



(f) Mode - 6



(g) Mode - 7

Fig. 2. Modes of operation

The different modes of operation of the proposed fifteen level inverter are shown in Fig. 2. In mode-1, the voltage V_1 is obtained across the load. In this mode, the switches S_1 and S_2 are ON as shown in Fig. 2(a). During mode-2, the switches S_2 and S_8 are ON and the voltage V_2 is obtained across the load as shown in Fig. 2(b). The voltage V_1+V_2 is obtained during the mode-3 operation. In this mode, the switches S_1, S_3 and S_7 are ON as shown in Fig. 2(c). Fig. 2(d) shows mode-4 operation of the proposed inverter, where the switches S_2, S_3 and S_4 are ON and the voltage V_3 is obtained. The mode-5 is shown in Fig. 2(e). In this mode, the voltage V_1+V_3 is obtained by turning ON the switches S_1 and S_4. During mode-6, the switches S_2 and S_5 are ON and the voltage V_2+V_3 is obtained across the load as shown in Fig. 2 (f). The maximum voltage $V_1+ V_2+V_3$ is obtained during the mode-7 operation as shown is Fig. 2(g). During this mode, the switches S_1, S_3 and S_5 are ON.

The mode-1 to mode-7 are positive modes of operation where the positive voltages obtained across the load. In these modes of operation, the switches S_8 and S_{10} are ON. When the switches S_9 and S_{11} are ON, the negative modes of operation is achieved, where the voltages are negative. The different switching states of the proposed fifteen level inverter is given in Table 1.

Table 1
Switching states

S.No	S_1	S_2	S_3	S_4	S_5	S_6	S_7	Voltage
1	0	1	1	0	0	1	0	0
2	1	0	0	0	0	1	0	$V_1 = V_{dc}$
3	0	1	0	0	0	0	1	$V_2 = 2V_{dc}$
4	1	0	1	0	0	0	1	$V_1 + V_2 = 3V_{dc}$
5	0	1	1	1	0	0	0	$V_3 = 4V_{dc}$
6	1	0	0	1	0	0	0	$V_1 + V_3 = 5V_{dc}$
7	0	1	0	0	1	0	0	$V_2 + V_3 = 6V_{dc}$
8	1	0	1	0	1	0	0	$V_1 + V_2 + V_3 = 7V_{dc}$

The comparison of the output voltage levels with the number of DC voltage sources and the number of switches for different topologies of multilevel inverter are given in Table 2.

Table 2
Comparison of different Multilevel Inverters

Inverter	Number of DC Sources (N_{dc})	Number of Switches (N_S)	Number of level (N)	Ratio (N_{dc} / N)	Ratio (N_S / N)
Cascaded H-bridge inverter	3	12	15	0.20	0.80
Ref. [15]	4	5	7	0.57	0.71
Ref. [16]	4	11	15	0.27	0.73
Ref. [17]	4	12	17	0.24	0.71
Ref. [18]	4	12	9	0.44	1.33
Proposed inverter	**3**	**11**	**15**	**0.20**	**0.73**

From the above table, it is clear that the proposed multilevel inverter uses minimum number of switches to achieve fifteen level output voltage.

3. Switching Angle Calculation

Switching angles plays an important role in the reduction of total harmonic distortion (THD). It is known that 2(n-1) switching angles has to be determined for 'n' level inverter[19]. An 'n' level inverter has (n-1)/2 main switching angles corresponding to the period 0 to π/2. The switching angles of n-level inverter is shown in Fig. 3. The different methods of calculating switching angles are given below:

Method - 1
In method-1, the switching angles are distributed averagely over the range 0–π and are determined by,

$$\theta_k = k\left(\frac{180^0}{n}\right) \text{where}, k = 1,2,...,\left(\frac{n-1}{2}\right)$$

Method - 2
In method-1, the main switching angles are determined by,

$$\theta_k = k\left(\frac{180^0}{n+1}\right) \text{where}, k = 1,2,...,\left(\frac{n-1}{2}\right)$$

Method - 3
In method-3, the gaps between the positive half-cycle and the negative half-cycle were reduced by using the following formula,

$$\theta_k = \frac{1}{2}\sin^{-1}\left(\frac{2k-1}{n-1}\right) \text{where}, k = 1,2,...,\left(\frac{n-1}{2}\right)$$

Method - 4
The method-4 gives better output voltage waveform. The main switching angles are determined by the following formula,

$$\theta_k = \sin^{-1}\left(\frac{2k-1}{n-1}\right) \text{where}, k = 1,2,...,\left(\frac{n-1}{2}\right)$$

For the proposed multilevel inverter, there are seven main switching angles and are given in Table 3.

Table 3
Switching Angles

Angle	Main Switching Angles (in degree)			
	Method- 1	**Method- 2**	**Method- 3**	**Method- 4**
θ_1	12	11.25	2.048	4.096
θ_2	24	22.5	6.1868	12.3736
θ_3	36	33.75	10.4624	20.9248
θ_4	48	45	15	30
θ_5	60	56.25	20.0026	40.0052
θ_6	72	67.5	25.8934	51.7868
θ_7	84	78.75	34.1066	68.2132

The other switching angles are obtained using the following relations [19]:

1. For period 0 to π/2 : $\theta_1, \theta_2, \ldots, \theta_{(n-1)/2}$.

2. For period π/2 to π : $\theta_{(n+1)/2}. . ., \theta_{(n-1)}. = (\pi-\theta_{(n-1)/2}),. . .,(\pi-\theta_1)$.

3. For period π to 3π/2 : $\theta_n, . . ., \theta_{3(n-1)/2} = (\pi+\theta_1),. . .,(\pi+\theta_{(n-1)/2})$.

4. For period 3π/2 to 2π : $\theta_{(3n-1)/2}, . . ., \theta_{2(n-1)} = (2\pi-\theta_{(n-1)/2}),. . .,(2\pi-\theta_1)$.

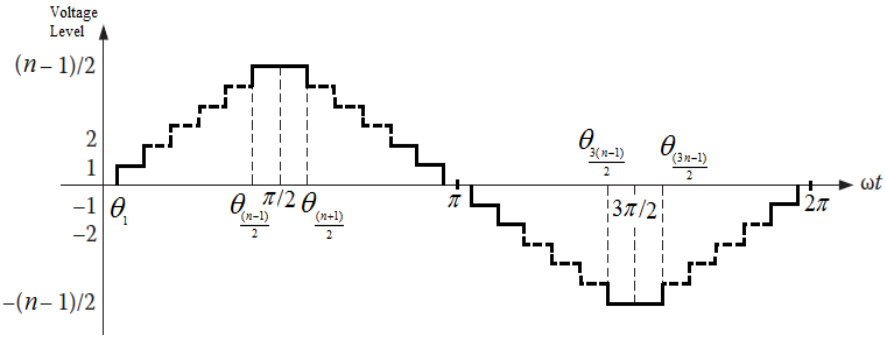
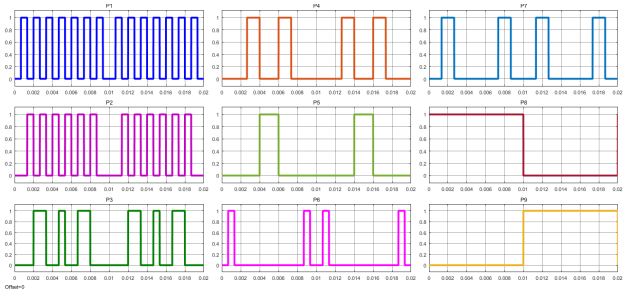
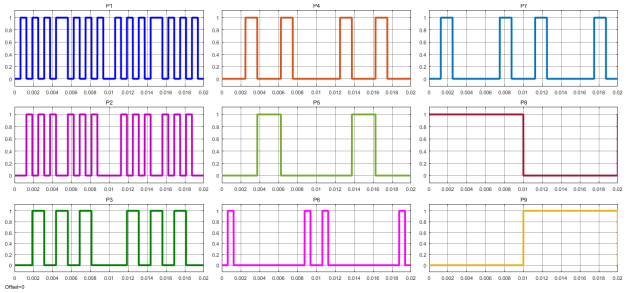


Fig. 3. Output Voltage with switching angles of 'n' level inverter

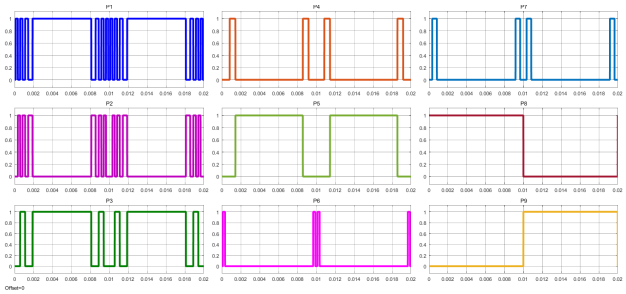
The switching pulses generated using the different methods are shown in Fig. 4.



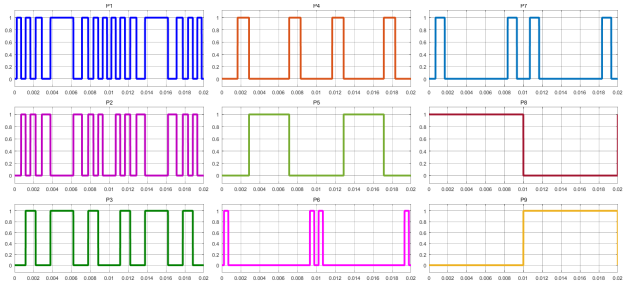
(a)



(b)



(c)

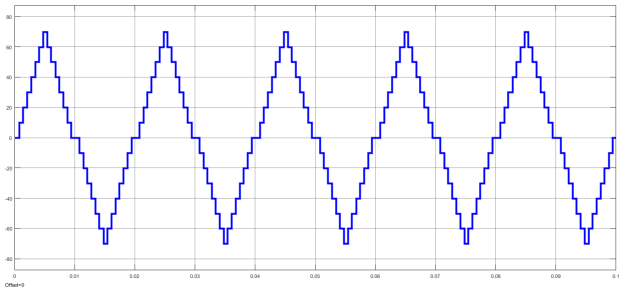


(d)

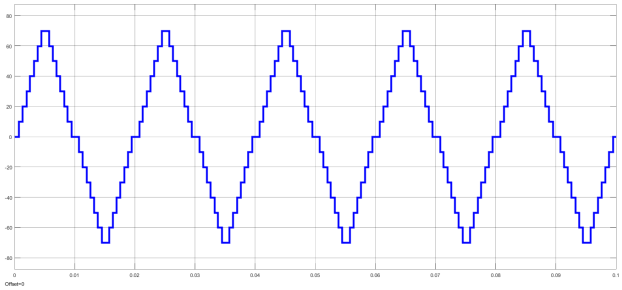
Fig. 4. Switching pulses (a) Method - 1 (b) Method - 2 (c) Method - 3 and (d) Method - 4

4. Simulation Results

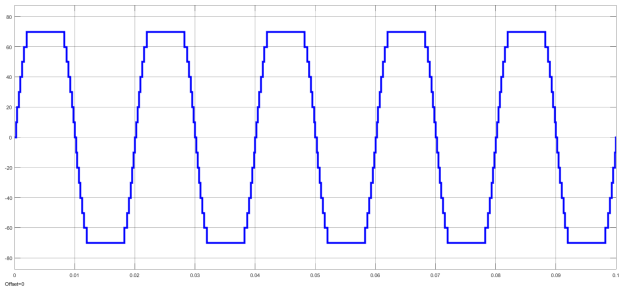
The simulation results obtained using MATLAB software are presented in this section. The different DC voltage sources have the following magnitudes: $V_1 = V_{dc} = 10V$, $V_2 = 2V_{dc} = 20V$ and $V_3 = 4V_{dc} = 40V$ i.e., the voltages are in the ratio $V_1 : V_2 : V_3 = 1 : 2 : 4$. The maximum output voltage obtained is 70V (i.e. $V_1+V_2+V_3$). The output voltage of the proposed fifteen level inverter for different methods are shown in Fig. 5. The output voltage has 15 levels (i.e., 7 positive, 7 negative and 1 zero).



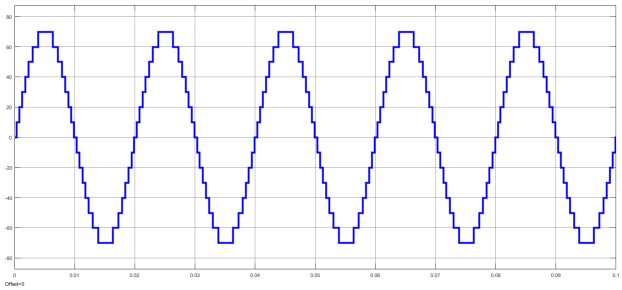
(a)



(b)



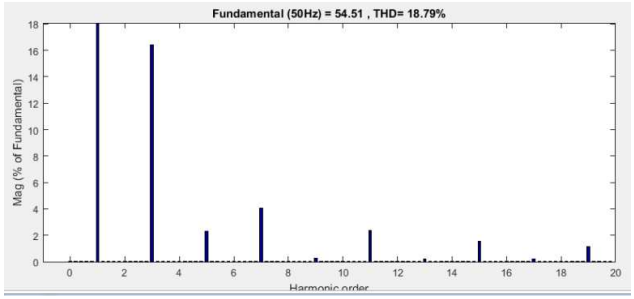
(c)



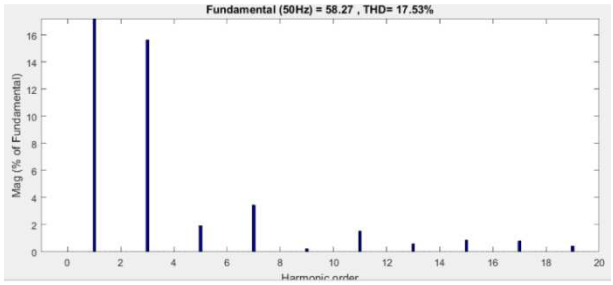
(d)

Fig. 5. Output Voltage (a) Method - 1 (b) Method - 2 (c) Method -3 and (d) Method - 4.

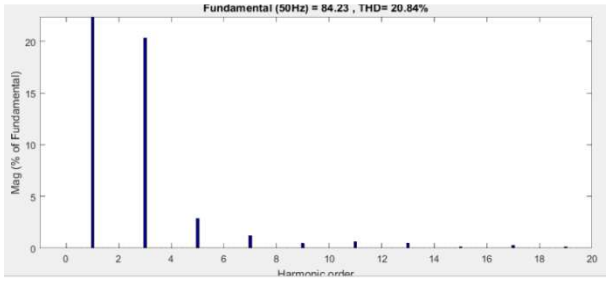
Fig. 6 shows the FFT analysis of the output voltage of the proposed fifteen level inverter for different methods.



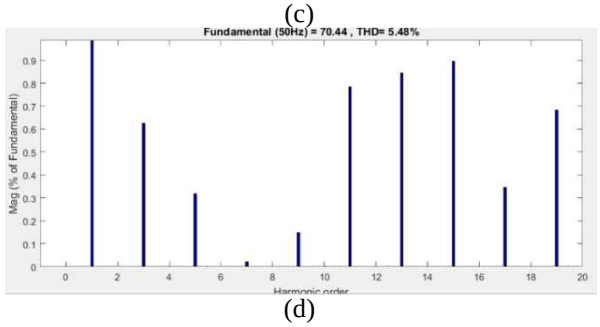
(a)



(b)



(c)



(d)

Fig. 6. FFT Analysis (a) Method - 1 (b) Method - 2 (c) Method - 3 and (d) Method - 4

From the results, it is observed that the method - 4 gives the output voltage similar to the sinusoidal waveform with minimum THD of 5.48% and the fundamental output voltage of 70.44 V. Table 4 shows the comparison of the THD of the output voltage waveform and fundamental output voltage obtained using different methods.

Table 4
Comparison of THD and Fundamental output voltage

Method	THD (%)	Fundamental output Voltage (V)
Method - 1	18.79	54.51
Method - 2	17.53	58.27
Method - 3	20.84	84.23
Method - 4	**5.48**	70.44

The above table shows that the proposed fifteen level inverter achieves minimum THD and higher output level with minimum number of power electronic switches. Table 5 shows the comparison of the THD of the fifteen level output voltage waveform with the available references.

Table 5
Comparison of THD

THD	Ref.[19]	Ref.[20]	Proposed
THD (%)	5.67	6.12	**5.48**

The above table shows that the proposed fifteen level inverter achieves minimum THD as compared with the references.

5. Hardware setup

The hardware setup of the proposed fifteen level inverter is shown in Fig. 7.

Fig. 7. Hardware of the Proposed Multilevel Inverter

The MOSFET ISA04N60A is used as a switching device. The gate pulses are generated using PIC16F877A microcontroller. TLP250 powered from a 0-12V transformer is used for a

gate driver circuit. The operating frequency of the microcontroller is 20 MHz. The fifteen level output voltage waveform of the hardware setup is shown in Fig. 8.

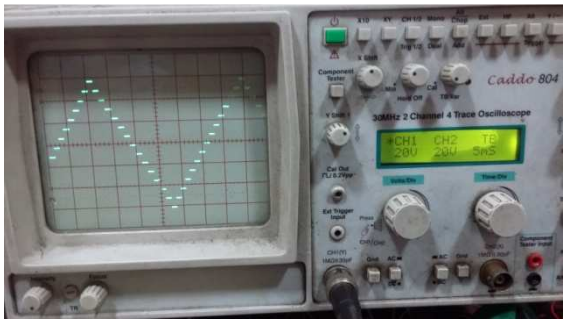


Fig. 8. Hardware Result

The experimental result of the proposed fifteen level inverter matches very closely to the simulation result.

6. Conclusion

This paper proposed a modified topology of asymmetric fifteen level inverter with minimum number of switching components. The proposed inverter achieves fifteen level output voltage with 3 DC voltage sources, 7 main switches and 4 H-bridge switches. The DC voltage sources have different voltage magnitudes. The different methods of calculating the switching angles are presented. A comparison of the proposed multilevel inverter topology with other topologies is presented in this paper. The performance of the proposed inverter is analysed using MATLAB software. The simulation and hardware results exhibit the better performance and feasibility of the proposed inverter. The result shows that maximum voltage obtained is 7Vdc and the method - 4 achieves minimum THD of the output voltage waveform.

References

[1] M.H. Rashid: *Power Electronics Handbook*. In: Elsevier, 2001.

[2] R. H. Baker and L. H. Bannister: *Electric Power Converter*. In: U.S. Patent 3 867 643, Feb. 1975.

[3] K. K. Gupta, A. Ranjan, P. Bhatnagar, L. K. Sahu and S. Jain: *Multilevel Inverter Topologies With Reduced Device Count: A Review*. In: IEEE Trans. on Power Electronics, vol. 31, no. 1, pp. 135-151, Jan. 2016.

[4] S. Daher, J. Schmid, and F. L. M. Antunes: *Multilevel inverter topologies for stand-alone PV systems*. In: IEEE Trans. Ind. Electron., vol. 55, no. 7, pp. 2703–2712, Jul. 2008.

[5] S. De, D. Banerjee, K. S. Kumar, K. Gopakumar, R. Ramchand and C. Patel: *Multilevel inverters for low-power application*. In IET Power Electron., vol. 4, no. 4, pp. 384-392, April 2011.

[6] Boora, A. A., Nami, A., Zare, F., Ghosh, A. and Blaabjerg, F.: *Voltage sharing converter to supply single-phase asymmetric four-level diode clamped inverter with high power factor loads*. In: IEEE Trans. Power Electron., vol. 25, no. 10, pp. 2507–2520, Oct. 2010.

[7] Khazraei, M., Sepahvand, H., Corzine, K. A. and Ferdowsi, M.: *Active Capacitor Voltage Balancing in Single-Phase Flying-Capacitor Multilevel Power Converters.* In*:* IEEE Trans. Ind. Electron. vol. 59, no. 2, pp. 769-778, Feb. 2012.

[8] Rodriguez, J., Bernet, S., Steimer, P. and Lizama, I.: *A survey on natural point clamped inverters.* In: IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2219–2230, Jul. 2010.

[9] Ding, K., Cheng, K. W. E., and Zou, Y. P.: *Analysis, of an asymmetric modulation methods for cascaded multilevel inverters*. In. IET Power Electron., vol. 5, no. 1, pp. 74–85, Jan. 2012.

[10] J. Napoles, A. J. Watson, and J. J. Padilla: *Selective harmonic mitigation technique for cascaded H-bridge converter with nonequal dc link voltages*. In: IEEE Trans. Ind. Electron., vol. 60, no. 5, pp. 1963–1971, May 2013.

[11] A. Moeini, H. Iman-Eini and M. Bakhshizadeh: *Selective harmonic mitigation-pulse-width modulation technique with variable DC-link voltages in single and three-phase cascaded H-bridge inverters*. In: IET Power Electronics, vol. 7, no. 4, pp. 924-932, April 2014.

[12] N. A. Rahim, M. F. M. Elias and W. P. Hew: *Transistor-Clamped H-Bridge Based Cascaded Multilevel Inverter With New Method of Capacitor Voltage Balancing*. In: IEEE Trans. Ind. Electron., vol. 60, no. 8, pp. 2943-2956, Aug. 2013

[13] P. Lezana, J. Rodriguez and D. A. Oyarzun: *Cascaded Multilevel Inverter With Regeneration Capability and Reduced Number of Switches*. In: IEEE Trans. Ind. Electron., vol. 55, no. 3, pp. 1059-1066, March 2008.

[14] Venkataramanan K., Shanthi B., and Sivakumaran T.S.: *Investigations on Inverted Sine PWM Strategies for Symmetric Multilevel Inverter*. In: Journal of Electrical Engineering, Vol. 16, No. 3, pp. 83-88, 2016.

[15] A. Chitra and S. Himavathi: *Reduced switch multilevel inverter for performance enhancement of induction motor drive with intelligent rotor resistance estimator*. In: IET Power Electronics, vol. 8, no. 12, pp. 2444-2453, 12 2015.

[16] E. Babaei, S. Laali and Z. Bayat: *A Single-Phase Cascaded Multilevel Inverter Based on a New Basic Unit With Reduced Number of Power Switches*. In: IEEE Trans. Ind. Electron., vol. 62, no. 2, pp. 922-929, Feb. 2015.

[17] A. Mokhberdoran and A. Ajami: *Symmetric and Asymmetric Design and Implementation of New Cascaded Multilevel Inverter Topology.* In: IEEE Transactions on Power Electronics, vol. 29, no. 12, pp. 6712-6724, Dec. 2014.

[18] Siva Sai Krishna, Chandra Sekhar, Nagi Reddy : *Simulation of a Cascaded Multilevel Inverter Topology with Reduced Number of Switches and Sources Arranged in Matrix Structure*. In: Journal of Electrical Engineering, Vol. 16, No. 4, pp. 375-383, 2016.

[19] Luo F. L. and Ye H.: *Advanced DC/AC Inverters*. In: CRC Press LLC, 2013. ISBN: 978-1-4665-1138-5.

[20] H.B. FAROUK and A. FOUAD: *Comparison of Cascaded Fifteen Level Inverter Multicarrier SPWM Strategies*. In: Journal of Electrical Engineering, Vol. 15, No. 3, pp. 270-279, 2015.