Comparison and Mitigation of Harmonics Using Different Optimization Techniques for SHE-PWM of Single-Phase Novel Symmetrical Multilevel Inverter

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Abstract

This paper suggests a novel configuration symmetrical single phase multilevel inverter topology which imposes a minimum count of switches and driver circuits while contrasted with conservative multilevel inverter topologies. A nine level single phase output voltage is engendered using eight switches. The proposed topology can be able to elongate effortlessly to obtain 'n' levels in the output voltage. The simulation result of nine level multilevel inverter is obtained from MATLAB®Simulink. The desired output voltage is obtained by mitigating low order harmonics offered by Selective Harmonic Elimination - Pulse Width Modulation (SHE-PWM). Distinct optimization techniques such as Particle Swarm Optimization (PSO), Bee Colony Optimization (BCO) and Ant colony optimization (ACO) are adopted for the proposed inverter. On comparing the optimization techniques, Ant colony optimization mitigates the 5^{th} and 7^{th} order harmonics to a great extent. Conclusively, the framework is done which validate the opportune experimental result with simulated response.

Key words: Multilevel inverter, SHE, PSO, BCO, ACO

I. INTRODUCTION

In recent years of electric power generation, transmission, distribution and utilization, power conversion is an essential innovation. Multilevel inverters are key innovation in conversion of dc to ac power which plays a substantial role in variable frequency drives, filter networks, non conventional energy resources, traction systems, UPS, etc. [1–6]. Conventional inverters can engender only two levels of output voltage $+V_{dc}$ and $-V_{dc}$. The two level output voltage has huge number of harmonics. To obtain a sinusoidal waveform, an inexorable filter is utilized. Though, the above said inverter has few impediments when operated in high voltage / current application. High voltage in multilevel inverters can be acquired through low power rating devices [7–9]. Multilevel inverter (MLI) has countless benefits when contrasted with conventional two-level inverter. Minimal electromagnetic interference, device stress and reduced harmonic distortion are the effects caused by increased number of output voltage level in the inverter [5, 6, 10–13].

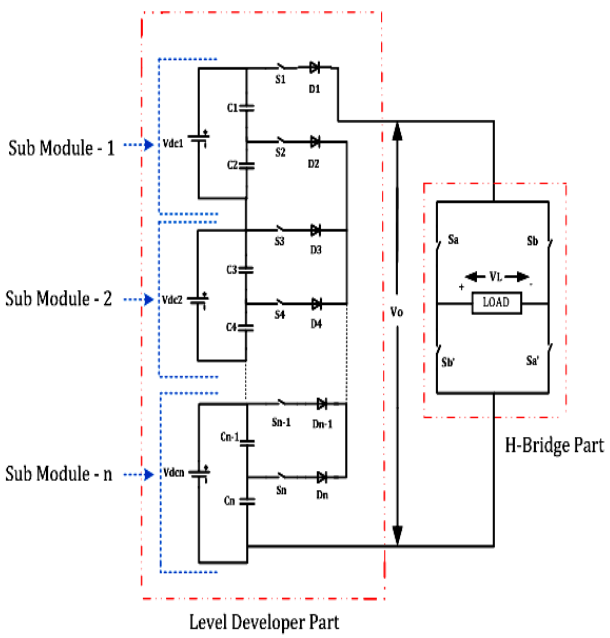


Fig.1 Generalized model of proposed n-level MLI

The multilevel inverter engenders a stepped output voltage by turning on the power semiconductor devices in a specific sequence utilizing numerous dc voltage sources. MLIs are predominantly categorized as flying capacitor type (FCMLI), cascaded H-bridge type (CHB) and neutral point clamped type (NPC) [14–16]. Nevertheless, these topologies have few shortcomings such as immense in size, incremented count of electronic components and intricate control systems. The main

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obstacle in NPC multilevel inverter is, when the number of levels in the output voltage is increased more number of clamping diodes are entailed and unequal voltage is shared amid the series connected capacitors. Flying capacitors are utilized for clamping in FCMLI topology. Conversely, if the step in output voltage is increased then an ample number of storage capacitors are needed. CHB multilevel inverters are popular because of its modularized structure and symmetrical arrangement. These inverters are in need of more number of DC sources and power semiconductor switches which increase the overall system size and cost which became an obstacle for CHB topology. A novel multilevel inverter topology is suggested in this paper which performs as a generalized model. The output voltage level waveform can be increased up to 'n' level by connecting minimum count of dc sources and power switches with the generalized model. Using the suggested topology, a nine level symmetrical MLI is designed and simulated using MATLAB®Simulink.

II. NOVEL MULTILEVEL INVERTER TOPOLOGY

Fig.1 shows the generalized diagram of proposed n-level MLI. It comprises of two parts, H-Bridge part and level developer part. The H-Bridge part is made up of four switches S_a, S_a', S_b, S_b' which transmutes the polarity of the output voltage in every half cycle. The level developer part is a sub module circuit which can be extended up to n-level. Each sub module circuit contains a single dc source. A pair of capacitors is connected across the single dc source. The switches S_1, S_2,…..S_{n-1}, S_n generates the output voltage level.

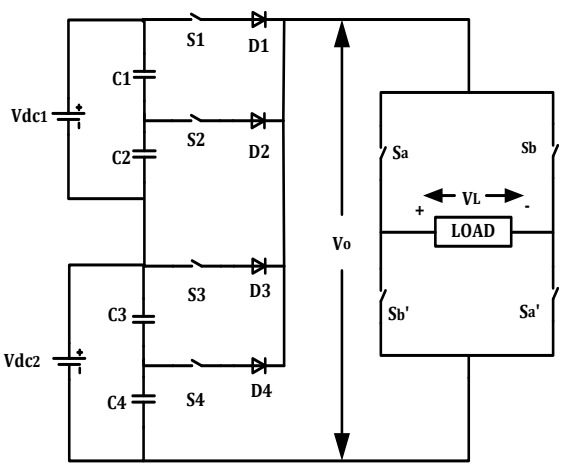


Fig.2 Proposed nine level MLI

A single phase nine level output voltage can be generated by the use of two sub module level developer part integrated with H- bridge part. The circuit incorporates eight power semiconductor switches like MOSFET, IGBT, etc., four capacitors and two dc voltage sources. Fig.2 shows the circuit diagram of proposed nine level MLI. The generalized expression to determine the output voltage level is given below.

$$N_c = 2 * N_s \quad (1)$$

$$N_{switch} = N_c + 4 \quad (2)$$

$$N_d = N_c \quad (3)$$

$$N_{step} = 2*N_c + 1 \quad (4)$$

Where

N_s	-	Number of dc voltage sources
N_{switch}	-	Number of switches
N_c	-	Number of capacitor
N_{step}	-	Number of output voltage levels
N_d	-	Number of diodes

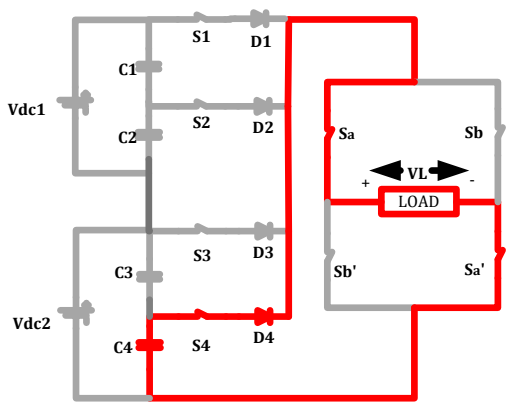


Fig.3. (a) Mode 1 = $+V_{dc}/2$

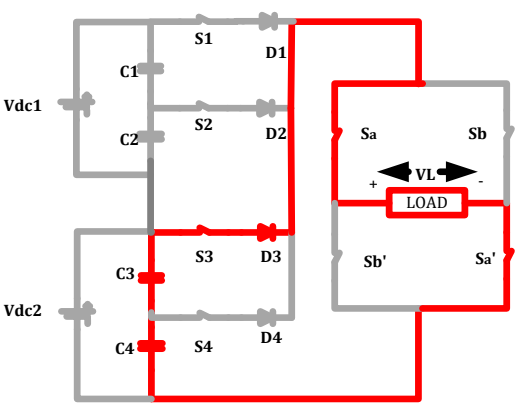


Fig.3. (b) Mode 2 = $+V_{dc}$

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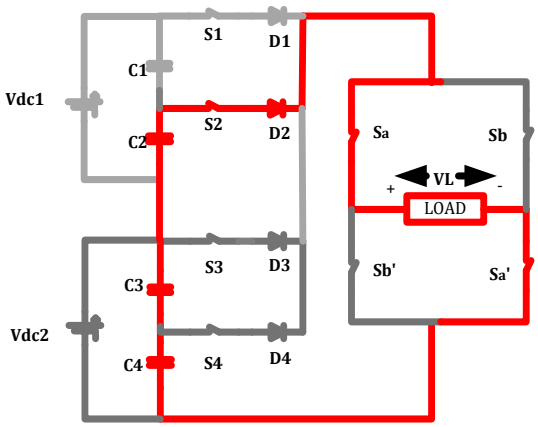


Fig.3. (c) Mode 3 = $+3V_{dc}/2$

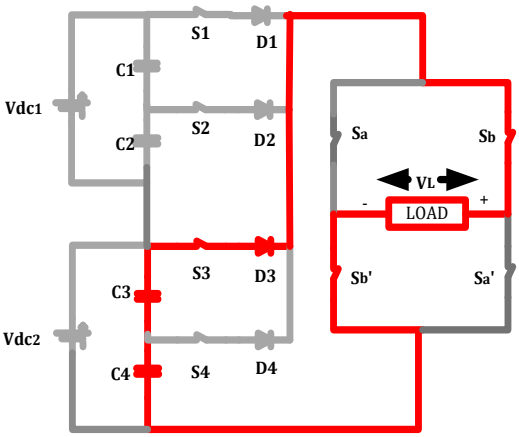


Fig.3. (f) Mode 6 = $-V_{dc}$

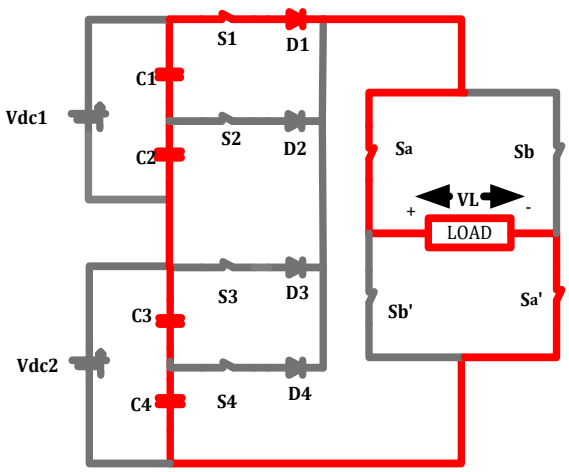


Fig.3. (d) Mode 4 = $+2V_{dc}$

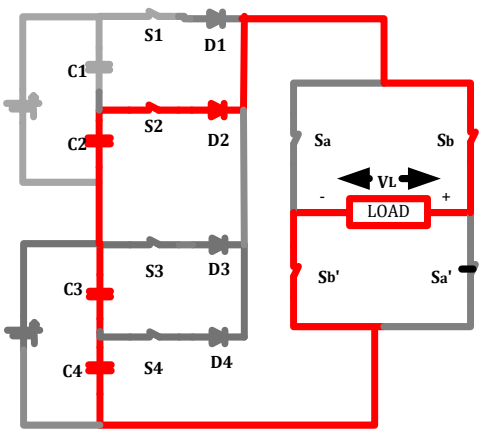


Fig.3. (g) Mode 7 = $-3V_{dc}/2$

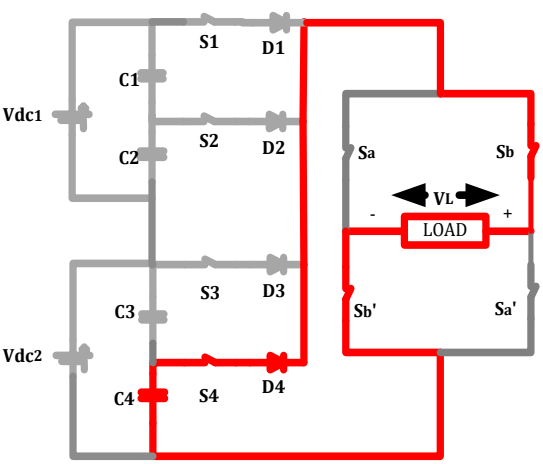


Fig.3. (e) Mode 5 = $-V_{dc}/2$

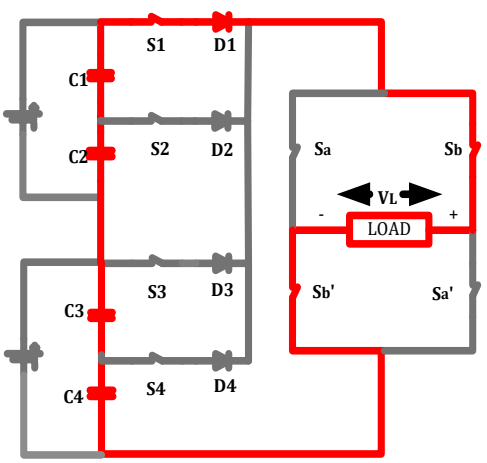


Fig. 3. (h) Mode 8 = $+2V_{dc}$

Fig.3 Mode of operation for different output voltage level of proposed nine level MLI

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Fig.3 (a-h) shows the operational diagram of proposed nine level inverter for different output voltage levels. In Mode1&5, the capacitor C_4 voltage $V_{dc}/2$ connected to H-Bridge through S_4 and D_4. The voltage V_{dc} connected to H-bridge through S_3 and D_3 in Mode 2&6. In Mode 3&7, the voltage $3V_{dc}/2$ connected to H-bridge through S_2 and D_2. In the Mode 4&8, the $2V_{dc}$ voltage connected to H-bridge through S_1 and D_1. During positive half cycle, the output voltage connected to the load through switches S_a and S_a'. During negative half cycle, the output voltage connected to the load through switches S_b and S_b'. Table I illustrates the summarized output voltage level of the proposed nine level inverter.

Table I

OUTPUT VOLTAGE LEVEL OF PROPOSED NINE LEVEL INVERTER

Mode	**S_1**	**S_2**	**S_3**	**S_4**	**S_a**	**S_a'**	**S_b**	**S_b'**	**Output voltage (V_L)**
1	0	0	0	1	1	1	0	0	$+V_{dc}/2$
2	0	0	1	0	1	1	0	0	$+V_{dc}$
3	0	1	1	0	1	1	0	0	$+3V_{dc}/2$
4	1	0	1	0	1	1	0	0	$+2V_{dc}$
5	0	0	0	0	0	0	1	1	$-V_{dc}/2$
6	0	0	0	0	0	0	1	1	$-V_{dc}$
7	0	0	0	0	0	0	1	1	$-3V_{dc}/2$
8	0	0	0	0	0	0	1	1	$-2V_{dc}$

0 = OFF State, 1 = ON State

The proposed nine level inverter is developed in MATLAB®Simulink. The simulink realization of proposed nine level inverter output is shown in Fig.4. Total Harmonic Distortion (THD) is found to be 26.32% in the output voltage is shown in Fig.5.

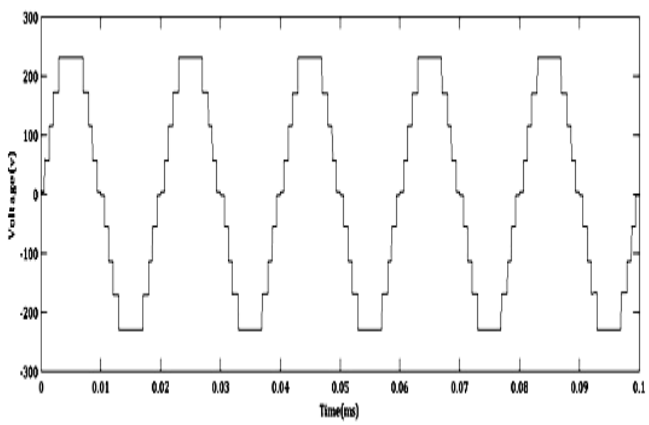


Fig.4 Nine level MLI output voltage waveform

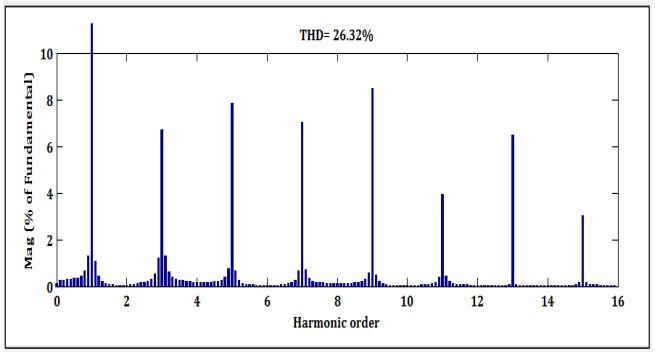


Fig.5 THD of proposed nine level MLI with harmonics

III. COMPARATIVE STUDY OF MULTI-LEVEL INVERTERS

The suggested MLI topology is compared with few existing topologies in terms of switches and DC sources as a function of voltage levels are analyzed to explore its supremacy and plotted in Fig. 6. The proposed MLI utilizes minimum number of DC sources and switches compared with customary topologies.

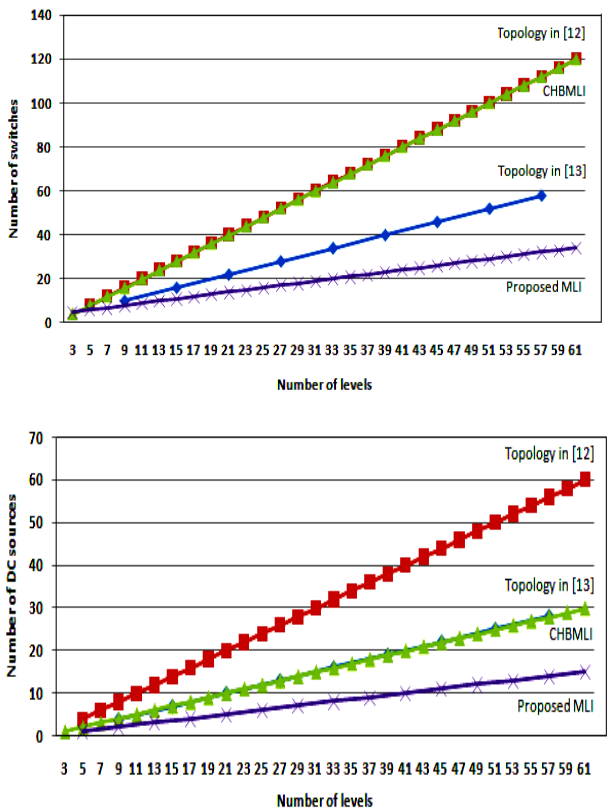


Fig.6 Comparative plot of proposed topology with conventional topology in terms of number of switches and DC sources as a function of the number of voltage levels

The performance comparison of proposed MLI in terms of number of output voltage levels, switches and DC sources

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as a function of the number of sub modules are tabularized in Table II

TABLE II

COMPARISON OF PROPOSED MLI WITH EXISTING TOPOLOGIES

	Topology in [12]	Topology in [13]	CHBMLI	Proposed MLI
Levels	2q+3	6q+3	2q+1	4q+1
Switches	4q+4	6q+4	4q	2q
DC sources	2q+2	3q+1	q	q

Where q = No. of sub modules (or H-bridges for CHBMLI) for each phase

IV. SELECTIVE HARMONIC ELIMINATION

Mitigation of harmonics exist in the output voltage waveform of MLI is attained by various PWM techniques. Staircase modulation, optimal-combination modulation, space vector control and selective harmonic elimination are low switching frequency schemes [17,8]. High switching frequency techniques are sinusoidal PWM and space vector PWM results in frequent switching in one period of the fundamental voltage. Currently, SHE-PWM technique has obtained an immense consideration because of their benefits over other modulation strategies. Hence it results in adequate execution with direct control over the output waveform harmonics, lower switching losses, low cost, lower EMIs, higher conversion efficiency and the capability to cancel triplen harmonics in three phase systems [18].

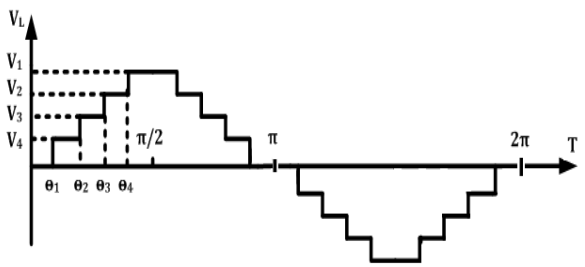


Fig.7 Switching angles θ1, θ2, θ3, and θ4 for nine level MLI.

A nine level inverter output waveform is shown in Fig.7. It has four switching angles $\theta_1, \theta_2, \theta_3, \theta_4$ .On considering the waveform characteristics, the generalized stepped voltage waveform in fourier series expansion is as follows [19, 20].

$$V_{(\omega t)} \sum_{i=1}^{\infty} \frac{4V_{dc}}{i\pi} \left((\cos i\theta_1) + (\cos i\theta_2) + \cdots (\cos i\theta_n)\right).\sin(i\omega t) \quad (5)$$

The switching angles $\theta_1 - \theta_n$ should satisfy the following prerequisite:

$$0 \leq \theta_1 < \theta_2 < \theta_3 < \theta_4 \leq \theta_n \leq \frac{\pi}{2} \quad (6)$$

In the inverter output, the number of harmonics to be eliminated is $2N_s$-1.The harmonics of order up to $6N_s$-2 when K is odd, and up to $6N_s$-1, when K is even must be eliminated from the output waveform where K is the order of harmonics. Therefore with a nine level inverter having two DC sources, the 5th, 7th, and 11th harmonics must be eliminated and the transcendental equations to be satisfied are as follows.

$$(\cos\theta_1 + \cos\theta_2 + \cos\theta_3 + \cos\theta_4)/4 = \text{MI}$$

$$V_5 = \frac{4V_{dc}}{5\pi}[(\cos 5\theta_1 + \cos 5\theta_2 + \cos 5\theta_3 + \cos 5\theta_4)] = 0$$

$$V_7 = \frac{4V_{dc}}{7\pi}[(\cos 7\theta_1 + \cos 7\theta_2 + \cos 7\theta_3 + \cos 7\theta_4)] = 0$$

$$V_{11} = \frac{4V_{dc}}{11\pi}[(\cos 11\theta_1 + \cos 11\theta_2 + \cos 11\theta_3 + \cos 11\theta_4)] = 0 \quad (7)$$

To obtain the optimum switching angles, the modulation index (MI) is defined to be a representative of voltage V_1 as

$$\text{MI} = \frac{V_1}{16\frac{V_{dc}}{\pi}} ; 0 \leq \text{MI} \leq 1 \quad (8)$$

To solve the non linear transcendental equations, the following optimization techniques such as Particle Swarm Optimization (PSO), Bee Colony Optimization (BCO) and Ant Colony Optimization (ACO) are taken into consideration for the proposed nine level MLI and differentiated. This part briefly clarifies about different optimization techniques to solve SHE equations.

The significant step of any optimization technique is to coin the fitness function. The fitness function relates the variables to be evaluated. The main objectives are,

a) to get the magnitude of the fundamental voltage equal to any desired or preset value and

b) to eliminate or at least to minimize few lower order harmonics.

The magnitude of fundamental and harmonics are dependent on the switching angles. The Fitness Function (FF) to achieve the above objectives takes the form as

$$FF=100 * \frac{(V_{1d}-V_1)^4}{(V_{1d})^4} + \left(\frac{50}{V_1}\right)^2 * \left\{\frac{(V_5)^2}{5} + \frac{(V_7)^2}{7} + \frac{(V_{11})^2}{11}\right\} \quad (9)$$

A. Particle Swarm Optimization (PSO)

PSO is well adapted to solve complex problems with less computational effort and simple computer coding. PSO does not require any initial values like other conventional iterative methods [21,22]. Steps entailed in PSO are as follows.

Step 1: Initialize populace.

Step 2: Compute fitness values of particles.

Step 3: Reform the particle fitness values from best to least.

Step 4: Choose genus seed.

Step 5: Allocate every genus seed acknowledged as the lbest to all individuals recognized in the same genus

Step 6: Reinstate excess particles in genus.

Step 7: Update position of particles according to (6) and (8).

Step 8: Until prerequisites met.

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This algorithm is implemented and executed in MATLAB® platform. The THD in the output voltage of the proposed inverter for 0.8 MI is found to be 12.44% is shown in Fig.8.

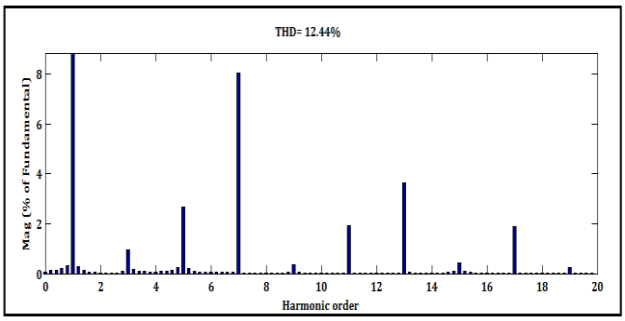


Fig.8 THD of proposed nine level MLI using PSO technique

B. Bee Colony Optimization

Bee Colony Optimization (BCO) is nature inspired technique, which imitates maturing activities of bees. It is a stochastic method can implement easily, has less control variables, and could modify easily and hybridized with other complex algorithms. Moreover, BCO has been customized successfully; to solve a vast range of discrete and continuous optimization problems. Some different works have altered and hybridized BCO to different algorithms, to additionally upgrade the structure of its system [23].

Step 1: Initialization to generate food sources

Step 2: Estimate fitness of food sources and enhance the food source.

Step 3: choose preeminent food sources and enhance the food sources

Step 4: Pursuit for new food sources

Step 5: Memorize the elite food source

Step 6: Replicate step (2) to (5) until requisites met.

This algorithm is implemented and executed in MATLAB® platform. The THD is found to be 10.27% in the output voltage of the proposed inverter for 0.8 MI is shown in Fig.9.

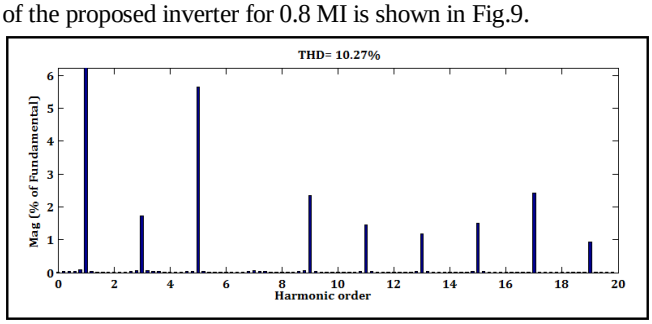


Fig.9 THD of proposed nine level MLI using BCO technique

C. Ant Colony Optimization

Ant colony optimization (ACO) is the foremost one which explores an optimal path in a graph based on the activities of ants searching a pathway among their colony and food resource [24,25].

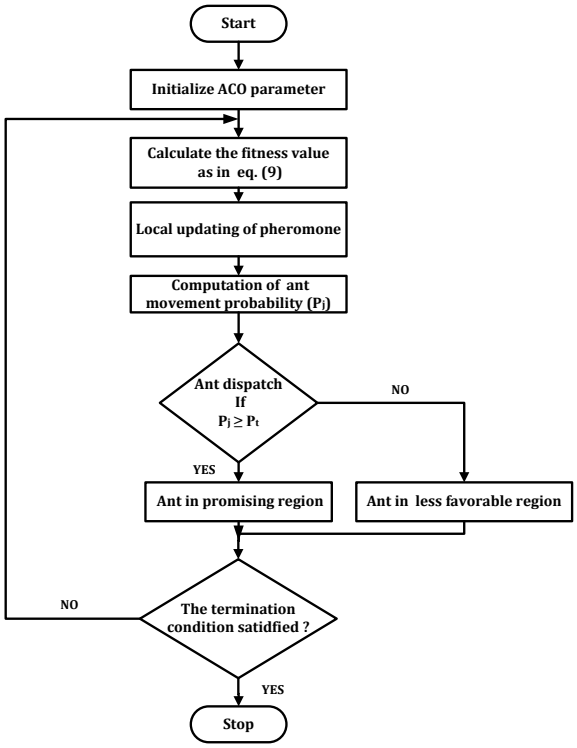


Fig.10 Flowchart for Ant colony optimization (ACO)

This flowchart in fig.10 is implemented and executed in MATLAB® platform. The THD in the output voltage of the proposed inverter for 0.8 MI is found to be 4.00% is shown in Fig.11.

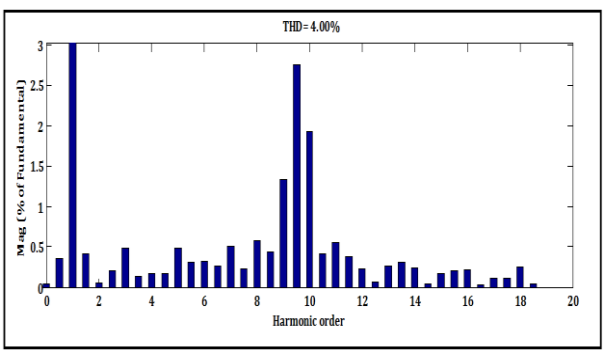


Fig.11 THD of proposed nine level MLI using ACO technique

Table III
THD comparison of proposed nine level MLI with different Optimization techniques for 0.8 MI

Methods	Modulation Index (MI)	Optimum Switching Angles obtained from algorithm (degrees)				THD (%)
		θ_1	θ_2	θ_3	θ_4	
PSO	0.8	9.83	20.32	38.32	60.21	12.44
BCO		9.65	20.41	38.48	60.15	10.27
ACO		9.71	20.44	38.51	60.51	4.00

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Table III shows the THD comparison of proposed nine level MLI obtained from different optimization techniques such as PSO, BCO and ACO respectively. On comparing, it is found that ACO yields best solution in every independent trial with fewer tuned parameters. Though the other methods gives solution, the consistency of the solution is found to be elite with ACO. Thus Ant Colony Optimization is suggested for Selective Harmonic Elimination in real time applications.

V. PRACTICAL IMPLEMENTATION

The framework of proposed nine level MLI is developed. Fig. 12 shows the consummate hardware setup. The H-bridge part and level developer part of the MLI consisting of 8 switches (IRF840N MOSFET). Gate pulses to the MOSFET Switches are engendered by means IC AT89C51 microcontroller and pulses are boosted through driver circuits. The pulses from driver circuits are given to gate terminals of MOSFET switches. Fig.13 shows the output load voltage waveform for R Load (100Ω). Ant colony optimization technique is applied for computing optimum switching angles to remove 5^{th} and 7^{th} order harmonics. Fig. 14 shows the THD in the output voltage of framework and is found to be 5.97%. The simulation and experimental results shows that the proposed nine level Multilevel Inverter design has validity and feasibility.

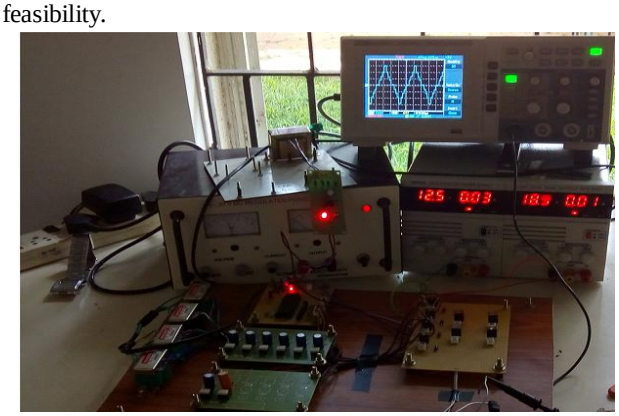


Fig.12 Framework of nine level MLI

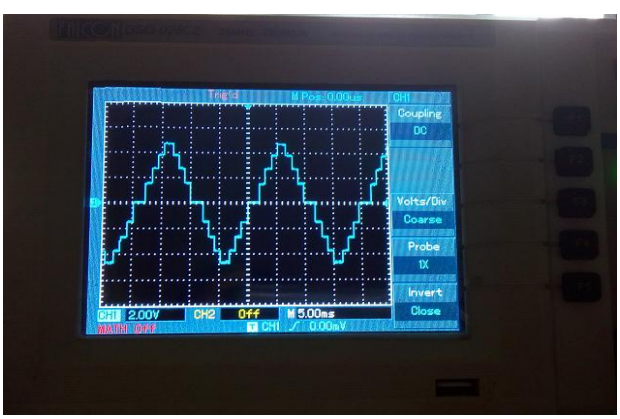


Fig. 13 Nine level output voltage of MLI



Fig.14 THD of nine level MLI from Power Quality Analyzer

VI. CONCLUSION

In this paper, a novel configuration Multilevel inverter is proposed and a nine level MLI is designed and simulated using MATLAB® Simulink from the generalized model which requires minimal switch counts and dc voltage sources contrasted with customary model. Furthermore, a comparative study on various algorithms such as PSO, BCO and ACO has been carried out for the proposed nine level inverter and it accomplishes less THD by adopting Ant Colony Optimization technique. The obtained output voltage is approximately, a sinusoidal wave.

THD analysis made on the inverter output voltage shows that THD is 4.00% from MATLAB® Simulink and 5.97% from framework. Therefore, the proposed inverter is compatible for various single phase applications.

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