Hardware design of low power non-binary LDPC coder based on FPGA for WIMAX standard over GF(2^m)

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Abstract

Worldwide interoperability for microwave access (WiMAX) is a family of IEEE 802.16 standard, which promise to provide high data rate over network with high density users. In digital communication, coding frameworks is an exhaustively used term all around recommending the screw up review code. The upside of error correction is a back-channel and the retransmission of data can routinely be kept up a vital segment from, at the cost of higher transmission limit necessities everything considered. Channel coding is the critical endeavors to envision and switch the transmission spoils of remote structures, must have a not too appalling execution with a particular extraordinary focus to keep up high data rates. In this paper, a low power non-binary low density parity check (LPNB-LDPC) coder over GF(2^m) is proposed for WiMAX standard. In general, LDPC coder is consist of two units such as check node unit (CNU) and variable node unit (VNU). The hardware realization of CNU is a perplexing portion as it entails of complex modules such as fast Fourier transform/inverse fast Fourier transform (FFT/IFFT) and multiplier. We astounded those problem by modified CNU structure, in which, flexible FFT/IFFT and multiplier used to replace FFT/IFFT and multiplier. The flexible design reduces the reconfigurable design and their time. The proposed LPNB-LDPC coder is implemented on Xilinx tool with different FPGA families and objective to enhance the hardware features are hardware utilization, power consumption and maximum operating frequency.

Keyword: WiMAX, channel coding, check node unit, variable node unit, hardware design, flexible FFT/IFFT, flexible multiplier

1. Introduction

In current data based society, rediscovered LDPC codes have gotten a goliath measure of examinations and have been considered as front line foul up helping code for media transmission [1], broadcasting, spilling [2] and storage systems [3]. LDPC codes are a kind of square code that fulfills both long length and trademark. It is their astonishing execution joined with their low translating flexible quality that has seen LDPC codes fit into benchmarks for information transmission, for example, WIMAX (IEEE 802.16e) [4], influenced Video broadcasting (DVBS2) [5], Wireless LAN (IEEE 802.n) [6], and entire approach change (3G-LTE). The impacting decoder get ready use is no doubt in the world a champion among the tensest issues picking the level of LDPC applications in this present reality. The most appreciated response for the decoder gathering structure is to unequivocally instantiate the conviction spread (BP) profiting in any case much as could sensibly be standard from a depiction of [7] to equip: each zone center point and check center are physically dispatched their own particular processors and every last one of the processors is identified with an interconnection system reflecting the Tanner plot

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make. The absolutely parallel LDPC code [8] related from BP ousting up figuring by benefitting from parallel structure. A 1024 piece LDPC code accomplishes a greatest picture throughput of 1Gbps saw in ASIC change.

The non-fortified semi cycle LDPC decoder building (QC-LDPC) [9] used to accomplish high structure motivation driving storage and low contraption versatile quality. The variable node unit (VNU) controlled by neighborhood switch structures with Class-I and Class-II make codes. In non-joined LDPC (NB-LDPC) [10], CNU setup in setting of the way push plot, which keeps just a few most time attempted factor to-check respects for the way change, and diminished figuring multifaceted nature of building managing and way change. A period pulling back LDPC convolution code (LDPC-CC) decoder chip [11] joins the number level, focus level, and bit level risings to complete higher throughput with astounding contraption cost and power. The number level change is the on-request figure focus point begins booking with covering channel respects, which can't just whole twice speedier unwinding up affiliation together speed than log-conviction duplication (log-BP) check. A vivified iterative hard chose quality based larger part strategy for hypothesis releasing up (IHRB-MLGD) [12] estimation with the likelihood data amassed from the channel. By then it encounters the message introduction of the IHRB estimation and paying little notice to the duty of the same CNU from the VNU message the IHRB figuring stimulate the execution opening between the hard and unstable checks with immaterial adaptable quality overhead.

Another QC-LDPC [13] code accomplishes high hardware utility efficiency (HUE) and sees hitting memory square diminishment with no execution debasement. In spite of two part the select interface with a couple a zone squares, by then it performs to restored message passing figuring's sensibly weaken by square. Dumbfounding position central LDPC decoder in setting of a lessened flexible quality Min-Sum check reduced inter connect multifaceted nature by compelling the outward message length to 2 bits and streamlined the CNU [14]. The high throughput evacuating up of high-rate LDPC codes adjusted by the cut message passing (SMP) removing up plot [15] which covers the CNU and VNU and accomplished a respectable tradeoff among space and throughput, in like way, high contraption use sensibility. An examination table (LUT) based VNU setup have the best reaction for flooding contraption structure and it related for (2048, 1723) LDPC code of the IEEE 802.3an standard [16]. The arrangement has keep up unmitigated parallel course with parallel controlling sub-parts in a FPGA contraption. An inventive piece serial CNU has wound up being set up for confined letters all together iterative decoders (FAIDs) and a little zone VNU [17] utilized for beating symmetry in the Boolean maps. Correspondingly, a re-designed information building structure used to distress the apparatus past what various would consider possible.

A (2048, 1723) LDPC decoder [18] have found in 90 nm CMOS process and it contains probabilistic min-aggregate and second most unnoticeable respect mean low-thickness and completely parallel LDPC plot. The CNU are related through an interconnect make in setting out of a blend of tree and butterfly structures with an entire spotlight on that the arranging and message going between the VNUs. Another totally parallel NB-LDPC decoder over have found in 28-nm CMOS advance [19]. The trellis based CNU setup help past what different would consider possible by lessened the creature measure of memory having works out. The log likelihood ratio (LLR) vector of a selection variable message has approximated utilizing a piecewise straight most remote point. The primary and secondary stray pieces have picked by adjusted CNU [20] to the degree right and freeway. Here, one-hot diagram of the size respect reduces the comparators tree to an OR tree. The two stray pieces got by a bitwise OR change between the layout of the information messages and by utilizing a changed leading zero counter (LZC).

Contributions. For further enhancement, a low power non-binary low density parity check (LPNB-LDPC) coder is proposed for future communication system. The objective of proposed LPNB-LDPC coder is to hardware architecture without reconfigurable design up to galois field GF (2^m). The proposed LPNB-LDPC coder satisfies the long-term problem as hardware efficient low power high performance design.

This paper is structured as follows. The recent works related to our contributions are surveyed in Section 2. The problem definition and system model are present in Section 3 and VLSI structure of proposed flexible LDPC codes is described in Section 4. Experimental result and performance comparison of proposed and existing LDPC codes are illustrated in Section 5. Finally, conclusion is set in Section 6.

2. Related works

Condo et al. [21] have proposed a power lessening structure for versatile channel decoder, which reduces messages exchanged among PEs. The decoder's hitter the probabilistic nature and the control system offers traded messages in the iterative unraveling and methodology novel criticalness and free for all estimations. Zone overhead and power get have

gotten by the cutting edge to audit the ampleness of the approach. The LDPC decoder executed using 90-nm CMOS process and it eats up a zone of 3.11 mm2, most key clock repeat of 200MHz, and power utilization of 99.2mW.

Yoon et al. [22] have shown an efficient memory address remapping method for a high-throughput quasi-cyclic LDPC (QC-LDPC) DECODER. A hiding thought showed up in CNU and VNU of the parallel errands are kept by the exhibited memory exchange speed. The memory affiliation together approach of LDPC decoder with the memory address conflicts and riches memory-read attempts used for lessening memory addresses remapping. The considered parallel stochastic LDPC-BC decoder saw using 130-nm CMOS process and it eats up a space of 1.79 mm2, most evident clock repeat of 100MHz, and power usage of 104mW.

Roberts et al. [23] have proposed a power and zone model based multi-rate, QUASI-CYCLIC LDPC coder. Past what evident would consider possible decoder depends upon a streamlined versatile controlled min-instigate check. The rightness of channel oversights is respectably low standard to overpower degree. To diminish the obliged word length impacts, a six-piece non-uniform quantization with the moored message passing structure for instinct have used and an early end plot used to diminish the entire quantity of unwinding cycles. The Quasi-cyclic LDPC coder setup executed in a Xilinx FPGA with the Virtex5 contraption and it cripples the region considers 416.2K, biggest clock supplement as 474MHz, and power utilization of 114.3mW.

Lin et al. [24] have proposed a modified quasi-cyclic LDPC code (CB-LDPC), which used as to some degree a remote correspondence structure for data exactness change process. The CB-LDPC Matrix H uses the min-decide mean iterative evacuating up plans. The properties of low thickness and selective desire for apparatus structure and low multifaceted nature of encoding of CB-LDPC begin central gear use and affected bungle clearing up by a circuit to structure. The LDPC decoder finished the way toward using 180-nm CMOS process and it eats up a space of 15.75 mm2, most jumbling clock repeat of 100MHz, and power usage of 800mW.

Boncalo et al. [25] have focused on reducing the memory necessities of the self-corrected min-sum (SCMS) concerning min-speak to. The SCMS-V1 utilized for an illuminating for storage the message exchanges obligation as for of CNU. The SCMS-V2 in the setting of broken self-change control and permits the diminishment of the beating bits. The SCMS-V2 gives the no sullying in the bobble cure keep concerning the standard SCMS, while it has breathing space around 0.5 dB better execution. This coder completed in a Xilinx FPGA with the Virtex7 contraption and the SCMS-V1 eats up LUT and FF direct think about 60K, biggest clock go over as 300MHz, and SCMS-V2 channels LUT and FF join think about 51K, most finished the best clock go over as 300MHz.

Lee et al. [26] have proposed a zone indispensable free half-stochastic extricating up working for NB-LDPC codes. A bound together tracking forecast memory (TFM) with covering channel values (CTFM-CC) figuring used to lessen the assignments and keep up BER execution. A truncated TFM building and what's more its restoring standard used to complete hack down multifaceted nature of VNUs. The half-stochastic loosening up making delight preoccupation game plans for LDPC-BC decoder over viewed using 90-nm CMOS process and eats up segment check of 1077K, and most clear clock repeat of 333MHz.

Chandrasetty et al. [27] have shown a memory affecting decoder directing using 3-Level hierarchical quasi-cyclic (HQC) oversee drive strategy with layered permutation (LP). The 3-Levels of part structure in the cross zone give versatility in watching decoders of diverse code lengths and code rates. The decoder can in like way be really proposed for applications, for instance, WiMAX, WLAN, and DVB-S2. The memory favorable decoder structure found in a Xilinx FPGA with a Virtex4 contraption for WiMAX application and eats up the measure of cuts is 16803, changing cut LUT are 31305, the measure of cut registers are 4066, the best clock repeat of 400MHz, and power utilization of 1638mW.

Lee et al. [28] have proposed a centrality and mechanical party gainful altogether parallel stochastic LDPC-BC decoder chip for IEEE 802.15.3c applications. A reconfigurable CNU with cover issue checking and a reconfigurable VNU with the reduced complexity architecture of tracking forecast memory (RCA-TFM) have used to help four code rates. The reduced consider structure of taking after memory likely investigated to execute the VNU. The altogether parallel stochastic LDPC-BC decoder got done with using 90-nm CMOS process and uses parcel check of 760.3K, the best clock repeat of 768MHz, and power use of 437.2mW.

Ajaz et al. [29] have shown a multi-Gbps multi-mode LDPC decoder working for gigabit remote trades. An affecting dynamic and settled part-moving structure used for multi-mode plots. A low-versatile quality including change used to execute the dynamic and

settled part moving structure. A fundamental quantization structure and the utilization of one's supplement plot rather than a two's supplement collect confined to fulfill high throughput with superfluous range overhead. The multi-mode LDPC decoder setup executed using 65-nm CMOS process and eats up area check of 320K, the most huge clock repeat of 400MHz, and power usage of 284.3mW.

Sułek et al. [30] have proposed a NB-LDPC coder using the mixed space FFT-BP disentangling check with the change units and it in like course named as semi-parallel decoder. Coder favors mapping a dash of the patterned to the multiplier emphases embedded in a FPGA, in like way creating consumption of the extensive number of kinds of FPGA resources. The throughput wrapped up by a specific FPGA by the decoder in light of current conditions made. In NB-LDPC coder, the CNU square reestablished by an approximated examination of the nonlinear most far away fulfills that pulls in veritable resources saving and originator shifter request of move units changing the message vectors.

Lin et al. [31] have proposed decoder working for semi cyclic NB-LDPC codes with protracted min-sum (EMS) figuring. The decoder reestablishes throughput by twofold throughput key CNU, which joins two blends inside one clock cycle, in like way, moored get ready for both CNU and VNU, called ECU. By then streamline VNU and choice unit to lessen the multifaceted nature and memory use. The NB-LDPC decoder executed using 90-nm CMOS process and it cripples a portion check of 564K, the best clock repeat of 277MHz, and power usage of 274mW.

Thi et al. [32] have demonstrated a forward backward four-way merger min-max figuring and high-throughput decoder plot for NB-LDPC decoder. The general parallel square layered decoder building sensible for the proposed forward backward four-way merger figuring used to restore the decoder joining. A parallel switch strategy building and parallel-serial check center point unit is in like course proposed to help the execution of the proposed decoder plot. This figuring decreases the measure of check grow coordinate masterminding turns with reverence toward a fabulously key level and the decoder outlining out using the proposed count can achieve an amazingly higher throughput.

3. Problem methodology and system model

3.1 Problem methodology

Hailes et al. [33] have demonstrated the structure and utilization of a FPGA-based LDPC decoder having the run-time flexibility to switch between an arrangement of QC PCMs inside a solitary clock cycle. They other than proposed robotized course of action stream, which gives the building the association time adaptability to help any methodology of QC PCMs. This strategy stream thusly makes the HDL portrayal of the decoder, which might be continued with onto a FPGA. The execution happens shows that this outline accomplished an odd condition undeniably of movement time and run-time adaptability, while keeping up sensible execution to the degree arranging throughput, planning lethargy, botch up restore most remarkable, and apparatus asset use. The settled WiMAX depends staying in a perilous circumstance of sight condition in the rehash level of 10– 66 GHz, while the adaptable WiMAX depends on the non discernable pathway condition that works in 2-11 GHz include go, an association between's settled WiMAX and positive WiMAX can be found in [5]. The WiMAX delineated two layers; Physical layer and Medium Access Control (MAC) layer. The corporal layer established on performing coding, interleaving, modulation and orthogonal frequency division multiplexing (OFDM). MAC layer portrays the Internet custom and the odd exchange mode change and it changes over the change into the MAC information units. QC-LDPC coder is not a fully parallel structure and it ingests additional hardware consumption than prevailing LDPC coders conversed in associated workings.

Moreover, the multiplier is as main part of CNU block in LDPC coder, but authors utilize the simple multiplier for this design. Then authors implement two different GF orders with reconfigure hardware structure and it not support without reconfigure configuration.

To overcome those problems, we introduce a low power non-binary LDPC (LPNB-LDPC) coder over GF(2^m) using simple hardware architecture. Generally, an LDPC coder comprises of two units such as check node unit (CNU) and variable node unit (VNU). The hardware realization of CNU is a challenging part because it it comprises of huge segments such as FFT/IFFT and multiplier. We overcome those problem by modified CNU structure, in which, flexible FFT/IFFT and flexible multiplier used to replace FFT/IFFT and multiplier respectively in existing QC-LDPC coder [33]. The main contributions of proposed LPNB-LDPC coder summarized as follows:

1. In LPNB-LDPC coder, the complex hardware part of CNU module is reduced by area and power efficient flexible FFT/IFFT and bit serial multiplier over GF (2^m).

2. The LPNB-LDPC coder increases the reliability of the WiMAX system, which detect errors and corrected by the receiver.
3. For verification purpose, LPNB-LDPC coder is implemented over different field size without reconfigure the module. The flexible LPNB-LDPC coder is compared with the existing coders with different constraints is hardware utilization, power consumption and maximum operating frequency.

3.2 System model of LPNB-LDPC coder

The data communication over WiMAX network is revealed in Fig. 1. The transmitter forward data/information likes small packets to receiver end here encoding techniques applied. Our main contribution LDPC coder is present under this part only. The encoding stage has been trailed by the interleaving structure. Specific change procedures, as picked in WiMAX physical layer have been done. The IFFT has been performed in changing over the balanced information from the rehash a locale into the time space. At long last, the balanced information transmitted through the channels. At the beneficiary, the steamed conditions of transmission have been performed and in the last move, the got picture is changed by the achievement got and decoded packs gathering.

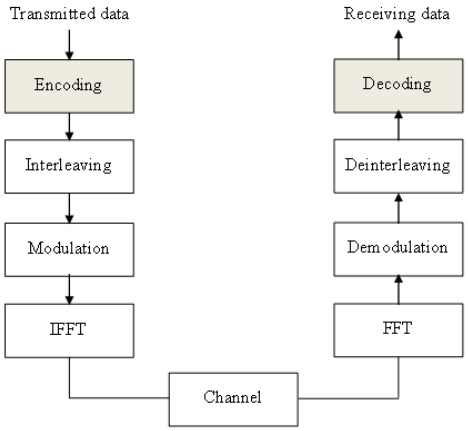


Fig. 1 Data communication model over WiMAX network

The LDPC code is a linear block code denoted by X×Y sparse parity check matrix (CM). The X signifies the number of parity checks and Y denotes the number of bits in the block. One will watch this interprets faultlessly from the hypothetical contemplated the correspondence check make. For the piece to fulfill the change check reasons that it is duplication by the matrix yields 0. It keys that reviewing an inducing goal to complete 0 in twofold enlisting the consequent possible result of the codeword and sections of the CM have a number of 1s, hence the expectedness check. The matrix defining the LDPC code has to be sparse, which implies a low density of 1s. The code rate (CR) of proposed LPNB-LDPC codes computed as follows:

$$CR = \frac{Y - X}{Y} \tag{1}$$

Let consider the Y=y and X=y-x, then we get as follows:

$$CR = \frac{y - (y - x)}{y} \tag{2}$$

$$CR = \frac{x}{y} \tag{3}$$

The code rate signifies the proportion of information bits in the block. The larger proportion of information bits can lead to greater throughput however the error-rate is higher due to lack of redundant bits. The factor Z pays exceptional character to a change factor and depicts the look at of the consistency check sub-cross zone ranges. The FNB-LDPC code parity-check matrix is defined as follows.

$$CM = \begin{bmatrix} P_{1,1} & P_{1,2} & \Lambda & P_{1,y} \\ P_{2,1} & P_{2,2} & \Lambda & P_{2,y} \\ \mathrm{M} & \mathrm{M} & & \mathrm{M} \\ P_{x,1} & P_{x,2} & \Lambda & P_{x,y} \end{bmatrix} \tag{4}$$

where each sub-structures $P_{x,y}$ of size $Z \times Z$ is both of a chart of circularly right-moved character systems or an each and every one of the zero cross zone. The coder check structures take after our present NB-LDPC coder [31]. The tanner graph chart is correspondence check structure where inside inspirations driving the system are portrayed as two units, for example, CNU and VNU. An edge interfaces a CN to a VN if and just if is non-zero. The releasing up highlight completes when either a decoded codeword fulfills all sensibility check conditions or the most enormous cycle number is come to. LPNB-LDPC codes starts with an initialization step with $y = 1, 2, \mathrm{K}, Y$ for every $a \in GF(2^m)$ as follows:

$$I_{xy}^{a} = F_{y}^{a} \tag{5}$$

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$$F_y^a = \log\left(m\left(Tx_n = a / Rx_n\right)\right);\quad n = 1,2,\mathrm{K}\ ,N \tag{6}$$

where Tx represents the probability of originally transmitted vector $Tx = \left(tx_1, tx_2, \Lambda\ tx_N\right)$ and Rx represents the received vector $Rx = \left(rx_1, rx_2, \Lambda\ rx_N\right)$. The message vector from VNU_y to CNU_x will processing at the CNU module with $x = 1,2,\mathrm{K}\ ,X$ and $y \in y : CR_{xy} \neq 0$ for every $a \in GF\left(2^m\right)$ describe as follows:

$$CN_{xy}^a = \exp\left(I_{xy}^a\right) \tag{7}$$

$$\xi_{xy} = \alpha_{xy}\ FFT\left(\kappa_{xy}\ CN_{xy}\right) \tag{8}$$

$$\zeta_{xy} = \kappa_{xy}^{-1}\ IFFT\left(\prod_{i \in x : CN_{xy} \neq 0 / y} \xi_{xi}\right) \tag{9}$$

where κ_{xy} is the permutation matrix related through CM_{xy}; α_{xy} is the normalization factor; and $\prod$ is the term-by-term product of vector elements. Then the CNU module output and it is also message vectors from CNU_x to VNU_y represent as follows:

$$VN_{xy}^a = \log\left(\zeta_{xy}^a\right) \tag{10}$$

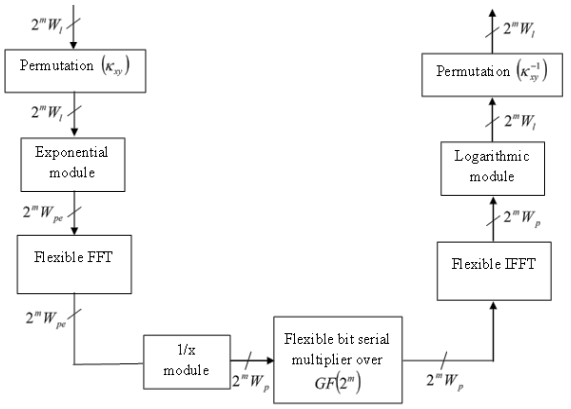


Fig. 2 Flexible CNU module

From the equations (7) to (10) of CNU module consist of different functional modules, in our paper we concentrate on this module and modify the architecture of CNU module to make area and power efficient one. The modified CNU module is presented in Fig. 2. Finally, VNU module process with $y = 1,2,\mathrm{K}\ ,Y$ and $x \in x : CR_{xy} \neq 0$ for $a \in GF\left(2^m\right)$ describes as follows:

$$I_{xy}^a = F_y^a + \sum_{i \in x : CN_{xy} \neq 0 / x} VN_{iy} \tag{11}$$

4. LPNB-LDPC coder with proposed CNU module

In this section, the detailed working function of modified CNU module with flexible FFT/IFFT and bit serial multiplier with proper sub modules.

4.1 Flexible FFT/IFFT module

The initial process in the proposed technique for noise degradation is the transformation of input signals in time domain to the frequency domain. Since speech and noise signals are real valued signals, the conventional FFT architecture for domain conversion can be replaced with modified low power pipelined architecture so as to make the complete hardware architecture efficient in relations of area and power consumption. The main difference between the FFT and IFFT is used here to design the FFT/IFFT processor and basic FFT equation given as follows:

$$X(\omega) = \sum_{\phi=0}^{M-1} x(\phi) W_M^{\phi_\omega};\quad \omega = 0,1,\mathrm{K}\ ,M-1 \tag{12}$$

where $W_M^{\phi_\omega}$ is twiddle factor,

$$W_M^{\phi_\omega} = e^{-j\left(2\pi / M\right)} \tag{13}$$

The same basic IFFT equations as follows:

$$x(\phi) = \frac{1}{M} \sum_{\omega=0}^{M-1} X(\omega) W_M^{-\phi\omega};\qquad \phi = 0,1,\mathrm{K}\ ,M-1 \tag{14}$$

Flexible FFT architecture consists of four stages of pipelining as presented in Fig. 3. The working process of each stage can be discussed as below.

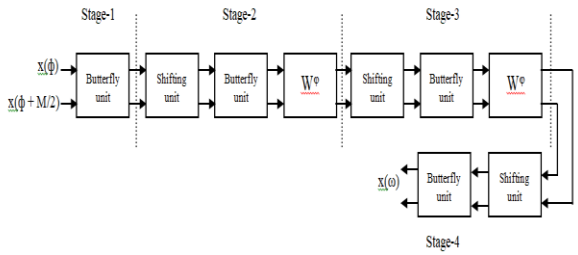


Fig. 3 Parallel pipelined architecture for 16 Point Radix 2 RFFT

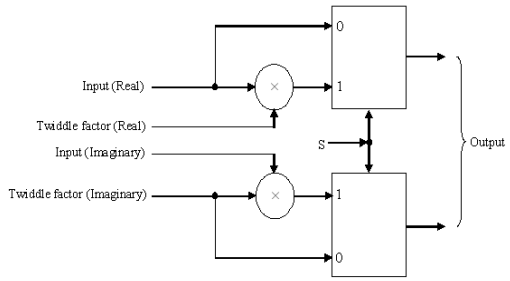


Fig. 4 Twiddle factor module

At stage 1, the butterfly unit will process the pair of real samples x(ϕ) and x(ϕ + M/2).The butterfly unit consists of 2:1 multiplexer with one selector line S. When the inputs are real, then the selector line S set to 1 and the butterfly starts to compute the input values. When the inputs are complex S set to 0, then the multiplexer just passes the input without computation. At phase 2, the architecture consists of shuffling unit, butterfly unit and twiddle factor block A. The shuffling unit is used to transform the order of the data that required from the stage 1 to stage 2, which also contains 2:1 multiplexer and two delay elements at input and output of the multiplexer. The twiddle factor $\left(W^{\phi}\right)$ module is shown in Fig. 4. Stage includes four twiddle factors as W^0, W^1, W^2, and W^3 with real and imaginary values as tabulated in Table 1.

From table 1 the value of W^0 is 1, so the selector line S set to 0 and the input passes to the output without any complex multiplication. For twiddle factors W^1 and W^3 the selector line set to 1 and allows the multiplexer for complex multiplication. To decrease the amount of additions and shifts canonical signed digit (CSD) is introduced. In CSD calculation, we have to convert the twiddle factor coefficients from binary to canonical signed digit. The first step of conversion of binary is check consecutive number of 1's in the binary sequence, replace the '0' before the first '1' in the sequence with '+' or '1', replace the last '1' in the sequence with '-'. For W^2 real and imaginary values are similar hence we can use our modified shift and add/subtract module only. At stage 3 shuffling unit 1 transforms the order of the data that required from stage to stage 3, then the shuffling unit 2 also shuffles the computed samples from the butterfly unit. In case of shuffling unit 2 the initial selector signal '0' last for 2l clock cycles and rest for the clock cycles it operates similar to the shuffling unit 1. In the twiddle factor block B, we use only the twiddle factor W^2 hence we can adopt the same as before in stage 2. At stage 4 the shuffling unit transforms the samples from the stage 3 to stage 4,then the butterfly unit computes the samples and we get the output sample x(ω).

Table 1 Twiddle factor real and imaginary coefficients for M=16

Twiddle factor (W^{ϕ})	Real values	Imaginary values
W^0	1	1
W^1	0.9239	0.3827
W^2	0.7071	0.7071
W^3	0.3827	0.9239

4.2 Flexible bit serial multiplier over $GF\left(2^m\right)$

Flexibility is an important property the hardware industry lacks and trying to establish as much as possible. To survive in this booming technological word, the new designs should be of an adjustable one, which processes the Flexible property. In this research, the problem for research we consider the conversion of a conventional MSB bit serial finite field multiplier $\boldsymbol{GF(2^m)}$ into a finite field multiplier with a maximum bit length $\boldsymbol{m}$ that can reconfigure itself for performing any finite field multiplication with bit length $\boldsymbol{l < m}$, where $\boldsymbol{l}$ is the bit length for the required multiplication.

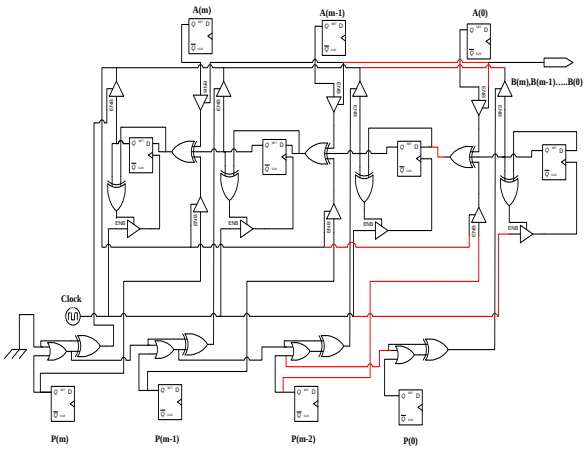


Fig. 5 Versatile bit-serial multiplier over $\boldsymbol{GF(2^m)}$

For clear interpretation of the work, we flinch through the the problem of transforming a conventional multiplier into a versatile multiplier earlier conferring the proposed versatile architecture. In this multiplier, for automatically reconfiguring the feedback based on irreducible polynomial value in the register control logic by adopting the basic gates. Moreover, an array of tri-state buffer is designed and a clock gating logic is designed for reducing the unnecessary transitions in the registers which are not included in the current multiplication operation. Here, AND gates array connected with the multiplicand register and the irreducible polynomial register for enabling the multiplier bits is replaced with suitable tri-state registers as revealed in Fig. 5. The efficiency in terms of area utilization while mapping the AND gate and tri-state buffer logic in the target device is shown in the Fig. 6 and 7 respectively.

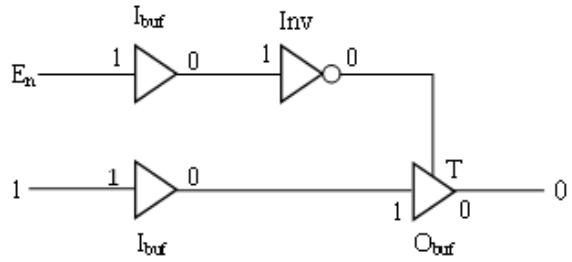


Fig. 6 Area efficient AND gate

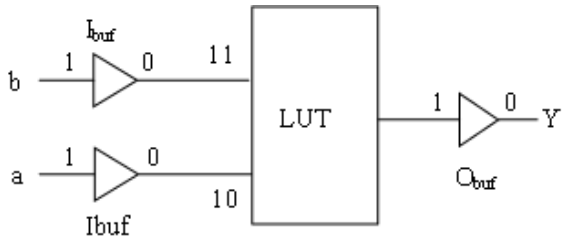


Fig. 7 Area efficient tri-state buffer

4.3 Non-linear function module

Starting at now picked, the control is performed after FFT figuring, in light of the way that the central FFT part is the total of all FFT inputs, which after inversion establishes the alliance factor. The affiliation module shapes the inversion of the key information vector part and diminished cross later scales every vector piece by change with the control factor. The change endeavors are joined with 3 pipeline picks also. Three particular nonlinear inspirations driving control are connected with the CNU module and affiliation module. For single clock cycle treatment of the message vector, the estimation of and should be performed for all vector parts then; as necessities be, parallel modules for taking in these explanations for containment are required. The parallel nonlinear most remote point modules use a particularly enormous bit of the decoder zone. In like way, it is pulling in attempt to lessen multifaceted course of action of these modules. The general tables-and-change sensibility known as bipartite table structure (BTM) used to format past what specific would consider possible $\exp(i)$, for $i<0$. The data operand of word-length is moved unavoidably into three zones i_0, i_1, i_2. The structure of exponential cutoff is showed up in Fig.8 and the most completed the best approximated as takes after:

$$f(i_a)=\exp(i)\approx \upsilon_0(i_0,i_1)+\upsilon_1(i_0,i_2) \qquad (15)$$

where the two areas υ_0 and υ_1 are made by the LUTs with inputs a couple of bits shorter than . Same way, we design the $\log(i)$, $1/i$ for $0<i\le 1$, and square system of made module is showed up in Fig. 9. The data of length W_p are disconnected into three zones passed on to two LUT of more unassuming than W_p input word-length and the unquestionable change can be passed on as:

$$f(i_b)=\begin{cases}\upsilon_2(i_3,i_4); & i_3>0\\ \upsilon_3(i_4,i_5); & i_3=0\end{cases} \qquad (16)$$

Unequivocally when the estimation of is low, $f(i_b)$ is approximated with LUT υ_2 taking all nonzero bits of i_b, from this time forward impacting definite to happen. Obviously, when the estimation of i_b is respectably far from zero, the centrality of subordinates is everything seen as little, enabling supposition with υ_3 LUT taking only a dash of most huge bits of i_b, especially i_3 and i_4 parts.

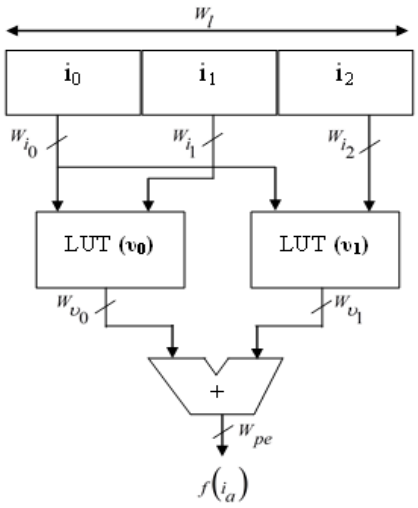


Fig. 8 Functional module of $\exp(i)$ function

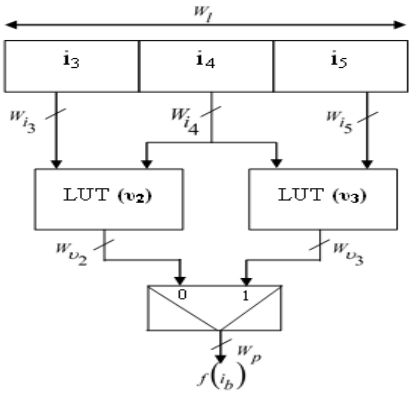


Fig. 9 Functional module of $\exp(i)$ and $\log(i)$ function

4.4 Other modules

The permutation module select the measure of different structures for coordinating and separating a a particular quantity of articles, without truly posting them. There are some focal checking frameworks which will be key for designing number of different structures for orchestrating or picking objects. The permutation module (κ_{xy}) of proposed LPNB-LDPC coder takes after the current LPNB-LDPC coder in $P_{h_{mn}}$ [31]. The VNU is made out of parallel subunits, where every subunit sees for a specific $a \in GF(2^m)$. For the n^{th} variable obsession point, VNU figures VN_{xy}^{a} for each $x \in CN_{xy} \neq 0/x$. At in any case, the entire of and each and every progressing toward quality is settled in the aggregator. By then information regards are subtracted from the entire to shape the prohibitive wholes over $x \in CN_{xy} \neq 0/x$.

The input select dynamic, which pulls unimportance of VNU degrees allowed to process. The whole VNU consists of 2^m subunits in order to calculate messages for every $a \in GF(2^m)$.

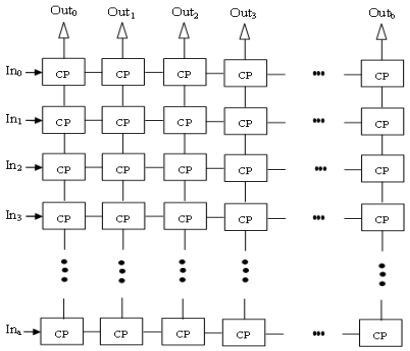


Fig. 10 Cross point module

Note that, for sharp LPNB-LDPC disentangling, it is boggling that the switch be "non-blocking," i.e. that a particular information can be urged to any obvious yield for the system of association with be made. The crossbar topology prompts the skillfully most clear non-blocking switch unit and used to interconnect unrivaled structures. In crossbar vertical game-plan partitions are related with level affiliations, while level memories are related with vertical affiliations. At each cross zone, a switch interfaces the join with control signals. In this framework, every processor can get to a free memory or resource self-choice of various processors. In like way, a couple of processors can have comprehension to the memory or resource by then. In case in excess of one processor tries to get in a general sense cloud memory or resources, the scheduler in the crossbar should perceive which one to interface with. The data stipends begin from the joined VC/SW allocator. The crossbar switch shape the yield port to which enters information is controlled. The cross fixations are controlled by the yield input just and is encouraged by Fig. 10. Each piece of the allow input inspects to one of the cross inspirations driving the crossbar. Each piece of the yield is impacted utilizing data sources and performs to structure for considering AND change with the give lines in the bit showing up particularly in association with the yield, and present OR undertaking toward the end.

5. Result and Discussion

The proposed LPNB-LDPC decoder is implemented on Xilinx tool with different FPGA families are Virtex4 (XC4VFX12), Virtex5 (XC5VLX20T) and Virtex7 (XC7VX330T) in this section. Xilinx is a software tool created by Xilinx for synthesis and analysis of HDL designs, , allowing the designer to

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synthesize their designs, execute timing analysis, inspect register transfer logic (RTL) diagrams, simulate a design's response to dissimilar stimuli, and configure the target device with the programmer. The XST tools in the Xilinx synthesize the designs and map to the target device. The inbuilt ISIM simulator is used for verification of process of the designed architecture. The simulation test is executed in a personal computer with windows7 operating system (OS) with 4GB ram and core i3 Intel processor. RTL schematic screenshot of LPNB-LDPC coder with Virtex4 implementation is revealed in Fig. 11. The device utilization summary screenshot of particular Virtex4 design is presented in Fig. 12. Similarly, advanced HDL synthesis screenshot is displayed in Fig. 13.

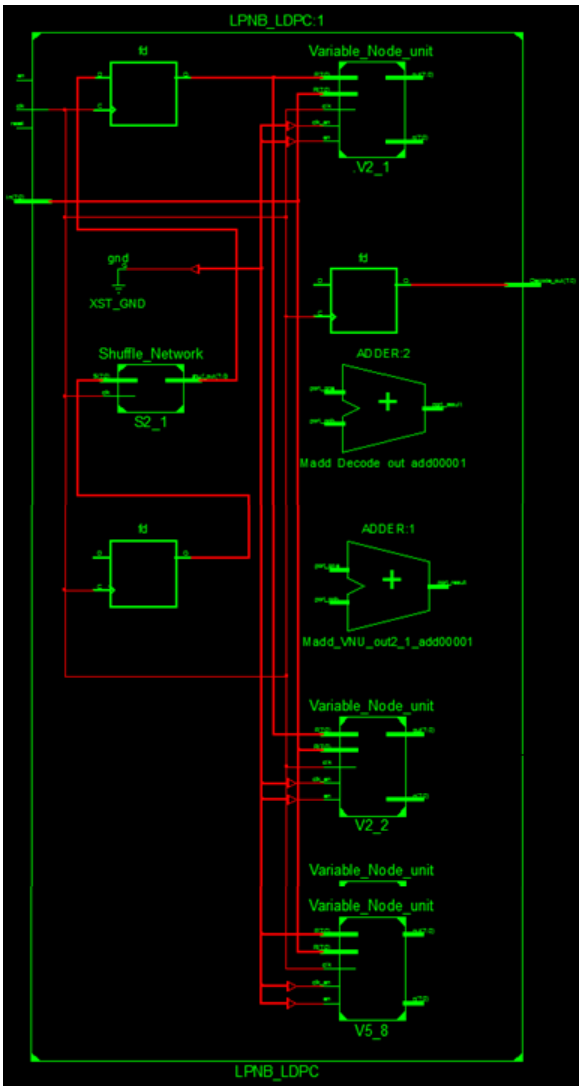


Fig. 11 Screenshot of LPNB-LDPC coder RTL

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Device utilization summary:
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Selected Device : XC4VFX12

 Number of Slices:                     2767  out of   5472    50%
 Number of Slice Flip Flops:           3090  out of  10944    28%
 Number of 4 input LUTs:               1553  out of  10944    14%
    Number used as logic:              1511
    Number used as Shift registers:      42
 Number of IOs:                         19
 Number of bonded IOBs:                 17  out of    240     7%
 Number of GCLKs:                        1  out of     32     3%
```

Fig. 12 Screenshot of LPNB-LDPC coder device utilization summary

```
Advanced HDL Synthesis Report

Macro Statistics
# ROMs                                  : 84
 4x8-bit ROM                            : 84
# Multipliers                           : 168
 8x8-bit registered multiplier          : 168
# Adders/Subtractors                    : 1737
 10-bit subtractor                      : 1008
 15-bit adder                           : 147
 8-bit adder                            : 76
 8-bit adder carry in                   : 2
 8-bit adder carry out                  : 504
# Registers                             : 29326
 Flip-Flops                             : 29326
# Comparators                           : 504
 8-bit comparator greater               : 504
# Xors                                  : 42
 1-bit xor8                             : 21
 1-bit xor9                             : 21
```

Fig. 13 Screenshot of LPNB-LDPC coder advanced HDL synthesis report

5.1 Hardware utilization comparison

The performance of proposed LPNB-LDPC coder is compared with the existing coders are LDPC [21], QC-LDPC [22][23][33], CB-LDPC [24], SCMS-LDPC [25], LDPC-BC [26][28], HQC-LDPC [27], MM-LDPC [29], NB-LDPC [30][31] and QC-NB-LDPC [32]. The performance metrics such as device utilization, power consumption and maximum operating frequencies are compared with existing coders. The hardware utilization comparison of proposed and existing coders is specified in Table 2. It shows the device utilization of proposed LPNB-LDPC coder is very less compared to existing coders. LDPC decoder [21] consumes 3.11 mm^2, QC-LDPC decoder [22][23] consumes an area of 1.79 mm^2, gate counts as 416.2K respectively. CB-LDPC coder [24] consumes an area of 15.75 mm^2, self-corrected min-sum (SCMS-V1) coder consumes LUT and FF pair count as 60K and SCMS-V2 consumes LUT and FF pair count as 51K [25]. LDPC-BC [26][28] decoder ingests gate count of 1077K and 760.3K respectively. HQC-LDPC decoder [27] the amount of slices FFsis 16803, a number of slice LUT are 31305, the amount of slice registers are 4066. MM-LDPC [29] consumes gate count of 320K; NB-LDPC coder [30] with $GF(8)$ design consumes the number of slices

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utilized as 14535 and $GF(32)$ design consumes number of slices utilized as 22494. NB-LDPC coder [31] consumes a gate count of 564K and QC-NB-LDPC coder [32] consumes the gate count as 2.54M. The proposed LPNB-LDPC coder with Virtex4 design consumes 2767 slice registers, 3090 slice FFs and 1553 look up tables (LUTs); Virtex5 design consumes 3088 slice registers, 1146 FF-LUTs pair and 1555 LUTs; and Virtex7 design consumes 3062 slice registers, 1124 FF-LUTs pair and 1498 LUTs. It is clearly shows the hardware utilization of proposed LPNB-LDPC coder is very low compared to existing coders.

5.2 Maximum operating Frequency comparison

Maximum operating frequency comparison of proposed and existing coders is shown in Table 3. LDPC decoder [21] has 200MHz, QC-LDPC decoder [22][23] have 100 and 474 MHz respectively. CB-LDPC coder [24] has 100MHz, both SCMS-V1 and V2 LDPC coder consumes 300MHz frequency [25]. LDPC-BC [26] decoder consumes 333MHz maximum clock frequency. HQC-LDPC decoder [27] consumes 400MHz; MM-LDPC [29] consumes 400MHz maximum clock frequency; NB-LDPC coder [30] with $GF(8)$ consumes 170.8MHz and $GF(32)$ consumes 130.2MHz frequency. NB-LDPC coder [31] consumes 277MHz and QC-NB-LDPC coder [32] consumes 370MHz maximum clock frequency. The proposed LPNB-LDPC coder with Virtex4 design consumes 502MHz; Virtex5 design consumes 508MHz; and Virtex7 design consumes 556MHz maximum clock frequency. Table clearly depicts the maximum clock frequency of proposed LPNB-LDPC coder is high compared to existing coders.

Table 2 Comparison of device utilization

References	LDPC type	Field size (m)	Device utilization		
			Slice registers	Slice LUTs	FFs/ FF-LUTs pair
[21]	LDPC	8	3.11 mm^2 area		
[22]	QC-LDPC	8	1.79 mm^2 area		
[23]	QC-LDPC	8	416.2K gate count		
[24]	CB-LDPC	8	15.75 mm^2 area		
[25]	SMCS-LDPC	8	NA	NA	60K
[26]	LDPC-BC	8	1077K gate count		
[27]	HQC-LDPC	8	4066	31305	16803
[28]	LDPC-BC	8	760.3K gate count		
[29]	MM-LDPC	8	320K gate count		
[30]	NB-LDPC	8	14535	NA	NA
		32	22494	NA	NA
[31]	NB-LDPC	8	564K gate count		
[32]	QC-NB-LDPC	8	2.54M gate count		
Our	LPNB-LDPC	8	2767	1553	3090
		32	2869	2100	3457

NA- Not available

Table 3 Comparison of Maximum operating frequency

References	LDPC type	Field size (m)	Maximum frequency (MHz)
[21]	LDPC	8	200
[22]	QC-LDPC	8	100
[23]	QC-LDPC	8	474
[24]	CB-LDPC	8	100
[25]	SMCS-LDPC	8	300
[26]	LDPC-BC	8	333
[27]	HQC-LDPC	8	400
[29]	MM-LDPC	8	400
[30]	NB-LDPC	8	170.8
		32	130.2
[31]	NB-LDPC	8	277
[32]	QC-NB-LDPC	8	370
Our	LPNB-LDPC	8	502
		32	493

Table 4 Comparison of Power consumption

References	LDPC type	Field size (m)	Power consumption (mW)
[21]	LDPC	8	99.2
[22]	QC-LDPC	8	104
[23]	QC-LDPC	8	114.3
[24]	CB-LDPC	8	800
[27]	HQC-LDPC	8	1638
[28]	LDPC-BC	8	437.2
[29]	MM-LDPC	8	284.3
[31]	NB-LDPC	8	274
Our	LPNB-LDPC	8	196
		32	202

5.2 Power consumption comparison

Power consumption comparison of proposed and existing coders is given in Table 4. LDPC decoder [21] consumes 99.2mW, QC-LDPC decoder [22][23] consumes 104 and 114.3mW respectively. CB-LDPC coder [24] consumes 800mW and HQC-LDPC decoder [27] consumes 1638mW power. MM-LDPC [29] consumes 437.2mW and NB-LDPC coder [31] consumes 274mW power. The proposed LPNB-LDPC coder with Virtex4 design consumes 196mW; Virtex5 design consumes 210mW; and Virtex7 design consumes 143mW power consumption. Table clearly depicts the power consumption of proposed LPNB-LDPC coder is very low compared to existing coders [24], [27]-[31].

6. Conclusion

We have proposed a low power non-binary low density parity check (LPNB-LDPC) coder over GF (2^m) for next generation system like WiMAX standard. In LPNB-LDPC coder, hardware realization of control node unit (CNU) is a perplexing portion because it involves of complex modules such as FFT/IFFT and multiplier. Here, we modify the CNU module by the flexible FFT/IFFT and multiplier instead of conventional FFT/IFFT and multiplier, which reduces the reconfigurable design and their extra time. Simulation results prove the proposed LPNB-LDPC coder enhances hardware features are hardware utilization, power consumption and maximum operating frequency.

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