LOW POWER VLSI ARCHITECTURE FOR MINING MEDICAL DATA CHIP

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Abstract: *Investigators gape on the scheme of devices with low power as they remain reining the electronics engineering nowadays. Power Dissipation is an serious design parameter in Very Large Scale Integration (VLSI) circuits as it shows an exciting part in the concert approximation of the battery-operated devices predominantly castoff in Health care applications. There are several algorithms and systems aimed at mining data that are existence continually settled and upgraded through investigation communities and industrial establishments worldwide, nonetheless selecting the greatest satisfactory and through the utmost optimum outcomes for the problem at hand remnants a main concern and a critical decision to make. The reduction of the chip size and growth of the chip density and complexity intensify the trouble in designing higher performance low power overwhelming system on a chip. Additional, global power management on a chip is fetching a giant challenge below 100 nm node because of its enlarged design complexity. Low power VLSI architecture is designed for Layered Two Phase message passing (LTPMP) medical chip Health application (MCHA) architecture, micron technologies, dynamic, statics and leakage power consumption is fetching an indispensable design parameter by way of it is dispelling a noteworthy percentage of the whole power consumption. This paper delivers a vision around the numerous strategies, methodologies, and power management techniques to be cast-off the scheme Data mining (DM) medical chip for Health Application (MCHA) low power circuit based systems.*

Key words: *VLSI, MCHA, Biomedical, sub micron, dynamic power, LTPMP* `

1. Introduction

There is a big prosperous in microelectronics organization meanwhile the innovation of transistor that sets the grounds for low power overshadowing devices. The very large scale integrated circuits (VLSI)[1] enriched enactment of the devices and also commanded to size decrease. This consequences the development of power unit area in Integrated Circuits(ICs)[2][3]. The paper focus on developing the low power elements [4]-[6] and low power methods and techniques. The reduction in size of the chip and increase in the density of the chip hence the complexity intensify the exertion in designing advanced performance low power consuming system on a chip(SoC)[7]. Reducing power is a paranormal progress which collected position with the growths of deep submicron[8] and nanometer technologies

2. Existing hardware architecture for MCHA

The Medical Chip Healthcare Application(MCHA)[9] VLSI reconfigurable structures or the architecture can be considered into three domains (1) Partially Parallel architecture. (2) Fully Parallel architecture and (3) Serial architecture The existing VLSI design architecture be categorized into fully parallel architecture designs, fully serial architecture designs, and partly parallel architecture designs. Although fully partial parallel design architecture exploits the inherent parallelism using Leaning Vector Quantization(LVQ) algorithms and revises all extrinsic dataset in one clock cycle, fully serial architecture designs bring up to date only one extrinsic message in each clock cycle.

The dataset throughput of the low power VLSI architecture s twice by means of architectures with Layered two-phase flooding message passing(LTMPM) rendering to LVS algorithm compared to one-phase message passing(OMPM). The layered LVS[9] algorithm intensifications the convergence speed by using efficient values during the current iteration. This reduces the number of necessary datamining iterations and consequently upturns the data throughput. Nevertheless, memory right of entry is fundamentally dissimilar for the one-phase message passing and two-phase message passing [10][11]. Thus different approaches are requisite to resolve memory access crashes in the equivalent VLSI architectures.

2.1 Architecture using MCHA

Partly parallel VLSI architectures for MCHA[12] can be employed in several straight forward ways. In this section three basic VLSI design style. types by way of displayed in Figure 1 are conversed. Architectures that utilize two-phase message passing (TPMP) is shown in the Figure 1

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The partly parallel VLSI architectures consider preparation of the data calculations. The TPMP[9] architecture contains of sequential functional unit (FU) accomplishment check nodes and variable nodes calculations alternately, a barrel shifter register network (shifter), and extrinsic dual-port memory external memories (EM). The intrinsic standards remain warehoused in the intermediate memory (IM) and the interpreted dataset is kept in data memories.

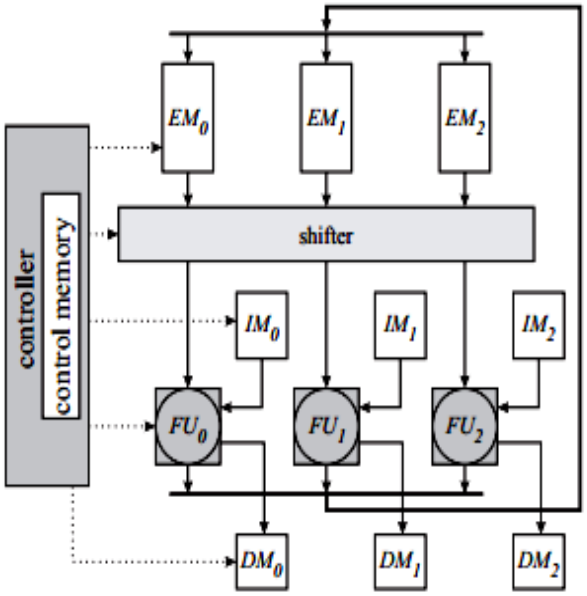


Figure 1 TPMP architecture MCHA

2.2 OPMP Architecture using MCHA

The OPMP in contrast to TPMP[10] has twice the data throughput that can be achieve using committed Check Functional Unit (CFU) and Variable Floating Unit(VFU) for check and variable node computations as an alternative of collective functional units (FU).The data memory of the One phase message passing (OPMP) architecture is replaced by the sum memories and the additional shifter network is instantiated. The architecture for the one phase message passing is shown in the Figure 2.The VLSI architecture for the medical and health care application is designed by OPMP in which the learning vector quantization(LVQ) algorithm. The one phase message passing algorithms are the most primary type of Low per VLSI architecture.

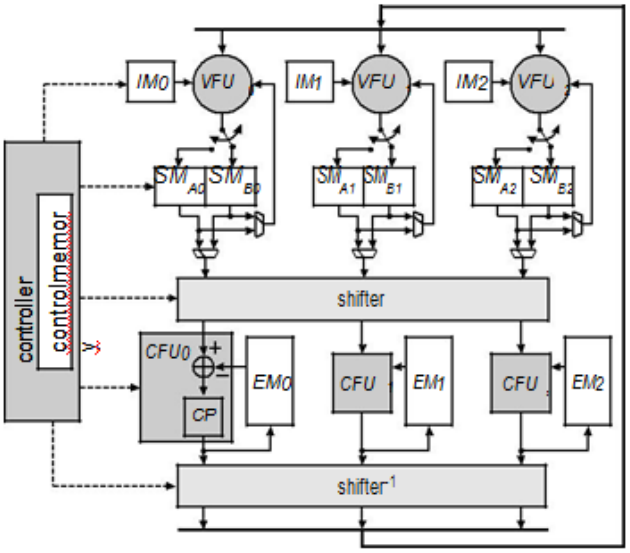


Figure 2 Architecture of One Phase Message Passing for MCHA

2.3 Layered Architecture using MCHA

For a layered decoding schedule the MCHA architecture is derived from the OPMP[12] architecture model. The layered architecture for MCHA is shown in the Figure 3. The layered two phase message passing architecture when compared with the OPMP architecture has one shift register, memory bank and the intrinsic memory being saved. In totting up to the hardware reserves, the modified layered LTPMP scheduling is known to enlarge the meeting speed of the data mining algorithm, thus fewer iterations are wanted to attain the same error correction enactment.

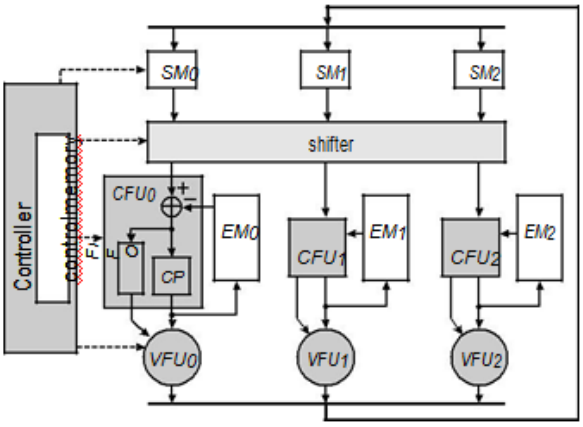


Figure 3 Architecture of layered LTPMP of MCHA

The conventional Layered architecture for medical chip health care applications has better performances compared to the other VLSI architectures.

3. PROPOSED LTPMP MCHA ARCHITECTURE

In the proposed low power VLSI architectures, nodes are assembled organized like that every bit node has at the most one construction to respectively node group. Medical Chip Health application MCHA codes are previously naturally grouped; respectively bit node needs at most one construction to the nodes. The parity nodes in a lump row with the edges are signified by either a shifted individuality matrix or zero matrix. The MCHA inform themselves so willingly to layered message passing agenda, consequently it is the unique accepted for parity check matrix as exposed in the Figure 4

A number of iterative Learning Vector unitization (LVQ) data mining algorithms with high-quality error correcting performance and altering complexity for hardware operation of MCHA codes have been proposed. In the midst of various iterative datamining algorithms the Learning vector Quantization (LVQ) and its variants accomplish a superior trade-off between data mining.

Compared to fully parallel data mining architecture, partially parallel data mining architectures have fewer processing units deprived of the prerequisite for supplementary memory storage blocks and can capitulate better data mining throughput than serial kind of datamining architectures. Therefore, due to their well-organized memory usage and better parallel level decoding and high core consumption partially parallel data mining architectures agree extensively and are adopted in much high speed medical data mining applications.

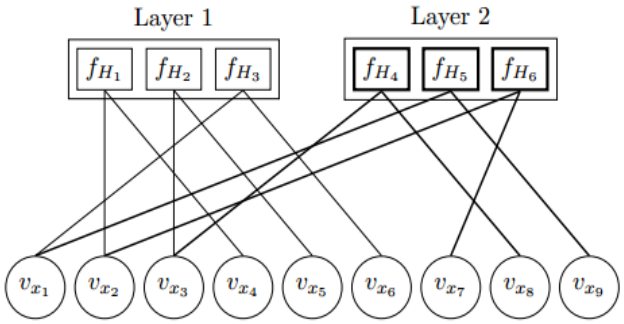


Figure 4 MCHA and layered tanner graph

4. IMPLEMENTATION RESULTS OF MCHA IN FPGA

The implementation of the MCHA is done in the Field programmable gate array (FPGA) device Xilinx 2v8000ff1152-5 for MCHA in LTPMP.. The number of the slices, CNU, VNU, IOB and routers is estimated for various code length.

In order to design layered datamining, the medical data mining needs to know which of the data set is currently used data in the system. This is identified as the active data. The data miners job is to collect

The power distribution of the LTPMP architecture is shown in the Figure 4.10. The power distribution is done with Logic which consists of CNU, VNU and shifters, memory, clock and wiring power consumption given in terms of mW. The Table 1 gives the detailed power distribution in the LTPMP architecture.
the likelihood datas into codeword data according to the MCHA decoding algorithm. This is shown in Figure 5. The MCHA decoder has the following modules

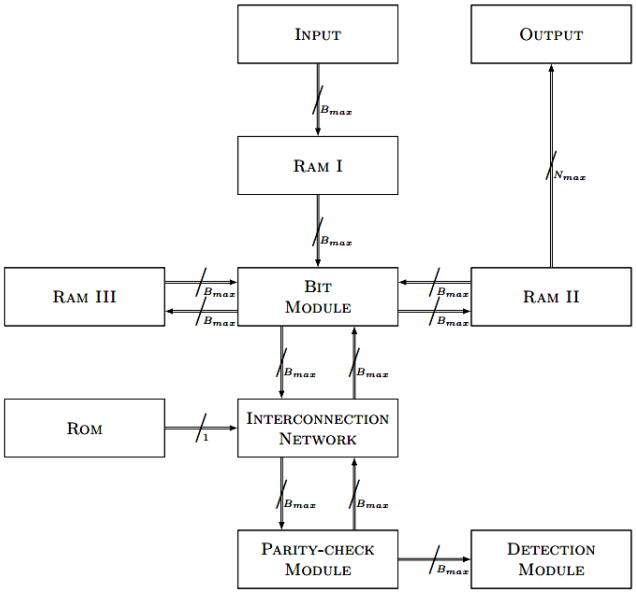


Figure 5 MCHA LTPMP VLSI module connections

5. RESULTS AND DISCUSSIONS

The implementation of the MCHA is done in the Field programmable gate array (FPGA) device Xilinx 2v8000ff1152-5 for QC-LDPC in LTPMP. Figure 6 gives the comparison with the implementation of the TPMP with LMP architecture. The detailed FPGA results of the Layered Two phase Message Passing (LTPMP) architecture for MCHA are given in the Table 1. The quantity of the slices, Check Node Units (CNU), Variable Node Units (VNU), Input Output Block (IOB) and routers is estimated for various data sets.

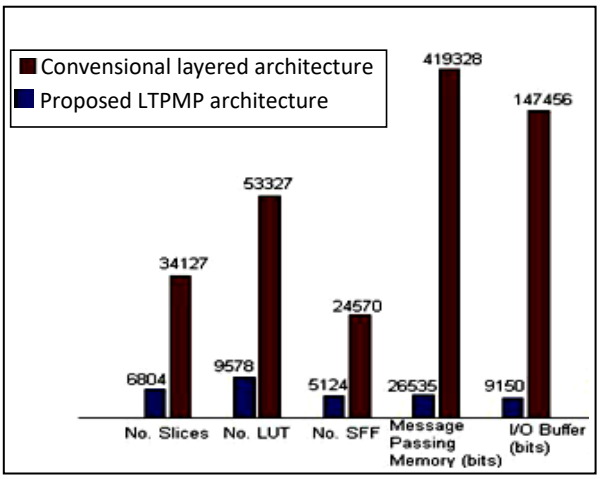


Figure 6 Comparison of components in LTPMP architecture

The power distribution of the LTPMP architecture is shown in the Figure 4.10. The power distribution is done with Logic which consists of CNU, VNU and shifters, memory, clock and wiring power consumption given in terms of mW. The Table 1 gives the detailed power distribution in the LTPMP architecture.

Table 2 Detailed building block of MCHA decoder architectures

Architecture	Sum Memory		External Memory		Intrinsic Memoy		CFU	VFU		Shifter
	Bank	Depth	Bank	Depth	Bank	Depth				
TPMP	-	E/p	p	E/p	P	N/p	p	P		1
OPMP	2p	E/p	p	E/p	P	N/p	p	P		2
LMP				P	E/p	E/p	-	-		2
LTPMP				-	E/p	E/p	K	N/k		-

The memory mode types are the single port or dual ports are in the sequential node implementations. The check nodes and variable nodes computation are performed alternatively.

6. CONCLUSION

The essential for lower power systems is existence obsessed by numerous market sections. Unfortunately scheming for low power enhances additional dimension to the previously compound design delinquent and the design has to be enhanced for power in addition to performance power and area. In conclusion various issues and major challenges regarding low power The classification of MCHA with respect to various architecture is done. The implementation of the MCHA in layered TPMP architecture is analyzed. The power analysis of the LTPMP architecture is performed and the total power estimation is done.

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