POWER FACTOR CORRECTION USING BL-CSC CONVERTER FOR BLDC MOTOR DRIVE

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Abstract: *This paper presents a Power Factor Correction (PFC) based Bridge less Canonical Switching Cell (BL-CSC) converter-fed Brushless DC (BLDC) motor drive. The BL-CSC converter works in a discontinuous inductor current mode in order to obtain a 0.99 power factor of operation. The speed control of the BLDC motor is achieved by adjusting the DC bus voltage using a PI controller. Voltage Source Inverter (VSI) is operated at the fundamental frequency for reducing the switching losses of BLDC motor electronic commutation. By the partial elimination of the diode Bridge rectifier at the front end the bridgeless configuration of CSC converter has low conduction losses. The proposed configuration is validated using a MATLAB simulation and laboratory experimental setup, which shows a considerable increase in the efficiency.*

Key words: *BLDC Motor, VSI, CSC, BL-CSC, sensor-less, diode bridge rectifier.*

1. Introduction

Brushless DC (BLDC) motors are suggested for many medium and low power drives applications due to their following characteristics such as high flux density per unit volume, high efficiency, low maintenance requirement, reduced Electromagnetic Interference (EMI), ruggedness, and an extensive range of speed control [1][7][10].

BLDC motors [2] have applications in many areas such as household appliances, transportation (hybrid vehicle) aerospace heating, ventilation and air conditioning system, motion control and robotics, renewable energy, etc.

The BLDC motor is an AC motor with dc characteristics consisting of three-phase concentrated stator windings and a permanent magnet rotor. As the BLDC motor does not have any mechanical brushes and commutator assembly the wear and tear of the brushes and sparking issues are eliminated in BLDC motor [3][17].

Conventionally BLDC drive is fed by an uncontrolled rectifier through a DC link capacitor followed by a three-phase Pulse Width Modulation (PWM)-based VSI [4][18]. The diode bridge rectifier draws harmonic-rich current from the supply and leads to very low power factor at AC supply [5][14]. The total harmonic distortion THD of the supply current is above 10% and poor power factor ranges around 0.72, which is not accepted by IEC 61000-3-2. These THD and power factor problem can be reduced by the variable DC-link voltage based speed control of BLDC motor, here the VSI is utilized to operate in low switching frequency. Variable DC-link voltage is obtained by the SEPIC AND CUK converter at the front end of the VSI feeding BLDC motor using a variable voltage control using two current sensors [6][19].

The front SEPIC and CUK converter helps in the reduction of drawing the harmonic current from the source and improves the power factor up to 0.9. Selection of operating mode of the front-end converter plays an important role between the stresses on PFC switches and the cost of the overall system [8]. Designed front-end converter operates in two different modes such as Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM), was a voltage follower approach is considered as one of the control schemes for PFC converter at DCM mode [7][13].

BL-CSC converter is operated in Discontinuous Inductor Current Mode (DICM) were the inductor l_1 & l_2 current is discontinuous, on the other hand, the voltage across the capacitors C_1& C_2 are continuous [8]. An approach of variable DC link voltage based speed control of the BLDC motor is used and implemented by electronic commutation with reduced switching losses in the VSI [9]. PI control is employed in DC Link voltage control with its optimized k_p and k_i constants by using GENETIC ALGORITHM optimization.

2. BLDC Motor Drive

System configurations of the proposed BLDCM drive are shown in Fig. (1), the system comprises of a Diode Bridge Rectifier (DBR), PFC-CSC converter and a three-phase VSI connected to the BLDCM. A sensorless control of BLDCM is used in order to eliminate the rotor position sensors for electronic commutation [1] [11].

Speed control of BLDCM over a wide range is achieved by varying the voltage at DC bus of VSI. The VSI feeding the BLDCM is operated at a fundamental switching frequency to obtain electronic commutation at minimal switching losses [12].

Diode bridge Rectifier (DBR), converts AC signal to DC signal, a dc filter is placed next to reduce the harmonics from the DBR. The Bridgeless Canonical Switching Cell (BL-CSC) is introduced in order to reduce the usage of diodes, thereby reducing the harmonics generated by the diode bridge rectifier. From BL-CSC converter, the BLDC motor is fed through voltage source inverter and the motor rotates. The PI controller is used to find the controlling signal with respect to the error signal and driver units are used generate trigger pulse, s for the voltage source inverter using the control signal got from the PI controller. The FPGA controller has the voltage of minimum 5v, so driver unit is used for the purpose of optical isolation between the FPGA board and the inverter circuits.

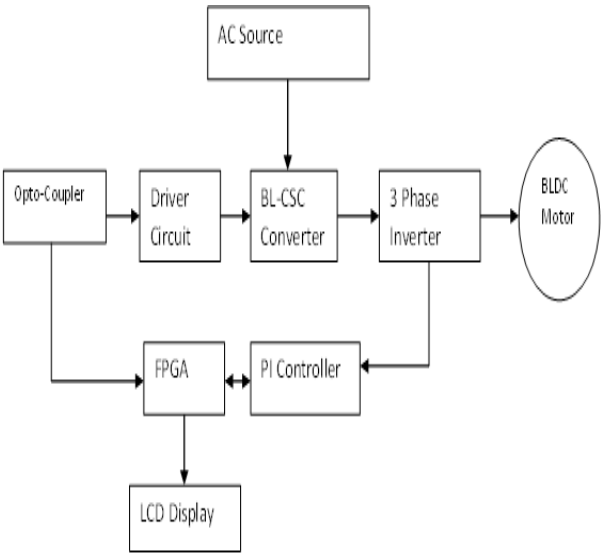


Fig. 1 Block Diagram of the proposed system

A. Bridgeless Rectifier and Boost Converter

Fig. 2 shows the circuit diagram of the PFC with bridgeless rectifier with the BL-CSC converter. Two buck converters connected in a parallel input series output manner comprises the bridgeless rectifier whose output is given to a boost converter to get improved power factor. The upper buck converter comprises of switch S1 and diode D1, freewheeling diode D3, and inductor L1 and capacitor C1 conducts during the positive half cycle and the lower buck converter comprises of switch S2 and diode D2, freewheeling diode D4 and inductor L2 and capacitor C2 operates during the negative half cycle. On the other hand, the boost converter consists of inductor L3, switch S3, diode D5 and capacitor C0.

During the positive half cycle, the upper buck converter of the bridge rectifier consists of diode D1, switch S1 inductor L1, capacitor C1, freewheeling diode D3, and the boost converter consists of inductor L3, Diode D5, switch S3 and capacitor C0 operates. While the switch S1 is on inductor L2 stores energy and when S1 is off the stored energy in inductor L2 freewheel through the diode D3, during the above said operation voltage develops across the capacitor C1 is fed as input to the boost converter Vin. Fig. 3 and Fig. 4 depicts the operation of the circuit during the line voltage at positive and negative half cycle.

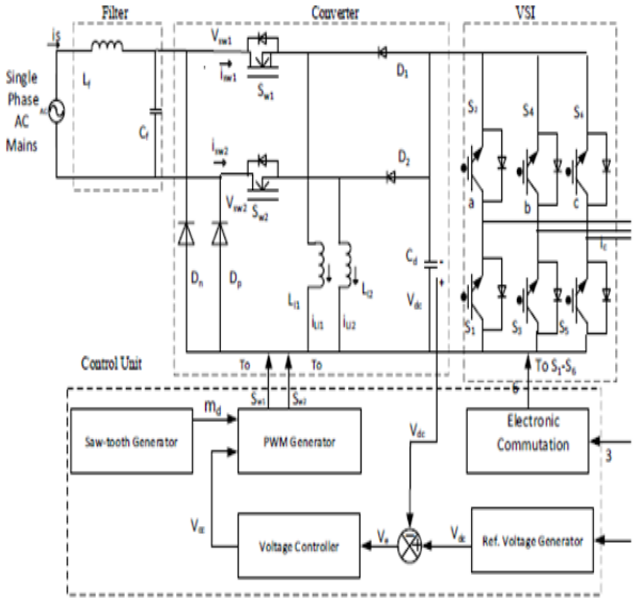


Fig. 2 Topology of the Novel Three-Phase Bridgeless BL-CSC Converter

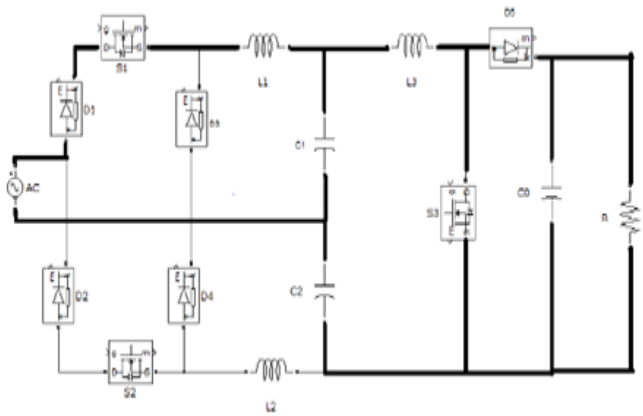


Fig. 3 Operation of the Circuit during the Period when Line Voltage is Positive

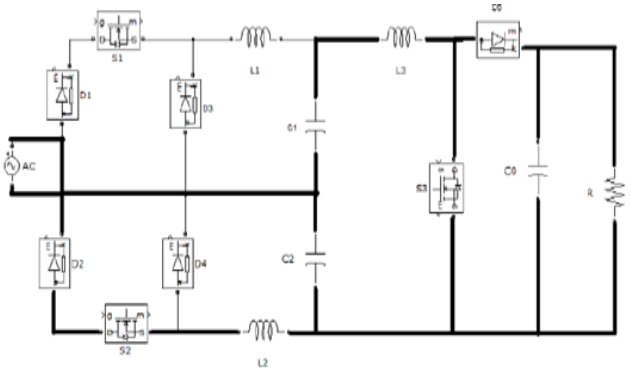


Fig. 4 Operation of the Circuit during the Period When Line Voltage Is Negative

Each phase of the three-phase bridgeless boost PFC are capable of working independently, during the positive and negative semi-cycles of the AC input, the circuit of A-phase is equivalent to an arrangement of two boosts PFC circuits with opposite voltage.

3. DESIGN PROCEDURE

Phase-delay (phase-lag) generated by sensing circuitry and a hysteresis comparator is compensated by phase lead compensator. The phase delay occurs between the virtual Hall signals and the actual zero crossing of the line back-EMF measured.

Phase-delay of 17-18 is got at the rated speed, the phase-lead compensator is designed using the transfer function in Eqn. (1),

$$G_c(S) = a\left(\frac{a(s+\omega_{c1})}{(s+\omega_{c2})}\right) = a\left(\frac{(s+1)/aT}{(s+1)/T}\right) \quad (1)$$

Where the $\omega_{c1}$and $\omega_{c2}$are the two corner frequencies, constants a and T is the time constant shown in Eqn. (2),

$$a = \frac{(1+\sin(\varphi_m))}{(1-\sin(\varphi_m))};\ T = \frac{1}{(\omega_m\sqrt{a})} \quad (2)$$

where φ_m is the required phase lead angle and ω_m is the frequency analogous to the maximum phase lead angle (φ_m). In addition, ω_m can also be represented as Eqn. (3),

$$Log_{10}(\omega_m) = \frac{1}{2}\{log_{10}(\omega_{c1}) + log_{10}(\omega_{c2})\} \quad (3)$$

The value of constant 'a' is determined using Eqn. (2) as 1.8944 and the time constant, T is calculated as $1.44x10^{-3}$ rad/sec using Eqn. (3). Two corner frequencies, ωc1 and ωc2 are obtained as ω_{c1} = 1/T = 692 rad/sec and ω_{c2}= 1/(aT) = 365 rad/sec. In order to obtain a maximum phase shift of 18^0at rated speed, subsequently to the frequency of 80 Hz (i.e. $\omega_m \approx$ 503 rad/sec), By substituting the above-said values in Eqn. (1), the transfer function of the required phase lead compensator as Eqn. (4) can be got,

$$G_c(s) = 1.8944\left(\frac{(s+365)}{s+692}\right) \quad (4)$$

$$G_c(s) = \frac{(s+(\frac{1}{R_aC_a}))}{(s+(\frac{1}{R_aC_a})+(\frac{1}{R_bC_a}))} \quad (5)$$

thereby equating the Eqn. (5), the value of R_a and R_b are calculated as 27.4 kΩ and 30.6 kΩ (Ca = 0.1μF).

4. SOFTWARE RESULTS

The simulation diagram of the BL-CSC converter-fed BLDC motor drive is shown in Fig.5. The input Voltage and current are shown in figure 6. The filtered current and power are shown in figure 7. The motor speed and torque developed is shown in figure 8. Table 1 shows the evaluation parameters.

Table 1. List of Parameters

Input Voltage	50 V
Filter (LC)	L=1.5e^{-3} and C= 330e^{-9}
Switching Frequency	50 Hz
Motor	3 Phase BLDC
Set Speed	1200 rpm
Reference Speed	2000 rpm

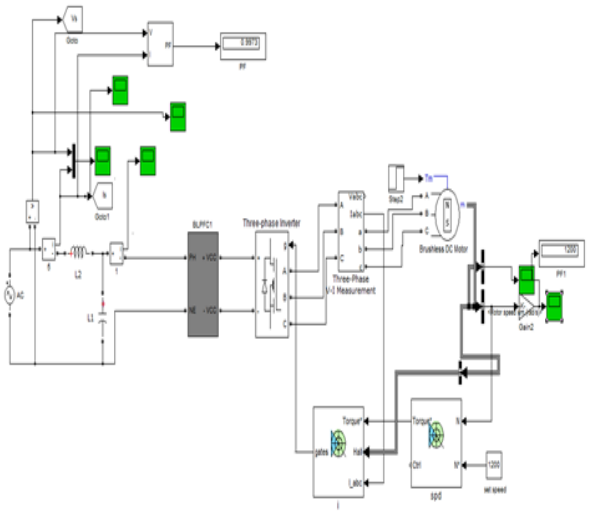
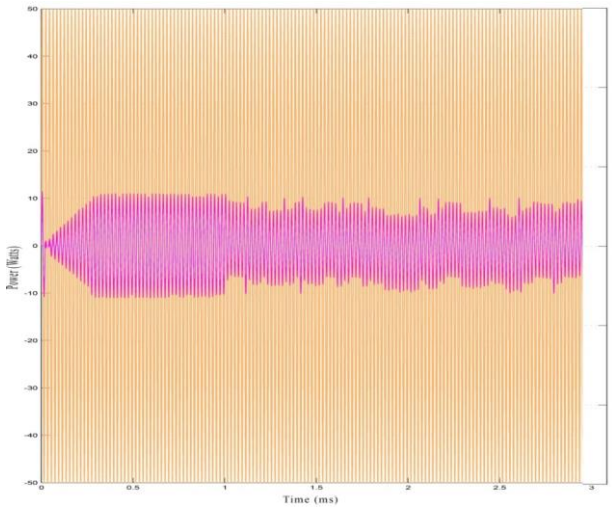
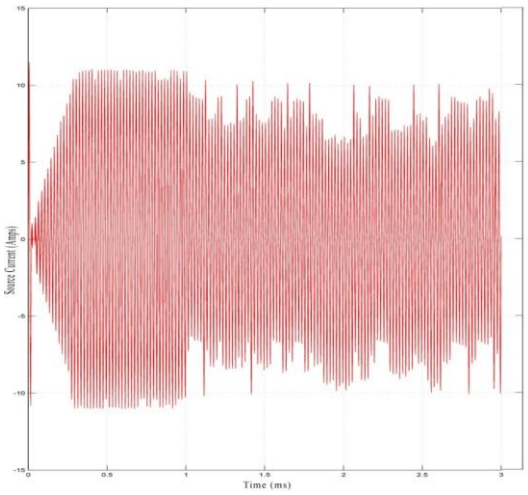
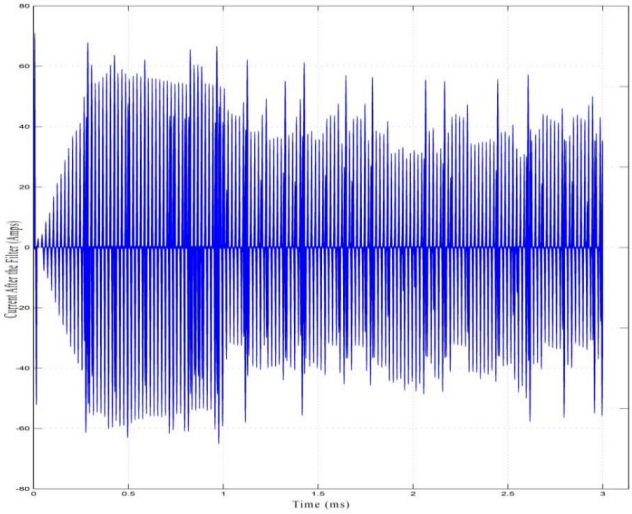


Fig. 5 MATLAB Simulation Diagram



(a)





(b)

Fig. 7 (a) & (b) Filter Current and Power of the Motor

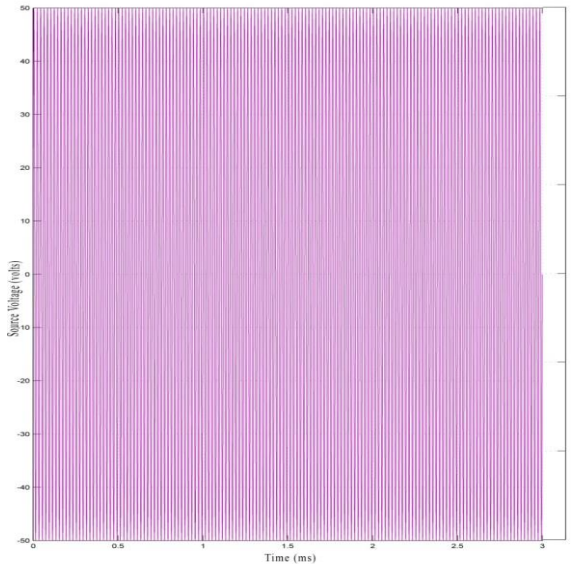
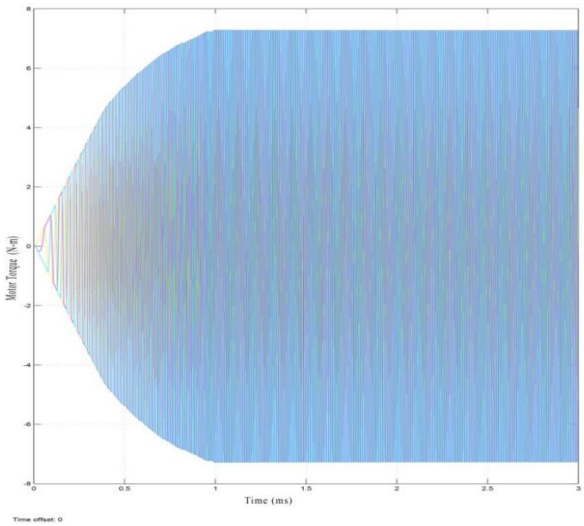
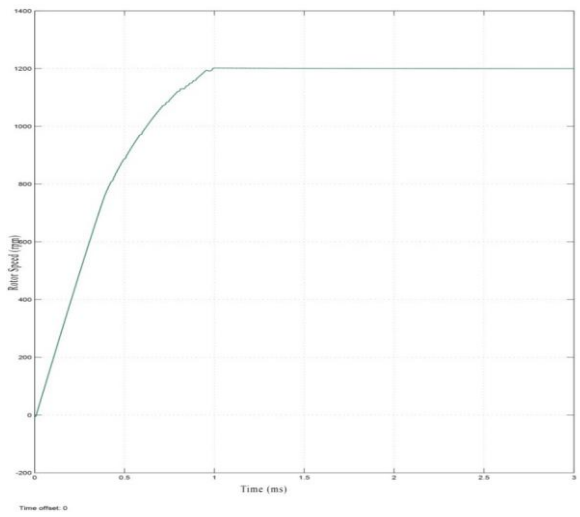


Fig 6. Source Current and Voltage



(a)

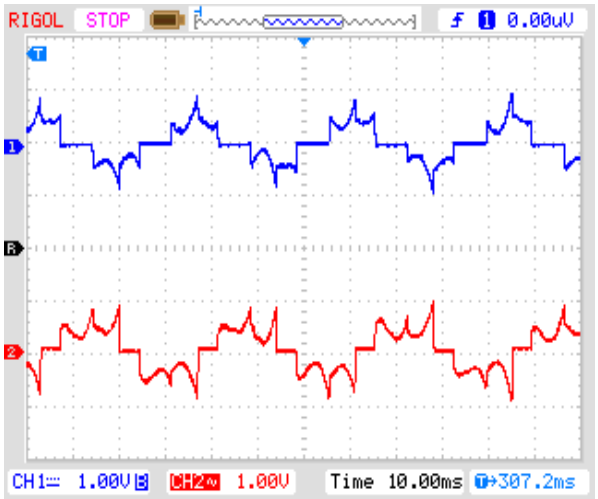


(b)

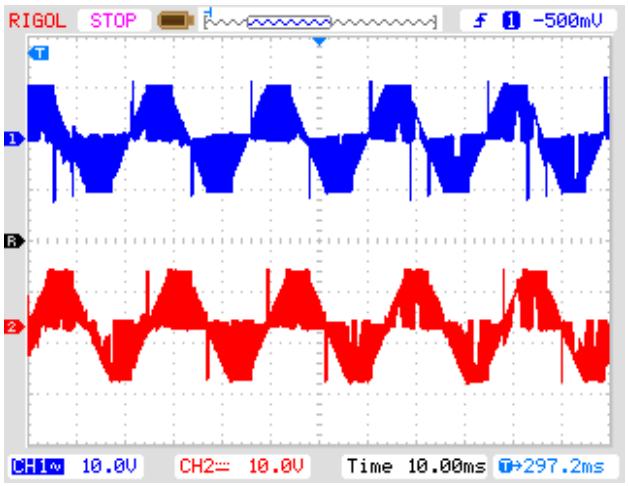
Fig. 8 (a) & (b) Motor Torque and Speed of the Rotor

A. Hardware Results

AHMY_SP6_LX9_LC FPGA board is used due to it's a low-cost board featuring Xilinx Spartan-6 FPGA. It is specially designed FPGA board for research, experimentation and learning system. The TOSHIBA TLP250 consists of a GaAlAs light emitting diode and an integrated photodetector is used as an optocoupler. This unit is 8−lead DIP package.TLP250 provides isolation and gate driving circuit of IGBT or power MOSFET.

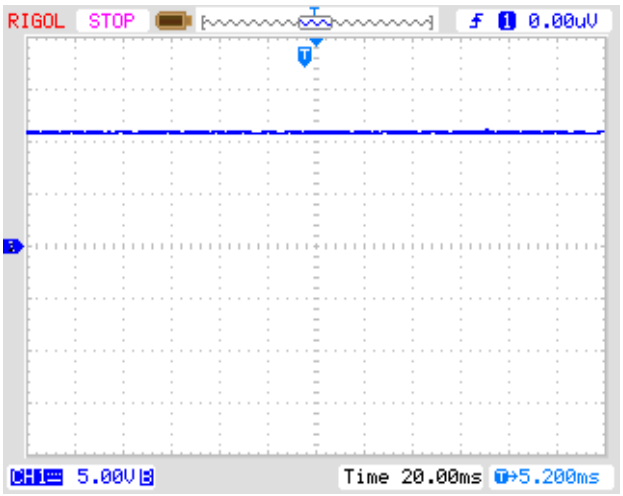


(a)

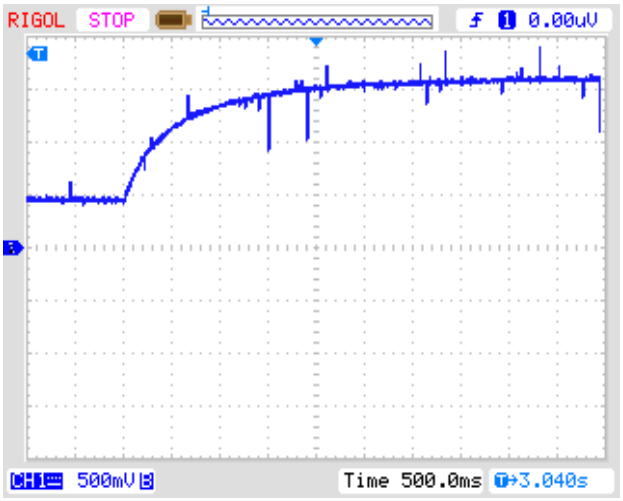


(b)

Fig. 9 (a) & (b) Current and Voltage of the BLDC Motor

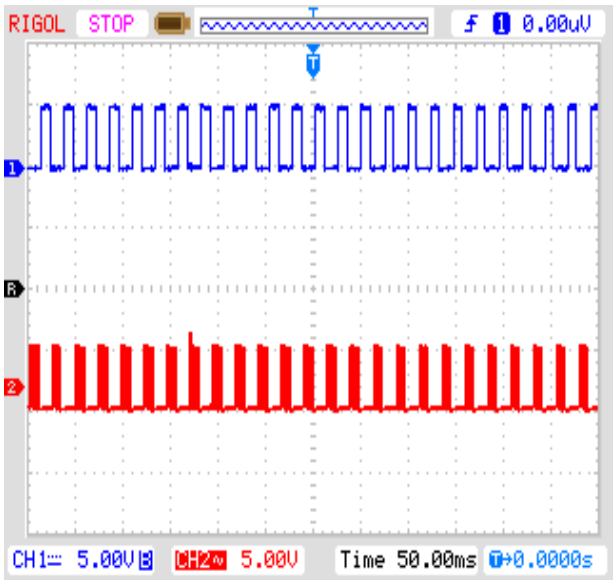


(a)

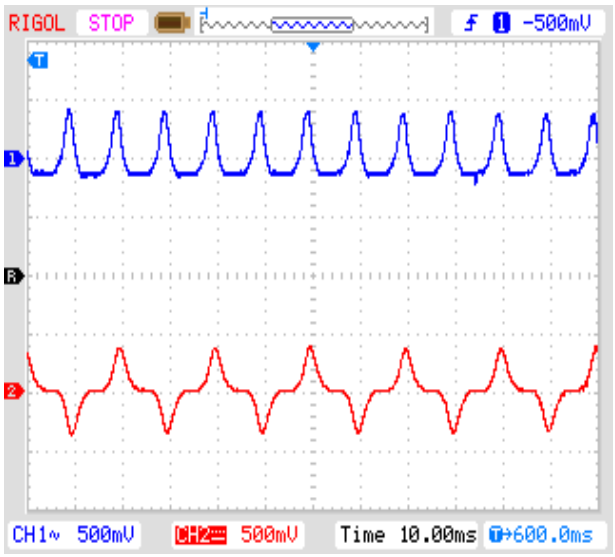


(b)

Fig. 10 (a) & (b) DC Link Voltage and Transient Voltage Waveform

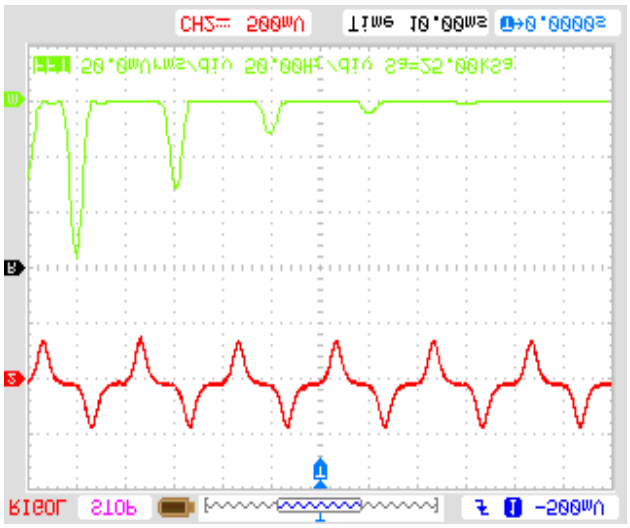


(a)

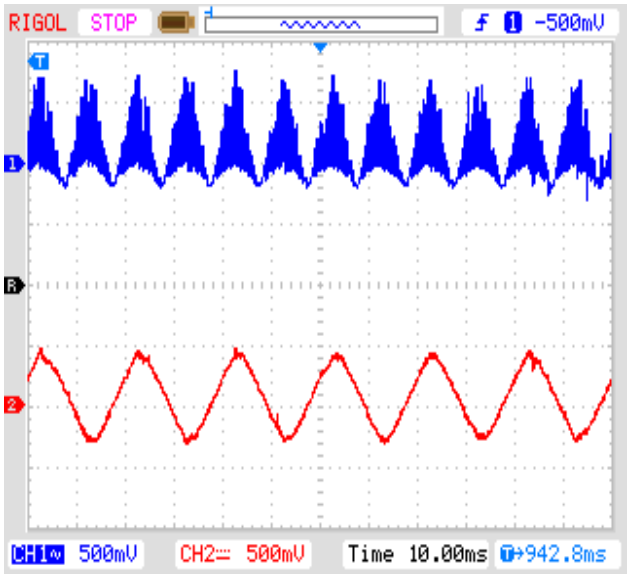


(b)

Fig. 11 (a) & (b) PWM Pulses and Inductor Current & Source Current before Converter ON



(a)

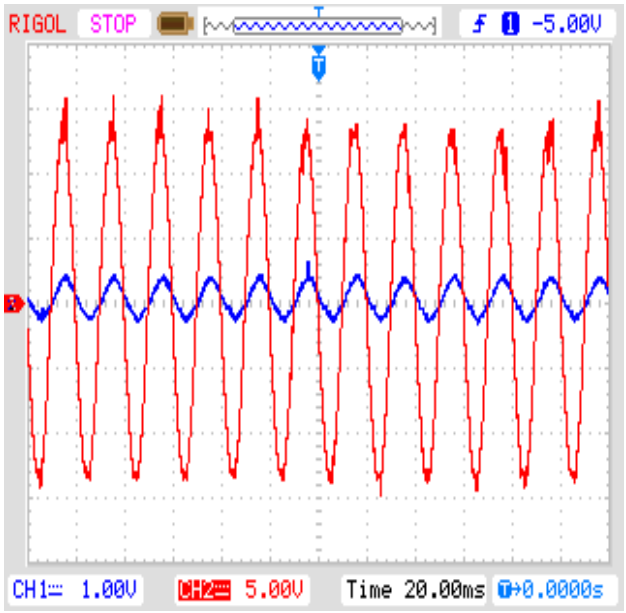


(b)

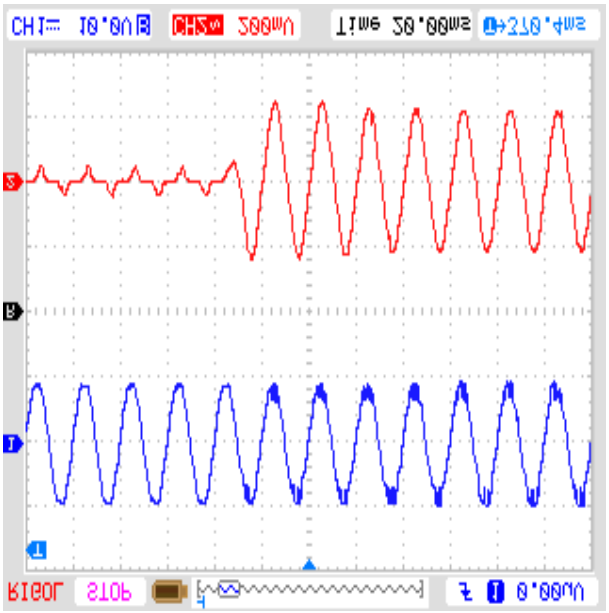
Fig. 12 (a) & (b) Source Current and FFT before Converter Switched ON & Source Current and Inductor Current after Converter ON

The BLDC motor stator voltage and current are as shown in Fig. 9.The DC link voltage and its transient are shown in Fig. 10. The inductor current and source current before converter ON state waveform and the converter PWM signal is as shown in Fig. 11. Source current and FFT before converter switched ON state waveform and source current and FFT, after converter switched ON state waveform, is as shown in Fig. 12. Source voltage and current after converter ON state and source voltage and current transient are as shown in Fig. 13. The Source voltage and corresponding FFT is

as shown in Fig. 14.



(a)



(b)

Fig. 13 (a) & (b) Source Voltage and Current after Converter ON and Source Voltage and Current-Transient

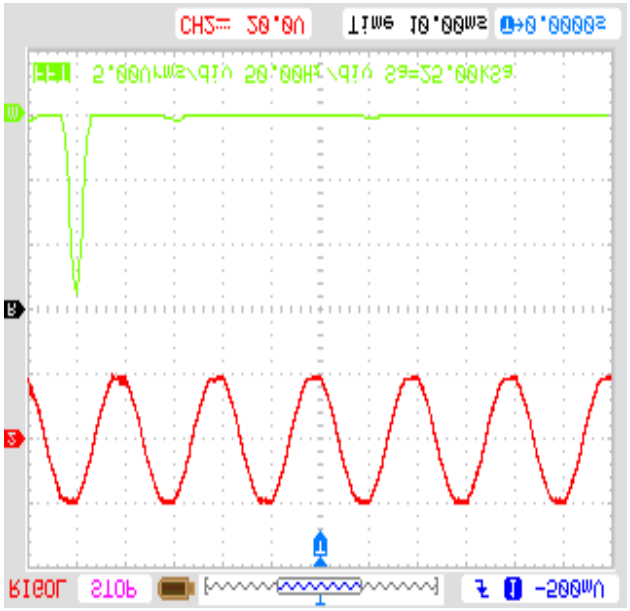


Fig. 14 Source Voltage and FFT

5. CONCLUSION

BL-CSC Converter for BLDC Motor Drive is proposed in this paper. The proposed system is first designed in MATLAB simulation environment. The circuit modes of operation are elaborated and the simulation of the circuit is performed. The results are displayed and they show an improvement in power factor. The hardware prototype is implemented using FPGA board. The hardware results are also showing that the proposed system has successfully reduced the power factor problems. The system transients are also shown in the hardware results.

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