A SIMPLE AND COST-EFFECTIVE MODULAR INTELLIGENT TRANSFORMER FOR LOW AND MEDIUM VOLTAGE APPLICATIONS

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Abstract: *Intelligent transformer has not seen wide proliferation into the market despite its introduction in early 90's because of the lack of development of a simple and rugged model which is both economical and multifunctional. This paper is aimed at presenting the design and development of an Intelligent Transformer (ITR) with a simple and cost effective control scheme and a modular structure to facilitate commercial deployment in an extensive scale for low and medium voltage applications in power distribution networks. The Modular ITR (MITR) as it is named is constructed with well-known topologies of solid state converters in three stages coupled with a medium frequency transformer. Each stage of MITR is individually controlled to ensure high degree of modularity and a well regulated output voltage so that issues with interconnection are avoided. Simulation results are presented to demonstrate the performance characteristics as well as additional functionalities of MITR beside voltage transformation. A scaled down laboratory prototype is developed to prove the choice of topologies of individual stages and the concept of MITR.*

Key words: *AC-DC Converter, DC-DC Converter, medium frequency transformer, Voltage regulation*

1. Introduction

For decades now, conventional transformers operating at low mains frequency (50Hz/60Hz) have been essential elements of power distribution networks wherein they provide isolation between network sections characterized by different voltage levels. These transformers though highly efficient and reliable, have their inherent drawbacks of being bulky and sensitive to harmonics, environmental concerns regarding mineral oil, lack of controllability, losses at no load etc [1-2]. Thus they are deemed unsuitable for use in future smart grids which demand compact electrical equipment with sophisticated control offering multiple services in a single embodiment. With the onset of solid state switching technology, the conventional low frequency transformers deployed for decades in power distribution networks are being upgraded with smart control ability to alleviate power quality disturbances [3-7]. Researchers in the past have attempted to modernize conventional distribution transformers under several names [1-17] including Power Electronic based Distribution Transformers, Solid state transformers (SSTs), Intelligent Universal Transformers (IUTs) and Intelligent Distribution Transformers (IDTs) to match advanced power supply demands from consumers.

The basic idea behind incorporating solid state devices into the traditional transformer design is to extend its services by making it a multifunctional system with many integrated features such as output voltage regulation, power factor correction, voltage sag, outage and reactive power compensation, possibility of a dc input or output, and many other protection functions [2-3]. Also the use of solid state technology permits the use of high mains frequency (>1 kHz) thereby allowing for higher utilization of magnetic core and reduction in size of the transformer.

Initially, effort was made to duplicate the function of the power transformer using power semiconductor devices [6]. However, it failed to demonstrate the isolation characteristic of the traditional low frequency transformer. Later, Intelligent transformer (ITR) concept was proposed in 1996 by Koosuke Harada [7], whose primary aim was to miniaturize the size of the commercial frequency power transformer. Subsequently, scientists and researchers from Electric Power Research Institute (EPRI) [1-2], [8-11] Future Renewable Electric Energy Delivery and Management (FREEDM) Systems Center [12], General Electric Company [13], Siemens [19], ABB [21], ETH Zurich Laboratories [25-26] were involved in developing new architecture, topologies and control schemes to improve the performance and services provided by ITR. These efforts however did not largely culminate into commercialization of the product because of complex control schemes and

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time and cost involved in developing and testing the field models.

The ITR architectures proposed so far in literature have hardly reported on the overall efficiency of the device under varying load conditions, percentage THD levels of output voltage and current and the effect of source voltage variation on output voltage which are imperative to establish proof of the concept of ITR in mitigating power quality issues.

This paper presents the design and development of MITR with simple and cost-effective control schemes and investigates the performance of the device under varying input, load and transient conditions. The designed MITR is capable of providing better isolation between source and load besides allowing for extended voltage levels, possibility of scaling and ease of service because of its extremely modular structure. Furthermore, the three stages of ITR are individually controlled to add to the portability of the device.

The MITR comprises of solid state converters in three stages: input, isolation and output as shown in Fig.1. The input stage of MITR is a single phase bidirectional multilevel AC-DC converter operating at high switching frequency. The isolation stage constitutes medium frequency isolated DC-DC converter followed by a single phase DC-AC converter at the output stage. The input is coupled to high-voltage distribution system, and the output is tied to low-voltage household applications. DC voltage at medium and low levels with minimal ripple content, if needed, can be tapped at intermediate dc links.

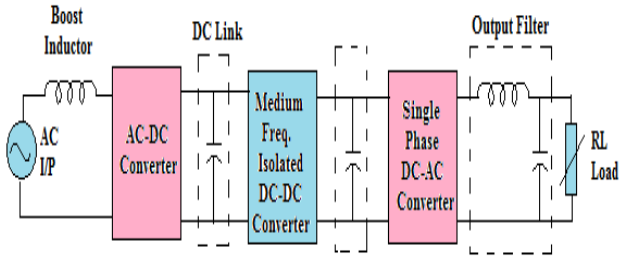


Fig. 1 Block Diagram of Modular Intelligent Transformer

The paper is organized as follows: Section 2 presents the choice of topologies for three individual stages and modeling of MITR. Section 3 describes the performance characteristics of the developed MITR and the experimental setup along with its results are detailed in Section 4. Section 5 presents the conclusion of the work.

2. Modeling and Design of MITR

The modeling of MITR involves modeling of individual converters with appropriate closed loop control schemes and interconnecting them to form a module. Though the converters employed for the individual stages are of well-known topologies, the challenge lies in selecting the suitable topologies for successful interconnection to ensure better performance of MITR.

The selection of topology for each of the three different stages of ITR has been explored in detail and the merits and demerits of those topologies were reported in literature [19-24]. Nevertheless, no consensus has been arrived at the appropriate choice of topology for distribution voltage level applications. This has paved way for the researchers to experiment on a variety of topologies available for each of the three stages based on several factors including components count, filter requirements, ability to handle unbalanced loads, desired voltage levels, allowable switching frequency etc.

The focus of this work lies in developing a MITR for low and medium voltage applications. The complete circuit of MITR is shown in Fig.2. The input stage employs a three-level neutral point clamped converter. The choice of multilevel topology for the input stage is justified by the fact it is scalable to any desired voltage rating and has minimum demands for the input filter [26-27]. Also, it has more control degrees of freedom which can be used to enhance power quality and efficiency. Among the basic multilevel topologies available namely, neutral point clamped (NPC), capacitor-clamped and cascaded inverters, the latter requires numerous isolated dc sources and hence not economical for distribution voltage applications. Between the other two, the NPC seems to be the better choice considering dynamic voltage balancing among different levels.

Upon choosing three - level NPC for the front end converter, the isolation stage employs a half-bridge NPC connected to the primary of the medium frequency transformer and a two-level diode bridge rectifier connected to the secondary. A single phase bridge inverter with sinusoidal PWM is chosen for the output stage DC-AC conversion with minimum THD levels.

A simulation model of 1.2kV, 5kVA MITR is developed, wherein the design of each stage with their control scheme is discussed below:

2.1 Input Stage:

Each input module of MITR consists of a single

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phase three level neutral point clamped converter as

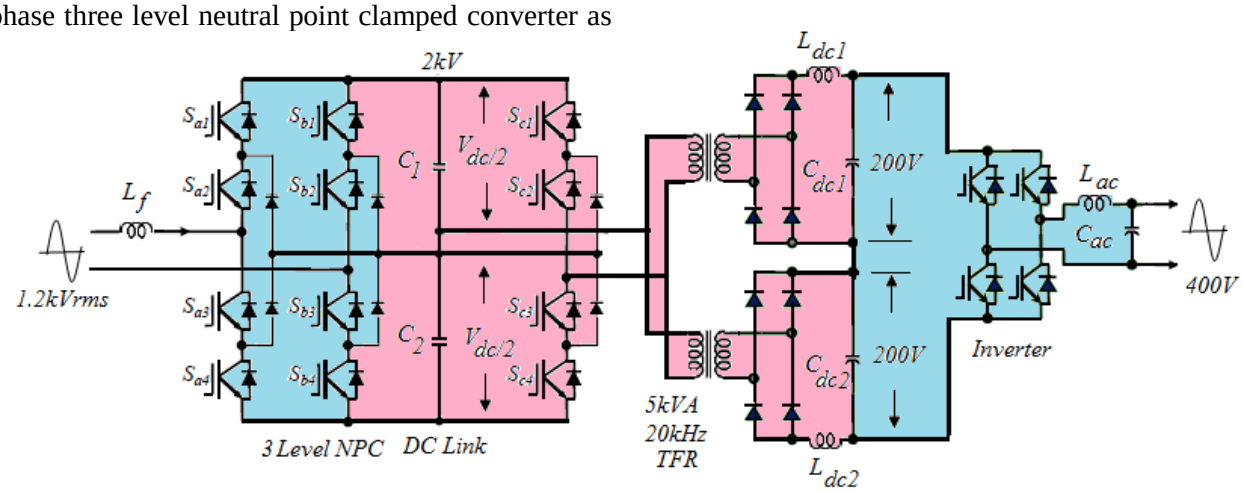


Fig.2 Circuit Schematic of MITR

shown in Fig.2. With the dc voltage and inductor current ripples assumed to be 2.5% and 10% respectively at a switching frequency of 20 kHz, the dc link capacitors and boost inductor values are computed as

$$C_1 = C_2 = \frac{I_{srms}}{2 f_r * \Delta V_{dc}} \approx 420\mu F \quad (1)$$

$$L_f = D_m * \frac{|V_m - V_{dc}|}{2 f_{sw} * \Delta I_a} \approx 15mH \quad (2)$$

The voltage across dc link must be higher than the peak input voltage for the input current waveform to remain sinusoidal. Therefore, for an input rms voltage of 1.2kV and a modulation index of 0.85, the dc link voltage is typically 2kV and the switching devices are chosen to block at least 1kV.

The control circuit for the converter is developed based on small signal averaged transfer function model with simple PI control of voltage and current as shown in Fig.3. The open loop transfer function of inductor current is given by

$$\frac{\hat{i}_{lf}(s)}{\hat{d}_1(s)} = \frac{-V_{dc}}{sL_f} = G_i(s) \quad (3)$$

Similarly, the open loop voltage-to-current transfer function is given by

$$\frac{\hat{V}_{dc}(s)}{\hat{i}_{lf}(s)} = \frac{D_1}{sC_f} = G_v(s) \quad (4)$$

The pole-zero plot of the converter with the designed controller is depicted in Fig.4. It is observed from the figure that the designed controller has roots in the left half of the S-plane thus maintaining stability.

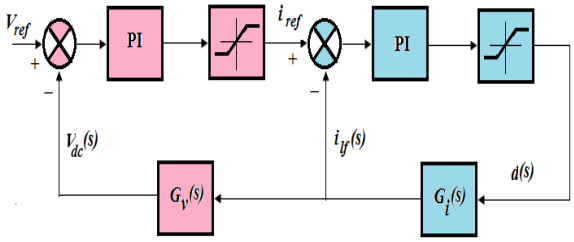


Fig.3 Closed Loop Control Scheme of Front End AC/DC Converter

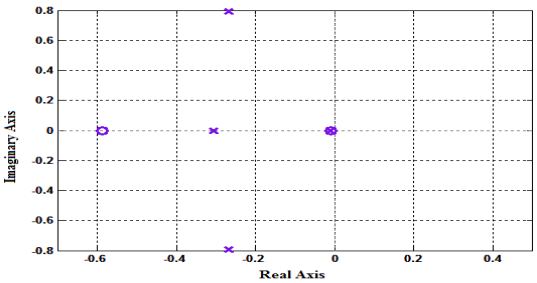


Fig. 4. Pole-zero Plot of NPC with the designed controller

The optimum values of proportional and integral gains for the voltage and current controllers are obtained using MATLAB SISOTOOL. The gain values are found to be K_p=0.05 & K_i=50 for the outer voltage loop and K_p=0.1 & K_i=10 for the inner current loop respectively. The technique employed for gating signal generation is phase opposition disposition pwm because it generates lower harmonics compared to other pwm techniques.

The design values are used to model the converter in MATLAB/Simulink platform and the simulation results are presented to verify the performance of the converter. The source voltage and current waveforms are depicted in Fig. 5(a). The dc link voltage across two capacitors C_1 and C_2 are very

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well balanced at 1kV as shown in Fig. 5(b).

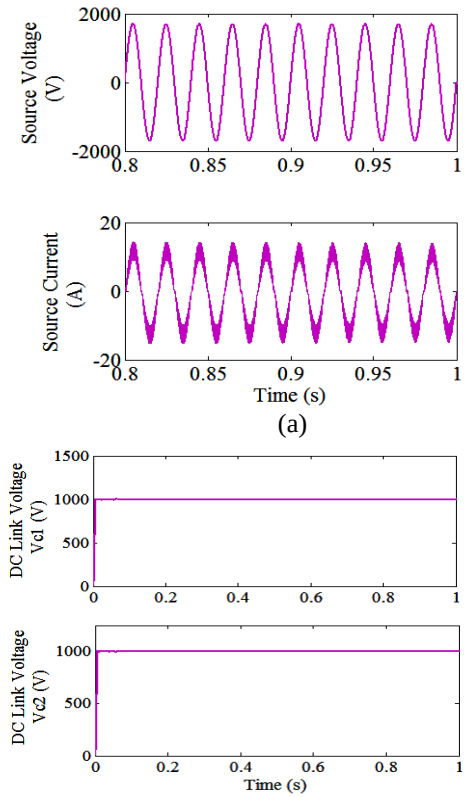


Fig.5 (a) Source Voltage and Source Current
(b) Voltage across DC Link Capacitors

2.2 Isolation Stage

The isolation stage comprises of a medium frequency transformer whose primary is connected to a three level half-bridge diode clamped inverter and secondary connected to a diode bridge rectifier with LC filter at the output as illustrated in Fig.2. With the assumption that the duty cycle achievable is 90%,

Turn's ratio of the transformer

$$n = \frac{1*10^3 * 0.9}{400} \approx 2 \tag{5}$$

The switching frequency of the isolated dc-dc converter is chosen to be 20 kHz and the dc-dc converter is designed to produce 200V dc across each of the dc bus capacitor. The Output LC filter is designed assuming 10% inductor current ripple and 5% capacitor voltage ripple.

$$C_{dc1} = C_{dc2} = \frac{\Delta I}{8 f * \Delta V} \approx 370\mu F \tag{6}$$

$$L_{dc1} = L_{dc2} = \frac{\Delta V}{\Delta I}\Delta t \approx 765\mu H \tag{7}$$

The dc bus capacitance can be increased proportionally for enhanced sag ride-through capability. The isolated dc-dc converter employs open loop PWM control of dc bus voltage. This is because the converter is fed from a well-regulated input rectifier. The waveforms for the converter are shown in Fig. 6 below.

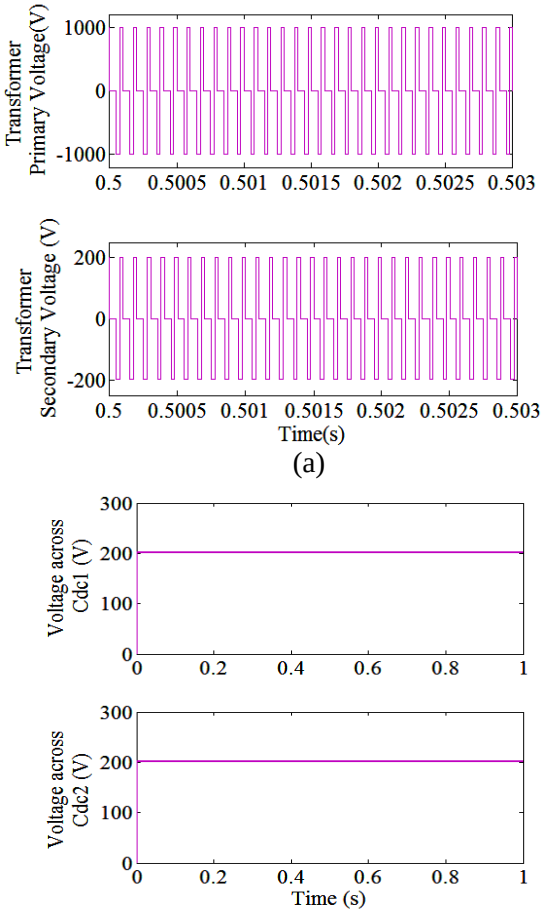


Fig.6 (a) Voltages across primary and secondary of the transformer (b) Output Voltage of DC-DC Converter

2.3 Output Stage

The output of the dc-dc converter is connected to a single phase full bridge inverter designed to produce sinusoidal output voltage with percentage THD below the limits specified by IEEE 519 standards. With 20 kHz switching frequency, 20% inductor current ripple and 1% capacitor voltage ripple, the output filter components are calculated as L_{ac} = 0.5mH and C_{ac} = 7.8μH.

Similar to the input stage converter, the control circuit here is developed based on small signal averaged transfer function model with simple PI control of voltage and current as shown in Fig.7. The current-to-voltage transfer function of the bridge inverter is derived as

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$$\frac{\hat{i}_c(s)}{\hat{V}_o(s)} = \frac{sC_{ac}}{1+s^2L_{ac}C_{ac}+sL_{ac}/Z_L} = G_{inv}(s) \qquad (8)$$

The pole-zero plot of the converter with the designed controller is depicted in Fig.8. It is understood from the figure that the designed controller has roots in the left half of the S-plane thus retaining stability.

The control circuit of the inverter has two loops as shown in Fig.7: the first loop is a fast internal current loop that reduces the percentage THD of the output voltage as well as increases the speed of the response; the second loop is a slow external voltage loop, which provides output voltage regulation. The gain values for the proportional and integral controllers for the current and voltage loops are found using SISOTOOL in MATLAB. The gain values are K_p=10 and K_i=35 for the outer loop and K_p=0.11 and K_i=640 for the inner current loop.

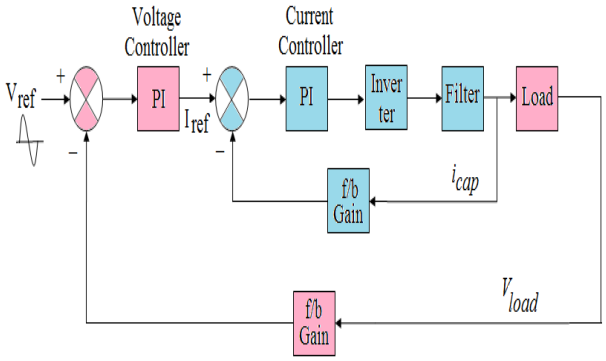


Fig.7 Closed Loop Control Scheme of Inverter

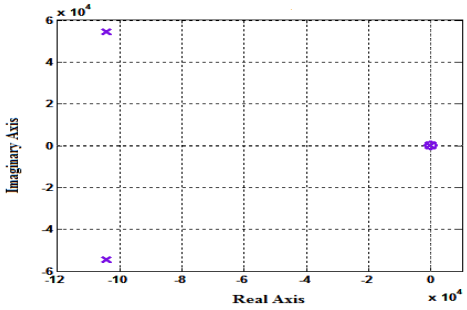


Fig 8. Pole-zero Plot of NPC with the designed controller

The internal current control can be carried out either by sensing the filter inductor current or the filter capacitor current. Here, capacitor current control is adopted to improve the dynamic response of the inverter in addition to lessening the requirement for current sensors.

3. Performance Studies of MITR

Following the design of individual stages, they are integrated into a single entity as MITR and its performance characteristics under various operating conditions are investigated. This calls for a meticulous approach as the output voltages of individual converters get pulled down upon interconnection. The aforementioned issue is resolved by proper tuning of individual controllers so that the need for impedance matching network between stages is eliminated. Also, it is noted that the intermediate dc-dc converter offers desirable performance with open loop control and does not require closed loop tuning thus contributing to percentage reduction in overall cost of the module.

3.1 Estimation of Efficiency

The developed simulation model of MITR is subjected to varying load conditions with reactive component of load held constant at 2kVar and the variation of efficiency for % variation in load from no load to full load is plotted as shown in Fig.9(a). It is found that the MITR has a maximum efficiency of 84.8% at full load.

Conversion Stage	Power Losses (W)	Efficiency (%)
AC-DC	370W	92.6
DC-DC	90W	98.2
DC-AC	330W	93.3

Table 1. Conversion Efficiency of each stage of MITR at Full Load

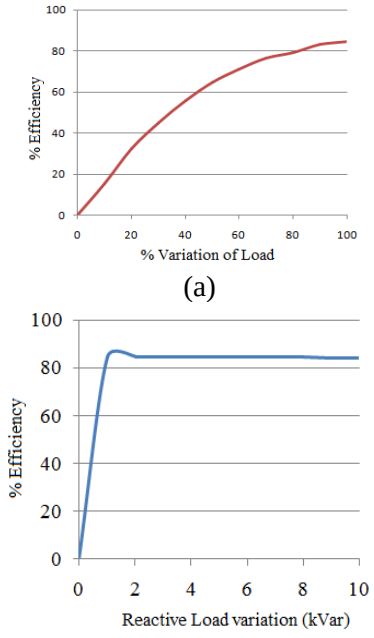


Fig.9 (a) Plot of % Efficiency Vs Load Variation
(b) % Efficiency Vs Reactive Load Variation

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The power losses and conversion efficiency of each stage of MITR are presented in Table 1. The computation of power losses and efficiency for each stage is made by considering the rms values of source and output voltages and currents. For the input and output stages, the input displacement power factor and the output power factor are taken into account for efficiency calculation. At full load, the input displacement power factor is found to be 0.9775 and the output power factor is 0.9856. The plot of % efficiency for variation in reactive component of load is shown in Fig. 9(b).

3.2 Voltage sag, Voltage Swell and outage compensation

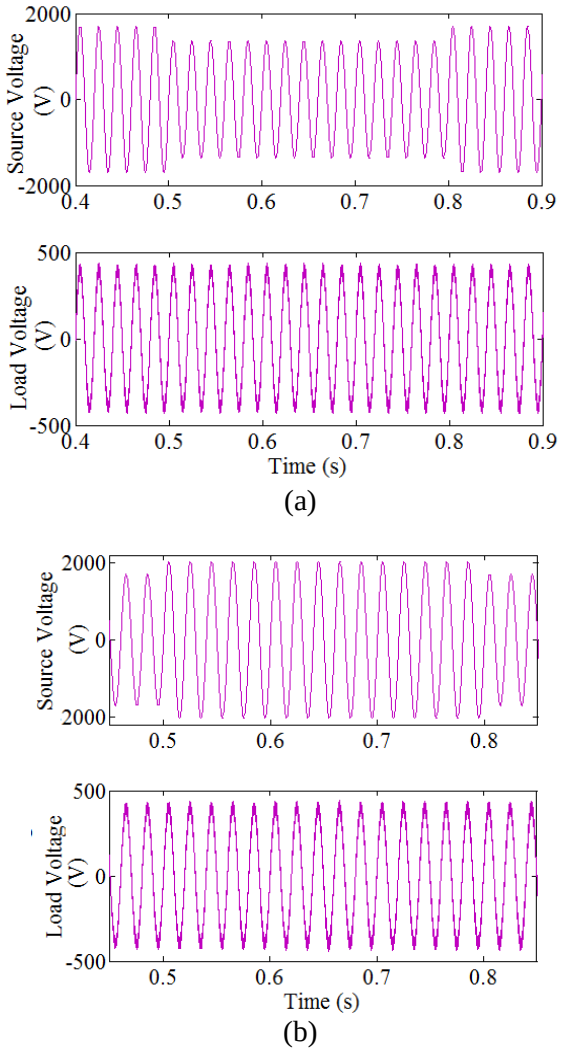


Fig.10 Simulated Source and Load Voltage waveforms with (a) 20% sag and (b) 20% swell

Voltage sag, swell and outage are the common power quality issues experienced in distribution networks. These issues related to quality of distributed power are generally compensated or mitigated to a larger extent by the use of FACTS devices on the utility side or custom power devices on the distribution side which necessitates additional investment on the power system. Nevertheless, MITR provides compensation for all the above mentioned issues at no additional cost. This is possible by designing the MITR with adequate energy storage elements or by increasing the duty cycle of the control voltage.

In the simulation model of MITR, no additional storage elements are used other than the dc bus capacitors on the low and high voltage side. Simulation is carried out with 20% voltage sag and 20% voltage swell for a period of 0.3 seconds and the results are presented in Fig. 10 (a) and (b). It is observed from these figures that the output voltage is not at all affected by the voltage sag and swell conditions.

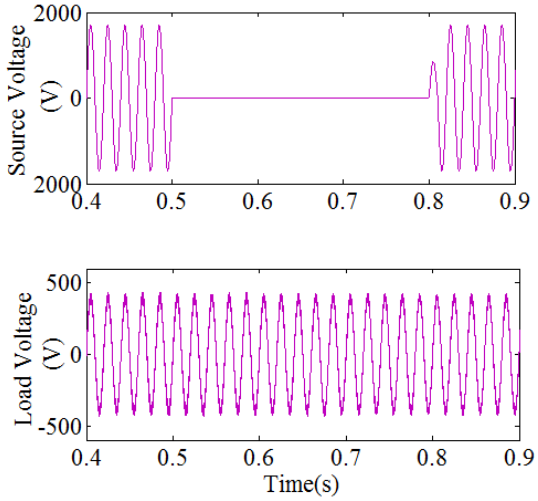


Fig. 11 Simulated Source and Load Voltage waveforms with Outage lasting for 0.3s

Further, the model is subjected to an outage for duration of 0.3s from 0.5s to 0.8s and the result is shown in Fig. 11. It is clear from the figure that the output voltage of MITR remains unchanged for the entire duration of outage.

3.3 Effect of Load Transients

With well-defined closed loop controllers for the input and output stages, the MITR is expected to provide complete isolation between the source and the load. Accordingly, any disturbance on the load side should not affect the source side parameters and vice-versa. The effect of load transients on the performance of MITR is shown in Fig.12.

Here, the output stage of MITR is initially loaded with 50A-rms. A resistive load of 20A-rms is

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applied at 0.5s and a further reactive load of 20A-rms is applied at 0.7s. It is seen that the output voltage is instantly regulated upon application of sudden resistive as well as reactive loads. The source voltage and source current remain undisturbed with the load side disturbance thereby providing better isolation. Also, the source current is in phase with the source voltage thus maintaining unity power factor.

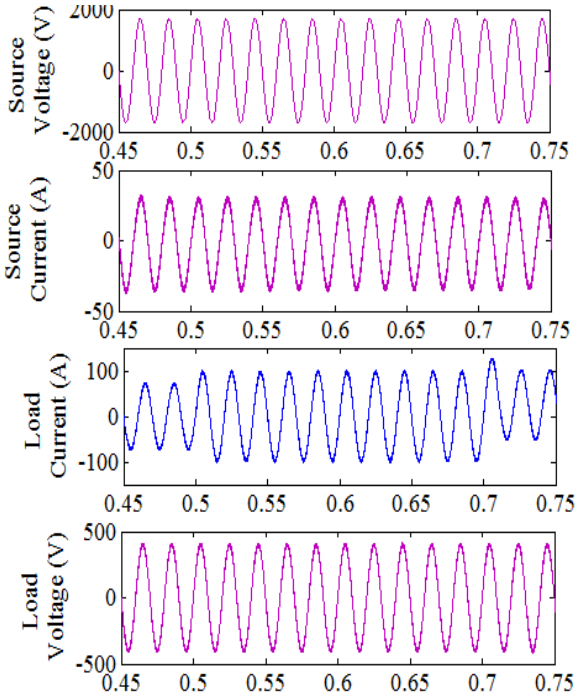


Fig.12 Simulated waveforms under load transients

3.4 Effect of Source voltage variation on output voltage

The developed simulation model of MITR is subjected to ±5% variation in source voltage under full load and its consequence in output voltage expressed as percentage regulation is plotted in Fig.13 (a) below. It is observed from the figure that the MITR shows tight voltage regulation as minimal as 0.11% at full load. Also, the maximum allowable % variation in source voltage without causing distortion in the output voltage for different reactive loads is shown in Fig.13 (b).

3.5 Harmonic Compensation

It is often necessary that the harmonic levels of end-user facility be kept within the limits specified by the International standards on power quality.

According to IEEE 519-1992 standards, the THD level expressed as a measure of effective value of harmonic distortion should be within 5% for voltage levels <69kV.

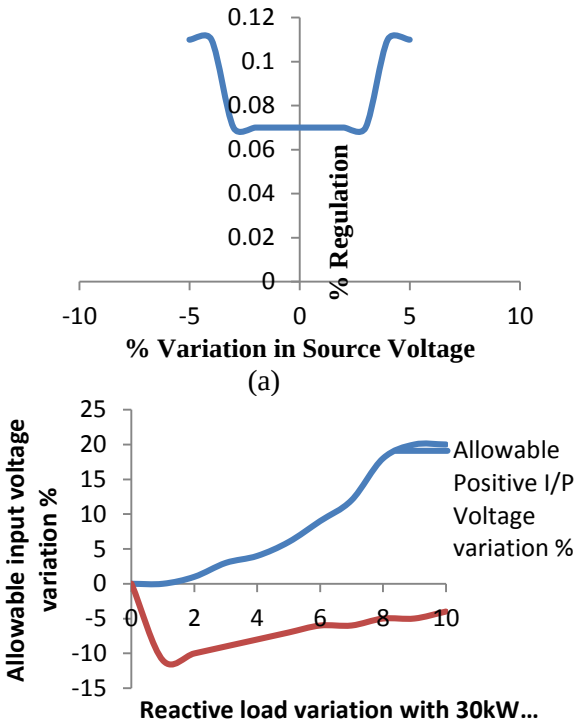


Fig.13 (a) Source Voltage variation Vs % Regulation (b) allowable % input voltage variation for varying reactive load conditions

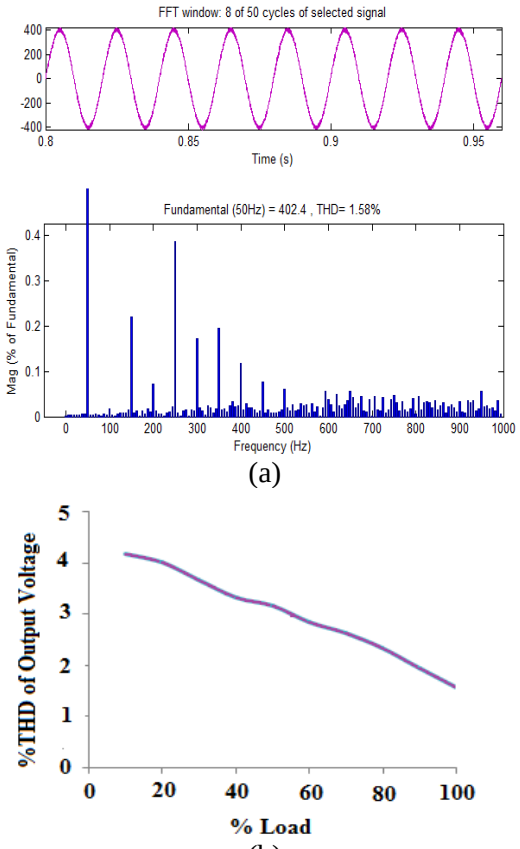


Fig.14 (a) FFT Window for Output Voltage of MITR at Full load (b) %THD variation of Output voltage

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The FFT spectrum of the simulated MITR model at full load is depicted in Fig. 14(a) which shows that the %THD is 1.58 which is well below the limits specified by IEEE standards. A plot of %THD of output voltage for % variation in load from no load to full load is shown in Fig.14 (b). It is clear from the plot that the % THD is less than 5 from no load to full load.

4. Experimental Prototype and Results

A scaled down experimental prototype of 48V, 48VA MITR has been developed to validate the choice of topologies for the three individual stages and to establish stability of interconnection of stages.

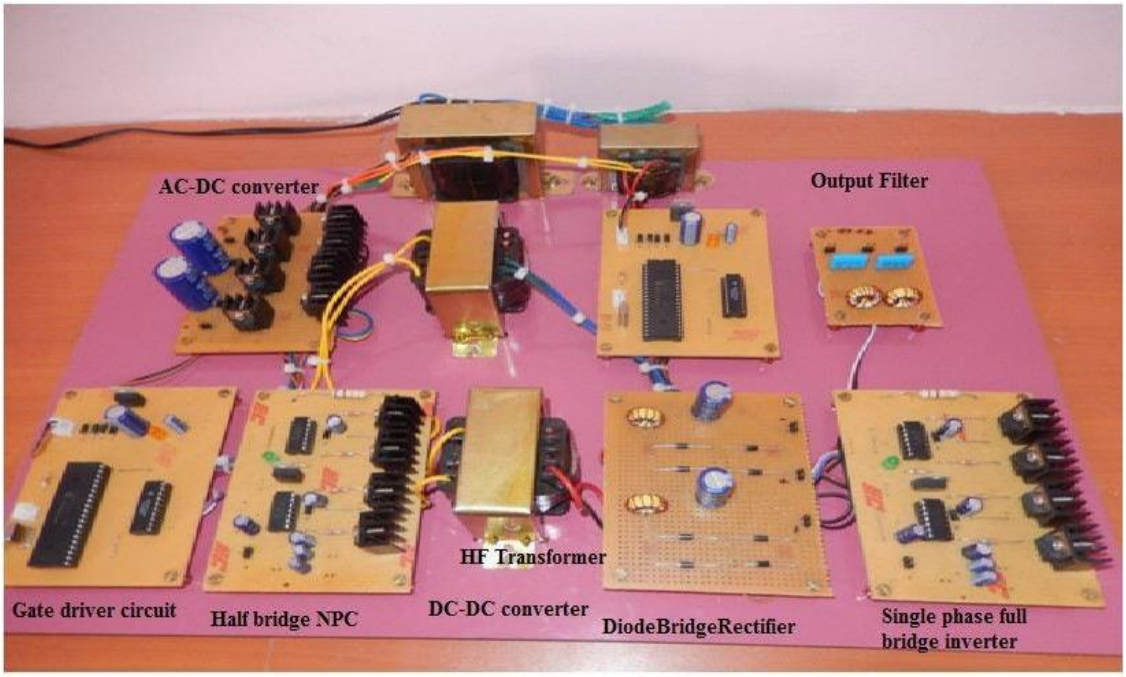


Fig. 15 Experimental Prototype of MITR

Device	Rating
Front End Converter	
Transformer	230/48V, 2A
MOSFET –IRF510	100V, 5.6A, 0.54Ω
Diode – 1N4007	1000V, 1A
Capacitors	63V, 2200µF
Switching Frequency	33kHz
DC-DC Converter	
MOSFET –IRF510	100V, 5.6A, 0.54Ω
Diode – 1N4007	1000V, 1A
Capacitors	450V,22 µF
Isolation Transformer	10kHz, 1:1
Inverter	
MOSFET –IRF510	100V, 5.6A, 0.54Ω
Switching Frequency	33kHz
Others	
Gate Drive IC- FAN7392N	50V,1A
Voltage Regulator IC-7805CT	+5V
AC Filter Capacitors	1 µF
Filter Inductors	1.5mH

Table 2. Ratings of hardware components

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The input stage AC-DC converter circuit is a three level Neutral point clamped converter consisting of eight MOSFET switches, four neutral clamping diodes and two DC bus capacitors. The dc-dc converter comprises of a half-bridge NPC converter connected to the primary of high frequency transformer and a diode bridge circuit connected to the secondary of the transformer. A single phase bridge inverter forms the output stage which is designed to provide 30V alternating current output. The control circuit is implemented using PIC Controller. The hardware setup for the MITR is shown in Fig. 15. The ratings of components for the developed prototype are listed in Table 2.

The results obtained from the prototype are presented in Fig. 16 to 22. The gate pulses to the MOSFET switches of front end converter and the output stage inverter are shown in Fig. 16 and Fig. 17 respectively. For the scaled down prototype, closed loop control is employed only for the output stage inverter and results obtained are satisfactory. However, for real time implementation of the circuit, closed loop control needs to be employed for the front end converter also so that a balanced voltage is obtained across dc link capacitors. The dc-dc converter in the isolation stage need not require closed loop control because it receives a well regulated input voltage from the front end converter. Use of closed loop control for the isolation stage however results in marginal improvement in performance of the converter and hence can be avoided to minimize the overall cost of the product.

The MITR output voltage with open loop inverter control is shown in Fig. 19 and its corresponding THD plot is shown in Fig.20. It is noted that under open loop, the magnitude of output voltage is around 25V and its % THD is 28.15. Nevertheless, closed loop control of inverter shows a better performance with the magnitude of output voltage equal to 29.37Vwhich is close to the desired value and % THD equal to 2.6 which is well below the permissible limits as shown in Fig. 21 & 22.

The performance of the device can further be improved by replacing the conventional power switching devices by more reliable, low loss, high power, high frequency wide band gap devices which are becoming increasingly available in the market today.

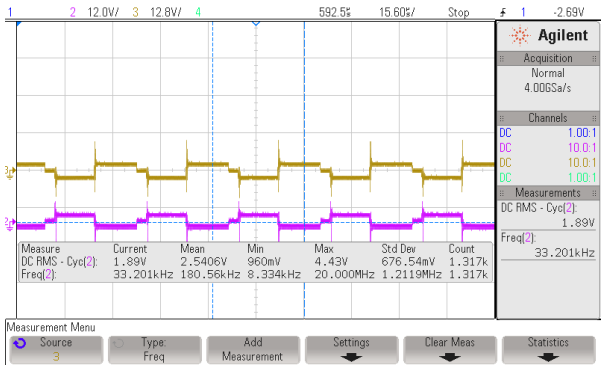


Fig.16 Gate Pulses to Front End Converter

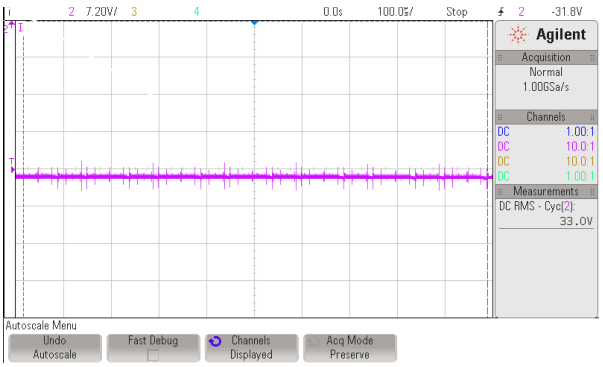


Fig. 18 Output Voltage of DC-DC Converter

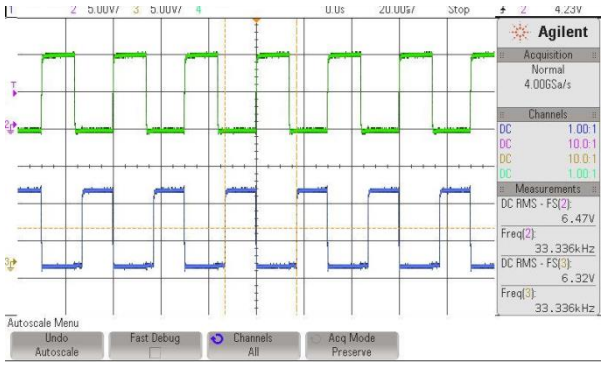


Fig.17 Gate pulses to Inverter

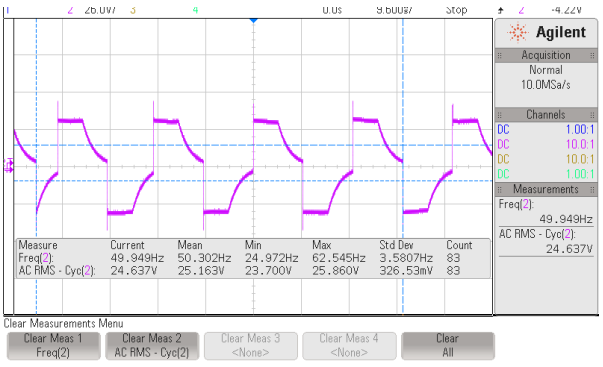


Fig.19 Output Voltage of MITR under open loop

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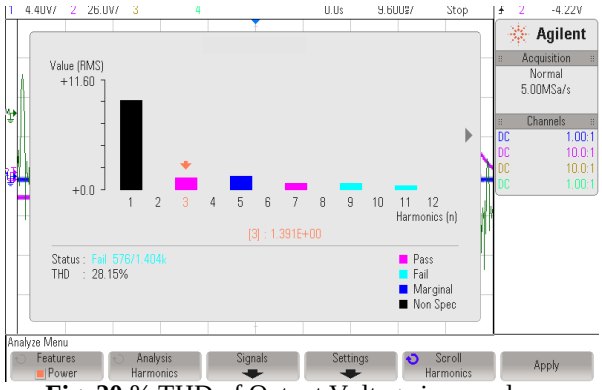


Fig. 20 % THD of Output Voltage in open loop

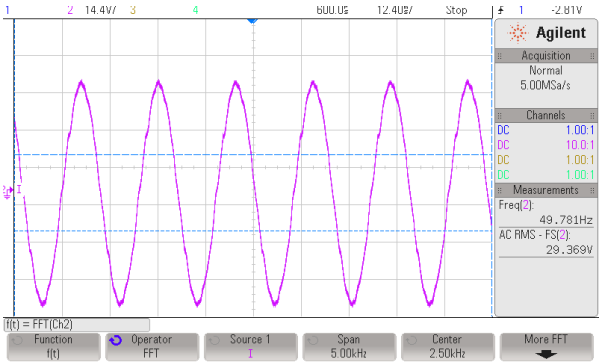


Fig. 21 Output Voltage of MITR with closed loop control for Inverter

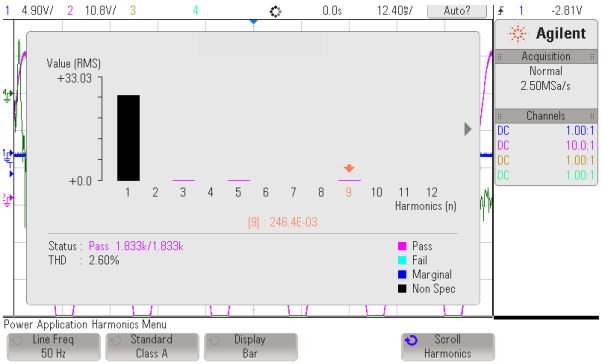


Fig. 22 % THD of output voltage with closed loop control for Inverter

5. Conclusion

With transformers forming key components of power distribution networks, it is essential that these transformers be modernized to match the intelligence associated with future smart grids in controlling power flow across the network. This paper has attempted to develop a Modular Intelligent Transformer (MITR) with very simple and cost- effective control schemes which will help its extensive market penetration in future for low and medium voltage applications. The performance characteristics of MITR are evaluated with a simulation model and a prototype is built to validate the concept.

The benefits of this concept are that, in many cases, regionalized power sources can easily be incorporated into the existing distribution grid without resorting to grid expansion. Thus, a stable grid offering reduced downtimes is guaranteed. Moreover, with the use of new wide band gap devices (SiC, GaN) in place of conventional power semiconductor devices, the MITR can be made substantially lighter, more compact, efficient, environmental friendly, and flexible with better thermal capabilities in comparison to conventional distribution transformers.

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