PLL-Less Adaline-Based Control Of Self Supported DVR For Grid Voltage Distortion And Imbalances

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Abstract: For shielding voltage sensitive loads from diverse power quality problems (Voltage harmonic distortion and voltage sag/swell) a wide variety of custom power devices are used. For the mitigation of above mentioned power quality issue, dynamic voltage restorer (DVR) is widely used custom power device. In this paper, a self-supported dynamic voltage restorer is discussed. The control methodology based on calculation of unit templates is used for dynamic voltage restorer (DVR). PLL-Less Adaline (Adaptive linear element) Artificial Neural Network is used to extract the fundamental component of load voltage and reference load voltage is obtained. The performance of this technique is better than the other existing techniques and it is very simple to implement, less complex, very flexible and robust in nature. In this paper, designing of main system parameters such as VSC-DC link capacitance, ripple filter and AC side inductance is given in detail. The simulation results for voltage harmonic distortion, balanced voltage sag/swell, unbalanced voltage sag/swell, balanced voltage sag/swell with harmonic distortion and unbalanced voltage sag/swell with harmonic distortion shows the viability of DVR controller.

Key words: *dynamic voltage restorer (DVR), voltage sag/swell, total harmonic distortion (THD), power quality, artificial neural network (ANN).*

1. Introduction

A number of power quality problems such as voltage sag/swell, voltage unbalancing and voltage harmonic distortion are reported in literature [1-4] due to the extensive use of power electronics devices, integration of renewable power sources such as wind and solar in the micro-grid and occurrence of various types of faults on the distribution network. Many sensitive loads such as medical equipment, communication networks, semiconductor industries, computer loads etc are extremely sensitive towards the power quality problems. Thus the custom power devices for the betterment of above mentioned power quality problems are widely used. Basically three categories of custom power devices exist, which can be categorized on their respective functionality. For the mitigation of current quality problems, a shunt connected device called Distributed Static Synchronous Compensator (D-STATCOM) [5-6] is used, whereas a series connected device namely DVR [8-9] is used for the rectification of voltage quality problems. Further, in certain situations where mitigation of both current as well as voltage quality is required, unified power quality conditioner (UPQC) [7] is applied. DVR is connected between the load and supply via the injection transformer. It can protect the voltage sensitive loads by mitigating various power quality problems.

There are many types of DVR topologies discussed in the literature [10]. Many types of voltage injection methods [11] are discussed. In [12-18], various types of control strategies are discussed for controlling of DVR. Some of the famous control strategies are Adaline based fundamental extraction, space vector modulation, energy optimized control and synchronous reference frame theory

Singh et.al [11] have demonstrated and implemented the DVR based on calculation of unit templates and synchronous reference frame (SRF) theory is used for extraction the fundamental of terminal voltage. In SRF theory based fundamental extraction, there is use of phase locked loop (PLL) block which is very difficult to design in real time implementation.

Singh et.al [12] have implemented the DVR based on unit templates calculations and fundamental of terminal voltage is extracted using artificial neural network (ANN) theory. But in this theory, the extraction of unit three phase voltage vectors is done by using complex PLL. But the real time implementation of PLL is really a difficult task.

In this paper, for the controlling of DVR, control algorithm based on calculation of unit templates is used and fundamental of terminal voltage is extracted using PLL-Less adaline artificial neural network (ANN). Unit templates based extraction of unit voltage vectors is adopted to replace complex PLL block.

The working of the proposed controller is found suitable to handle various types of power quality problems at the source side such as balanced voltage sag/swell, unbalanced voltage sag/swell, voltage harmonic distortion, balanced voltage sag/swell with harmonic distortion and unbalanced voltage sag/swell with harmonic distortion.

The main contributions of this paper are:

1. PLL-Less adaline artificial neural network (ANN) based extraction of fundamental voltage is used for DVR, which is not reported in literature.
2. In this paper, complex PLL block for the calculation of unit three phase voltage vectors is replaced by very simple calculation of unit templates approach which makes the system less complex and is very easily implemented in the hardware.
3. Maintaining the stability of the system with various types of power quality problems such as balanced voltage sag/swell, unbalanced voltage sag/swell, voltage harmonic distortion, balanced voltage sag/swell with harmonic distortion and unbalanced voltage sag/swell with harmonic distortion.

The schematic diagram of self-supported DVR is shown in Fig. 1. The main components of DVR are 3-Phase programmable voltage source, injection transformer, IGBT based VSC, ripple filter and DC link capacitance.

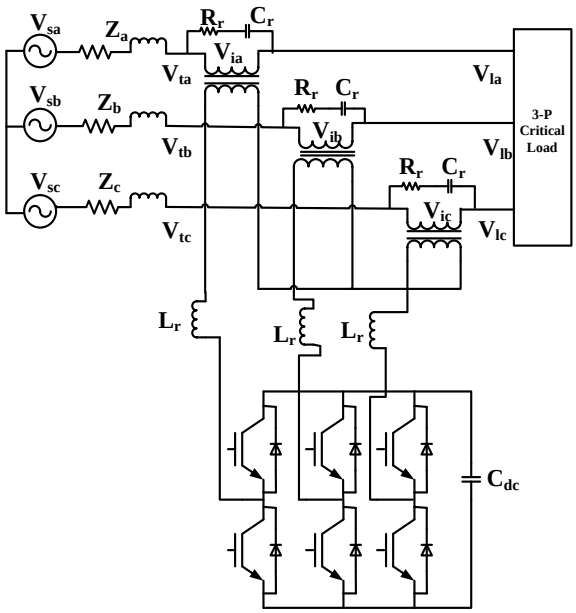


Fig. 1. Schematic outline of self supported DVR

2. Design of proposed configuration

The proposed system for DVR comprises of 3-Phase programmable voltage source, insulated gate bipolar transistor (IGBT) based VSC, ripple filter, injection transformer and three-phase linear lagging load. The system components to be designed are ripple filter, AC side inductance and DC link capacitance. The data for the system are given in Table 1.

2.1. Design of VSC DC link capacitance

Proper functioning of VSC depends upon the appropriate value of DC link capacitance for better regularization of load voltage during various power quality problems. During sag as well as swell, DC side capacitor supplies or absorbs the power to maintain the load voltage constant. So the value of capacitance can be calculated as [19,20],

$$\frac{1}{2} \times C_{dc}(V_{dc}^2 - V_{dco}^2) = nST \qquad (1)$$

$$\frac{1}{2} \times C_{dc}(300^2 - 297^2) = 0.1 \times 10000 \times .0042$$

$$C_{dc} \cong 4690\mu F$$

where, n=0.1 is the time taken by controller to regulate DC link voltage, S= 10 kVA shows the maximum load rating, T is the system time period, V_{dc}= 300V (DC link voltage) and V_{dco}= 297 shows the maximum change in DC link voltage during various power quality problems at source side. C_{dc} is calculated to be $4690\mu F$ and by further iteration, value of C_{dc} is taken to be $4700\mu F$(standard value).

2.2. Design of ripple filter

VSC switching frequency is used to design ripple filter [21-22]. Basically, ripple filter is designed to address the switching harmonics in VSC output voltage. It is a first order high pass filter whose RC time constant should be less than or equal to the time period at fundamental switching frequency as,

$$R_r \times C_r \leq T_s \qquad (2)$$

where switching time, $T_s = 1/f_s$ and f_s is the switching frequency (10 kHz), So the equation can be written as,

$$R_r \times C_r = \frac{1}{f_s} \qquad (3)$$

Let us take R_s = 2 **Ω** then the value of C can be calculated as,

$$2 \times C_r \leq \frac{1}{10000}$$

$$C_r \cong 50\mu F$$

2.3. Design of AC side inductor

AC side inductor can be designed as [21,22]

$$L_r = \frac{\sqrt{3} m V_{dc}}{12\, h\, f_s\, \Delta i} \quad (4)$$

$$L_r = \frac{\sqrt{3} \times 1 \times 300}{12 \times 1.2 \times 10000 \times 1.8} \cong 2.0046\, mH$$

where, V_{dc}= 300V (DC link voltage), m=1 (modulation index), overloading factor (h) =1.2, switching frequency (f_s) = 10 kHz and Δi = 2% of peak current. L_r is calculated to be 2.0046mH and by further iteration, the value of L_r is taken to be 2mH.

System Parameters	Data
Line Voltage	415V, 50 Hz
Line impedance	R_s = 0.01Ω, L_s = 3.5mH
DC link voltage	V_{DC}= 300V
DC link Capacitance	C_{DC}= 4700 µF
Ripple Filter	C_r = 52 µF, R_r = 2Ω
AC Side Inductance	L_r = 2mH
Injection Transformer	10 KVA, 200V/300V
PWM switching frequency	f_s = 10 kHz
Load	0.8pf lagging, 10KVA

Table 1 System parameters for simulation

3. Proposed control algorithm

Fig. 2 displays the fundamental block diagram of adopted control scheme. It is based on calculation of unit templates and adaline artificial neural network (ANN). Unit templates based extraction of unit three phase voltage vectors for extracting the fundamental components of voltage is adopted to replace complex PLL block. In this algorithm two PI controllers are used, VSC DC link voltage is maintained constant by using first PI controller and another PI controller is utilized to regulate the load voltage. The error between the reference DC link voltage and actual DC link voltage is processed by the first PI controller. Output of this PI controller is multiplied with the in-phase unit voltage vectors to generate the in-phase component of reference load voltage. The error between the actual load voltage and reference load voltage is processed by the second PI controller.

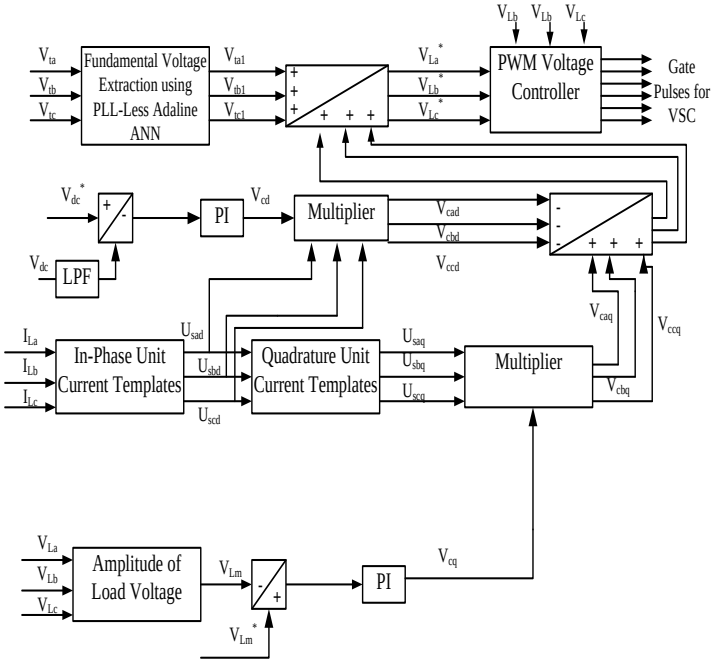


Fig. 2 Proposed control Algorithm

Output of this PI controller is multiplied with the quadrature unit voltage vectors to generate the quadrature component of reference load voltage and finally generating the gating pulses for the switching of IGBT based VSC.

3.1. Estimation of amplitude of load voltage, amplitude of load current and unit templates

The amplitude of load voltage (V_{Lm}) can be calculated from the sensed three phase load voltages as,

$$V_{Lm} = \sqrt{\frac{2}{3}}(V_{La}^2 + V_{Lb}^2 + V_{Lc}^2) \quad (5)$$

The amplitude of load current (I_{Lm}) can be calculated from the sensed three phase load currents as,

$$I_{Lm} = \sqrt{\frac{2}{3}}(I_{La}^2 + I_{Lb}^2 + I_{Lc}^2) \quad (6)$$

The in-phase unit voltage vectors can be calculated as,

$$I_{La} = \sin\theta, I_{Lb} = \sin(\theta - \frac{2\pi}{3}), I_{Lc} = \sin(\theta - \frac{4\pi}{3}) \quad (7)$$

$$U_{sad} = \frac{I_{La}}{I_{Lm}}, U_{sbd} = \frac{I_{Lb}}{I_{Lm}}, U_{scd} = \frac{I_{Lc}}{I_{Lm}} \quad (8)$$

Moreover, the in-phase unit voltage vectors can be used to calculate the quadrature unit voltage vectors as,

$$U_{saq} = \frac{-U_{sbd} + U_{scd}}{\sqrt{3}}$$

$$U_{sbq} = \frac{3U_{sad} + U_{sbd} - U_{scd}}{2\sqrt{3}}$$

$$U_{scq} = \frac{-3U_{sad} + U_{sbd} - U_{scd}}{2\sqrt{3}} \quad (9)$$

3.2. Estimation of in-phase component of reference load voltage

The amplitude of sensed DC link (V_{dc}) voltage is compared with the reference DC link voltage (V_{dc}^{*}) at k^{th} sample of time to generate error signal as,

$$V_{e(k)} = V_{dc(k)}^{*} - V_{dc(k)} \quad (10)$$

To compensate this error signal ($V_{e(k)}$), a PI controller is used. The output of this PI controller gives the in-phase component $V_{cd(k)}$ at k^{th} sample of time.

So the in-phase component of reference load voltage can be calculated as,

$$V_{cad} = V_{cd} \times U_{sad}, V_{cbd} = V_{cd} \times U_{sbd}, \quad V_{ccd} = V_{cd} \times U_{scd} \quad (11)$$

3.3. Estimation of quadrature component of reference load voltage

The amplitude of load terminal voltage (V_{Lm}) is estimated in eq (5). Now the estimated load terminal voltage (V_{Lm}) is compared with the reference value (V_{Lm}^{*}) to generate the error signal at k^{th} sample of time as,

$$V_{e(k)} = V_{Lm(k)}^{*} - V_{Lm(k)} \quad (12)$$

To compensate this error signal ($V_{e(k)}$), a PI controller is used. The output of this PI controller gives the quadrature component $V_{cq(k)}$ at k^{th} sample of time.

So the quadrature component of reference load voltage can be calculated as,

$$V_{caq} = V_{cq} \times U_{saq}, V_{cbq} = V_{cq} \times U_{sbq}, \quad V_{ccq} = V_{cq} \times U_{scq} \quad (13)$$

3.4. Extraction of fundamental positive sequence component of terminal voltage by using PLL-Less Artificial Neural Network

ANN based on least mean square (LMS) is used for the extraction of balanced positive sequence fundamental frequency component of terminal voltage (V_{ta1}, V_{tb1}, V_{tc1}). Basically in the ANN control algorithm as shown in fig. 3, there is a need of the extraction of component vector in-phase with the unit vector templates. Terminal voltages (V_{ta}, V_{tb}, V_{tc}) are utilized to generate unit vector templates (U_{pa}, U_{pb}, U_{pc}). Many authors [11,12] use the complex PLL block to generate the unit vector templates. But in this work basic unit templates theory is used to generate the in-phase unit vector templates. The positive sequence voltage is extracted from the sensed terminal voltage to avoid the effect of voltage imbalance and harmonics as,

$$\begin{bmatrix} V_{Pa} \\ V_{Pb} \\ V_{Pc} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & a^2 & a \\ a & 1 & a^2 \\ a^2 & a & 1 \end{bmatrix} \begin{bmatrix} V_{ta} \\ V_{tb} \\ V_{tc} \end{bmatrix} \quad (14)$$

Where, a = $1 \angle 120^0$ and $a^2 = 1 \angle 240^0$

Amplitude of terminal voltage and in-phase unit vectors are calculated as,

$$V_t = \sqrt{\frac{2}{3}}(V_{pa}^2 + V_{pb}^2 + V_{pc}^2) \quad (15)$$

$$U_{pa} = \frac{V_{pa}}{V_t}, U_{pb} = \frac{V_{pb}}{V_t}, U_{pc} = \frac{V_{pc}}{V_t} \quad (16)$$

These in-phase unit vectors are used to synchronize the obtained weights (W_{pa}, W_{pb}, W_{pc}) with the phase of supply voltage to obtain the error signals ($e_{a(n)}$, $e_{b(n)}$, $e_{c(n)}$).

Estimation of weights for each weights is calculated as,

$$W_{pa(n+1)} = W_{p(n)} + e_{a(n)}U_{pa(n)} \quad (17)$$

$$W_{pb(n+1)} = W_{p(n)} + e_{b(n)}U_{pb(n)} \quad (18)$$

$$W_{pc(n+1)} = W_{p(n)} + e_{c(n)}U_{pc(n)} \quad (19)$$

where,

$$e_{a(n)} = \mu[V_{ta(n)} - W_{p(n)}U_{pa(n)}] \quad (20)$$

$$e_{b(n)} = \mu[V_{tb(n)} - W_{p(n)}U_{pb(n)}] \quad (21)$$

$$e_{c(n)} = \mu[V_{tc(n)} - W_{p(n)}U_{pc(n)}] \quad (22)$$

where, μ is the convergence factor or the adaptive constant. It decides the convergence speed as well as accuracy of estimation. The value of μ lies between 0 to 1 but in this application μ is taken to be 0.2. The average weight is calculated as,

$$W_p = \frac{W_{pa} + W_{pb} + W_{pc}}{3} \quad (23)$$

Finally fundamental of terminal voltage of each phase can be calculated as,

$$V_{ta1} = W_p * U_{pa} \quad (24)$$

$$V_{tb1} = W_p * U_{pb} \quad (25)$$

$$V_{tc1} = W_p * U_{pc} \quad (26)$$

3.5. Estimation of reference load voltages

The reference load voltage can be calculated by using in-phase component and quadrature component of reference load voltage and positive sequence component of terminal voltage as,

$$V_{La}^* = V_{caq} - V_{cad} + V_{ta1} \quad (27)$$

$$V_{Lb}^* = V_{cbq} - V_{cbd} + V_{tb1} \quad (28)$$

$$V_{Lc}^* = V_{ccq} - V_{ccd} + V_{tc1} \quad (29)$$

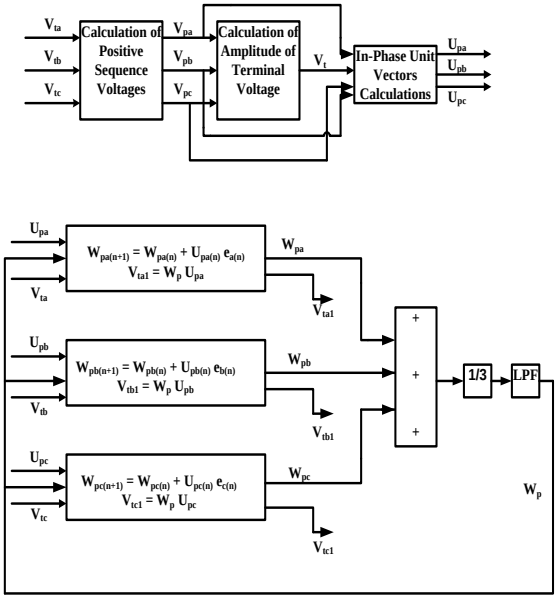


Fig.3 ANN based Control Algorithm

3.6. Generation of control pulses using PWM controller

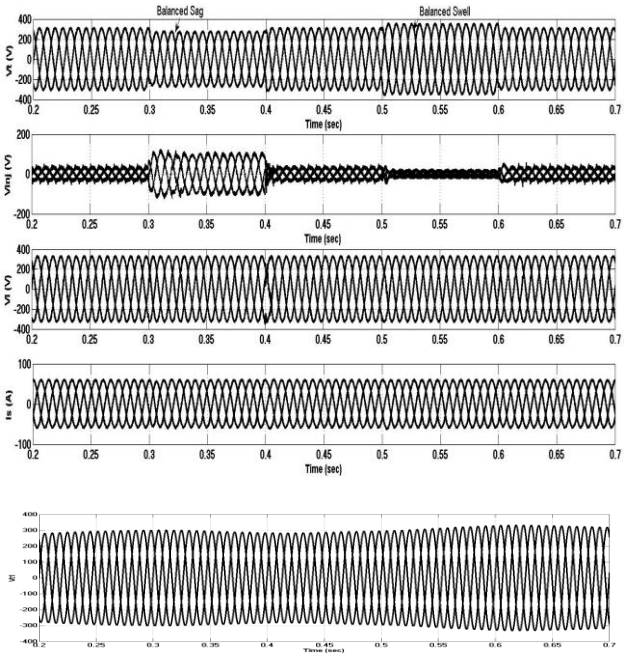
The error voltage signal is generated from the difference between the reference load voltage ($V_{La}^*, V_{Lb}^*, V_{Lc}^*$) and sensed load voltage (V_{La}, V_{Lb}, V_{Lc}). This error signal is passed through the pulse width modulation (PWM) controller to generate the gating signals of IGBT's of voltage source converter (VSC) of DVR.

4. Performance investigation

The DVR system is modeled, designed and simulated by using MATLAB/Simulink & SimPowerSystems environment. Moreover, the components of the system such as DC link capacitance, AC side inductance and ripple filter are designed in detail [19-22]. All the system parameters are given in table 1. The reference load voltages for VSC of DVR are generated from sensed load voltage (V_{La}, V_{Lb}, V_{Lc}), sensed source terminal voltage (V_{ta}, V_{tb}, V_{tc}) and load current (I_{La}, I_{Lb}, I_{Lc}). Performance of the designed system is evaluated for distinct power quality issues at source side like balanced as well as unbalanced voltage sag/swell, voltage harmonics distortion, and balanced as well as unbalanced voltage sag/swell with harmonics distortion.

4.1. Performance under balanced voltage sag/swell condition

Balanced voltage sag (15% of phase voltage) is introduced in the system at 0.3s and balanced voltage swell (15% of phase voltage) is introduced in the system at 0.5s for the duration of 5 cycles each. At the time of any disturbance (Voltage sag/swell), DVR will use the reactive power to maintain the load voltage constant. Source terminal voltage (V_t), DVR injected voltage (V_{inj}), load voltage(V_L), source current (I_s), ANN based extraction of fundamental voltage (V_{t1}), DC bus voltage (V_{dc}) and amplitude of source and load voltage (V_{tm}, V_{lm}) are depicted in Fig. 4.



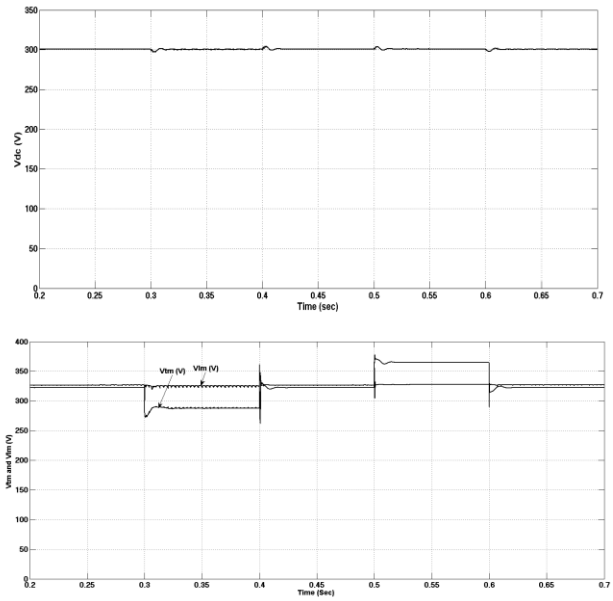


Fig. 4. Waveforms during balanced voltage sag and balanced voltage swell condition **(**a) Source terminal voltage V_t **(**b) injected voltage V_{inj} **(**c) Load voltage V_L **(**d) Source current I_s (e) ANN based extraction of fundamental voltage (V_{t1}) (f) DC bus voltage (V_{dc}) (g) Amplitude of source and load voltage (V_{tm}, V_{lm})

4.2. Performance under unbalanced voltage sag/swell condition

Unbalanced voltage sag (15% sag in phase A and 20% sag in phase B) is introduced in the system at 0.3s and unbalanced voltage swell (15% swell in phase A and 20% swell in phase B) is introduced in the system at 0.5s for the duration of 5 cycles. At the time of any disturbance (unbalanced voltage sag/swell), DVR will use the reactive power to regulate the load voltage. Source terminal voltage (V_t), DVR injected voltage (V_{inj}), load voltage(V_{L}), source current (I_s), ANN based extraction of fundamental voltage (V_{t1}), dc bus voltage (V_{dc}) and amplitude of source and load voltage (V_{tm}, V_{lm}) are depicted in Fig. 5.

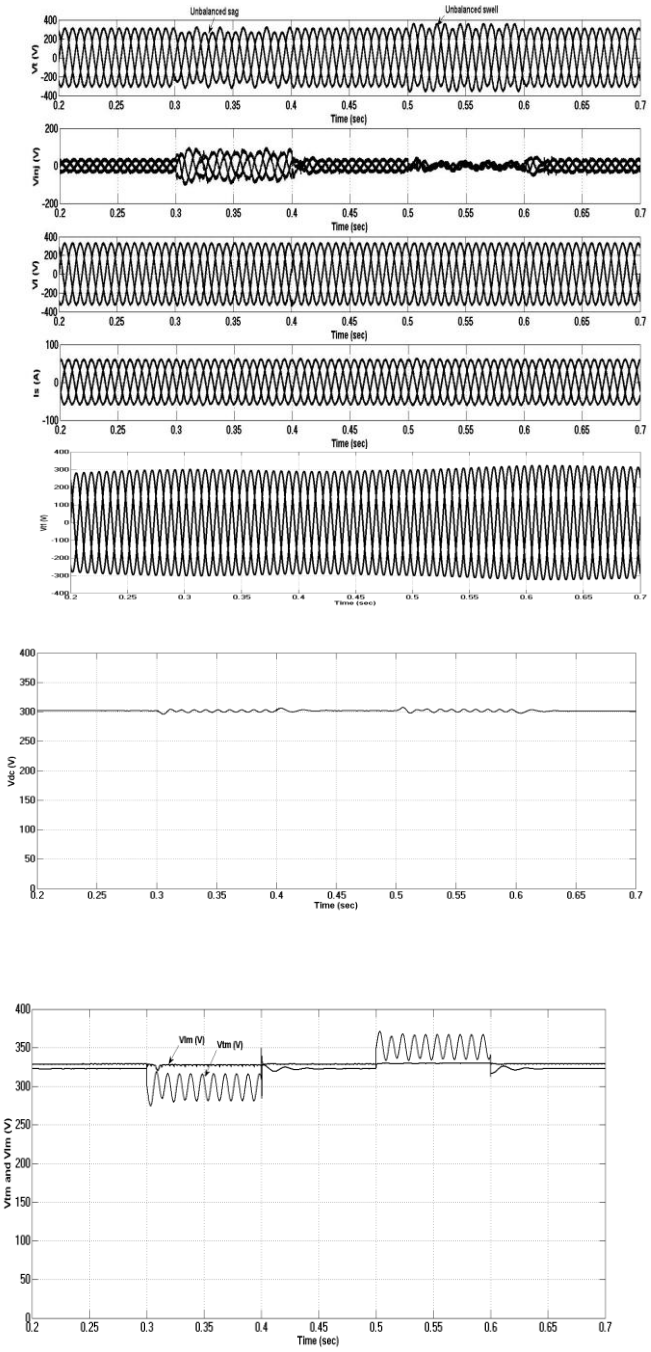


Fig. 5. Waveforms during unbalanced voltage sag and balanced voltage swell condition **(**a) Source terminal voltage V_t **(**b) injected voltage V_{inj} **(**c) Load voltage V_L **(**d) Source current I_s (e) ANN based extraction of fundamental voltage (V_{t1}) (f) DC bus voltage (V_{dc}) (g) Amplitude of source and load voltage (V_{tm}, V_{lm})

4.3. Performance under voltage harmonic distortion

5th (20%) and 7th (14%) harmonics distortion is inserted in the supply voltage by the programmable voltage source in all the three phases. DVR injects proper amount of

compensation voltage to regulate the load voltage and make it sinusoidal in nature. Source terminal voltage (V_t), DVR injected voltage (V_{inj}), load voltage(V_L), source current (I_s), ANN based extraction of fundamental voltage (V_{t1}), DC bus voltage (V_{dc}) and amplitude of source and load voltage (V_{tm}, V_{lm}) are depicted in Fig. 6. The total harmonic distortion (THD) is 26.91% in the supply voltage (Fig. 7). THD in load voltage is only 1.09% (Fig. 8) and only 0.22% (Fig. 9) in the source current after the excellent performance by DVR.

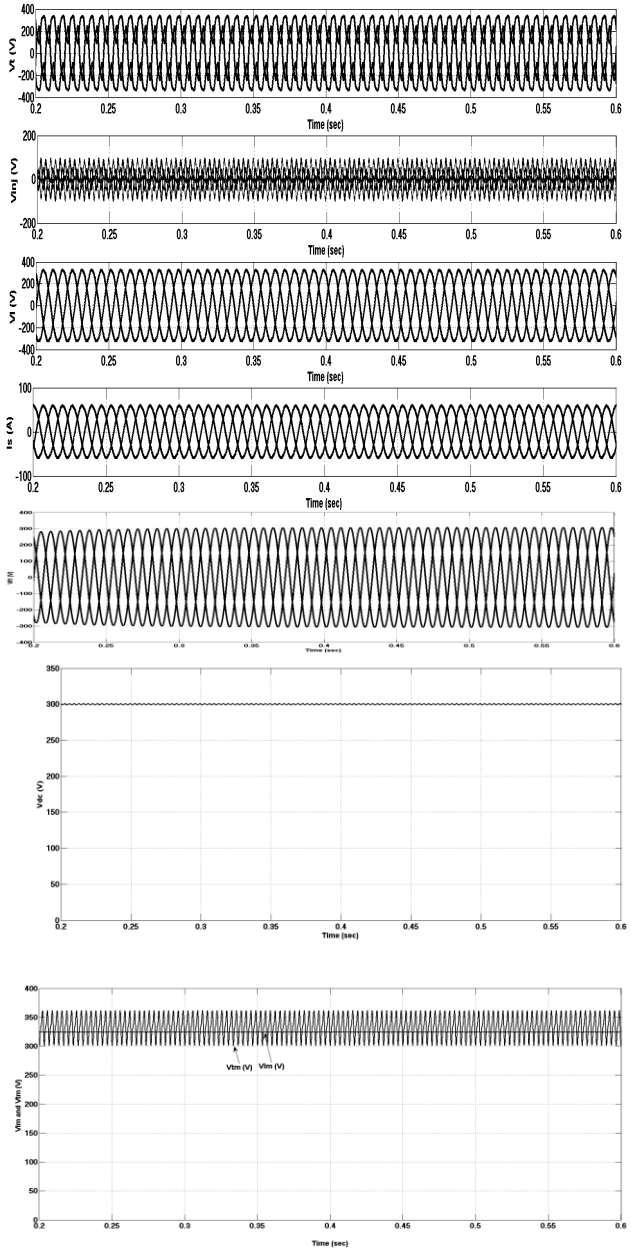


Fig. 6. Waveforms under voltage harmonic distortion **(**a) Source terminal voltage V_t **(**b) injected voltage V_{inj} **(**c) Load voltage V_L **(**d) Source current I_s (e) ANN based extraction of fundamental voltage (V_{t1}) (f) DC bus voltage (V_{dc}) (g) Amplitude of source and load voltage (V_{tm}, V_{lm})

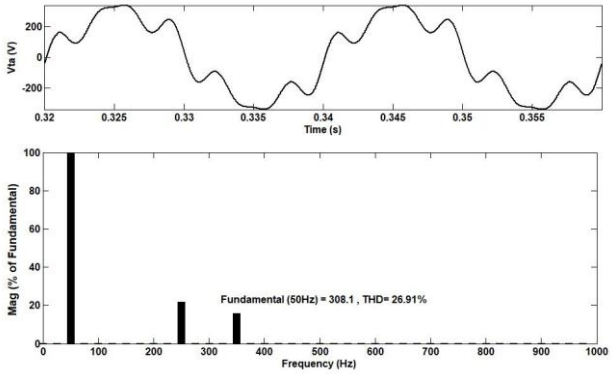


Fig. 7. Source terminal voltage and harmonic spectrum

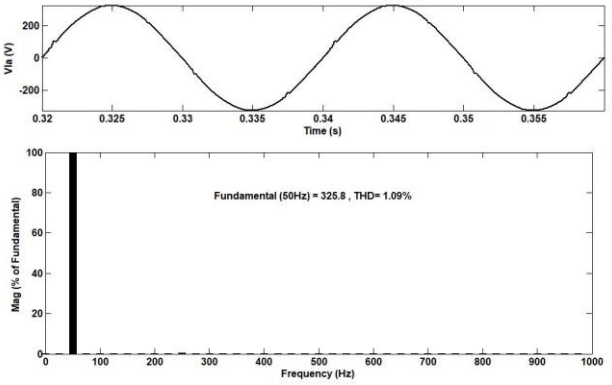


Fig. 8. Load voltage and harmonic spectrum

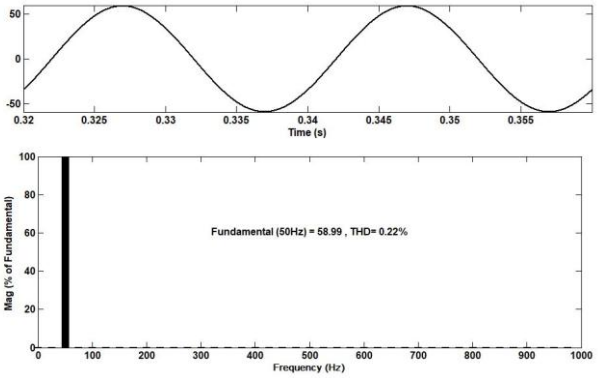
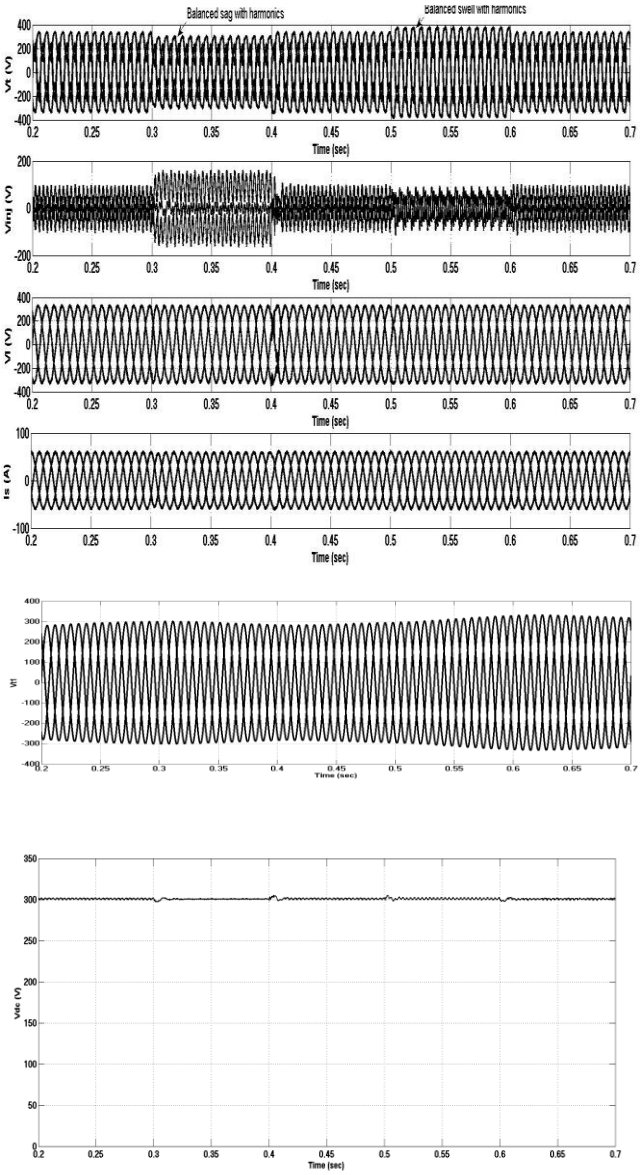


Fig. 9. Source current and harmonic spectrum

4.4. Performance under balanced voltage sag/swell with harmonic distortion

Balanced voltage sag (15% of phase voltage) is introduced in the system at 0.3s and balanced voltage swell (15% of phase voltage) is introduced in the system at 0.5s for the duration of 5 cycles and also the 5th (20%) as well as 7th (14%) harmonics distortion is inserted in the supply voltage by the programmable voltage source in all the three phases. At the time of any disturbance (Voltage sag/swell with harmonic distortion), DVR will use the reactive power to maintain the load voltage constant and sinusoidal in nature.

Source terminal voltage (V_t), DVR injected voltage (V_{inj}), load voltage(V_L), source current (I_s), ANN based extraction of fundamental voltage (V_{t1}), DC bus voltage (V_{dc}) and amplitude of source and load voltage (V_{tm}, V_{lm}) are depicted in Fig. 10. The total harmonic distortion (THD) is 30.61% in the supply voltage (Fig. 11). THD in load voltage is only 1.39% (Fig. 12) and only 0.46% (Fig. 13) in the source current after the excellent performance by DVR.



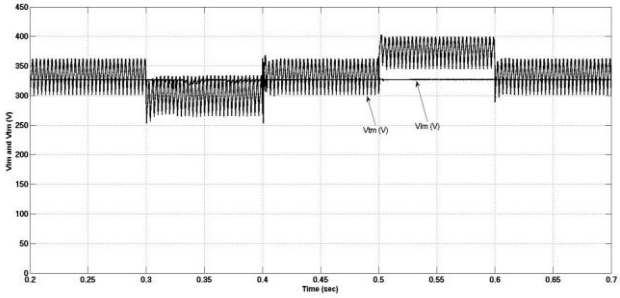


Fig. 10 Waveforms during balanced voltage sag/swell with harmonic distortion **(**a) Source terminal voltage V_t **(**b) injected voltage V_{inj} **(**c) Load voltage V_L **(**d) Source current I_s (e) ANN based extraction of fundamental voltage (V_{t1}) (f) DC bus voltage (V_{dc}) (g) Amplitude of source and load voltage (V_{tm}, V_{lm})

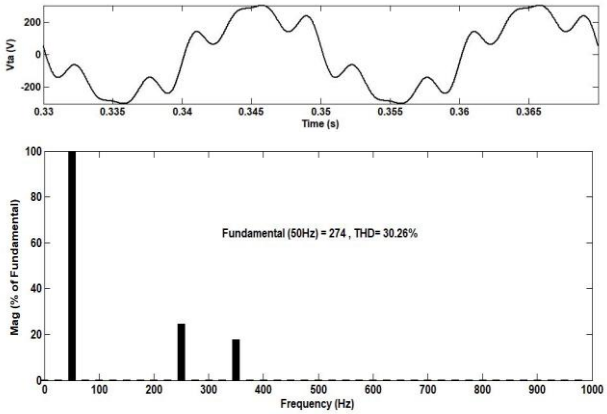


Fig. 11. Source terminal voltage and harmonic spectrum

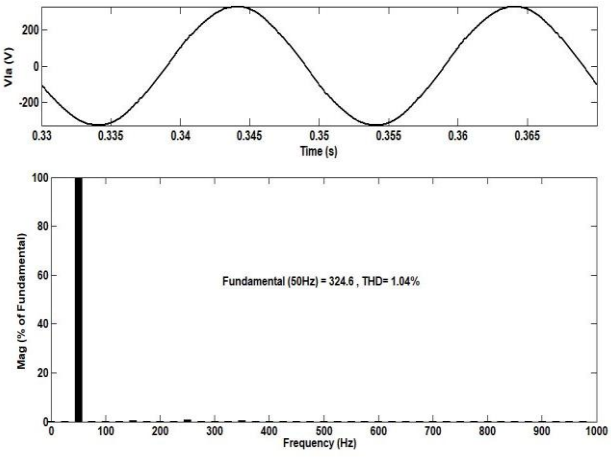
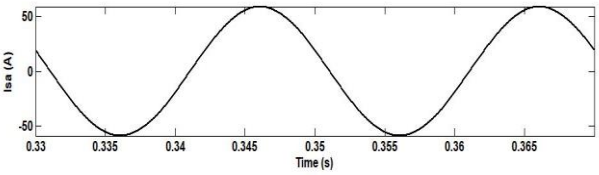


Fig. 12. Load voltage and harmonic spectrum



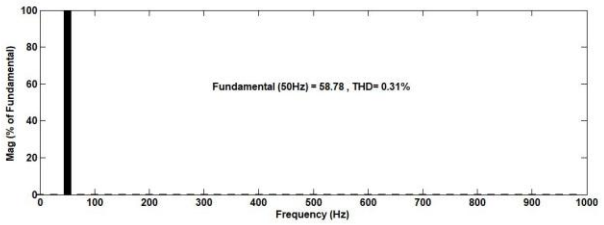
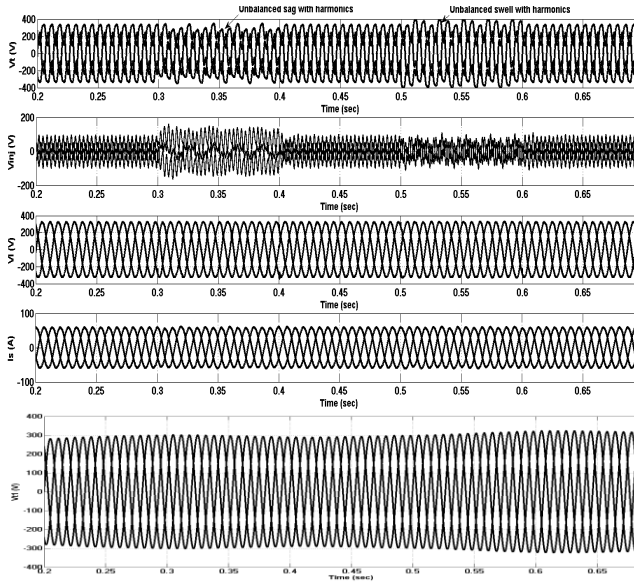


Fig. 13. Source current and harmonic spectrum

4.5. Performance under unbalanced voltage sag/swell with harmonic distortion

An unbalanced voltage sag (15% sag in phase A and 20% sag in phase B) is introduced in the system at 0.3s and unbalanced voltage swell (15% swell in phase A and 20% swell in phase B) is introduced in the system at 0.5s for the duration of 5 cycles and also the 5th (20%) as well as 7th (14%) harmonics distortion is inserted in the supply voltage by the programmable voltage source in all the three phases. At the time of any disturbance (unbalanced voltage sag/swell with harmonic distortion), DVR will use the reactive power to maintain the load voltage constant and sinusoidal in nature. Source terminal voltage (V_t), DVR injected voltage (V_{inj}), load voltage(V_L), source current (I_s), ANN based extraction of fundamental voltage (V_{t1}), DC bus voltage (V_{dc}) and amplitude of source and load voltage (V_{tm}, V_{lm}) are depicted in Fig 14. The total harmonic distortion (THD) is 30.86% in the supply voltage (Fig. 15). THD in load voltage is only 1.68% (Fig. 16) and only 0.94% (Fig. 17) in the source current after the excellent performance by DVR.



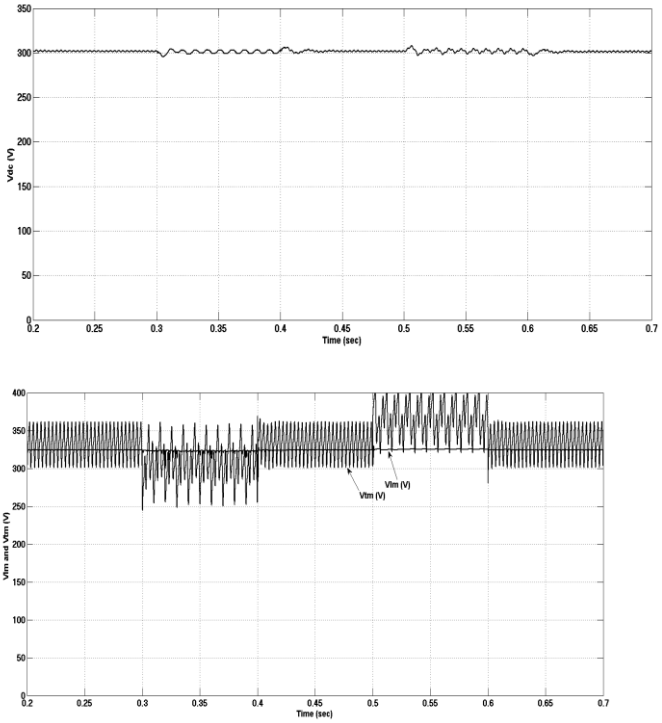


Fig. 14. Waveforms during unbalanced voltage sag/swell with harmonic distortion **(**a) Source terminal voltage V_t **(**b) injected voltage V_{inj} **(**c) Load voltage V_L **(**d) Source current I_s (e) ANN based extraction of fundamental voltage (V_{t1}) (f) DC bus voltage (V_{dc}) (g) Amplitude of source and load voltage (V_{tm}, V_{lm})

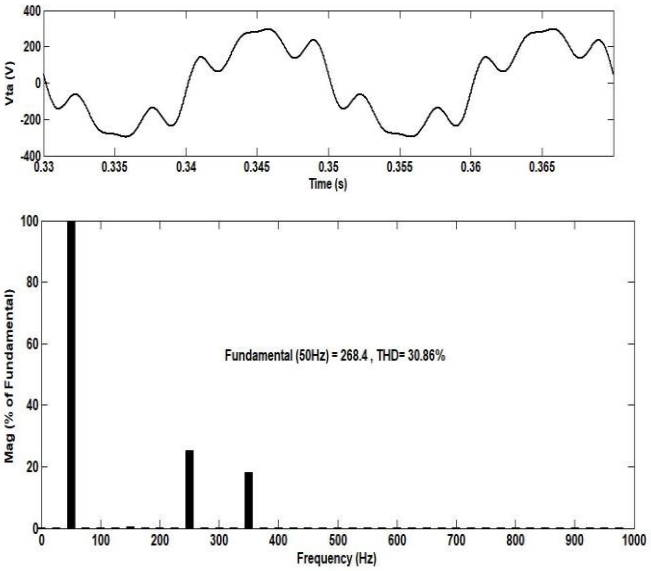
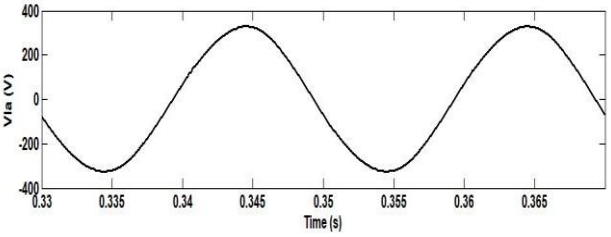


Fig. 15. Source terminal voltage and harmonic spectrum



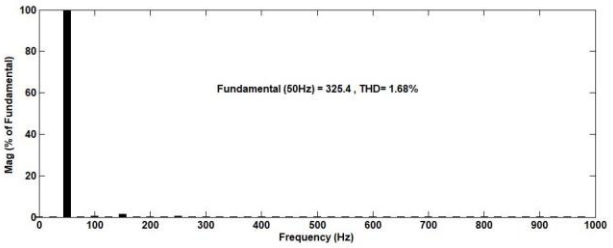


Fig. 16. Load voltage and harmonic spectrum

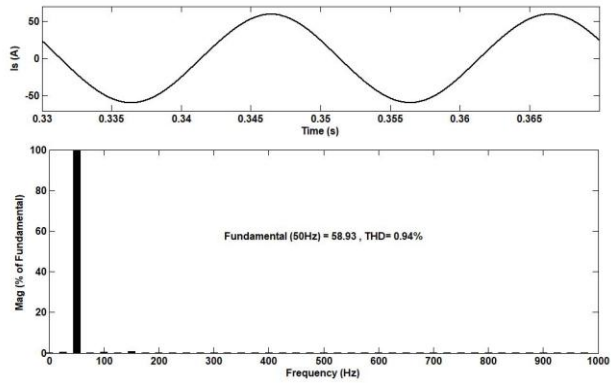


Fig. 17. Source current and harmonic spectrum

5. Conclusion

A control scheme based on PLL-Less adaline artificial neural network (ANN) is proposed in this paper. The proposed controller is capable to mitigating most types of power quality problems at source side i.e. balanced as well as unbalanced voltage sag/swell, voltage harmonic distortion and balanced as well as unbalanced voltage sag/swell with harmonic distortion. The fundamental component of terminal voltage is extracted using PLL-Less adaline based artificial neural network. Basic unit templates theory is used to replace complex PLL block which makes the system less complex. The performance of DVR is found suitable to address various power quality problems encountered by critical loads in power system.

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