HARDWARE IMPLEMENTATION AND ANALYSIS OF DIFFERENT SOURCES FED HYBRID CASCADED H-BRIDGE FIFTEEN LEVEL INVERTER

G. S. ARUNKUMAR
Research Scholar, Anna University, Chennai
Email:arunbe20@gmail.com

N. P. ANANTHAMOORTHY
Professor, Department of EEE,
Hindusthan College of Engineering and Technology, Coimbatore
Email: npaeee16@gmail.com

Abstract: *A new hybrid single phase H-bridge multilevel inverter (MLI) is designed with less number of power electronic switching devices in order to reduce the Total Harmonic distortion (THD) value of output voltage waveform. The hybrid MLI is designed by using two inverters, which are connected in cascaded to produce fifteen levels output voltage. The outputs of H-bridge MLIs which is fed with three types of inputs namely (i) three separate DC sources, (ii) with single input single output DC-DC boost converter and splitting capacitors, (iii) with single input multi output DC-DC boost converter without splitting capacitors, are compared in this paper. The performance of hybrid H-bridge multilevel inverter is analyzed at different asymmetric conditions using MATLAB (SIMULINK). In order to avoid the voltage balancing problem, multi output DC to DC boost converter is introduced in this proposed work. The simulation results are shown and compared with the results of hybrid 15level multilevel inverter which is fed with separate DC sources, to justify the superiority of proposed method and it is implemented by using SPARTAN 3 DSP kit and the waveforms are presented.*

Key words: *H-Bridge Multi-Level Inverter, Multi Output DC-DC Converter, MATLAB (SIMULINK), SPARTAN 3 DSP kit*

1. Introduction

With the aim of improving the power handling capability and to improve the power quality in the Renewable Energy Conversion Systems (RECS), nowadays MLIs are getting more popular. Among the types of MLIs, in order to reduce the complexity in the operation and because of its modularized circuit design, single phase cascaded H-Bridge inverters are mostly used because of their modularized circuit layout.

A various types of modulation techniques are available for CHB inverters. Increase in the number of switching devices in CHB increases the number of output voltage levels in CHB inverters. But in addition with this, separate DC sources are needed to get the desired multilevel output which makes the circuit further complex. But the only issue concentrated in the research is t0 limit the count of power electronic switches. So, constructing the MLI with reduced number of switching devices is being a big challenge because of the difficulties in selecting the proper Pulse Width Modulation (PWM). Junfeng Liu, Jialei Wu, Jun Zeng, and Huafang Guo designed a nine level inverter with less switching devices and voltage sources [1]. It is achieved by connecting the two capacitors and a voltage source in series and parallel.

Rasoul Shalchi Alishah, Seyed Hossein Hosseini, Ebrahim Babaei, and Mehran Sabahi proposed an optimized laddering technique is incorporated to design cascaded MLI structure [2] in which a new optimized pulse width modulation technique is proposed to improve the number of levels with less switching devices and DC sources. Amir Taghvaie, Jafar Adabi, and Mohammad Rezanejad introduced a new circuit topology of stepup MLI with a single DC source [3]. In that topology, by controlling the charging and discharging of switched capacitors in predetermined time, the number of levels in the output voltage is obtained. Amin Gholizad and Murtaza Farsadi proposed a improved staircase modulation for MLI [4] in which a solution for SOC for storage cells is examined. Reduced switch MLI topologies are proposed in which DC sources are connected in series and parallel [5-7] (MLISPC) and a circuit which consists of four diodes and a switch replaces the series and parallel combination of switches [8] in the MLISPC. For the same level of output voltage, only two isolated voltage sources are needed in [8]. The proposed MLI topologies in [9-14] can be used for the grid connected PV

systems application like hybrid electric vehicles etc. In all the above literatures, switching devices used to construct MLI is large and the THD value is also somewhat high.

To overcome the disadvantages of conventional MLIs, new hybrid MLI with less number of switches is designed in order to reduce the switching loss and to reduce the THD of output voltage. The MLI circuit is checked with different inputs and it is verified and simulated by using the MATLAB (SIMULINK) and the MLI is implemented by using Spartan3 FPGA kit.

2. Proposed Hybrid Multilevel Inverter

A hybrid MLI is proposed with reduced number of switches which is fed with three different types of inputs. The THD value of output voltage waveforms of all the three performance of proposed MLI. Hybrid H-Bridge MLI with Separate DC Sources topologies is analyzed and compared to find the

A. Hybrid H-Bridge MLI with Separate DC Sources

Fig. 1 shows the circuit diagram of proposed hybrid H-bridge MLI with separate DC sources.

In this circuit, asymmetric type of input voltage source is used. The upper inverter is fed with voltage level of V_{dc} in order to generate 3 output voltage levels namely V_{dc}, 0,-V_{dc} and lower inverter is fed with 3 voltage sources having the voltage levels of $2V_{dc}$ each in order to generate 7levels of output voltage namely $2V_{dc}$, $4V_{dc}$, $6V_{dc}$, 0, $-2V_{dc}$, $-4V_{dc}$, $-6V_{dc}$. (i.e) The voltage magnitude of each voltage source in the lower H-Bridge is two times the voltage magnitude of upper H bridge voltage source [15,16].

The number of output voltage levels generated by the lower inverter is given by the equation as,

$$n_{low} = (2a_{low} + 1) \text{ levels} \quad (1)$$

where a_{low}= number of DC voltage sources used in the lower inverter, n_{low}= number of output voltage levels of lower inverter.

The number of auxiliary switches used in the lower inverter for the generation of levels depends on the number of levels of output voltage required to be generated.

$$m_{low} = (a_{low} - 1) \quad (2)$$

where m_{low}= number of auxiliary switches.

Totally four sources are used in this fifteen level inverter which includes one DC source of V_{dc} in the upper inverter and three DC sources of $2V_{dc}$ each in the lower inverter.

$$V_{o,\max} = V_{dc} + (a_{low} * 2V_{dc}) \quad (3)$$

where $V_{o,max}$=maximum output voltage of MLI

When the conventional CHB inverter is driven by the hybrid modulation method, 12 switching devices are needed for 11 levels and 16 switching devices are needed for 15 levels. The proposed inverter as shown in Fig. 1 requires 9 switching devices for 11 levels and 10 switching devices for 15 levels and for 19 levels only 11 switches are required.

No. of power switching devices in MLI is given by

$$Q = \left(\frac{(n-11)}{4} + 9 \right) \quad (4)$$

where n= number of output voltage levels of MLI

In this topology, direct DC voltage sources are connected with the MLI. So, it is not needed to have splitting capacitors.

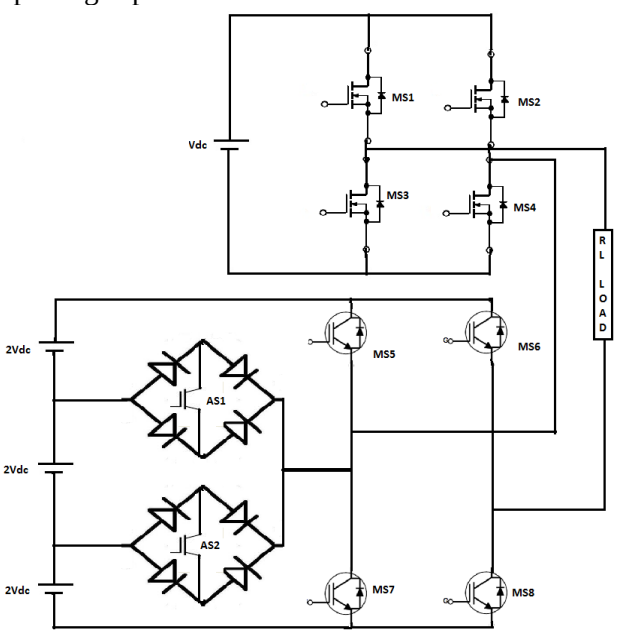

Fig. 1. Hybrid H-bridge 15level MLI with separate DC Sources

B. Hybrid H-Bridge MLI with Single DC Source and Splitting Capacitors

The second topology of the proposed circuit is MLI with a single DC source and splitting capacitors which is shown in the Fig. 2. The final output of proposed MLI is achieved as 4C + 3 levels by V_{low} + V_{up} or Vl_{ow}− V_{up}, where C is the number of capacitor sources in the lower H bridge inverter. The purpose of using the splitting capacitors is to give the splitted voltage of $6V_{dc}$ as $2V_{dc}$ each across every auxiliary switch. So, this splitting capacitors act as a voltage source for level generating network of lower inverter.

In this topology, only one DC voltage source of magnitude $6V_{dc}$ is used and the number of capacitors(C) required is given by

$$C = m_{low} + 1 \quad (5)$$

When compared with the previous topology, the DC voltage source is getting reduced which is due to the addition of capacitors.That single DC voltage with magnitude $6V_{dc}$ may be replaced with a single DC voltage with reduced magnitude and boost DC-DC converter which will be very suitable for the Solar PV application.

C. Hybrid H-Bridge MLI with Single Input Triple Output DC-DC Boost Converter

By utilizing this different capacitor source, a noteworthy issue is getting presented in this framework called "Voltage Balancing Problem". It must be lessened; else it will influence the execution of the inverter and proficiency of the inverter. Furthermore, this can be wiped out by presenting a Multi-Output DC-DC Converter. Also, in this proposed work, the different capacitor source is supplanted with a multi-output boost DC-DC converter for the accompanying reasons.

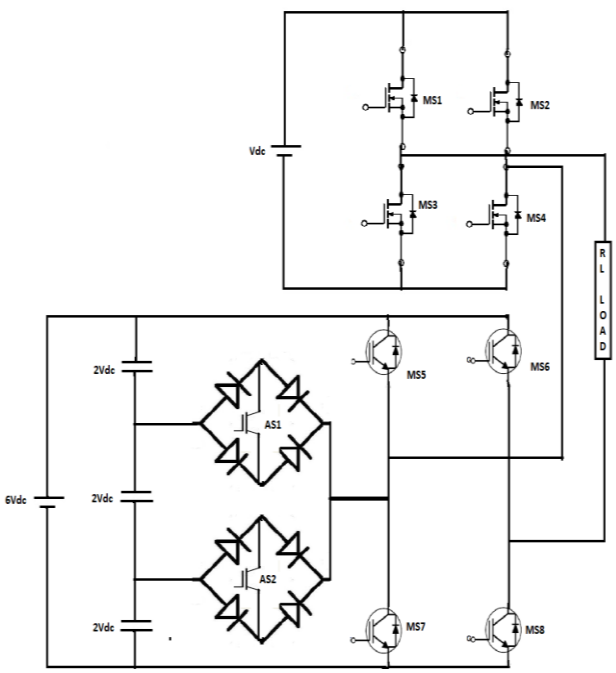

Fig. 2. Hybrid H-bridge 15level MLI with single DC source and splitting capacitors.

1. For boosting low output voltage of PV array or FC stacks to a desired value,
2. Balancing of DC link capacitors.

Multi-Output DC-DC boost converter [17] is associated with lower inverter and it is fed with a single DC Source. Furthermore, in the future, single DC Source can be supplanted with a PV Solar Array module. The switching sequence for the switches has to be formulated in order to get the desired boosted voltage. The switching sequence for different modes of operation for the switches which is used in the triple-output DC-DC boost converter is given in the below Table 1. In this proposed circuit, triple output DC-DC boost converter, which consists of 3 MOSFET switches and 3 diodes, is designed and the output of converter is given as the input for MLI. Fig. 3 shows the circuit diagram of triple output DC-DC boost converter fed proposed MLI.

So, the addition of this triple-output DC-DC boost converter, the number of power switching devices used in this topology of MLI increases by three in number as given below,

$$Q = \left(\left(\frac{(n-11)}{4} + 9 \right) + P \right) \quad (6)$$

where P=number of power switching devices used in multi output DC-DC boost converter which is equal to number of outputs needed to be generated by DC-DC converter. For example, if it is a triple output DC-DC boost converter, then P=3 and Q=13 for 15level inverter.

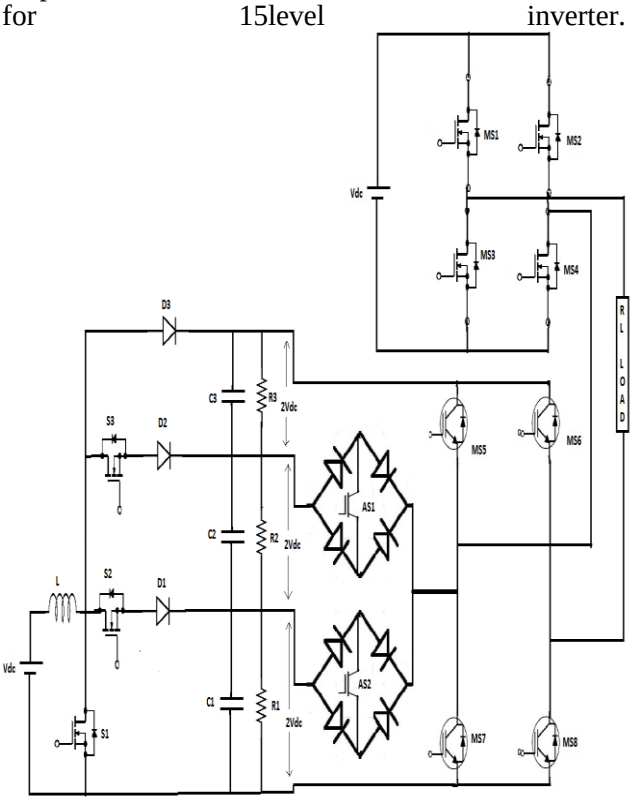

Fig. 3. Hybrid H-bridge 15level MLI with single input triple output boost DC-DC converter

D. Hybrid Modulation Technique

As two inverters are in cascaded connection to get the desired voltage levels, a hybrid modulation technique is used in this proposed work. A modified sinusoidal modulation technique with high frequency [18-20] is designed for upper level

inverter in order to produce three level voltages and staircase modulation technique with low frequency is proposed for lower level inverter in order to produce seven level voltages as output. The modulation techniques used here determines the switching function to obtain a output of 15 levels in the proposed inverter.

Table 1

Switching sequence of triple output dc-dc boost converter

Modes	S_1	S_2	S_3
1	1	0	0
2	0	1	0
3	1	0	0
4	0	0	1
5	1	0	0
6	0	0	0

The reference waveform for the upper inverter is given as

$$V_{ref} = B\sin(wt) \tag{7}$$

where B is the peak value of reference waveform which is given by B=(2P+1)

$$Z_1 = 1 \quad \text{if} \quad V_{ref} > 0 \tag{8}$$

$$Z_2 = 1 \text{if} \quad V_{ref} < 0 \tag{9}$$

$$V_{l,\exp} = (round(\frac{V_{ref}}{0.4}) * 0.4 * Z_1) + (round(\frac{V_{ref}}{0.4}) * 0.4 * (-Z_1)) \tag{10}$$

$$V_{up,ref} = (V_{ref} - V_{l,\exp}) \tag{11}$$

Thus the modified sinusoidal reference waveform is generated and compared with triangular carrier waveform with high frequency in order to get the switching pulses which are shown in the Table II to generate three level high frequency output voltage waveform.

Table 2

Switching sequence of upper inverter

Output Voltage Level	MS_1	MS_2	MS_3	MS_4
V_{dc}	1	0	0	1
0	0	0	0	0
$-V_{dc}$	0	1	1	0

A staircase modulation technique is proposed for generating the switching pulses to produce 7levels of output voltage from lower inverter. A three staircase reference waveform is generated and two more pulses (Z_1,Z_2) are generated as follows

$$Z_1 = 1 \quad \text{if} \quad V_{ref} > 0 \tag{12}$$

$$Z_2 = 1 \text{if} \quad V_{ref} < 0 \tag{13}$$

And three pulses are generated from the staircase waveform namely (P_1,P_2,P_3). Then by comparing Z_1, P_1 and P_3, switching gate pulse for main switch MS_5 is generated. Then by comparing Z_2, P_1 and P_3, switching gate pulse main switch for MS_7 is generated. Then by comparing Z_1, Z_2 and P_1, switching gate pulses for main switches MS_6 and MS_8 are generated. And by comparing Z_1, Z_2, P_1, P_2 and P_3, switching gate pulses for auxiliary switches AS_1 and AS_2 are generated which is shown in the below equations. The switching gate pulse sequence for lower inverter is shown in Table 3.

$$S_1 = \left(\overline{P_1}(or)P_3\right) * Z_1 \tag{14}$$

$$S_2 = \left[\left(P_1 * Z_2\right)(or)\left(\overline{P_1} * Z_1\right)\right] \tag{15}$$

$$S_3 = \left(\overline{P_1}(or)P_3\right) * Z_2 \tag{16}$$

$$S_4 = \left[\left(P_1 * Z_1\right)(or)\left(\overline{P_1} * Z_2\right)\right] \tag{17}$$

$$S_5 = \left[\left(P_1(xor)P_2\right) * Z_2\right](or)\left[\left(P_2(xor)P_3\right) * Z_1\right] \tag{18}$$

$$S_6 = \left[\left(P_1(xor)P_2\right) * Z_1\right](or)\left[\left(P_2(xor)P_3\right) * Z_2\right] \tag{19}$$

Table 3

Switching sequence of lower inverter

Output Voltage Level	MS_5	MS_6	MS_7	MS_8	AS_1	AS_2
2 V_{dc}	0	0	0	1	0	1
4 V_{dc}	1	0	0	1	1	1
6 V_{dc}	1	0	0	1	0	0
0	0	0	0	0	0	0
-2 V_{dc}	0	1	0	0	1	0
-4 V_{dc}	0	1	0	0	0	1
-6 V_{dc}	0	1	1	0	0	0

E. Voltage Rating of the Device

The rating of the switching devices should be selected prudently in the proposed inverter, because of the dissimilarities in the voltage rating of each device. Only one auxiliary switch is required in the proposed topology of 11-level inverter. In this case, the voltage of auxiliary switch will bounce between 0 and $2V_{dc}$ because the total voltage $4V_{dc}$ is alienated into two by splitting capacitors (i.e) $2V_{dc}$ each. Therefore, capacitor voltage of $2V_{dc}$ has to be blocked by the auxiliary switches. Likewise, two auxiliary switches are required in the proposed topology of 15-level inverter. The total voltage $6V_{dc}$ is alienated into three by three splitting capacitors (i.e) $2V_{dc}$ across each. Hence, the voltage of two auxiliary switches will bounce between 0 and 4Vdc. Further, three auxiliary switches are required in 19-level inverter. The voltages of first and last auxiliary switch will bounce between 0 and $6V_{dc}$ and the voltage of middle auxiliary switch will bounce between 0 and $4V_{dc}$. Similarly, for other levels of inverters of this topology, the voltage of first and last auxiliary switch voltage bounces between 0 and $\left((n-1)mV_{dc}/n\right)$, whereas the voltage of other auxiliary switch bounces between 0 and $\left((n-2)mV_{dc}/n\right)$, $\left((n-3)mV_{dc}/n\right)\ldots$ and so on and where n is the number of splitting capacitors and mV_{dc} is total voltage applied for the lower inverter.

3. Simulation Results and Experiment Verification

The software used to design the circuit is MATLAB (Simulink). Fig. 4 and Fig.5 show the gate pulse generation of upper inverter and lower inverter respectively.

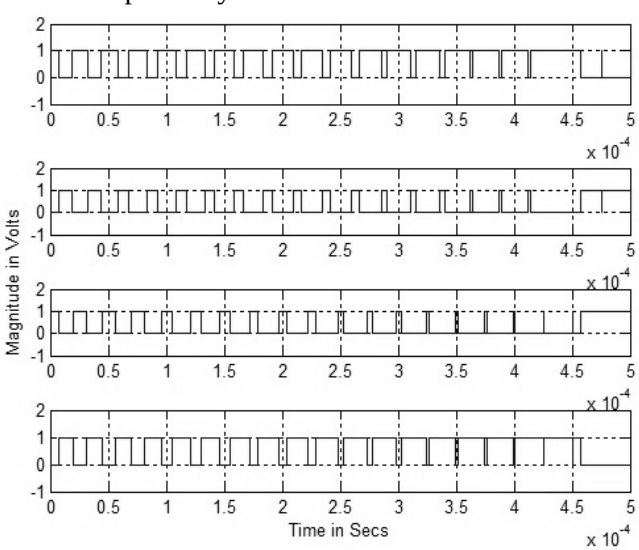

Fig. 4. Gate pulse of upper inverter

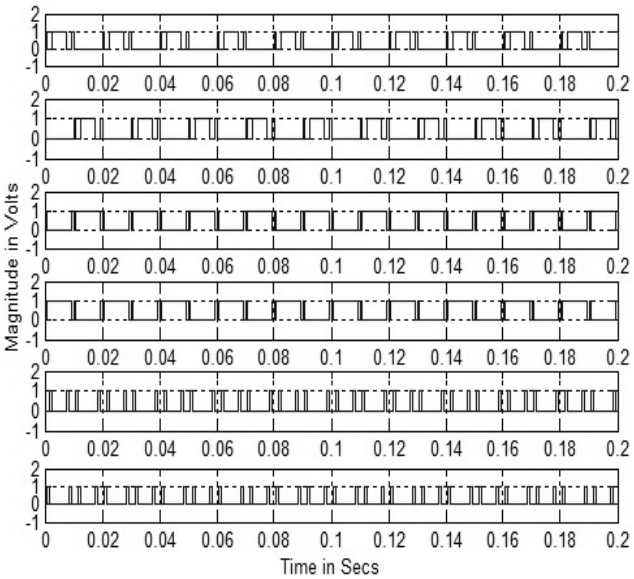

Fig. 5. Gate pulse of lower inverter

Fig. 6 and 7 shows the 15level output voltage waveform of MLI with a separate DC sources and its plot of THD done using FFT analysis in MATLAB/SIMULINK respectively.

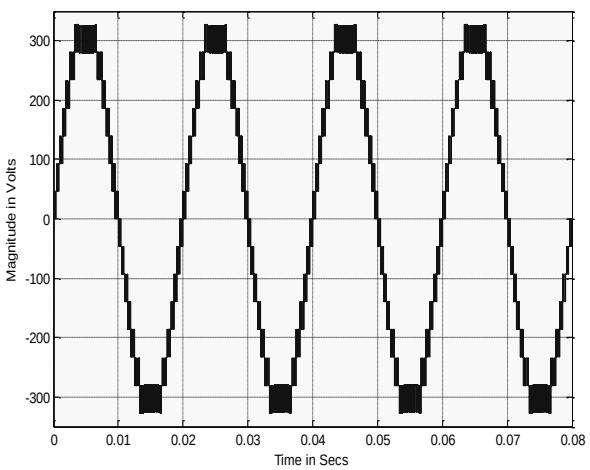

Fig. 6. Output voltage waveform of 15level MLI with separate DC source

In the above output voltage waveform of 15level MLI with separate DC source shown in Fig.6, it is observed that the magnitude of output voltage is 325V with 15levels. Because of using separate DC sources, there is no need of using splitting capacitors in this topology which eliminates the voltage balancing problem and the THD value of output voltage for this topology which is observed from Fig.7 is 7.62%.

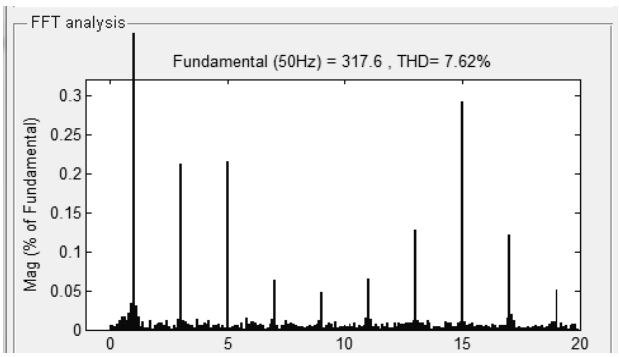

Fig. 7. THD plot of output voltage of 15level MLI with separate DC source

Fig. 8 and 9 shows the 15level MLI with single DC source and splitting capacitors and its plot of THD done using FFT analysis in MATLAB/SIMULINK respectively. In this output voltage waveform, it is observed that because of voltage balancing problems in the capacitors, there is a mismatch occurring in voltage sharing between the upper and lower inverter in order to produce the output of the MLI. THD value of output voltage of 15level MLI with single DC source and splitting capacitors is 14.11% which is shown in Fig.9.

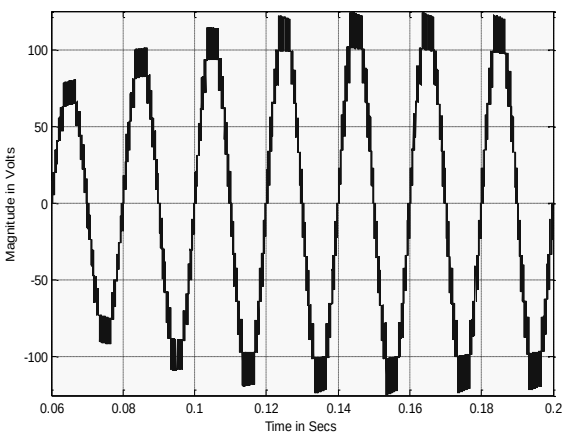

Fig. 8. Output voltage waveform of 15level MLI with single DC source and splitting capacitors

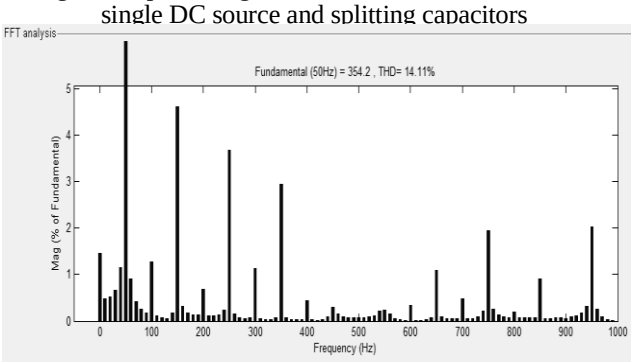

Fig. 9. THD plot of output voltage of 15level MLI with single DC source and splitting capacitors

Fig. 10 and 11 shows the 15level output voltage waveform of MLI with a single input triple output DC-DC boost converter and its plot of THD done using FFT analysis in MATLAB/SIMULINK respectively.

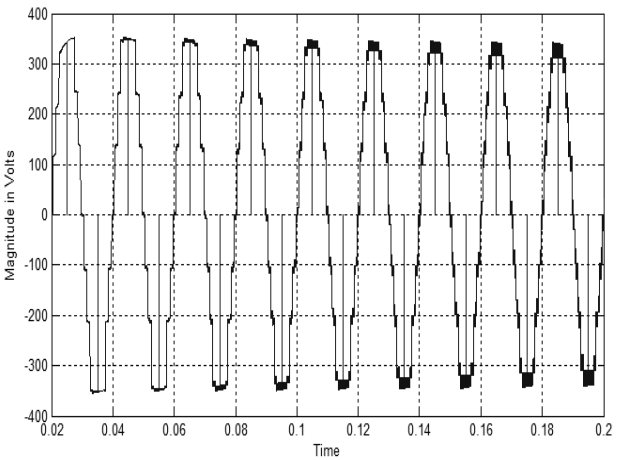

Fig. 10. Output voltage waveform of 15level MLI with single input triple output DC-DC boost converter

In this output voltage waveform, it is observed that the voltage mismatch is eliminated in this topology which is because of introducing single input multi output boost converter in front of MLI. THD value of output voltage of 15level MLI with single DC source and splitting capacitors is 8.02% which is shown in Fig.11.

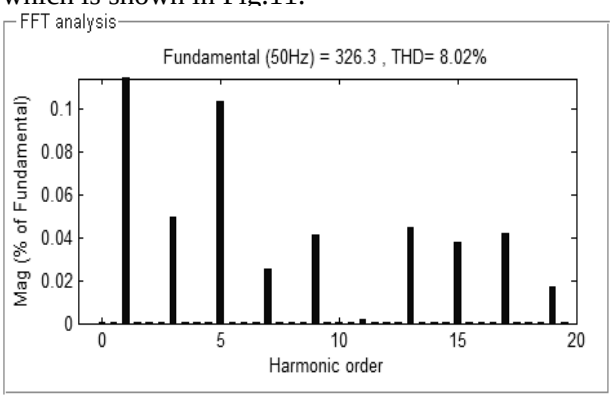

Fig. 11. THD plot of output voltage of 15level MLI with single input triple output DC-DC boost converter

Fig. 12.a. and 12.b. hardware output results of switching pulses for switches MS1,MS2,MS3 and MS4 of upper inverter of proposed 15level MLI which is observed using FPGA Spartan 3 kit.

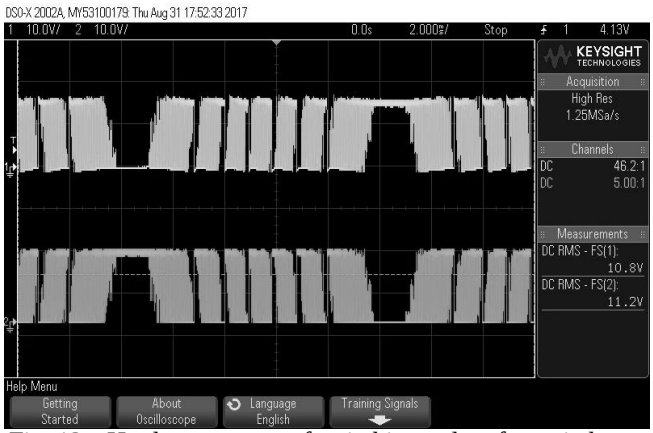

Fig. 12.a.Hardware output of switching pulses for switches MS1, MS3 of upper inverter

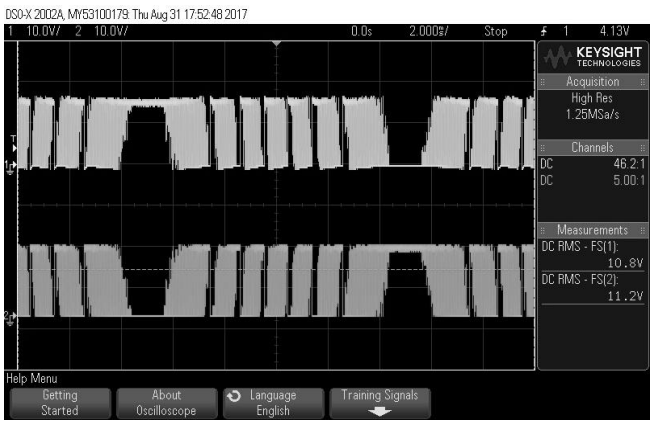

Fig. 12.b. Hardware output of switching pulses for switches MS2, MS4 of upper inverter

Fig. 13.a, 13.b and 13.c show the hardware output results of switching pulses for main switches MS5,MS6,MS7,MS8 and auxiliary switches AS1,AS2 of lower inverter of proposed 15level MLI which is observed using FPGA Spartan 3 kit.

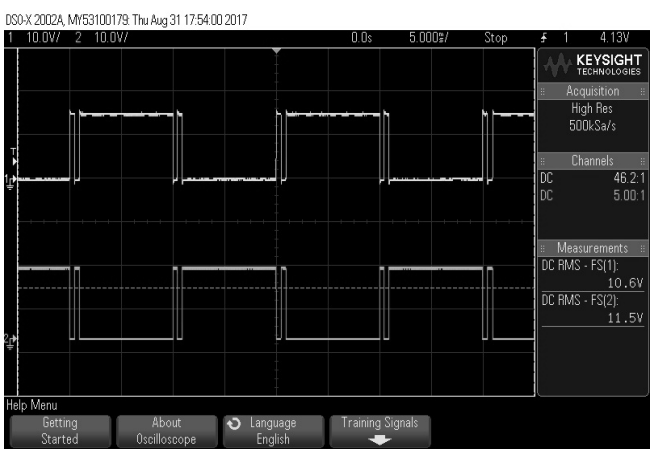

Fig. 13..a. Hardware output of switching pulses for switches MS5, MS7 of lower inverter

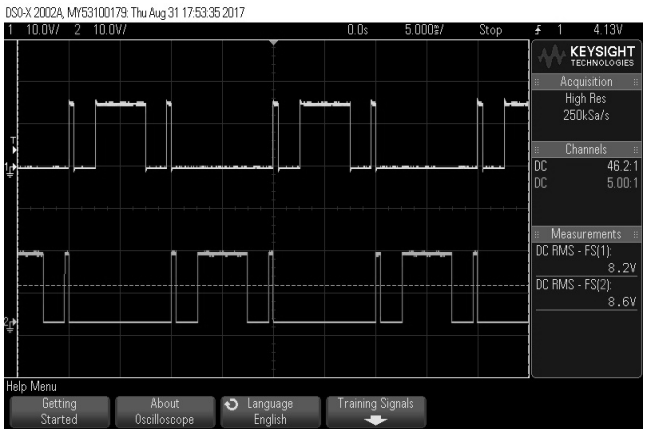

Fig. 13.b. Hardware output of switching pulses for switches MS6, MS8 of lower inverter

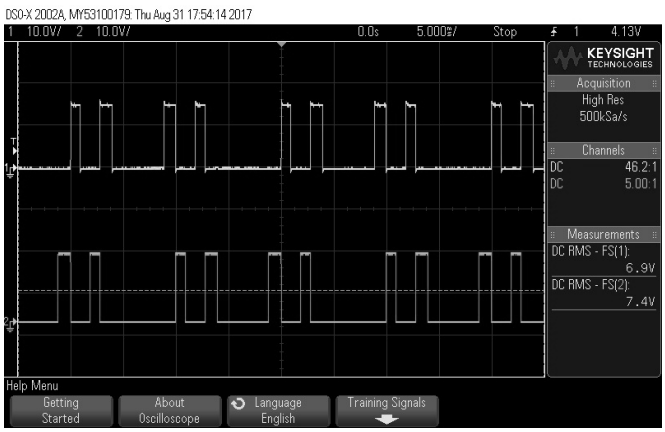

Fig. 13.c. Hardware output of switching pulses for switches AS1, AS2 of lower inverter

Fig. 14.a., 14.b. and Fig. 14.c. shows the 15level output voltage waveform, THD value of output voltage and hardware implementation of 15level hybrid MLI with separate DC sources respectively.

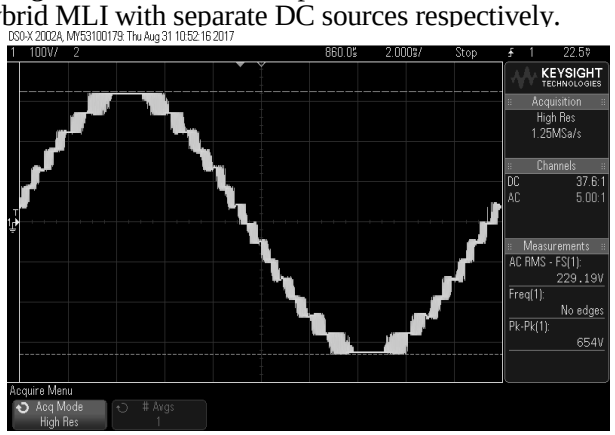

Fig. 14.a. Output voltage waveform of 15level MLI with separate DC sources

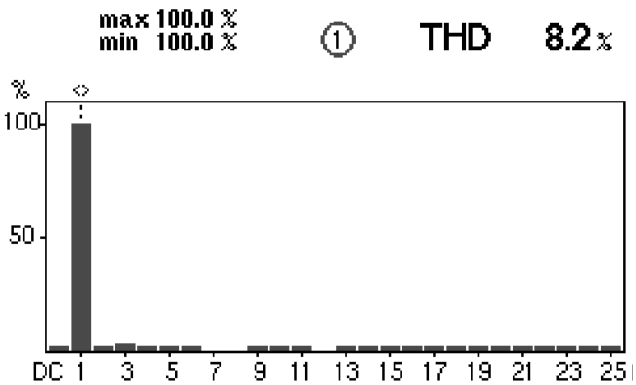

Fig. 14.b. THD value of Output voltage waveform of 15level MLI with separate DC sources

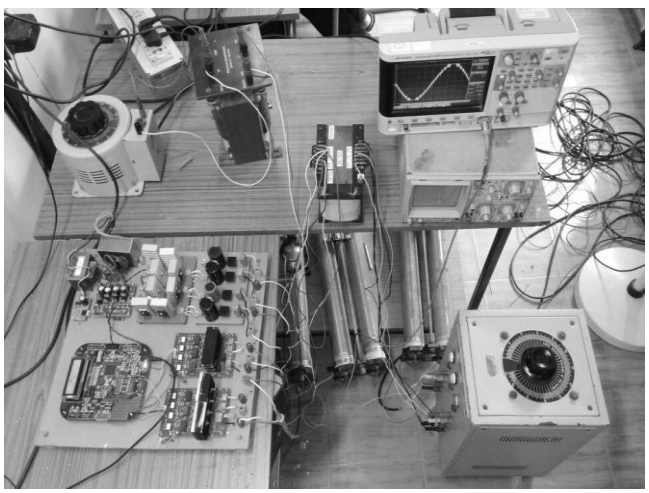

Fig. 14.c. Hardware implementation of 15level MLI with separate DC sources

Fig. 15.a., 15.b. and Fig. 15.c. shows the 15level output voltage waveform, THD value of output voltage and hardware implementation of 15level hybrid MLI with separate DC sources respectively.

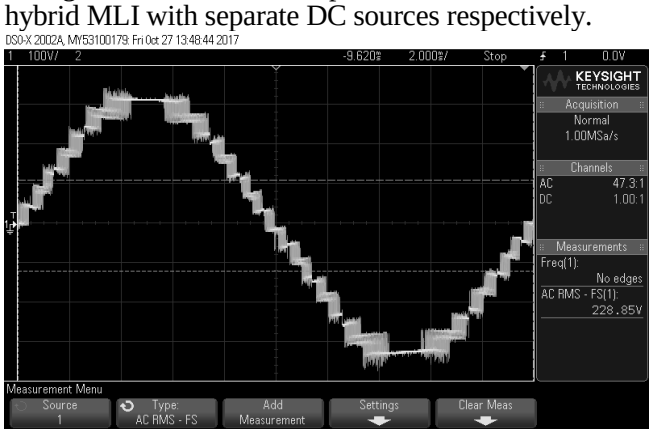

Fig. 15.a. Output voltage waveform of 15level MLI with single DC source and splitting capacitors

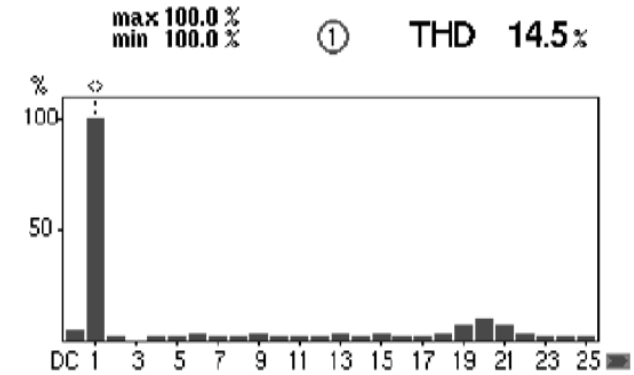

Fig. 15.b. THD value of Output voltage waveform of 15level MLI with single DC source and splitting capacitors

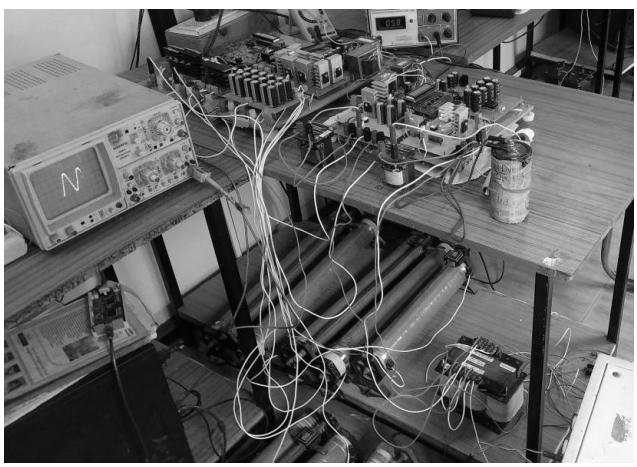

Fig. 15.c. Hardware implementation of 15level MLI with single DC source and splitting capacitors

Fig. 16.a., 16.b. and Fig. 16.c. shows the 15level output voltage waveform, THD value of output voltage and hardware implementation of 15level hybrid MLI with single input triple output DC-DC boost converter.

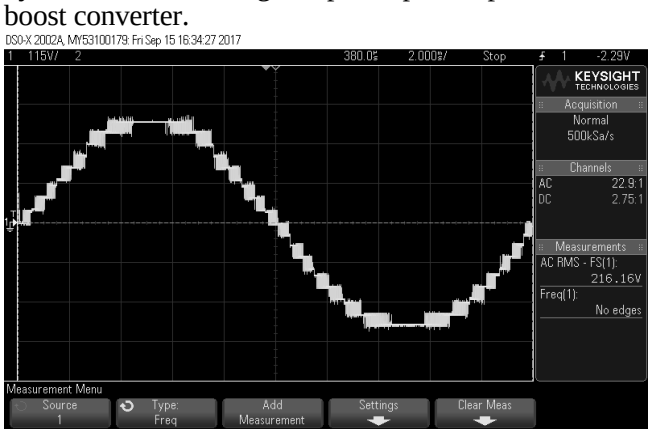

Fig. 16.a. Output voltage waveform of 15level MLI with single input triple output DC-DC boost converter

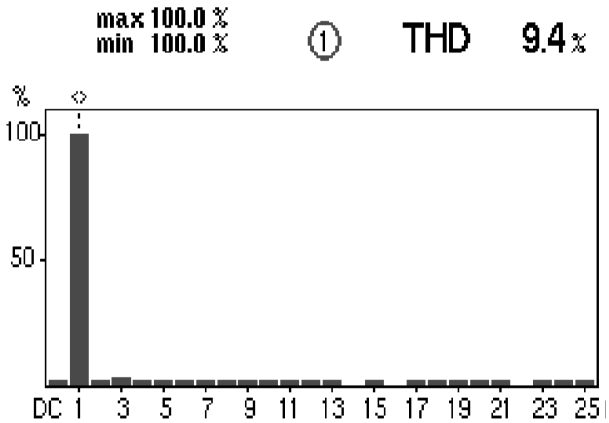

Fig. 16.b. THD value of Output voltage waveform of 15level MLI with single input triple output DC-DC boost converter

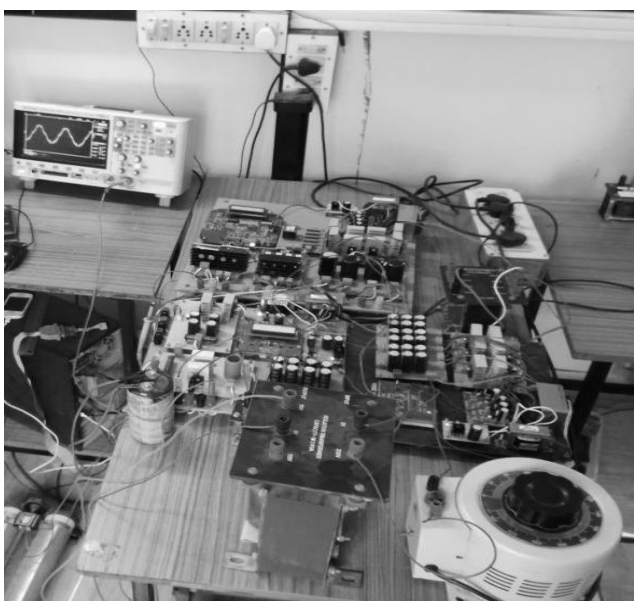

Fig. 16.c. Hardware implementation of 15level MLI with single input triple output DC-DC boost converter

Table IV, fig. 17 and fig.18 show the comparison of number of levels, number of switching devices used in MLIs, THD values in % and DC sources used in MLIs. In Table IV,

Type 1: MLI with separate DC sources (conventional) [6]

Type 2: Proposed MLI with separate DC sources

Type 3: Proposed MLI with single DC source and splitting capacitors

Type 4: Proposed MLI with single input triple output DC-DC boost converter

Table 4
Comparison of number of levels, number of switching devices, thd value and DC Sources

Method	Level	No of Switch Used	THD in %		DC Sources
			Simulation	Hardware	
Type 1	15	16	11.4	16.2	3
Type 2	15	10	7.62	8.2	3
Type 3	15	10	14.11	14.5	1
Type 4	15	10	8.02	9.4	1

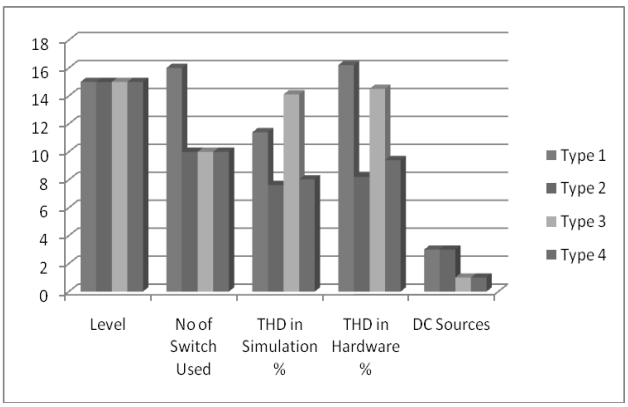

Fig. 17. Comparison chart of MLIs with different categories of inputs

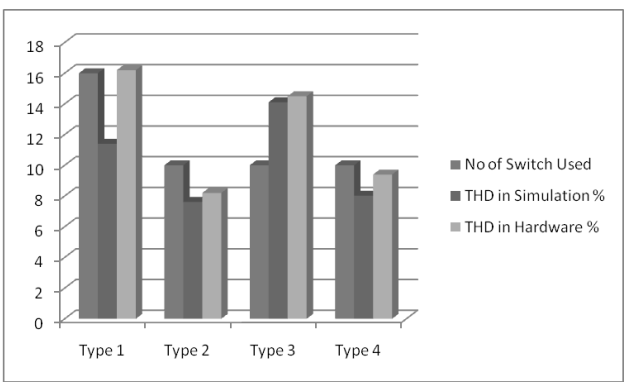

Fig. 18. Simulation and hardware of THD values comparison chart

4. Conclusion

The proposed novel single-phase multilevel inverter with single input triple output boost DC-DC converter and isolated DC sources offers enhanced output voltage with minimum THD, reduced switching devices and DC sources which is experimentally shown in above discussion in fig. 17 and fig.18. The capacitor voltage balancing problem is eliminated for higher levels by incorporating triple output DC-DC converter booster circuit in MLI. Thus, it is experimentally proved that the proposed novel multilevel inverter can be used for medium- and high-power applications.

5. References

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