A Self Balancing Space Vector PWM for Z Source T Multilevel Inverter

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Abstract— **This paper presents a Z Source -T shape - Neurtal point Diode Clamped (NPC) - Multi Level Inverter (MLI) power conversion system (Z-T-NPC-MLI) with the aid of New Space Vector PWM (SVPWM) scheme. The proposed impedance source (Z-Source) MLI associations the advantages of boosting operations with DC to AC power conversions. There are many MLI Z-Source research papers for concentrating the desired voltage generations with minimal switching and conduction losses. Nevertheless, the reported research on Z-NPC-MLI SVPWM has dealt with reduction of Shoot through (ST) options and voltage boosting operations enhancement; those are does not address the neutral point fluctuation (NPF) problems on the DC-Link. This paper offers improved SVPWM strategies for Z-source NPC-MLI with minimal ST state options. The proposed SVPWM exploits the redundancy switching vector option for both ST and regular switching (non-ST), which offers self-control to NP (DC-link capacitor) balancing. With this benefit of this self- control DC-link capacitors balancing, the inverter able to maintain their output quarter symmetry waveform and henceforth the harmonic spectra for the voltage and current waveform is maintained lesser. The proposed SVPWM for Z-T-NPC-MLI is simulated in MATLAB/SIMULINK 2011.b software environment, and the results confirm the advantages of the proposed inverter and its simplified PWM scheme. The experimentation is also performed for 1kW three-phase Z-T-NPC-MLI system using sparten-6 FPGA processor. The experimental results are confirmed the simulation results.**

Keywords- Z Source MLI, T-MLI, Neutral point Diode Clamped,Capacitor balancin.

I. INTRODUCTION

Renewable energy sources (RESs) are taking the top position in the field of electrical generation. Almost all the countries in the world are encouraging the RESs (mostly PV and wind), due to various reasons like scarcity of the fossil fuels, to reduce the emissions caused via green power generation. Solar energy is the most promising source of energy among the RESs [1].

The inverters are the mandatory segment in the photovoltaic (PV) systems, as the output of any PV system will be DC. Due to this fact, research in the field of inverters has improved a lot in the recent ages. Apart from the PV system, most of the industrial applications require high power/ medium power inverters. The two-level inverters ware ran out after the arrival of multilevel inverters (MLIs). The first concept of MLI was proposed by R H Baker [2] in the year 1975. The MLIs enables to attain the high voltage and power ratings without the use of transformers. The advantages of MLIs are reduced voltage stress, low switching losses and low common mode voltage. The total harmonic distortion (THD) will be reduced with the increase of the number of levels of an MLI. However, the number of levels is limited by constraints like voltage unbalance and circuit complexity. The first three - level (3L) MLI was implemented by Nabae [3] in 1981. After 1990s, numerous MLIs topologies are reported in the literature. Nevertheless, these MLIs are grouped in majorly only three types: neutral-point clamped (NPC), flying - capacitor (FC) and cascaded H-bridge (CHB). The FC-MLI was invented by Fazel *et.al* in 1990. It uses a higher number of capacitors to make a level, hence it is requires more protection to ensure the uniform capacitors charging and discharging. The CHB-MLI involves extra isolated DC sources, which is practically impossible with the use of PV based power system. All these pros and cons, the NPC–MLI is a better choice for medium voltage and power applications. The NPC-MLI uses clamping diodes to achieve the levels, which have additional losses. With the elimination of clamping diodes in the NPC MLI L Ma *et.al* [4] proposed T-Type NPC-MLI in the year 2009, which can also be called as the diode-less NPC-MLI. Here, the switches in single leg of T Type NPC-MLI will be arranged in the form of the alphabet 'T'. The T Type NPC-MLI will have all the reward of the NPC-MLI. Apart from the elimination of the clamping diodes these T Type NPC-MLI have lower switching losses as the switches 2 and 3 will behalf the rating of switches 1 and 4. Due to the low conduction and switching losses T-Type NPC -MLI can achieve an efficiency of 99% [5,6]. Due to all these advantages T Type NPC-MLI will be the best option for the PV applications. However, the DC-link balancing is a considerable element on it.

The output voltage boosting for any MLI topology is not possible without adding DC to DC converter in their input side; this become a main drawback in case of PV applications. Normally, the conventional two stage system structure as DC to DC boosting conversion (through boost converter) and DC to AC (through inverter). This increases the control circuit design complexity and cost. After arrival of impedance source (Z-source) in 2003, the two-stage power conversion is replaced by single-stage power conversion (DC to boosted AC) is becomes popular and recommended for many applications [7]. The reduction in control methods and power switch, the power electronics researchers are started to use Z – source concepts in MLIs and used in many electrical notable application such as wind power generation, HVDC systems etc., In Z-source inverter, the boosting is achieved in front end 'X'- shape elements, formed two though inductors and two

capacitors. The storing the energy in the inductors, it is needs to connect directly with input DC source. Therefore, the inductors need to short through MLI circuit switches. This proposes is called as shoot-through (ST). To organizing the regular switching and ST switching, the Z-source MLI PWM is fairly complex than that of a normal MLI PWM strategy. In carrier PWM methods, the maximum boosting and constant boosting carrier methods are the most acceptable for the Z-source MLI. Similar to MLIs, Z-source too absorbed mainly space vector PWM (SVPWM), since it has a great potential to deal the switching activation with direct control nature [12,13] The ST option for the Z-source NPC-MLIs precisely realized using by using SVPWM with redundant ST options [14]. The proposed method is offered a higher control degree of freedom to vary the output voltage boosting. The similar strategies with minimum ST switching actions are proposed in [15,8], which are mainly focusing to increasing the boosting function of the inverter. The methods are not solving the NP capacitors balancing; hence the output voltage of the inverter is ached with higher THD. The redundancy switching is allows the current flow in the NP in every phase and maintain the zero current at NP [16]. There some interesting paper is published in the literature to ensure the zero NP in every switching cycle interval, which are maintain the self- balancing he capacitors. Considering the NPC-MLI topology types, T-type topology have uses only main control power switches. The clamping diode is totally removed form T-type MLI, and hence it is offered a lesser loss than I-type NPC-MLI [6, 17]. Hence, the concentering the use T-type topology with Z-source is got a more interest in the power converter designer community.

Within this above discussed, the paper proposes a three-phase three- level Z-source T-type NPC-MLI and new SVPWM method for voltage-boosting improvement with DC-link NP capacitors balancing without comparing the voltage THD performances. The proposed SVPWM for Z-T-NPC-MLI is simulated in MATLAB/SIMULINK 2011.b software environment, and the results confirm the advantages of the proposed inverter and its simplified PWM scheme. The experimentation is also performed for 1kW three-phase Z-T-NPC-MLI system using sparten-6 FPGA processor. The experimental results are confirmed the simulation results.

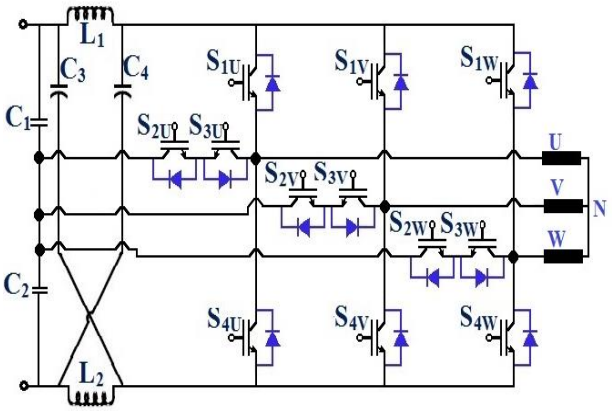


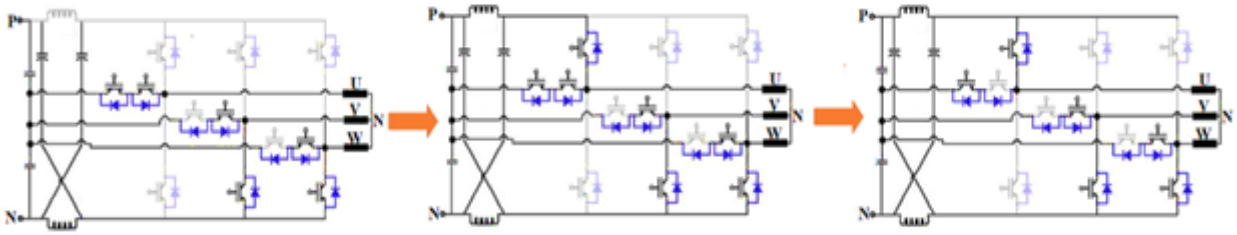
Figure.1 Topology circuit diagram of three-phase three-level Z- source T-NPC-MLI

II. CIRCUIT DIAGRAM OF THREE-PHASE THREE-LEVEL Z-SOURCE T-NPC-MLI

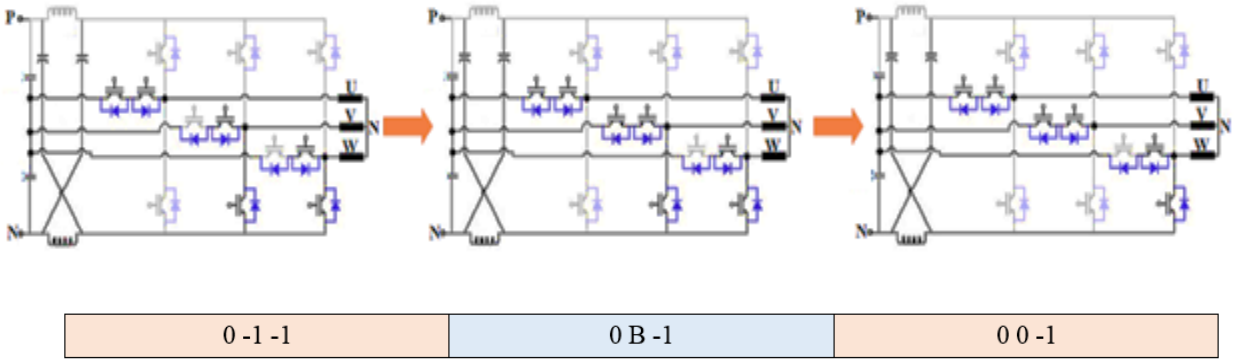
The three-phase three-level Z- source T-NPC-MLI is as presented in the Figure.1 and the working operation of the inverter can be elucidated with the aid of the single–leg switching shown in Table-1.

TABLE 1 Switching table of three-phase three-level Z- source T-NPC-MLI for leg-A

Mode	State	Switches Triggered	Diodes Forward biased	V_{OUT}
Non-ST Mode	+1	S_{1U} S_{3U}	D_{3U}	$(V_{DC}/2)+ L_1*(di/dt)$
	0	S_{2U}	-	0
	-1	S_{2U} S_{4U}	D_{2U}	$-(V_{DC}/2)- L_2*(di/dt)$
ST Mode	T	S_{1U} S_{2U} S_{3U}	-	0 (L_1 Charging)
	B	S_{2U} S_{3U} S_{4U}	-	0 (L_2 Charging)



(a)



(b)

Figure.2 **(a)** Top Shoot through **(b)** Bottom Shoot through

From the Table-1, when the switch S_1 and S_3 are 'ON', the positive current flow from the source (V_{DC}) to the load. Similarly, the negative current flow form load to source is achieved, S_2 and S_4 is 'ON'. When S_2 is 'ON', the current fall to NP and it is should be zero in ideal operation conditions. However, due to the non-uniform switching action maintaining the zero current at NP is challenging [1].

A. Non shoot-through mode:

During the non-shoot through mode the input DC-link voltage (V_{DC}) and the inductor voltage together are fed to the MLI, which leads to the boosting operation. The Non-ST mode (regular MLI switching) is divided into three modes [19].

- Mode-1: During this mode, the positive output voltage and positive current is achieved by triggering S_1 and S_3. The switch S_1 is only connected between source and load, where the S_3 connecting the NP with the help of D_{2U}. This allow the next cycle switching from +1 to 0.
- Mode-2: During this mode, the negative output voltage and negative current is achieved by triggering S_2 and S_4. The switch S_4 is only connected between source and load, where the S_2 connecting the NP with the help of D_{3U}. This allow the next cycle switching from -1 to 0.
- Mode-3: During this mode, the zero output voltage is achieved by tuned 'ON' switch S_2. In this mode the current fall to NP and it is should be zero in ideal operation conditions.

B. Shoot-through mode:

The Z-source MLI shoot-through options are considered to be in three categories, which are call it as, full-ST-state (FST), bottom- shoot-through (BST), top-through(TST) [16].

- FST: During this mode, all the four switches in the inverter leg is 'ON' and proving the direct path to short the inductor with input DC-supply (V_{DC}).
- TST: During this mode, the top three switches are turned 'ON' and proving the path to short the inductor. The TST is influenced by positive current on the V_{DC}.
- BST: During this mode, the bottom three switches are turned 'ON' and proving the path to short the inductor. The TST is influenced by positive current on the V_{DC}.

III. DESIGN OF Z SOURCE NETWORK:

In these sections, the paper takes an opportunity to analysis the Z-source inverter and to calculation of 'X' network elements (L and C) for find the boosting factor (B). Generally in buck-boost DC to DC converter uses the inductor and capacitor with power switch and blocking diode. The blocking diode is avoiding the reverse current flow form the load to source. Similar to buck-boost DC to DC converter, the Z-source inverter uses the L, C, blocking diodes in the positive and negative rail of the DC-bus [6].

As mentioned in Figure-1, the input side X-network (impedance network), and it's consist of two inductors (L_1 and L_2) and two capacitors (C_3 and C_4). The capacitor and inductor is used in the X-network is equal; therefore the voltage drop across them is related same.

$$V_{L1}=V_{L2}=V_L \quad (1)$$

$$V_{C1}=V_{C2}=V_C \quad (2)$$

Throughout the ST mode the voltage across the inductor (V_L) and capacitor (V_C) is same and the inductors are charging uniformly and maintain the voltage across the source X- network as $2V_C$.

$$V_L=V_C \quad (3)$$

During the ST;

$$V_i = 2V_C \quad (4)$$

During the non-ST;

$$V_0 = 0 \quad (5)$$

Let consider, T = total switching time, T_T = TST switching time, T_B= BST switching time, T_0 = commutation time (zero switching) and T_{NST} = nearest vector switching used for regular MLI switching []. The switching time T a

combination of the ST and non-ST time periods. The boosting factor (B) is given by

$$B=\frac{T}{T_{NST}-T_0}$$

Where $T=T_0+T_{NST}$, 20% of the ST time period is selected,

T_0 = 20% of the time period of one cycle

= 20% of 0.02

T_0 = 0.004 sec

$$B=\frac{1}{1-\left(2T_0/T\right)} \quad (6)$$

$$B=1.667$$

In the steady-state conditions, the voltage across the inductor (V_L) is zero, thus the V_L over one switching period is given by

$$\frac{\left(V_{DC}-V_C\right)T_{NST}+\left(V_{DC}/2\right)T_T+\left(V_{DC}/2\right)T_B}{T}=0$$

$$T=T_0+T_T+T \quad (7)$$

By solving equation (7), the voltage across the capacitor (V_C) is calculated as,

$$V_C=\left(V_{DC}\right)\left(\frac{1-T_0/2T}{1-T_0/T}\right) \quad (8)$$

$$V_C=50V$$

The output voltage of the Z-source network both in ST and non-ST states are calculated as,

$$V_0 \text{ (Non-shoot through)} = \frac{2V_{DC}}{1-T_0/T} \quad (9)$$

$$= 250V$$

$$V_0 \text{ (shoot through)} = \frac{V_{DC}}{1-T_0/T} \quad (10)$$

$$= 125V$$

Since the voltage across the inductor(V_L) is the difference of the V_{DC}(V_i) and capacitor voltage(V_C).
Average inductor current is given by

$$I_L = \frac{\text{Total power}}{V_{DC}} \quad (11)$$

The inverter power and DC-link is considering for this proposed Z-T-MLI is 1kW and 100V respectively. Hence From equation (11) becomes,

$$I_L=10V \quad (12)$$

Maximum current ripple on the inductors is estimated as 30%; therefore the maximum current (I_{LMax}) and minimum (I_{LMax}) are calculated as,

$I_{L\,MAX} = I_L + (30\% \text{ of } I_L)$ $\quad I_{L\,MIN} = I_L - (30\% \text{ of } I_L)$

$I_{L\,MAX} = 13$ amp , $I_{L\,MIN} = 7$ amp

Let, the consider voltage variations from the maximum boosted and un-boosted voltages, the inductor value is calculated as,

$$L = \frac{V * T_0}{I_{L\,MAX} - I_{L\,MIN}} \quad (13)$$

$$L = 10mH$$

Form the 1.2% voltage ripple is assumption; the capacitor value is calculated as,

$$C = \frac{I_L T_0}{\Delta V_C} \quad (14)$$

$$C = 333.33\mu F$$

IV. PROPOSED SVPWM SCHEME FOR Z-T NPC MLI

The Z-source MLI SVPWM schemes differ from MLI, only by adding the ST-switching states. This is because, Z-Source NPC-MLI needs ST vectors to charge the inductors present in Z-network in Figure-.1In three-phase three-level Z-source MLI SVPWM uses 54 ST-states, which are connected with 27 regular switching event of MLI and providing the zero neutral-point current in every switching , which allow the DC-link capacitors balancing. However, due to the large switching ST, the inverter suffered with large switching losses which affect the inverter efficiency. In this section, explains the switching method and its self-control option to the capacitor balancing. The proposed method uses the TST and BST with regular MLI switching sequentially for considering the NP balancing.

A. Proposed ST option:

To achieve the minimal switches options between two adjacent states, the nearest three vector (NTV) switching sequence is adopted in SVPWM. The NTV is uses the nearest three switching choice and providing the three-phase current to the NP uniformly. For example; when the reference vector (V_{ref}) positioned in sub-triangle, 'Δ_{12}' in sector-1, the switching states are altered from (0-1-1) to (00-1). In this circumstances, the U phase switching state is transformed from {OFF, OFF, ON, ON} through {OFF, ON, ON, ON} to {OFF, ON, ON, OFF} to create BST to charge the inductor, L_2. Here, the four switches are taken for the lag-U (U-phase). During the switching states from (100) to (110) using the NTV method. In this situation the U-phase switching state is transformed from {OFF, ON, ON, OFF} through {ON, ON, ON, OFF} to {ON, ON, OFF, OFF} to create top-ST to charge the inductor L_1. After the end of STs, the inductor voltage (V_L) is added with input voltage (V_{DC}) and this boosted voltage ($2V_C \approx 2V_{DC}$) will appear at the inverter input terminals and MLI will convert the boosted-voltage into AC output voltage. Figure.3. illustrations the switching conversion for Δ_{12} in sector-1. Similar, in all six sectors TST and BST are used with NTV and boosting the input voltage V_{DC}.

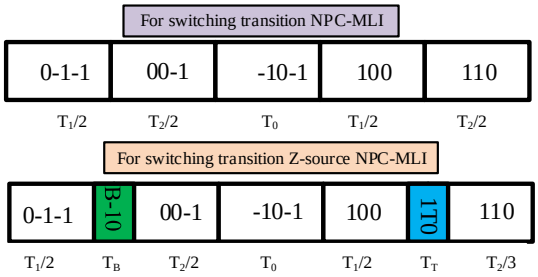


Figure.3 switching transition in linear modulation region for NPC-MLI and Z-source NPC-MLI

In the proposed SVPWM the ST operation is done only with the short vectors to achieve the TST and BST. Furthermore, the proposed SVPWM is fashioned based on the nearest three vector (NTV) switching approach [11], which ensures the circulation current flows in the capacitors. This will improve the quality of the shape of the output wave (quarter symmetry). In the simulation session the effect of capacitors balancing is discussed for both non-NTV and NTV schemes.

B. On-time calculation:

Generally the on-timings are calculated using the NTV scheme [13] in a triangle where the reference vector is located. In (15)-(18) are given the duty cycles for ST vectors and non-ST vectors.

The basic target vector with respect to volt-sec is

$$V_{ref} = T_1V_1 + T_2V_2 + T_0V_0 \quad (15)$$

Here, $T_1 = T_s(V^s_{\alpha o} - V^s_{\beta o}/\sqrt{3})$; $T_2 = T_s(V^s_{\beta o}/h$; $T_0 = T_s - T_1 - T_2$.

In BST based triangle ST periods are created by splitting the on-timing of T_0.

$$T_0 = T_T + T_B + T_{0(active)} \quad (16)$$

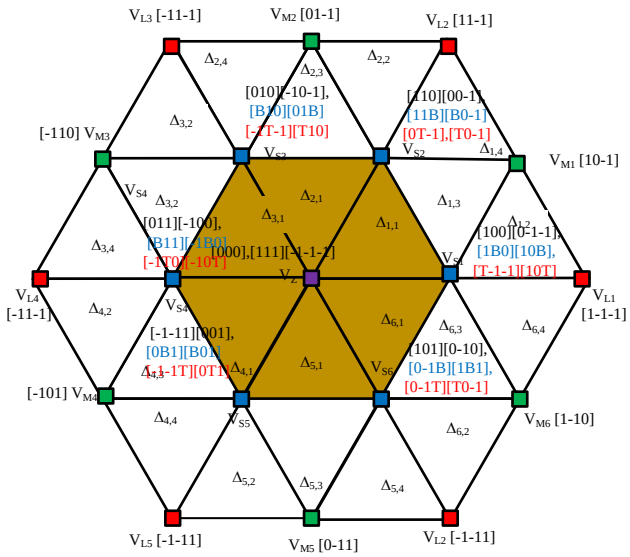


Figure.4. SVD for SVPWM scheme

In TST based triangle ST periods are created by splitting the timing of T_1 and T_2, since the ST creation in medium vector will disturb the inverter pole voltage.

$$T_1 = T_T + T_{1(active)} \quad (17)$$

$$T_2 = T_B + T_{2(active)} \quad (18)$$

C. SVPWM for the Z-MLI SVPWM:

Firstly, the three-phase voltage vectors are converted to two-phase using Park's transformation. The sector number S_i and angle in each sector γ is found by using the angle of the V_{ref} (θ). Each sector will be having four sub-triangles. If the V_{ref} lies in the sub-triangle 0 and 3 can be found easily by calculating rhombus calculations are to be performed using the slope of the reference vector. In the calculation of the sub-triangle, the Z-source SVPWM uses the published paper logic [13]. Once the sub-triangle number is identified, the ST vectors should be identified. Once the ST switching vectors are identified, the total on-time period should be split for ST and non-shoot-through operations.

Advantages of New SVPWM scheme

- Uses only 24 ST switching vectors, which reduces the complexity.
- The redundant technique on time calculation is easy and leads to easy timing calculation and hardware implementation.

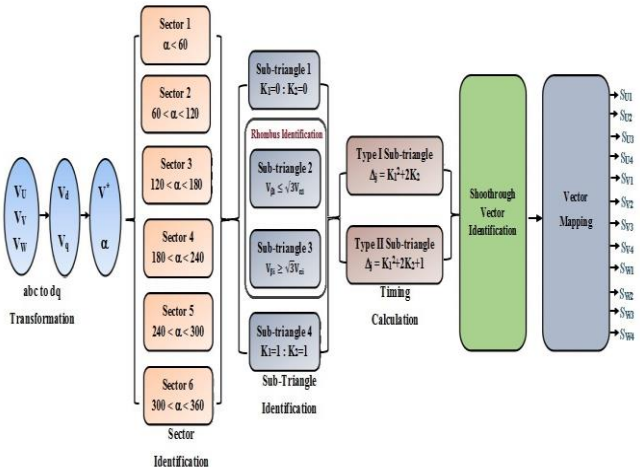
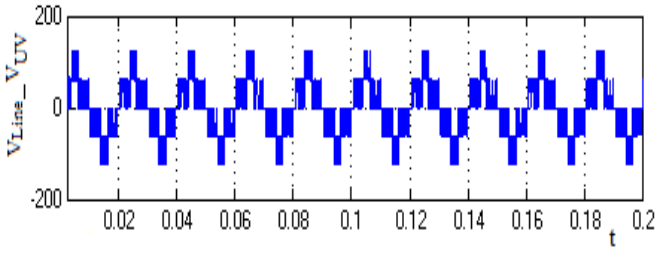


Figure.5. Proposed SVPWM switching pulse generation

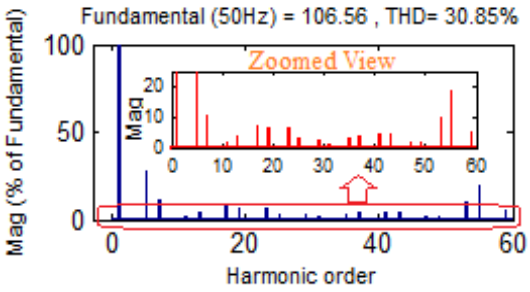
V. SIMULATION RESULTS & ANALYSIS

The performance of the Z-source SVPWM for Three-phase three-level Z-T NPC-MLI with an RL load is studied through MATLAB/Simulink 2013.a simulation. The input DC-link voltage is sustained as 100V with the aid of DC. The values of capacitance and inductance in the Z-source network are 340μF and 10 mH. The IGBT with a parallel diode for commutation is used as the switch in the circuit, the internal

resistance of IGBT is considered as 1mΩ and snubber resistance is 10μΩ [15]. Two equal capacitors are considered across the supply to split the supply voltage (V_{DC}) into two equal ($V_{DC}/2$) shares and to create a neutral-point voltage. The B is fixed to be 1.67. As a result for an input DC supply, V_{DC} =100V, theoretical output should be 142V in linear modulation range. The Figure.6. shows the line voltage (V_{Line}) and THD spectra at under modulation, M_a=0.6. Here, the V_{Line} and percentage of THD is observed to be 106.56V and 14.85%. The V_{Line} will be very low at the lower modulation indices because the on-time of the MLI will be less during this period, then the V_{Line} gradually increases with the increase of the M_a. Next, the proposed SVPWM is tested for extreme of linear modulation range (m_a=0.9) as shown in the Figure.7. At this M_a, the inverter delivered its maximum output link voltage as 164Vwith considered harmonics spectra of 31.38%. Based on the results it is evident that the proposed PWM, delivers the maximum output based on eq.(6). In addition, the proposed PWM output V_{line} and its respective % THDs are comparatively better when compared to the reported methods [6,11]. The main reason for the improvement of the V_{line} in Z-T NPC-MLI is due to employment of T-Type NPC-MLI rather than conventional NPC-MLI, which reduces the conduction losses to a better extent. The harmonics spectra and waveform quality improved by the selection of proper ST time periods by using the proposed SVPWM scheme. Figure.8 presents the different M_a performances for V_{line} and %THD of Z Source TMLI. Due to the redundancy and NTV switching logic, the -link capacitors (C_1 and C_2), whereas regular Z-SVPWM will not bother about the DC-link balancing. Figure.9. illustrates the capacitor balancing proposed–NTV based SVPWM and regular SVPWM. Based on the results, it could be deduced that the proposed scheme not only uses less ST States, but also balances the NP control, which makes better output quality.

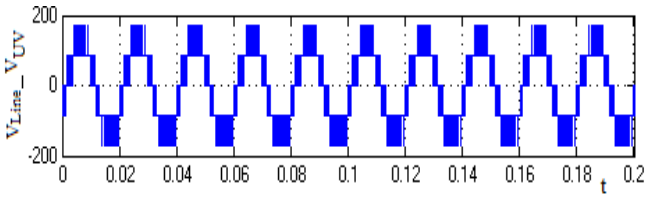


(a)

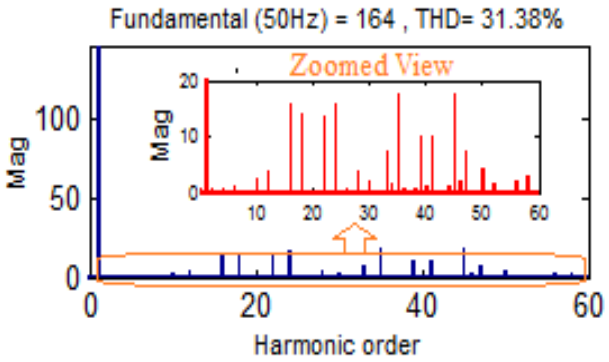


(b)

Figure.6 Simulation results for m_a=0.6; (a). line voltage(V_{LINE}), (b) m_a=0.5



(a)



(b)

Figure.7 Simulation results for m_a=0.8; (a). line voltage(V_{LINE}), (b) m_a=0.9

TABLE II- SIMULATION RESULT COMPERISION OF REGULAR SVPAM AND PROPOSED SVPWM FOR DIFFERENT M_a

M_a		0.2	0.4	0.6	0.8	0.907
Con SVPWM	V_{LINE}	40.7	69.5	102.1	136.7	156.9
	%THD	64.37	56.82	57.26	56.82	57.59
	%NPF	2.7	2.7	3.5	4.7	6.3
Proposed SVPWM	V_{LINE}	41.2	70.9	106.56	142.1	164
	%THD	34.37	36.82	30.85	31.82	31.38
	%NPF	2.7	2.7	2.8	2.9	2.9

Conduction Losses comparison

The Total conduction losses of the Z-T-NPC-MLI and conventional Z-NPC-MLI are calculated and plotted in Figure.9. for various M_a. These values are verified with the simulated tests. From the graph, it can be seen that the conduction losses are low throughout the operating value of M_a, which leads to better of Z-T-NPC-MLI.

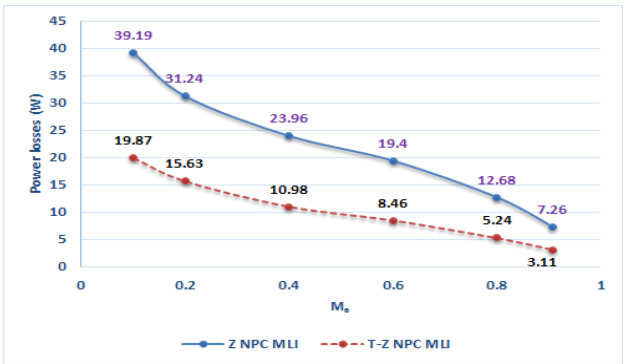
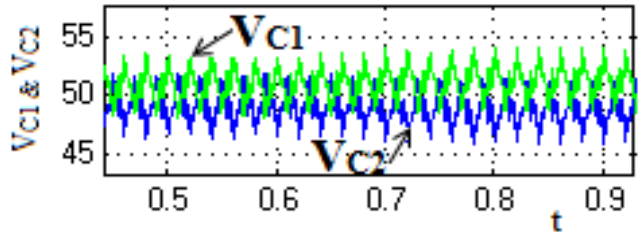
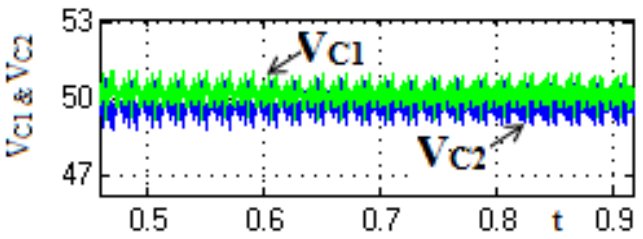


Figure.8 Conduction losses comparison of Z-T NPC-MLI and conventional Z Source NPC-MLI



(a)

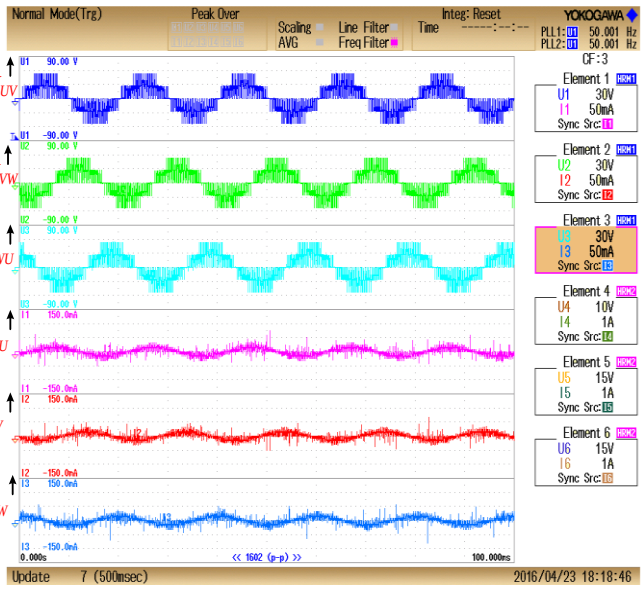


(b)

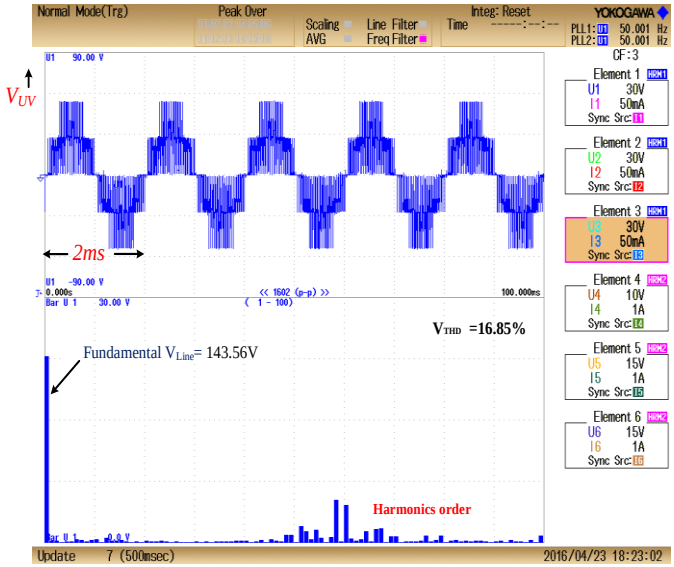
Figure. 9 Z-T NPC-MLI DC-link capacitors balancing simulation results; (a) Conventional ZSVPWM,(b) proposed ZSVPWM.I

VI. EXPERIMENTAL ANALYSIS

The simulation performance of the proposed SVPWM for Three phase - three level Z-T NPC MLI with an RL load is examined through FPGA based 1Kw Z-T NPC MLI simulation study was conducted. The input DC-Link voltage is maintained as 100V with the help of direct DC Source from 0 to 200 V RPS. The values of capacitance and inductance in the Z source network are 340μF and 10 mH respectively. The IGBT with a parallel diode for commutation is used as the switch in the circuit, the internal resistance of IGBT is considered as 1mΩ and snubber resistance is 10μΩ [22]. Two equal capacitors are considered across the supply to split the supply voltage into two equal halves and to create a neutral point. The boosting factor is considered to be 1.67. As a result, for an input DC supply voltage of 100V, theoretical output should be 142V in linear modulation. The Figure. 10, shows the line voltage (V_{Line}) and THD spectra at under modulation, M_a=0.9. Here, the V_{Line} and percentage of THD is observed to be 143.56V and 16.85%. Due to the redundancy ST switching logic, the DC-link capacitors (C_1 and C_2), is maintained their balancing and maintaining the NP. The Figure.11 (a) and (b) show the DC-link capacitors V_{C1} and V_{C2} voltages. Based on the results, it could see that the proposed SVPWM balancing the capacitors closely and ensuring the symmetry voltage waveform.



(a)



(b)

Figure. 10 Experimental line voltage (V_{LINE}), and its respective THD spectra at m_a=0.907.

From the experimental results, it is evident that the proposed SVPWM for Three-phase three-level Z- source T NPC-MLI gave a similar performance to simulation result obtained. The proposed Z-source SVPWM is compared with I-type NPC-MLI and T-NPC-MLI and the results are listed. For this comparisons, the both the MLIs are operated in m_a range from 0.4 to 0.8.

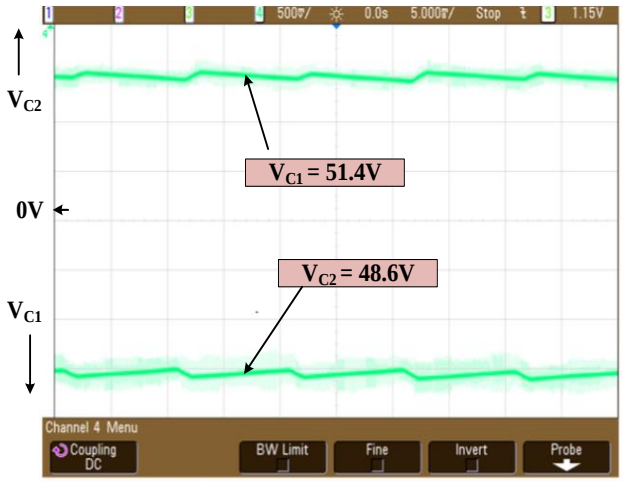
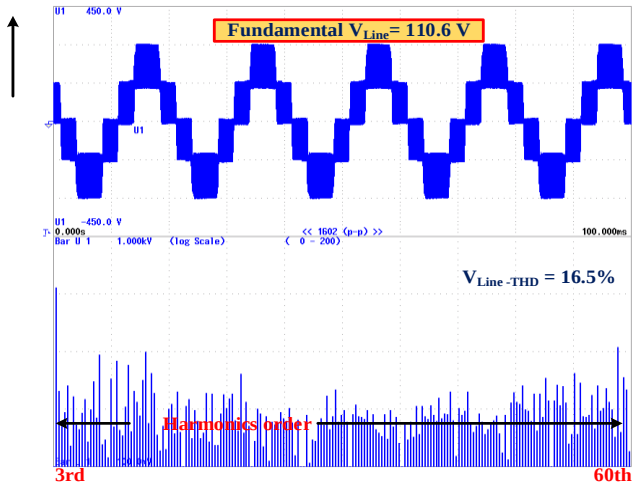
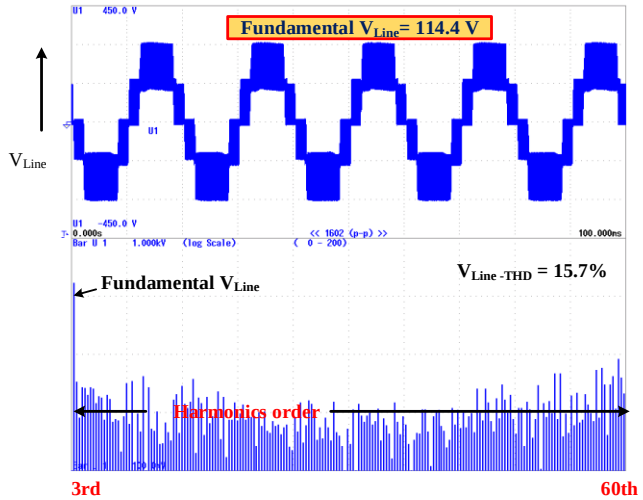


Figure. 11 Experimental Z-T NPC-MLI DC-link capacitors balancing for proposed ZSVPWM.I



(a)



(b)

Figure.12 Experimental line voltage (V_{LINE}), and its THD m_a=0.907;(a)Z-source I NPC-MLI,(b)Z-source T NPC-MLI.

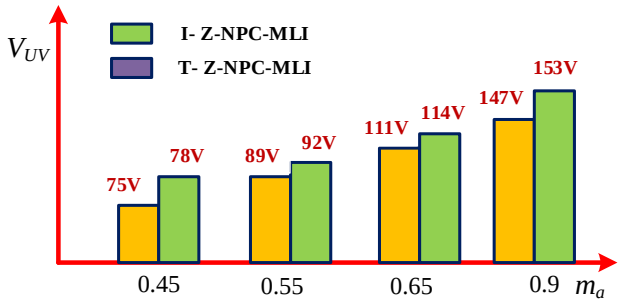


Figure.13 Experimental results; line voltage comparison between I-type and T type Z-source NPC-MLI

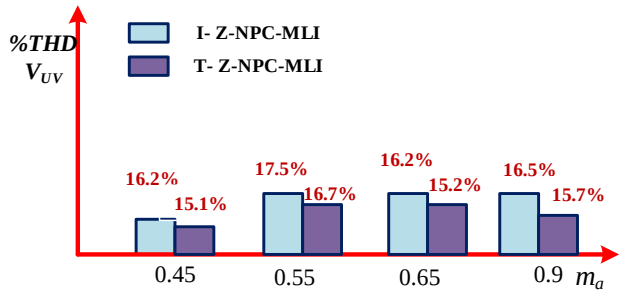


Figure.14 Experimental results; line voltage THD comparison between I-type and T type Z-source NPC-MLI

The inverters input voltages are fixed for 100V for this comparative study. Figure 12.(a) and 12.(b) are shows experimental results line voltage and its THD performance comparisons between I-type and T type Z-source NPC-MLI. From the results T-Z-source NPC-MLI show the better performance then I-type MLI. The fundamental line voltages are more in all the range of modulation Indies. The main reason for the improvement of the V_{line} in Z-T NPC-MLI is due to employment of T-Type NPC-MLI rather than conventional NPC-MLI, which reduces the conduction losses to a better extent. The efficiency of the inverter calculated for both I-type and T type Z-source NPC-MLI from the conduction losses. The T type Z-source NPC-MLI efficiency is estimated as 94.4% at m_a=0.9, whereas I-type has 91.3%. Based on the experimentation results and analysis, the T type Z-source NPC-MLI is provides a better with help of proposed Z-source SVPWM with minimal ST switching events.

V.CONCLUSION

A novel Z-T NPC MLI is implemented using the new SVPWM scheme and operated in the entire modulation region both in shoot through mode and non-shoot through mode. This proposed SVPWM scheme uses redundant technique, which provides the equal switching stress to all the phases which improves the performance of the inverter for long operations. Even though with the use of less

number of shoot through vectors more boosting factor of 1.67 is achieved for the inverter which reduces the complexity in the switching of the inverter. The conduction losses calculation is done for Z-T NPC-MLI and conventional Z source NPC-MLI. The conduction losses of the Z-T NPC-MLI are much lower when compared to conventional Z source NPC-MLI; this indicates that the designed Z-T NPC-MLI is the most efficient Z source inverter. The simulation and experimental results of three-level Z-T NPC-MLI inverter fed RL load with various modulation indices are implemented through MATLAB/SIMULINK 13.a and hardware realization is done using improved FPGA implementation. The novel Z-T NPC MLI has better boosted line voltage and THD profile when compared to the conventional Z source NPC0MLI discussed by various authors in the literature.

- As redundant scheme is used in SVPWM scheme the switching stress will be uniform, thus reducing the complexity in timing calculations and can be implemented in hardware easily.
- Only 24 shoot through states out of 54 possible shoot through states are used, which reduces the complexity in the SVPWM scheme.
- Improved FPGA implementation enables the advantage of less device utilization. Therefore, the device memory saved by using improved FPGA implementation can be used for the other purposes like the developments in the scheme or closed loop operation.

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