A NEW MULTILEVEL INVERTER WITH MINIMUM NUMBER OF SWITCHES AND REDUCTION IN THD

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Abstract: *The main objective of this paper is to propose a new single phase asymmetrical type multilevel inverter with minimum number of switches. The proposed multilevel inverter consists of level creator unit which generate only positive levels of outputs. The H-bridge inverter is added to change the polarity of the output voltage. The comparison between the proposed topology with existing inverter topologies is presented. The proposed inverter consist of six voltage sources, 11 main switches and 4 H-bridge inverter switches. Different algorithms are used to calculate the switching angles and the results are compared with the reference. The proposed inverter produces output voltage waveform with minimum THD as compared with the reference. The computer based simulation model is developed using MATLAB/SIMULINK software to verify the function of the proposed inverter.*

Key words: *Multilevel inverter, Switching angle, Symmetric, Asymmetric, THD.*

1. Introduction

The concept of multilevel inverters is introduced in 1975 [1]. The term 'multilevel' began with three-level converter and then several multilevel topologies have been proposed over the last few decades. The basic concept of multilevel inverter is to synthesize the staircase output voltage from the several low or medium DC voltage sources. It achieves high power ratings and enables the use of renewable energy resources, capacitors or batteries as inputs. It has received major interest by the researchers because of their inherent advantageous features such as low distortion, high power quality, low dv/dt stress, minimum switching losses and better electromagnetic interference [2]. The major drawback of the multilevel inverter is it requires greater number of power electronic switches and associated gate driver circuit to achieve higher output levels.

The conventional topologies of multilevel inverters are diode-clamped, flying capacitor and cascaded H-bridge inverters[2-6]. In diode-clamped multilevel inverters, diodes are used as a clamping devices. The n-level diode-clamped multilevel inverters requires n-1 switching pairs and n-1 capacitors for clamping DC voltage[2]. The switches are operate at low switching frequency. The main advantage is that the diode transfers very limited amount of voltage and thereby reduces the stress on the switching devices. However, it requires more number of clamping diodes to achieve higher level of output voltage and hence increases the cost and size. The capacitor clamped multilevel inverter uses capacitors instead of clamping diodes which controls both the real and reactive power flow. The large number of clamping capacitors helps to ride through short duration outages and deep voltage sags [3]. The major drawbacks includes need of large number of storage capacitors, pre-charging of capacitors, high switching losses, poor efficiency, more expensive and bulky. The cascade H-bridge multilevel inverter consists of full H-bridges with independent DC voltage sources. Each full H-bridges provide three different levels of voltages like zero, positive DC and negative DC voltages. The main advantages include robustness and ease of control. The number of output voltage levels depends on the number of individual H-bridges and is given by 2k+1, where k is the number of H-bridges[4-6]. The multilevel inverter can be symmetric or asymmetric. In symmetric multilevel inverter, the values of all DC voltage sources are equal and has the advantage of high modularity. However, the values of DC voltage sources are different in asymmetrical inverter and hence it loses modularity.

Modern-day researchers focused on developing new topologies of multilevel inverters, novel pulse-width modulation (PWM) techniques and improved control techniques for various applications. This paper proposes a new multilevel inverter with reduction in number of power electronic switches. The proposed inverter produces 33 level output voltage during asymmetrical mode with minimum THD. The simulation results are presented in Section-5.

2. Existing Multilevel Inverter Topologies

The asymmetric multilevel inverter proposed in [7] is shown in Fig.1(a). This inverter able to bypass or conduct the DC voltage sources separately to generate the desired voltage levels. The relation between the number of levels 'n' and number of switches 'ns' used is given by $n = 2^{(ns-2)/2} - 1$. Fig. 1(b) shows double source sub-multilevel inverter

proposed in [8]. This topology consists of level generator unit and polarity changing unit. The level generating unit consists of single and double source sub multilevel inverter and H-bridge inverter acts as a polarity changer. The drawback of this topology is it have separate structure for even and odd number of DC voltage sources. The relation between the number of levels 'n' and number of switches 'ns' used is given by n = 2(ns)-7.

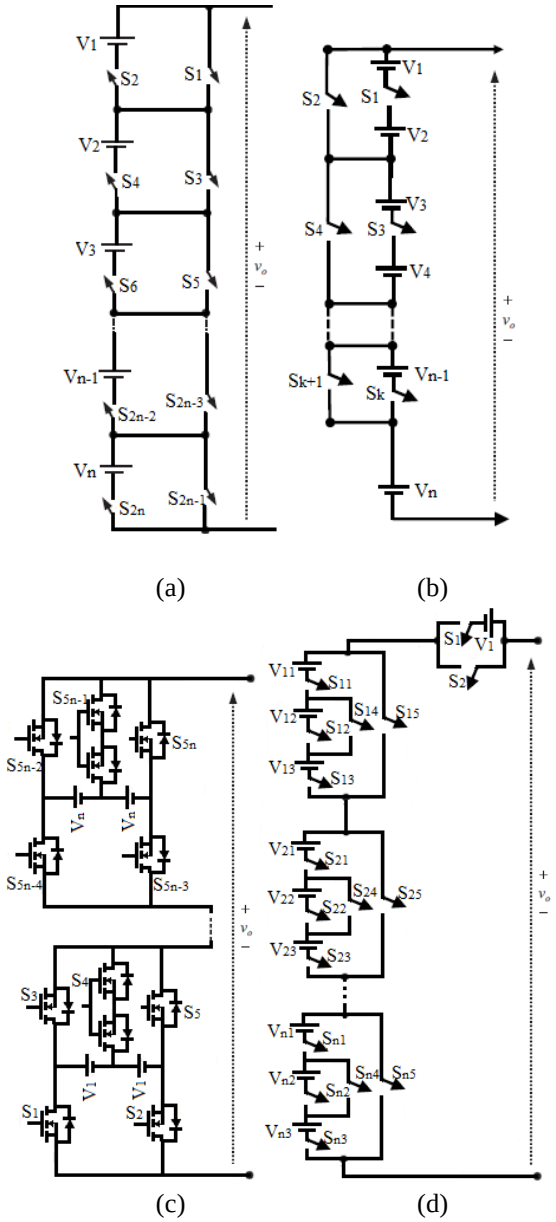


Fig. 1. Existing topologies of Multilevel Inverter (a) Ref.[7], (b) Ref. [8], (c) Ref. [9] and (d) Ref. [10].

The cascaded sub-multilevel cells based inverter proposed in Ref.[9] is shown in Fig. 1(c). It operates in both symmetric and asymmetric state. This topology needs minimum number of bi-directional switches and great number of IGBTs. This paper presented four different algorithms to calculate the magnitude of DC voltage sources. Another topology of multilevel inverter proposed in Ref. [10] is shown in Fig. 1 (d). The basic unit consists of three DC voltage sources and five switches to achieve five level output voltage. The major drawback of this topology is it is not able to generate V_{dc} level of voltage. To achieve this level, an additional DC voltage source of amplitude Vdc and two unidirectional power switches are connected in series with the basic units.

In this paper, the new topology of multilevel inverter with reduced number of power switches have been proposed. The proposed inverter achieves 33 level output voltage during asymmetrical mode with 15 switches and 6 DC voltage sources.

3. Proposed Multilevel Inverter

The proposed asymmetric type 33-level inverter topology is shown in Fig. 2.

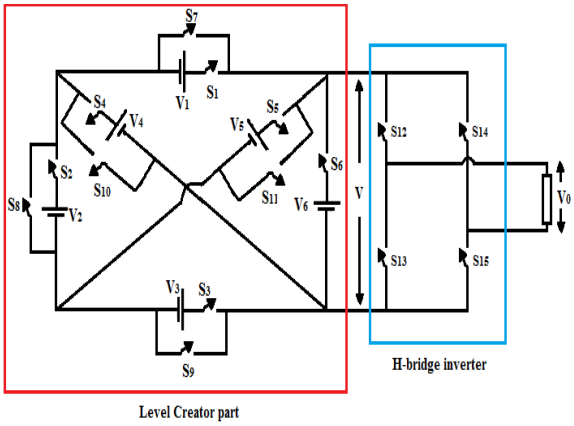


Fig. 2. Proposed topology of Multilevel Inverter

The proposed inverter consists of two units: (1) level creator unit and (2) polarity changing unit. The level creator unit consist of 6 DC voltage sources and 11 switches. This level creator unit produces unidirectional output voltage with various voltage levels as 0, V_{dc}, $2V_{dc}$,... and $16V_{dc}$. The voltage magnitude of each DC voltage sources are different. The polarity changing unit is simply a H-bridge inverter which helps to convert the unidirectional output voltage of the level creator unit into bidirectional output voltage. When the switches S_{12} and S_{15} are ON, positive levels of voltages are obtained and when S_{13} and S_{14} are ON, negative levels of voltages are obtained. Hence, the proposed multilevel inverter with level creator unit and polarity changing unit can able to produce 33 level of output voltage such as $-16V_{dc}$, $-15V_{dc}$, . . . , $-V_{dc}$, 0, V_{dc},. . ., $15V_{dc}$ and $16V_{dc}$.The magnitude of DC voltage sources are : $V_1= V_{dc}$, $V_2= 4V_{dc}$, $V_3=$

$10V_{dc}$,V_4= $7V_{dc}$, V_5= $6V_{dc}$, and V_6= $12V_{dc}$. The switching states for the level creator unit of the proposed multilevel inverter during asymmetrical mode are given in Table 1. When the switches S_{12} and S_{15} are ON, 16 levels of positive voltages are obtained with the above mentioned switching states. Similarly, when S_{13} and S_{14} are ON, 16 levels of negative voltages are obtained with the above mentioned switching states. The zero level is also obtained for any of the following switching conditions: (1) S_{12} and S_{14} are OFF and (2) S_{13} and S_{15} are OFF. At any switching condition, maximum 3 switches of the level creator unit are ON. Therefore, the total number of conduction switches for the proposed inverter topology is 5 i.e., three switches in the level creator part and 2 switches in the polarity changing unit.

Table 1
Switching states

Voltage	**S_1**	**S_2**	**S_3**	**S_4**	**S_5**	**S_6**	**S_7**	**S_8**	**S_9**	**S_{10}**	**S_{11}**
$16V_{dc}$	0	0	1	0	1	0	0	0	0	0	0
$15V_{dc}$	1	1	1	0	0	0	0	0	0	0	0
$14V_{dc}$	0	1	1	0	0	0	1	0	0	0	0
$13V_{dc}$	0	0	0	1	1	0	0	1	0	0	0
$12V_{dc}$	0	0	0	0	1	0	0	0	0	0	0
$11V_{dc}$	1	0	1	0	0	0	0	1	0	0	0
$10V_{dc}$	0	0	1	0	0	0	1	1	0	0	0
$9V_{dc}$	0	1	0	1	1	0	0	0	0	0	0
$8V_{dc}$	1	0	0	1	0	0	0	0	0	0	0
$7V_{dc}$	0	0	0	1	0	0	1	0	0	0	0
$6V_{dc}$	0	0	0	0	1	0	0	0	1	0	0
$5V_{dc}$	1	1	0	0	0	0	0	0	1	0	0
$4V_{dc}$	0	1	0	0	0	0	1	0	1	0	0
$3V_{dc}$	0	1	0	1	0	0	0	0	0	0	1
$2V_{dc}$	0	1	0	0	1	0	0	0	0	1	0
V_{dc}	1	0	0	0	0	0	0	0	0	1	0
0	0	0	0	0	0	0	1	1	1	0	0

The comparison of the output voltage levels with the number of DC voltage sources and the number of switches for different multilevel inverter topologies are given in Table 2. The comparison of power components requirements for 33-level inverter is given in Table 3.

Table 2
Comparison of different Multilevel Inverters

Inverter	**Number of DC Sources**	**Number of Switches**	**Number of level**	**ON state switches**
[14]	6	12	23	5
[15]	6	12	25	5
[16]	6	14	17	6
[17]	6	16	23	8
[18]	6	16	31	8
[19]	6	18	29	9
Proposed inverter	**6**	**15**	**33**	**5**

Table 3
Comparison of power components requirements for 33-level inverter

Inverter	Number of DC sources	Maximum output voltage	Number of switches (IGBTs and drivers)	Maximum Voltage rating of main switches	Voltage rating of Half-bridge switches
[14]	8	$16V_{dc}$	15	$14V_{dc}$	$16V_{dc}$
Proposed	6	$16V_{dc}$	15	$14V_{dc}$	$16V_{dc}$

It is observed that, the presented inverter topology requires same number of switches to synthesize the 33- level output voltage as compared with [14]. In addition, the rating of these switches are also same. However, the topology presented in [14] requires greater number of voltage sources to synthesize 33-level output voltage as compared with the proposed inverter topology. From the above table, it is clear that the proposed multilevel inverter uses minimum number of switches and DC voltage sources to achieve higher output voltage level. In addition, it is also observed that the number of switches in the current conduction path for the proposed inverter topology is very less as compared with other presented topologies. This helps to reduce the switching losses and thereby increases the efficiency of the inverter.

4. Switching Angle Calculation

Switching angles plays an important role in the reduction of total harmonic distortion (THD). For 'n' level inverter, 2(n-1) switching angles has to be determined [11]. The switching angles corresponding to the period 0^o to 90^o are called as main switching angles. An 'n' level inverter has (n-1)/2 main switching angles. It is enough to determine the (n-1)/2 main switching angles and the other switching angles are obtained from the main switching angles using the following relations [11, 12]:

1. For period 0^o to 90^o
   $= \theta_1, \theta_2, \ldots, \theta_{(n-1)/2}$.
2. For period 90^o to 180^o
   $= \theta_{(n+1)/2}. \ldots, \theta_{(n-1)}. = (\pi-\theta_{(n-1)/2}),. \ldots,(\pi-\theta_1)$.
3. For period 180^o to 270^o
   $= \theta_n, \ldots, \theta_{3(n-1)/2} = (\pi+\theta_1),. \ldots,(\pi+\theta_{(n-1)/2})$.
4. For period 270^o to 360^o
   $= \theta_{(3n-1)/2}, \ldots, \theta_{2(n-1)} = (2\pi- \theta_{(n-1)/2}),. \ldots,(2\pi-\theta_1)$.

Algorithm - 1

$$\theta_k = k\frac{180^0}{n}, k = 1,2,\ldots,\left(\frac{n-1}{2}\right)$$

Algorithm - 2

$$\theta_k = k\frac{180^0}{n+1}, k = 1,2,\ldots,\left(\frac{n-1}{2}\right)$$

Algorithm - 3

$$\theta_k = \frac{1}{2}\sin^{-1}\left(\frac{2k-1}{n-1}\right), k = 1,2,\ldots,\left(\frac{n-1}{2}\right)$$

Algorithm - 4

$$\theta_k = \sin^{-1}\left(\frac{2k-1}{n-1}\right), k = 1,2,\ldots,\left(\frac{n-1}{2}\right)$$

The switching angles of n-level inverter is shown in Fig. 3. For the proposed multilevel inverter, there are 16 main switching angles and are determined using the different algorithms given below [11].The 16 main switching angles for the proposed multilevel inverter obtained using the above mentioned algorithms are given in Table 4.

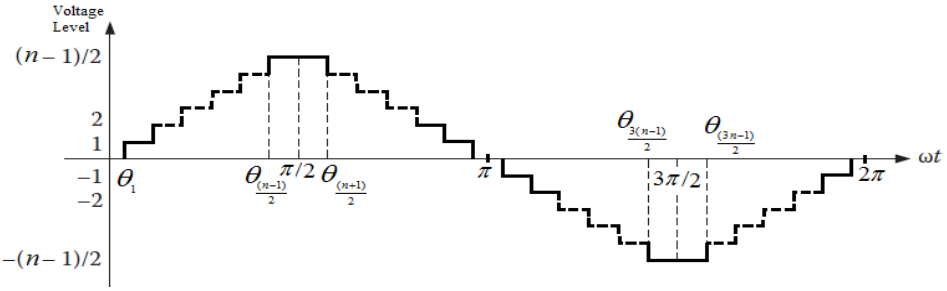
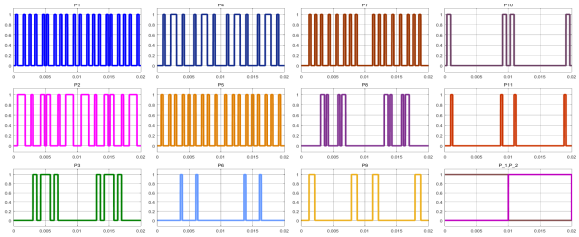


Fig. 3. Output Voltage with switching angles of 'n' level inverter

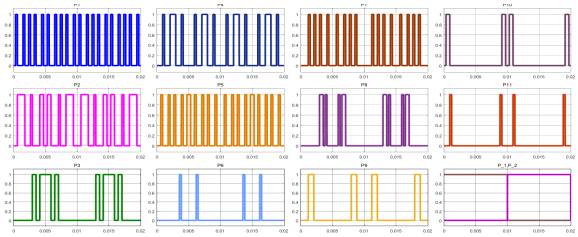
Table 4
Switching Angles

Angle	Switching Angles (in degree)			
	Algorithm - 1	Algorithm - 2	Algorithm - 3	Algorithm - 4
θ_1	5.4545	5.2941	0.8954	1.7908
θ_2	10.9091	10.5882	2.6897	5.3794
θ_3	16.3636	15.8824	4.4946	8.9893
θ_4	21.8182	21.1765	6.3178	12.6356
θ_5	27.2727	26.4706	8.1674	16.3348
θ_6	32.7273	31.7647	10.0528	20.1055
θ_7	38.1818	37.0588	11.9847	23.9695
θ_8	43.6364	42.3529	13.9766	27.9532
θ_9	49.0909	47.6471	16.045	32.09
θ_{10}	54.5455	52.9412	18.2118	36.4236
θ_{11}	60	58.2353	20.5072	41.0145
θ_{12}	65.4545	63.5294	22.9757	45.9514
θ_{13}	70.9091	68.8235	25.6876	51.3752
θ_{14}	76.3636	74.1176	28.7691	57.5383
θ_{15}	81.8182	79.4118	32.4961	64.9922
θ_{16}	87.2727	84.7059	37.8192	75.6385

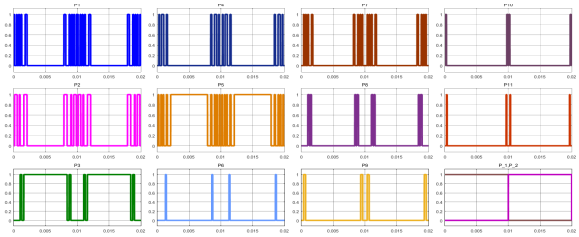
The switching pulses generated using the different algorithms are shown in Fig. 4.



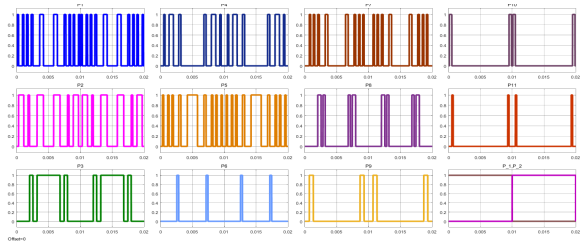
(a)



(b)



(c)

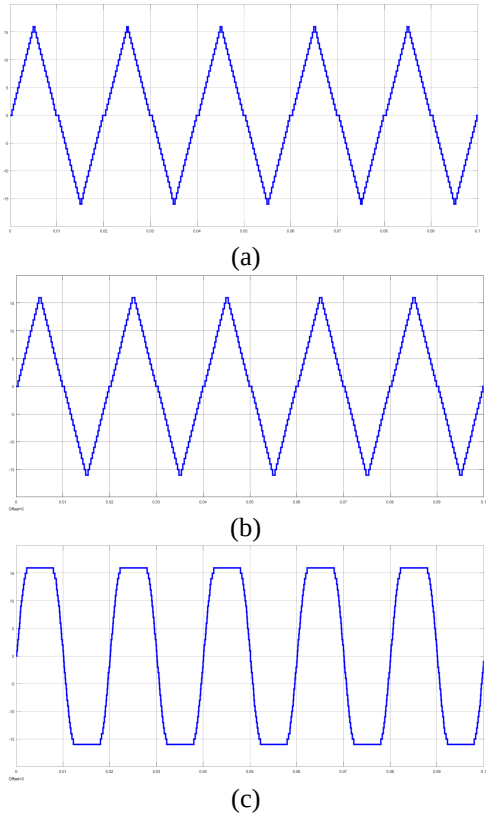


(d)

Fig. 4. Gate pulses generated using (a) Algorithm - 1 (b) Algorithm- 2 (c) Algorithm-3 and (d) Algorithm- 4

5. Simulation Results

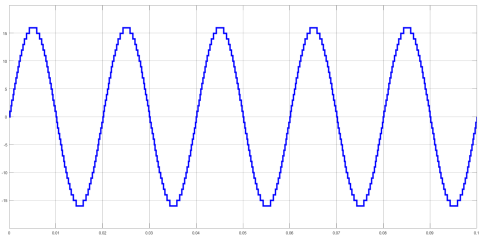
The simulation results are presented in this section. The different voltage sources have values V_1=1V, V_2=4V, V_3=10V, V_4=7V, V_5=6V, and V_6=12V. The maximum output voltage obtained is 16V (i.e. V_3+V_5). The output voltage of the proposed multilevel inverter for different algorithms are shown in Fig. 5. The result shows that the algorithm - 4 gives the output voltage similar to the sinusoidal output. The output voltage has 33 levels (i.e., 16 positive, 16 negative and 1 zero). The FFT analysis of the output voltage of the proposed multilevel inverter for different algorithms are shown in Fig. 6. The result shows that algorithm - 4 gives minimum THD of 2.50%.



(a)

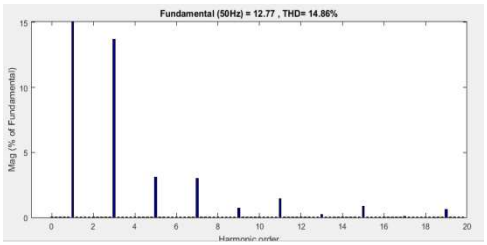
(b)

(c)

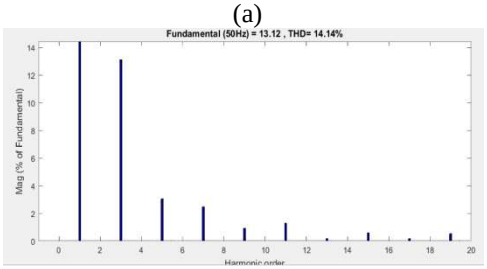


(d)

Fig. 5. Output Voltage (a) Algorithm - 1 (b) Algorithm - 2 (c) Algorithm -3 and (d) Algorithm - 4.



(a)



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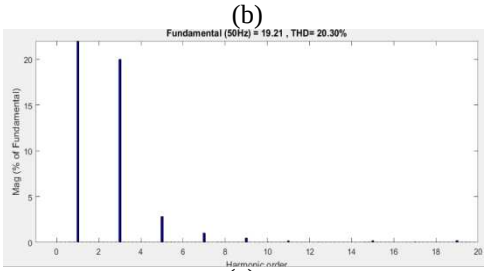
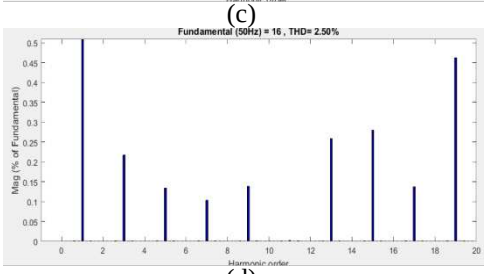


(c)



(d)

Fig. 6. FFT Analysis (a) Algorithm - 1 (b) Algorithm - 2 (c) Algorithm - 3 and (d) Algorithm - 4

Table 5 shows the comparison of the THD of the output voltage waveform obtained using different algorithms with Ref. [11] .

Table 5
Comparison of THD

Algorithm	THD (%)	
	Ref.[11]	Proposed
Algorithm - 1	14.26	14.86
Algorithm - 2	13.35	14.14
Algorithm - 3	20.46	20.30
Algorithm - 4	4.39	**2.50**

The above table shows that the proposed multilevel inverter achieves minimum THD for algorithm - 4. The proposed inverter also achieves higher output level with minimum number of switches and DC voltage sources. The measured input and output powers are about 500W and 466 W, respectively with the loss of 34W. Therefore, the efficiency of the proposed inverter is about 93.2%.

6. Conclusion

A new topology of multilevel inverter is proposed in this paper. The proposed inverter achieves 33 level output voltage with 6 DC voltage sources, 11 main switches and 4 H-bridge switches. Each voltage sources have different voltage magnitudes. The switching angles are determined using four different algorithms. A comparison of the proposed inverter topology with other existing topologies is presented in this paper. The performance of the proposed inverter is analysed using MATLAB software and the result exhibit the good performance and feasibility of the proposed inverter. The result shows that maximum voltage obtained is 16Vdc and the algorithm - 4 achieves minimum THD of the output voltage waveform.

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