Enhancement Of Power Quality Based On VSHDE Algorithm Incorporating DVR

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Abstract— **This paper presents a new meta-heuristic approach to control and generates reference currents and voltages for a Dynamic voltage restorer (DVR) to mitigate major power quality disturbances. The major disturbances that affect power quality (PQ) are voltage events such as voltage sag/swell. The synchronous reference frame (SRF) theory is used to generate the reference voltages, whereas differential evolution (DE), hybrid differential evolution (HDE), variable scaling hybrid differential evolution (VSHDE) is used to evolve proportional gain (K_p) and integral gain (K_i) values of the PI controller. The DVR comprises of voltage source converter connected to series injection transformer. Gating pulses required by the voltage source converter (VSC) of DVR is generated with the pulse width modulation (PWM) Technique. Effectiveness of the proposed work is validated by conducting simulations in MATLAB/SIMULINK software.**

Index Terms — **Power Quality, Dynamic Voltage Restorer, Variable Scaling Hybrid Differential Evolution.**

I. INTRODUCTION

In recent years, the growing need and widespread usage of electronic equipment at various levels in day to day life is perceptible. This electronic equipment, driving large machines, is a source of nonlinear impedances and sags/swells in the power utility systems. This may lead to adverse effects such as electromagnetic interference, flicker voltage distortion, low power factor, etc. These disturbances need to be addressed by power electronics engineers and researchers to diminish them [1], [2]. This power quality disturbance might also root problems related to industries ranging from not working of the system to total shutting down of the plants.

Nowadays, this research is making headway in different directions on several other issues of active power filters related to configuration, computation, control and induction. The series active power conditioner, refined based on power semiconductor technology, is presently taken as the most adaptable equipment for cutback and compensation of power quality disturbances like current harmonics and over/under voltages. In 1970's the concept of active power filter is primarily developed by L. Gyugyi [3].

H. Akagi [4] presented the three best ways of control methodologies viz. voltage detection, load current detection and supply current detection for active power filter applied in specific applications. International power quality standards for power quality problems and harmonic control in power utility systems impose some limitations on harmonics as given in [5].

Since 1970's, the power electronic based Active Power Filter (APF) is the majority opted attractive resolution to solve the power quality problems, which in turn ensures a better power distribution system. Usually, there are two types of active power conditioners connected in series as series active filter and other in shunt as shunt active filters [6], [7]. From the above context looking at Research & Development, the shunt connected active power conditioner is well-suited for reduction of harmonics in the supply current, while the series active power conditioner is best chosen to compensate voltage disturbances in load required voltage [3], [7].

In addition, DVR also has features like harmonic mitigation, reactive power compensation and power factor correction. So it is clear that, compared to other custom power devices like active power filters (APF), solid-state transfer switches (SSTS) etc., DVR is more efficient, cost effective, simple in control and responses in fast manner. This is the main reason for extensive use of the DVR out of all other custom power devices for the voltage restoration [8-10].

The required current or the voltage reference generation is done based on the reference currents and voltage theories [3-7]. The gating pulses required by VSI's are generated utilizing these referance currents and voltages. By controlling the switching of VSIs, the harmonic currents are mitigated and the sags are compensated. The PI controller, which controls the active and reactive power of VSIs, takes care of harmonic mitigation and the sags compensation. The PI controller needs the tuning of Proportional Gain (K_p) and Integral Gain (K_I) values. For linear systems with linear loads, methods like Ziegler–Nichols and Cohen-Coon tuning methods help in finding the K_P and K_I values empirically [11]. These methods are not easily applicable for a nonlinear system with nonlinear loads.

Hence, in recent years, heuristic algorithms such as Particle Swarm Optimization (PSO), , Simulated Annealing (Sa), Evolutionary Programming (EP) [12,13], Genetic Algorithm (GA)[14], Differential Evolution (DE)[15,16]and Tabu Search (TS) were implemented with Flexible Alternating

Current Transmission Systems (FACTS) devices to resolve the problems related to power systems[17]. In later recent years, many more hybrid algorithms have been introduced to enhance the search efficiency. The results obtained using the above algorithms, were promising and encouraging for further research using enhanced versions of these algorithms.

This paper proposes an enhanced HDE algorithm called as variable scaling hybrid differential evolution (VSHDE) algorithm [18-21] to solve the power quality problems. The DVR, which is a FACTS device, is incorporated to address the power quality problems in the power system like voltage swell and sag. SRF theory is used to generate reference currents and voltages. These reference currents and voltages are utilized to generate controlled gating pulses with the help of the Hysteresis Band Current Controller. By controlling switching of the VSI, harmonic currents and sags are mitigated. The PI controller in SRF theory needs the tuning of proportional and integral gain values. The K_P and K_I values of the PI controller are optimized with the help of VSHDE algorithm and are compared with its earlier versions DE and HDE algorithms.

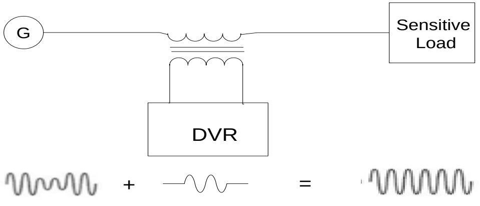

Fig.1. Single line diagram representing DVR

II. THE OPERATION OF DVR

The DVR is a solid state device connected in series as shown in Fig.1. It injects the required compensating voltage into the utility system such that the unbalanced or distorted load side voltage is regulated to the desired level [15], [16]. This phenomenon further takes care of injection of active/reactive power from the DVR to the utility [17].

The broad construction of the DVR consists of the power circuit and control circuit. The corresponding circuit diagram is as shown in the Fig. 2. The analogous circuit diagram is simply represented with an equation is as under:

$$V_{DVR} = V_L + Z_{TH} I_L + V_{TH} \quad (1)$$

where V_L is the desired load voltage magnitude, Z_{TH} is the load impedance, I_L is the load current and V_{TH} is the system voltage (during the faulty condition)

The load side current (I_L) is given by

$$I_L = \frac{P_L + jQ_L}{V_L} \quad (2)$$

When V_L is well thought-out as a reference quantity, the equation can be written as

$$V_{DVR}\angle\alpha = V_L\angle 0 + Z_{TH}\, I_L\angle(\beta - \theta) + V\angle\delta \quad (3)$$

Where α is the angle of VDVR, β is the angle of Z_{TH}, δ is the angle of V_{TH} and θ is the load power angle

$$\theta = \tan^{-1}\left(\frac{Q_L}{P_L}\right) \quad (4)$$

The complex power inoculation done by the DVR can be written as

$$S_{DVR} = V_{DVR} I_L^{*} \quad (5)$$

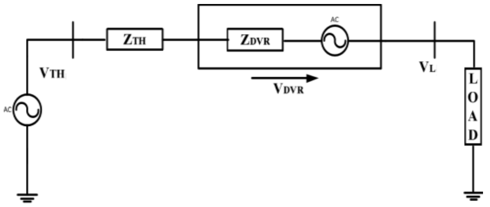

Fig.2. The equivalent circuit diagram for the single line diagram of Fig.1.

III. CONTROL OF DVR

The flow chart in Fig. 3 depicts how the DVR will be operated under sudden load/fault conditions.

At first, the line voltage (V_s) and the load voltage (V_{l1}) at the sensitive load end are measured. Under this case, measured values of both V_s and V_{L1} are maintained equal. When a sudden disturbance occurs (fault or application/ removal of load), then the magnitude of load side voltage (V_{L2}) is changed suddenly and is termed to be sag/swell. Then V_{l2} is compared with the $V_{L1.}$ If both are equal, then DVR is said to be in no operation, i.e., no voltage is injected into the line which is treated as DVR operating in Standby mode. But when V_{L2} is less/more than $V_{L1,}$ then DVR will be operating in boosting/bucking mode, i.e., the DVR will inject a sag or swell voltage ($V_{sag.}/V_{swell}$). The injection of voltage will be $V_{L1} = V_{L2} + V_{sag}$ in case of sag or $V_{L1} = V_{L2} - V_{swell}$ in case of swell. The DVR will inject/suck out the voltage till the normal voltage is reached.

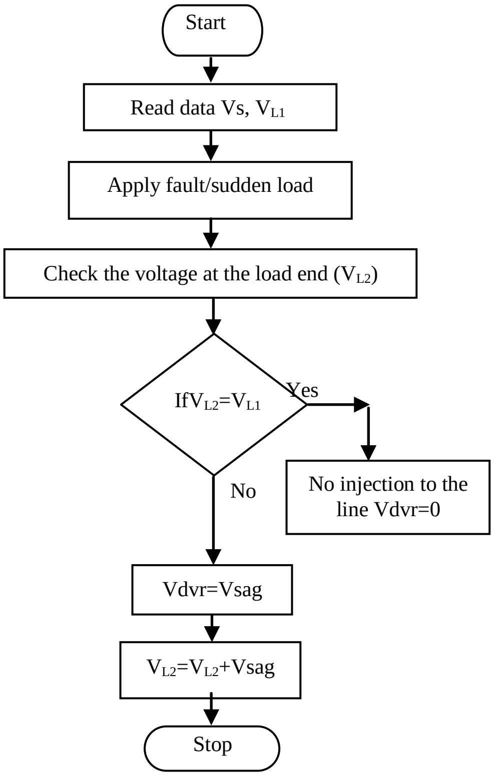

Fig.3. Flow chart of the control scheme of DVR

The necessary purpose of a controller in any DVR is to detect the voltage sag/swell power quality events in the utility system. In this paper, Synchronous Reference Frame (SRF) theory is used to control the DVR. The voltage sag can be detected when the supply voltage drops below 90% of the reference value, similarly voltage swell is above 10% of the reference value as per IEEE standard. The controller of this kind can also be used to shift the voltage in voltage source converter of the series active power conditioner into a rectifier mode and to charge the capacitor in the DC link in the absence of voltage sag/swells. The basic block representation of SRFT is illustrated as in Fig.4.

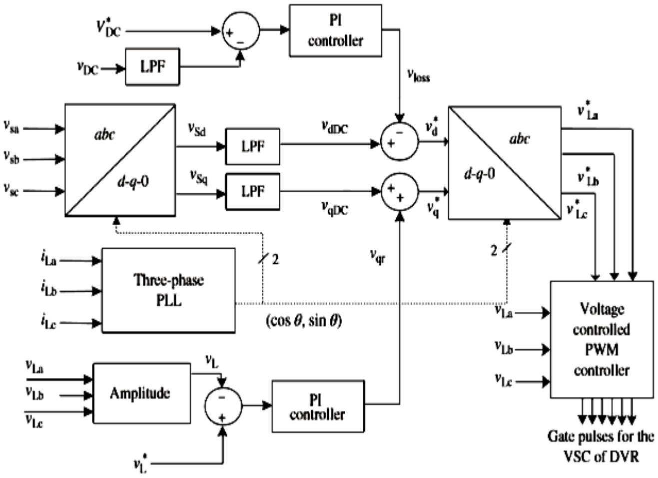

Fig.4. SRFT Control block of DVR

Park's transformation or dq0 transformation is used to maintain the power invariance, which is represented in below equations (6) and (7).

$$\begin{bmatrix} fqs \\ fds \\ f0s \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ \sin\theta & \sin(\theta - \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{matrix} fas \\ fbs \\ fcs \end{matrix}$$

$$(\mathbf{f}_{qd0s}) = \mathbf{K}\mathbf{f}_{abcs} \tag{6}$$

$$(\mathbf{f}_{abcs}) = \mathbf{K}^{-1}(f_{qd0s})^T \tag{7}$$

where '*f*' represents a voltage and

$$K^{-1} = \begin{bmatrix} \cos\theta & \sin\theta & 1 \\ \cos(\theta - \frac{2\pi}{3}) & \sin(\theta - \frac{2\pi}{3}) & 1 \\ \cos(\theta + \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) & 1 \end{bmatrix}$$

Instead of deriving the transformation for each and every particular reference, it is advantageous to derive the general transformation for any arbitrary rotating reference frame. The voltage equation (V_{sa}, V_{sb}, V_{sc}) in the three phase abc reference frame can be transformed into the stationary dq reference frame (V_d, V_q) (where d-represented as active power component, q is represented as the reactive power component). The components of voltages in the d- and q-axes are given by equations (8) and (9).

$$v_d = v_{ddc} + v_{dac} \tag{8}$$

$$v_q = v_{qdc} + v_{qac} \tag{9}$$

The error from the DC link capacitor voltage is utilized to find the amount of real voltage in phase with the line current to be injected into the utility system. The PI controller reduces the steady state as well as transient error and also increases the speed of response. After that, result is converted back to the original signal using inverse Park's transformation. These signals are combined and referred to as Reference signal (V_{sa}^*, V_{sb}^*, $VSI^* = V_{sabc}^*$). Then the reference voltage signal is compared with the actual load voltage (V_{Labc}) which gives an error signal. This error signal is used as a modulation signal to generate commutation pattern for the IGBT switches in the VSI. The pulses required for VSI are generated by means of pulse width modulation (PWM) technique.

IV. DESIGN SPECIFICATIONS

A 3-Φ, 415V, 50HZ power supply, transmission utility with nonlinear load and DVR system is developed in the MATLAB/SIMULINK using the simpower system tool box. A specification of different parameters of DVR is given in Table 1.

Design of the DVR, consists of voltage rating, current rating and KVA rating of the VSI, transformer rating, DC bus voltage and filter parameters, is illustrated as below:

Voltage rating of the VSI of DVR: The voltage rating of VSI depends on the utmost voltage to be injected in case of any voltage variations of the load. In case of self supported DVR, the injected voltage is in quadrature with the load current. So, the voltage rating of the VSI is calculated based on the load requirement. The injected voltage is estimated as;

$$V_C = \sqrt{(V_s^2 - V_L^2)} \tag{10}$$

KVA rating of the transformer: The *KVA* rating of the injection transformer is same as that of the VSI rating of DVR. *KVA* rating of the transformer is calculated as

$$S = (3V_{S*}I_S)/1000 \tag{11}$$

DC capacitor voltage:

The DC capacitor voltage is calculated based on following the relation

$$V_{dc} > 2\sqrt{2} * V_{DVR} \tag{12}$$

DC bus capacitance of the VSI: The DC bus capacitance is calculated based on how much energy is required during the change in load, it is calculated as

$$E = 1/2 * C_{dc}(V_{dc}^2 - V_{dc1}^2) \tag{13}$$

Where V_{dc} is DC bus voltage and V_{dc1} is change in bus voltage during the disturbance.

$$P * \Delta t = 1/2 * C_{dc}(V_{dc}^2 - V_{dc1}^2) \tag{14}$$

Where $P = 3 * V_C * I_S$

Ripple Filter: The ripple filter is intended to eliminate the switching frequency ripples from injected voltage. The DC side disturbance mitigating filter consists of a series connected R_r and C_r.

$$f_r = 1/(2\pi * R_{r*}C_r) \tag{15}$$

Where f_r is chosen as half of the switching frequency. The maximum and minimum limits of switching frequency are taken as 5KHz and 20KHz.

V. OPTIMAL TUNING METHODS

The present work in the paper exploit the fitness function as the minimization of THD in source current, the voltage sag and the DC link voltage. The objective function is mathematically represented as follows:

$$F = f(I_{THD}) + f(Vsag) + f(Vdc) \tag{16}$$

The optimal tuning parameters are the proportional gain (K_p) and the integral gain (K_i). The output function of the PI controller is mathematically represented by:

$$G_c(s) = k_p + \frac{k_i}{s} \tag{17}$$

The gains of the PI controller (Kp and K_I) are generated and updated by the DE, HDE and VSHDE algorithms for a given plant, as shown in Fig.5.

The output of the PI controller u(t) is given by:

$$u(t) = k_p e(t) + k_i \int_0^t e(t)dt \tag{18}$$

For the taken plant, the problem of designing a PI controller is to adjust the parameters Kp and Ki for getting a desired performance of the considered system.

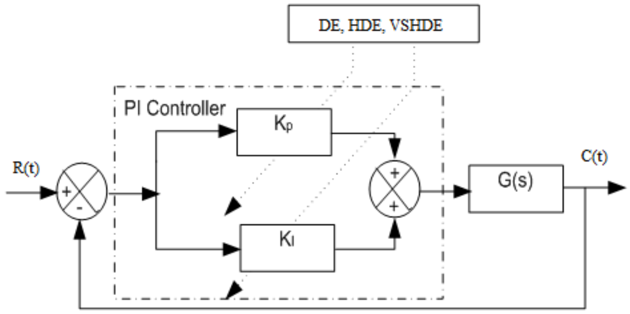

Fig.5. PI controller mechanism illustration

In this paper, three tuning methods are used; the description of each method is shown below:

Proposed VSHDE Algorithm For Power Quality Enhancement[18-21]

The variable scaling hybrid differential evolution algorithm is an improvement made for hybrid differential evolution algorithm. DE suffers from premature convergence[17]. To overcome this, migration operation is performed in HDE. But, HDE suffers from the fixed scaling factor (F) [18,19]. To overcome this drawback, variable scaling factor concept is introduced in VSHDE [20, 21].

Step 1: *Initialization*

The initial population required for the evaluation process is generated randomly and is given by the following equation.

$$U_i^0 = U_{i,\min} + rand() \,.\, (U_{i,\max} - U_{i,\min}),\ i = 1,\ldots\ldots, n_p \tag{19}$$

Where rand () denotes a uniformly distributed random number within the range [0, 1]. This produces n_p individuals of U_i^0 randomly.

During initial conditions, the process control variables are made to be within the allowable ranges.

The maximum and minimum values of the proportional gain (K_P) and the integral gain (K_I) decided heuristically are given in Table 1.

Table 1

Ranges of Control variables

Control variables	Min	Max
K_P	0	2
K_I	0	2

Step 2: Call the simulink model into the evaluation process to obtain THDs of load voltage, source current and voltage sag.

Step 3: Run the power system model network and evaluate the fitness of each individual.

Step 4: *Mutation operation*

The difference vector is the essential input in the mutation operation. The mutation operator is taken from [18] and is given below:

$$U_i^{G+1} = U_i^G + F\ (U_{best`}^G - U_i^G) + F\ (U_{r1}^G - U_{r2}^G) \tag{20}$$

Where F is the mutation constant, r_1, r_2, r_3, r_4.... are randomly chosen indices from the population, n_p.

Step 5: *Crossover operation*

The crossover aims to improve prior successes by generating offspring out of existing parent individuals. In order to increase the diversity of individuals for the next generation, the perturbed individual of $\hat{U}_i^{G+1}$ and the present individual of U_i^G are selected by a crossover constant (CR) and a random number to progress the crossover operation to generate child individuals. The purpose of CR is to determine the recombination of newly generated individuals. Each parameter j of the i^{th} individual is reproduced from the perturbed individual $\hat{U}_i^{G+1}$ and the present individual U_i^G as follows:

$$\hat{U}_{ij}^{G+1} = \begin{cases} U_{ij}^{G+1}, if\ \ rand(0,1) < CR \\ U_{ij}^G, \qquad\qquad Otherwise \end{cases} \tag{21}$$

Where $i = 1,\ldots N_p;\ j = 1,\ldots n;\ n =$ number of parameters.

Step 6: *Estimation and selection*

The fitness of the offspring is competed with its parent. If the fitness of the offspring is better than that of its parent then offspring replaces the parent. If the fitness of the offspring is worse than that of its parent, then the parent is retained. These two forms are presented as follows:

$$U_i^{G+1} = \arg\min\left\{f(U_i^G),\ f(\hat{U}_i^{G+1})\right\} \tag{22}$$

$$U_b^{G+1} = \arg\min\left\{f(U_i^{G+1})\right\} \tag{23}$$

where arg min means the argument of the minimum. Here f is the objective function that is to be minimized.

Step 7: *Migration operation if necessary*

So as to improve adequately the investigation of the search space and decrease the choice pressure to a small population, a migration operation is introduced to regenerate a new diverse population of individuals. The new population is yielded in view of the best individual X_b^{G+1}. The j-th gene of the i-th individual is given as takes after:

$$U_{ij}^{G+1} = \begin{cases} U_{bj}^{G+1} + \rho_1 \left(U_{j\min} - U_{bj}^{G+1}\right), & if \ \rho_2 < \dfrac{U_{ij}^{G+1} - U_{j\min}}{U_{j\max} - U_{j\min}} \\ U_{bj}^{G+1} + \rho_1 \left(U_{j\max} - U_{bj}^{G+1}\right), & otherwise \end{cases} \qquad (24)$$

Where ρ_1, ρ_2 are randomly generated numbers which are orderly distributed in the range of [0, 1]; $i = 1,\ldots N_p;\ j = 1,\ldots n;\ n =$ number of parameters. The migration is executed only if a measure fails to match the tolerance of population diversity. This measure is defined as follows:

$$\rho = \sum_{\substack{i=1 \\ i \neq b}}^{N_p} \sum_{j=1}^{n} \chi_{ij} \,/\, n(n_p - 1) < \varepsilon_1 \qquad (25)$$

Where

$$\chi_{ij} = \begin{cases} 1, \ if & \left| \dfrac{U_{ij}^{G+1} - U_{bj}^{G+1}}{U_{bj}^{G+1}} \right| > \varepsilon_2 \\ 0, & otherwise \end{cases} \qquad (26)$$

Parameters $\varepsilon_1 \in [0,1]$ *and* $\varepsilon_2 \in [0,1]$ respectively express the desired tolerance for the population diversity and gene diversity with respect to the best individual. Here χ_{ij} is defined as an index of gene diversity. A value of zero for χ_{ij} denotes that the j-th gene of the best individual. From eqs. (25) and (26), it can be seen that the value of ρ is in the range of [0,1]. If ρ is smaller than ε_1, then migration is performed to generate a new population to escape the local point; otherwise, migration is turned off and ordinary search direction is followed.

Step 8: *Variable Scaling of mutation constant (scaling factor) F*

The concept of the variable scaling hybrid differential evolution (VSHDE) [18] is to use the 1/5 success rule for the variable scaling factor [19, 20]. The rule of updating scaling factor is as follows [19, 21]:

$$F^{t+1} = \begin{cases} c_d \times F^t, \ if \ \rho_S^t < 1/5 \\ c_j \times F^t, \ if \ \rho_S^t > 1/5 \\ F^t, \quad if \ \rho_S^t = 1/5 \end{cases} \qquad (27)$$

Where ρ_S^t is the frequency of successful mutations measured. The initial value of the scaling factor, F, is set to 1.2 [19, 20]. The factors of C_d=0.82 and C_j=1/0.82 are used for adjustment, which should be taken place for every q iterations. The generation index q suggested by [17] is equal to 10b, where b is a constant. When the migration operator is performed, the value of the scaling factor is defined as below:

$$F = 1 - \frac{gen}{gen\max} \qquad (28)$$

Where gen and gen max are the number of the current iteration and the maximum iteration, respectively.

Whenever the scale factor is too small then it is reset as (28) to find the better solution in the solution process.

Step 9: Repeat steps 2 to 8 until maximum generation quantity is reached.

The flow chart representation of VSHDE algorithm is as shown in Fig. 6.

The hybrid differential evolution has the drawback of the fixed scaling factor. In VSHDE algorithm, the variable scaling factor is used to overcome the drawback of the fixed scaling factor. More over this alleviates the problem of selection of mutation constant in differential evolution [21].

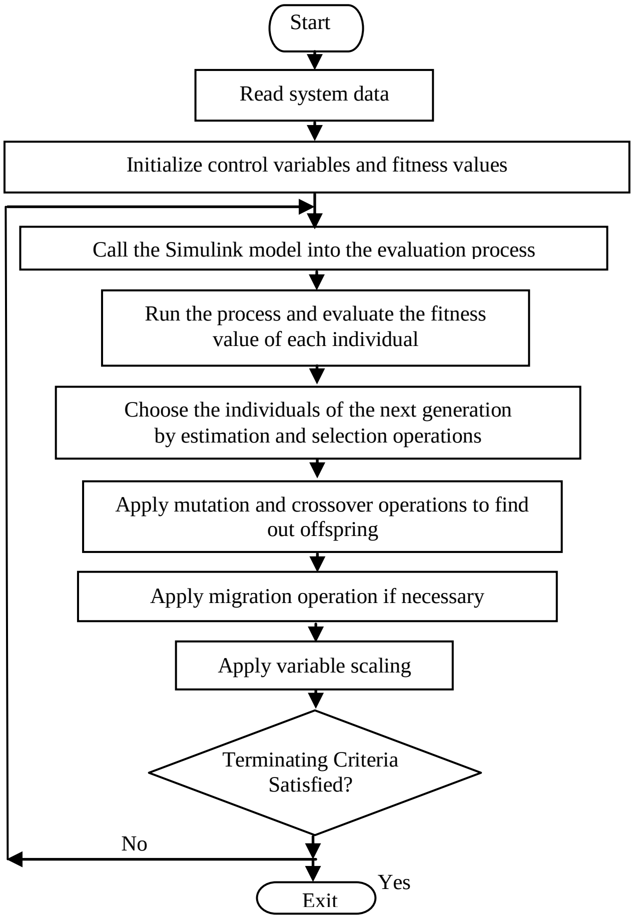

Fig. 6. Flow chart of the proposed VSHDE algorithm

VI. SIMULATION RESULTS

The simulations have been run on the MATLAB environment. The power quality disturbances focused in this paper are voltage sag/swell and current harmonics. The current harmonics are mainly caused due to nonlinear loads and voltage sag arises due to short circuits or starting/removal of large loads. The nonlinear load phenomenon is implemented with the help of power electronic converter (diode bridge rectifier). The DVR is applied to the power transmission line which is shown in the Fig.7.

The utility power supply is considered as 415V and 50Hz. Here voltage swell and then the sag is created by removing and adding a sudden load (V_{L2}) to the line through the circuit breaker phenomenon in the duration of (0.2 to 0.4) sec and (0.5 to 0.7) sec respectively, current hormonics into the system due to the nonlinear load as shown in Fig.7. The load on the system is increased/reduced by 10% as per IEEE norms to create a sag/swell which is shown as Fig. 8. In the duration of 0.2-0.4 the DVR will buck and in the duration of

0.5 to 0.7 the DVR will boost the required voltage into the system in order to maintain the presag/swell condition.

The minimization of error voltage, DC link error and current harmonics is ensured by using proposed DE, HDE and VSHDE algorithms. The main problem that one faces in voltage control is to determine the duty cycle. The primary goal is to accomplish the compensation of the required voltage all through sag/swell and the harmonic component in the source current. The Fig. 8 describes the total harmonic distortion, compensation of sag and swell and maintenance of dc-link error.

The fitness function is defined as:

Minimization of f

Where $f = (w_1)*(\text{THD of source current}) + (w_2)*(\text{THD of Load voltage}) + (w_3)*(V\text{sag})$ (29)

Where w_1, w_2, w_3 are the weights decided heuristically. The simulations have been run on the MATLAB environment with the dual core processor. The power quality disturbances focused in this paper are the voltage sag, voltage and harmonics. The current harmonics are mainly caused due to nonlinear loads and voltage sag arises due to short circuits or starting of large loads. The voltage sag is created with the help of a programmable source during 0.05-0.1 sec. DVR is applied to the power transmission line which is shown in the Fig. 7.

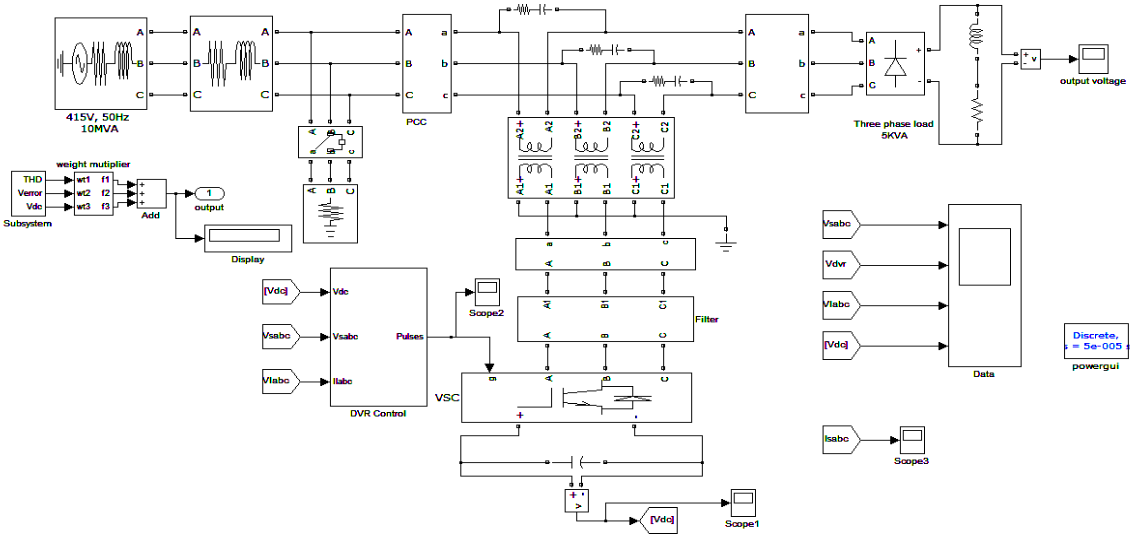

Fig. 7. MATLAB/Simulink illustration of the DVR and Transmission Line.

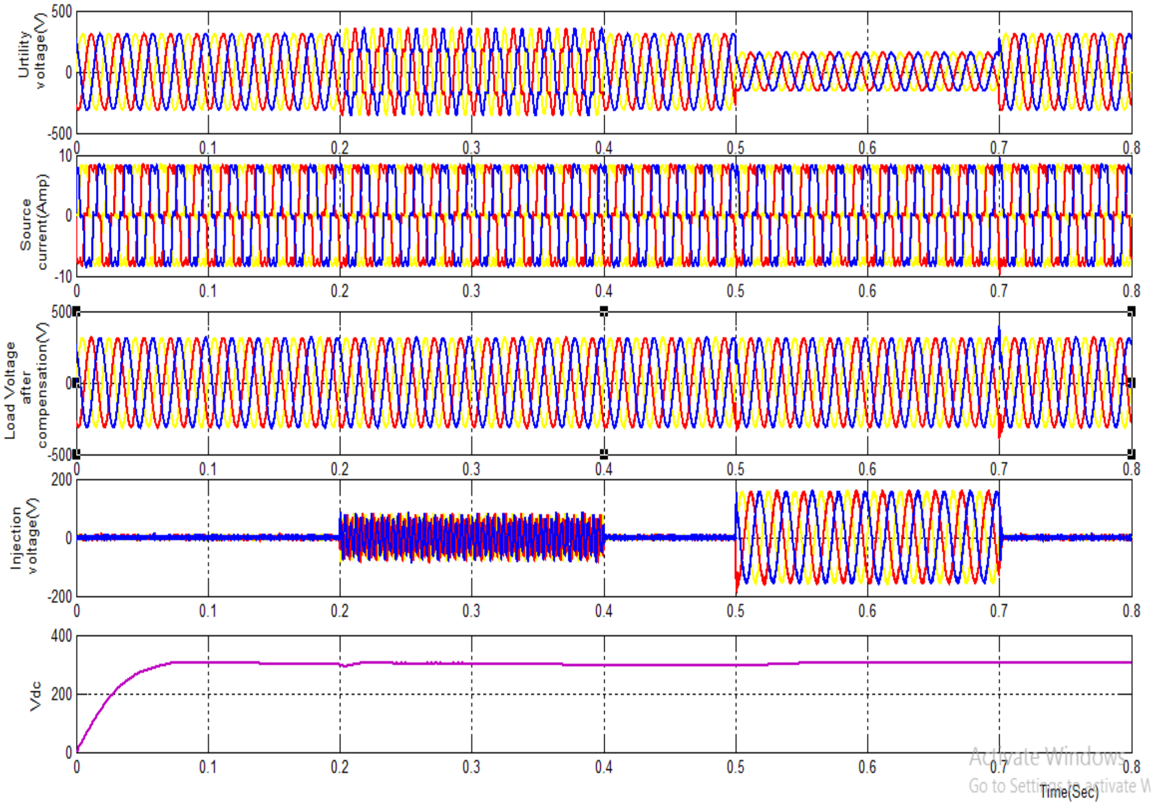

Fig. 8. Performance evaluation of DVR in utility system

The DVR complements the required compensating voltages into the line and helps to make voltage level with normal operating conditions. The complementing voltages of phases a, b and c and the load voltage after sag mitigation are shown in Fig 8.

The DC link capacitor comes into operation whenever abnormality occurs in power flow line. Here the programmable source is used for creating the voltage disturbances, the voltage during (0.2 to 0.4) sec is made swelled and during (0.5 to 0.7) sec is made dipped. Any deviation in voltage required or eased is taken care by dc link capacitor. The capacitor discharge or absorbs the energy during this ubnormal interval of time. Here during the intervals (0.2 to 0.4) sec and (0.5 to 0.7) sec the voltage is made constant with effect of the capacitor. By taking $K_{P1} = 5$, $K_{I1} = 5$, $K_{P2} = 5$, $K_{I2} = 5$; the K_p and K_i values by the expert knowledge (trial and error method) the THD of source current is 22.29% , THD of source voltage is 2.01% and load voltage has a dip variation of 10%. This way of designing the Kp and K_i values of the PI controller are designed by trial and error method particularly for nonlinear systems, but this is not a good practice.

In order to overcome this limitation and to find optimal values of K_p and K_I there is a need for evolutionary optimization techniques. VSHDE is a population based evolutionary optimization technique. The idea behind this technique is behavior of offspring, competing one-to-one with that of corresponding parents, and that represents fitness function. The optimization control variables are K_p and K_i of PI controller, where K_p and K_i are referred as proportional and integral gains respectively.

The transfer function of PI controller is represented as follows.

$$K_C(S) = K_P + (K_I/S) \tag{23}$$

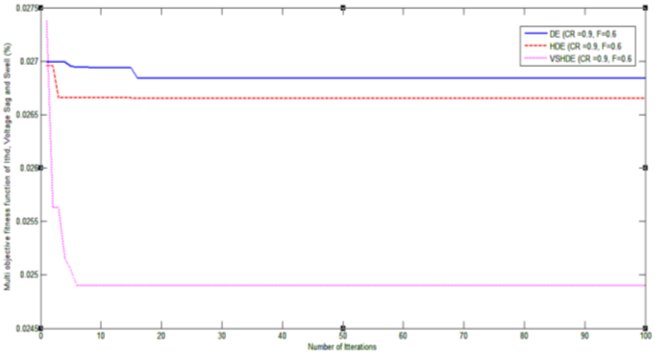

Fig. 9. Multi objective convergence of fitness (the voltage sag, source current THD and load voltage THD) with DVR using DE, HDE and VSHDE Algorithm

Here three objectives voltage sag, source current THD and load voltage THD are considered, which are assigned with weights decided heuristically (even can be optimized). The mutation constant (F) is varied in VSHDE algorithm as given in step 8 and crossover operator (CR) is varied from 0.5 to 0.9 (usually in between 0 to 1). The CR is selected in between 0.5 to 0.9 after running the dynamic simulation in between 0 to 1 as it is working better in that range.

Fig. 9. shows the comparison of multi objective convergence of fitness (voltage sag, source current THD and load voltage THD) with DE, HDE and VSHDE Algorithms

Table 2

Comparison of the UPQC performance with the PI(Trial and Error based), DE, HDE and VSHDE Algorithm.

Parameter	Is_{THD}	Vs_{THD}	Vs_{ERROR}
PI	22.29	3.018	10
DE	1.688	0.288	1.544
HDE	1.482	0.247	0.741
VSHDE	1.018	0.1680	0.504

Table 2 gives the performance evaluation with the conventional PI controller, DE, HDE and VSHDE Algorithms for the best run with the considered fitness function.

Though DE and HDE methods in the Table 3 also got THD values less than 5 % as prescribed by IEEE standards [4], it is always desirable to reduce THD as much as possible. Further reduction of THD is achieved by optimizing the PI parameters using VSHDE algorithm. This minimizes the heating of various equipment and mechanical stress on bearings and shafts of motors. This reduction in THD is achieved with optimizing the PI parameters and without any additional device or cost.

Table 3

Comparison of control parameters of UPQC with PI (Trial and Error based), DE, HDE and VSHDE Algorithm for the best run.

Parameter	PI	DE	HDE	VSHDE
K_{p1}	5	0.1863	0.1935	0.0819
K_{I1}	5	0.0103	0.0061	1.9852
K_{p2}	5	0.1863	0.1935	0.0075
K_{I2}	5	0.0103	0.0061	0.0052

The Table 3 gives the control parameter comparison with the conventional PI controller, DE, HDE and VSHDE Algorithm for the best run with the considered fitness function.

Table.4

Comparison of variation of fitness (V_{error},V_{dc} & THD) of Series APF with DE, HDE and VSHDE algorithms.

No.of Iterations	popula tion	Variation of average fitness from best fitness(after 10 runs each)		
		DE	HDE	VSHDE
100	10	0.30	0.23	0.04

Thus from the above discussion applying the proposed VSHDE algorithm the following observations are drawn:

- From Fig. 8. Performance evaluation of DVR in utility system, the voltage sag and swell during the interval (0.2 to 0.4) sec and (0.5 to 0.7) sec respectively, is compensated by the action of DC link capacitor whose action is taken care by optimal tuning of the PI controller.

- Table 2 and Table 3 clearly give the quantitative investigations that are required for critical detuning the voltage sag and swells by making the system robust at the optimal tuned kp and ki values with the respective performance evaluations.
- The proposed algorithm is run on offline mode, but it is not easy to install real time simulators at institutional level. To be efficacy with experimental determinations, each set of control variables with the corresponding mutation and crossover functions is run for 10 times each and the best, average and worst values of the fitness are observed . The best set of values is tabulated in table 2 and the variation of best vs average is tabulated in table 4.
- Finally from literature and proposed work, applying genetic algorithm over VSHDE is better for problems of this kind, as genetic algorithm is more like a framework than an algorithm which can be applied in scheduling engineering problems, whereas VSHDE is a control evolutionary algorithm.

V. CONCLUSION

In this paper, implementation of improved hybrid differential algorithm, VSHDE optimization algorithm is proposed to compensate the reactive power, and to decrease the adverse effect that occur during the starting of large machines and harmonic loads. The performance of the proposed approach is compared with the traditional PI controlled DVR. The comparative analysis of the PI controller, differential evolution, hybrid differential evolution and variable Scaling hybrid differential evolution has shown that VSHDE algorithm has been proved to be better in terms of harmonic reduction and voltage sag compensation (shown in Fig.). The DC bus voltage has been maintained constant equal to the reference voltage. The simulation results are presented to demonstrate the efficacy of the proposed algorithm.

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