A REDUCED SWITCH COUNT ASYMMETRICAL THREE PHASE MULTILEVEL INVERTER TOPOLOGY

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Abstract: A novel multilevel inverter topology for three-phase medium-voltage high power applications is proposed in this paper with a perspective to offer reduced number of power components. The topology is formulated using series connection of several fundamental inverter blocks. The fundamental block is constituted with two dc sources and six bidirectional switches by operating the topology in asymmetrical dc voltages to produce seven level output. The proposed multilevel inverter has the advantage of minimal switches in each conduction path. The simulation results are shown to prove the effectiveness of the proposed topology.

Key words: *Multilevel inverter, Asymmetrical, Operating modes, Pulse width modulation, Switch count.*

1. Introduction

The multilevel inverter becomes one of the most considerable power electronic devices for synthesizing the output voltage to suit specific application. Their competence leads to apply in high voltage aspect without affecting the voltage limit capability of power devices. This behavioral qualities benefit in good power quality, high voltage blocking capability and less EMI [1]. The first MLI structure is neutral point clamped inverter [2] which employs a series of capacitor banks to segregate the dc link voltages and succeed to voltage unbalance problems. The series of H-bridge cells are connected to synthesize stair case voltage is Cascaded H-bridge MLI which also suffers a major drawbacks of excessive H-bridge cell for higher voltage levels and each H-bridge requires multi-winding transformers [3]. The next conventional MLI is flying capacitor MLI which uses floating capacitors to clamp the voltage levels and also suffers voltage balancing problems [4]. A new multilevel inverter with a chain of dc sources arranged in cross fashion to synthesize the multilevel waveform and however the topology requires higher number of power components in its conduction path and devices with high blocking voltages [5]. A symmetric multilevel inverter using non insulated dc sources have been proposed with a view to defend reduced number of switching devices compared to conventional inverters and it has a problem of utilizing large number of bidirectional devices, an H-bridge inverter with high blocking voltages for polarity reversal and bulky high frequency transformers [6]. A dual dc source intertied with half bridge cells based multilevel inverter is proposed in [7] to produce multilevel waveform. The topology requires bulkier transformer to synthesize three phase waveform and control is complex. A hybrid multilevel inverter employing half bridge cells at each phase leg of six switch inverter is presented in [8] and the topology has circulating energy problems. A phase leg of back to back dc sources connected through six switches is addressed in [9] to offer less number of power components in multilevel inverter topologies. The topology requires switching devices with high blocking voltage which is equal to sum of dc sources. Several remarkable attempts have been made to add a boost to the innovations in multilevel topologies [10-15].

In this paper, an innovative idea in the area of three phase multilevel inverter topologies has been suggested. The detailed operation of the proposed topology is explained in section 2. The power loss analysis and comparison between the proposed and classical topologies have been addressed in section 3. Following simulation results are portrayed to corroborate the viability of the proposed inverter in medium voltage/high power applications.

2. Proposed Topology

The Fig.1 depicts the proposed three phase topology using series connected isolated dc sources, switching devices and high frequency transformers. The proposed topology is extended to any number of voltage levels with generalized dc sources as ($V_{dc1} - V_{dc(m-1/2)}$) and switching devices as ($S_{a1} - S_{a(m+1/2)}$, $S_{a1}' - S_{a(m+1/2)}$). The Table I illustrates switching sequence to drag the level magnitude in each phase per fundamental cycle.

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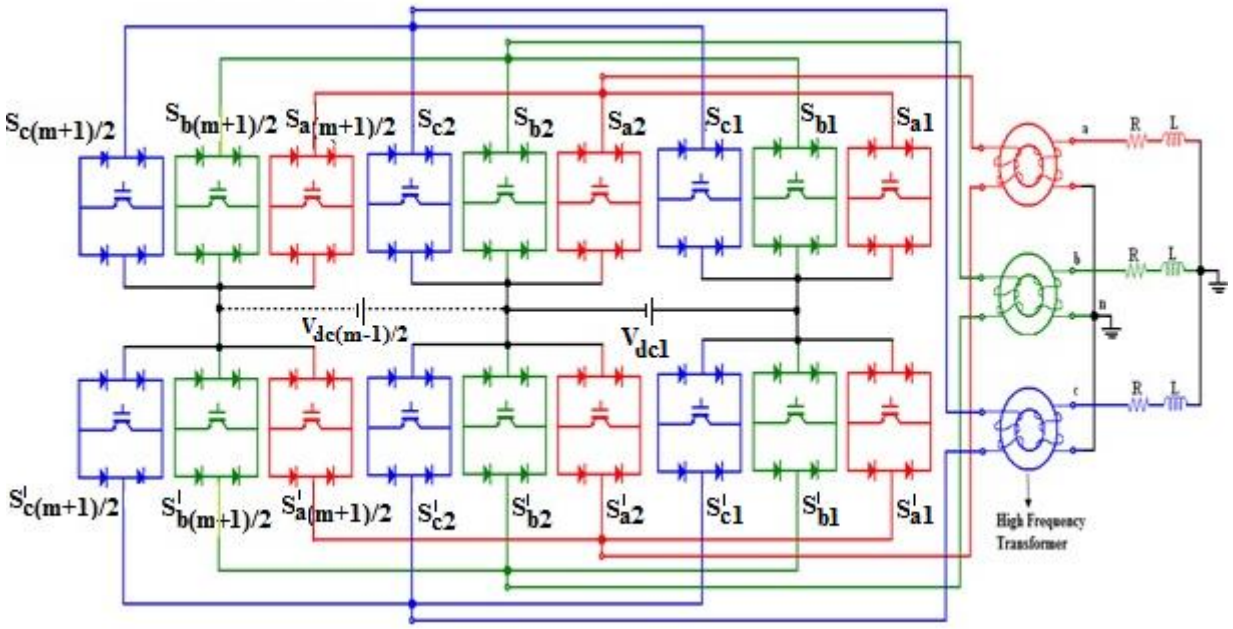


Fig. 1 Generalized structure of the proposed topology

For instance, the switches (S_{a3} , S_{a3}'), (S_{b1}, S_{b2}, S_{b3}') and (S_{c1}', S_{c2}', S_{c3}) are triggered to generate V_{an} =0, V_{bn} = -3V_{dc} and V_{cn} = 3V_{dc} and portrayed in Fig.2. The proposed three phase topology makes use of unequal DC sources and comes under the category of asymmetrical topology. The magnitudes of the dc sources are arranged in the factor of 2 produces (4n-1) and (8n-3) level in phase and line voltages respectively. The maximum output voltage for this proposed topology in asymmetric configuration is given by (2n-1)×V_{dc}. The entries in Table 1 and 2 portray the comparison between the proposed, conventional and recent topologies. It is inferred that the proposed topology claims one third of dc sources required for conventional topologies and switching devices in the conduction path while increasing the number of levels. Table 3 compares the power component required between symmetrical and asymmetrical configuration of the proposed topology. The comparisons of power components between proposed and other topologies for m level are presented in Table 4. The multicarrier PD-pulse width modulation generation shown in Fig.3 is used to buffer the switches in the proposed topology and the corresponding logical operation is tabulated in Table 5.

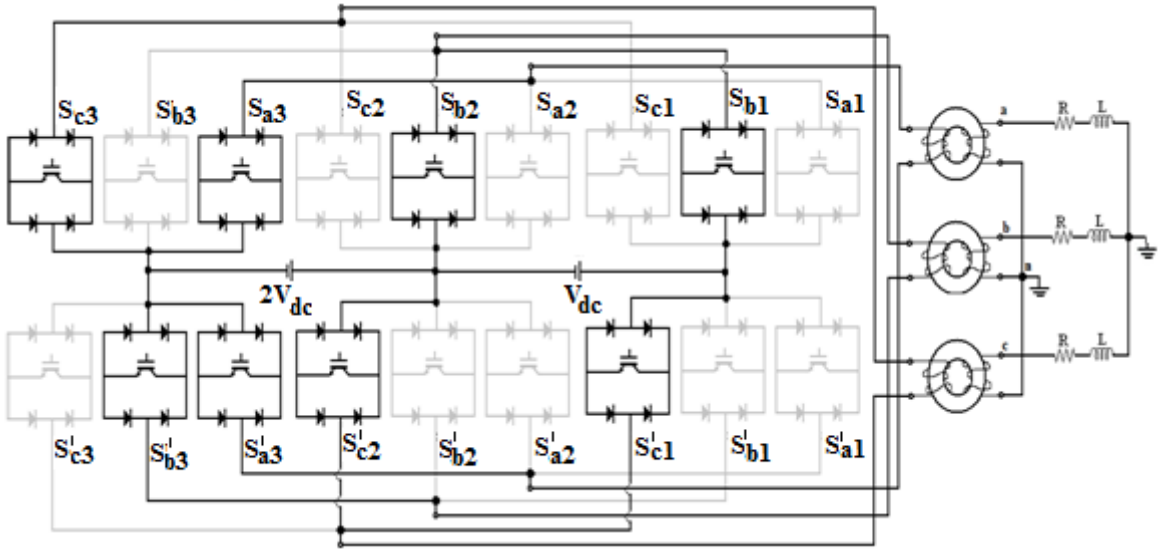


Fig. 2 Seven level inverter with mode diagram for V_{an} = 0 ,V_{bn} =-3V_{dc} and V_{cn} = +3V_{dc}

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Table 1 Asymmetrical Operating modes per cycle

Modes	Output Phase Voltages			Conducting Switches		
	V_{an}	V_{bn}	V_{cn}	V_{an}	V_{bn}	V_{cn}
1	0	$-3V_{dc}$	$3V_{dc}$	S_{a3} , S_{a3}'	S_{b1} , S_{b2} , S_{b3}'	S_{c1}' , S_{c2}' , S_{c3}
2	V_{dc}	$-3V_{dc}$	$3V_{dc}$	S_{a1}' , S_{a2} , S_{a3}	S_{b1} , S_{b2} , S_{b3}'	S_{c1}' , S_{c2}' , S_{c3}
3	V_{dc}	$-3V_{dc}$	$2V_{dc}$	S_{a1}' , S_{a2} , S_{a3}	S_{b1} , S_{b2} , S_{b3}'	S_{c1}' , $S_{c2,}$ S_{c2}' , S_{c3}
4	$2V_{dc}$	$-3V_{dc}$	$2V_{dc}$	S_{a1}' , $S_{a2,}$ S_{a2}' , S_{a3}	S_{b1} , S_{b2} , S_{b3}'	S_{c1}' , $S_{c2,}$ S_{c2}' , S_{c3}
5	$2V_{dc}$	$-3V_{dc}$	V_{dc}	S_{a1}' , $S_{a2,}$ S_{a2}' , S_{a3}	S_{b1} , S_{b2} , S_{b3}'	S_{c1}' , S_{c2} , S_{c3}
6	$3V_{dc}$	$-3V_{dc}$	V_{dc}	S_{a1}' , S_{a2}' , S_{a3}	S_{b1} , S_{b2} , S_{b3}'	S_{c1}' , S_{c2} , S_{c3}
7	$3V_{dc}$	$-3V_{dc}$	0	S_{a1}' , S_{a2}' , S_{a3}	S_{b1} , S_{b2} , S_{b3}'	S_{c3} , S_{c3}'
8	$3V_{dc}$	$-3V_{dc}$	$-V_{dc}$	S_{a1}' , S_{a2}' , S_{a3}	S_{b1} , S_{b2} , S_{b3}'	S_{c1} , S_{c2}', S_{c3} , S_{c3}'
9	$3V_{dc}$	$-2V_{dc}$	$-V_{dc}$	S_{a1}' , S_{a2}' , S_{a3}	S_{b1} , $S_{b2,}$ S_{b2}' , S_{b3}'	S_{c1} , S_{c2}', S_{c3} , S_{c3}'
10	$3V_{dc}$	$-2V_{dc}$	$-2V_{dc}$	S_{a1}' , S_{a2}' , S_{a3}	S_{b1} , $S_{b2,}$ S_{b2}' , S_{b3}'	S_{c1} , $S_{c2,}$ S_{c2}' , S_{c3}'
11	$3V_{dc}$	$-V_{dc}$	$-2V_{dc}$	S_{a1}' , S_{a2}' , S_{a3}	S_{b1} , S_{b2}', S_{b3} , S_{b3}'	S_{c1} , $S_{c2,}$ S_{c2}' , S_{c3}'
12	$3V_{dc}$	$-V_{dc}$	$-3V_{dc}$	S_{a1}' , S_{a2}' , S_{a3}	S_{b1} , S_{b2}', S_{b3} , S_{b3}'	S_{c1} , S_{c2} , S_{c3}'
13	$3V_{dc}$	0	$-3V_{dc}$	S_{a1}' , S_{a2}' , S_{a3}	S_{b3} , S_{b3}'	S_{c1} , S_{c2} , S_{c3}'
14	$3V_{dc}$	V_{dc}	$-3V_{dc}$	S_{a1}' , S_{a2}' , S_{a3}	S_{b1}' , S_{b2} , S_{b3}	S_{c1} , S_{c2} , S_{c3}'
15	$2V_{dc}$	V_{dc}	$-3V_{dc}$	S_{a1}' , $S_{a2,}$ S_{a2}' , S_{a3}	S_{b1}' , S_{b2} , S_{b3}	S_{c1} , S_{c2} , S_{c3}'
16	$2V_{dc}$	$2V_{dc}$	$-3V_{dc}$	S_{a1}' , $S_{a2,}$ S_{a2}' , S_{a3}	S_{b1}' , S_{b2} , S_{b3}	S_{c1} , S_{c2} , S_{c3}'
17	V_{dc}	$3V_{dc}$	$-3V_{dc}$	S_{a1}' , S_{a2} , S_{a3}	S_{b1}' , S_{b2}' , S_{b3}	S_{c1} , S_{c2} , S_{c3}'
18	V_{dc}	$3V_{dc}$	$-3V_{dc}$	S_{a1}' , S_{a2} , S_{a3}	S_{b1}' , S_{b2}' , S_{b3}	S_{c1} , S_{c2} , S_{c3}'

Table 2 Comparison between proposed and conventional topologies for 'm' level

Multilevel inverter structure	**Cascaded H-bridge**	**Diode clamped (1981)**	**Flying Capacitor**	**Proposed**
Main switches	6(m-1)	6(m-1)	6(m-1)	(m+5)/2
Bypass diodes	-	-	-	-
Clamping diodes	-	6(m-3)	-	-
DC split capacitors	-	3(m-1)/2	3(m-1)/2	-
Clamping capacitors	-	-	3(2m-6)/2	-
DC sources	3(m-1)/2	1	1	(m-1)/2

Table 4 Comparison between proposed and similar topologies for 'm' level

Multilevel inverter structure	Diode bypassed dc-link inverter	Diode bypass neutral point inverter	SPSMLDCLI	Cross switched MLI	Proposed
Main switches	3(m+7)/2	3(m+1)	3(3m-1)/2	3(m+3)	(m+5)/2
Bypass diodes	3(m-1)/2	3(m-1)/2	3	-	-
Clamping diodes	-	-	-	-	-
DC split capacitors	-	-	-	-	-
Clamping capacitors	-	-	-	-	-
No. of devices in the conduction path	3(m+3)/2	3(m+1)/2	3(m-1)	3(m+3)/2	2
DC sources	3(m-1)/2	3(m-1)/2	3(m-1)/2	3(m-1)/2	(m-1)/2

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Table 3 Comparison of power components required for proposed inverters

Parameters	Symmetrical	Asymmetrical
No. of DC sources	n	N
No. of switches	2n+2	2n+2
No. of output levels	(2×n)+1	(4×n)-1
Maximum voltage	$n\times V_{dc}$	$((2\times n)-1)\times V_{dc}$
Standing voltages on all the switches	$n\times V_{dc}$	$((2\times n)-1)\times V_{dc}$
(S_1-S_n) and (S_1'-S_n')		

Table 5 Digital process of control signals

Switches	Control Signals
S_{a1}	(P_5 XOR P_6) OR P_7
S_{a1}'	(P_2 XOR P_3) OR P_4
S_{a2}	(P_2 XOR P_3) OR (P_6 XOR P_7)
S_{a2}'	(P_3 XOR P_4) OR (P_5 XOR P_6)
S_{a3}	P_1 OR P_4 OR (P_3 XOR P_4)
S_{a3}'	P_1 OR P_7 OR (P_6 XOR P_7)

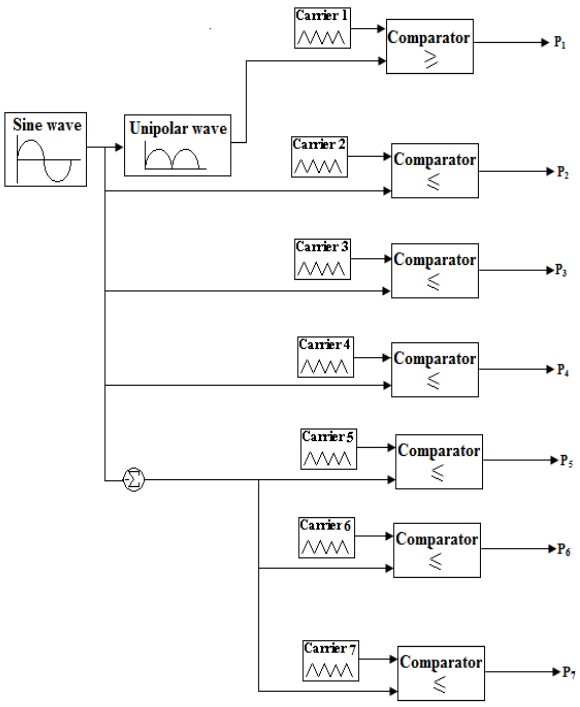


Fig.3 Pulse generation methodologies per phase.

3. Power loss analysis and comparison graph

The energy lost during turn-on and turn-off interval of a switch is considered to compute the switching loss of the proposed topology. To simply the analysis, it is assumed that the voltage and current of a switch during switching varies linearly. Using this approximation, the energy lost during every turn-on and turn-off period of a switch can be obtained as

$$E_{on} = \frac{1}{6} V_{sw} I t_{on}$$

$$E_{toff} = \frac{1}{6} V_{sw} I t_{off}$$

where E_{on} and E_{off} are the energy lost during turn-on and turn-off period of a switch and t_{on} and t_{off} are the turn-on and turn-off time of the switch. V_{sw} and I are voltage on and current through the switch before turning on or after turning off. For the multilevel inverter, the switching power loss can be computed as follows

$$P_{sw} = \frac{1}{T}(N_{on}E_{on} + N_{off}E_{off})$$

Where T is a fundamental cycle and (N_{on} and N_{off}) is the number of times that the switches are turned on and off respectively. The total power loss of the switches can be obtained by adding the conduction and switching losses as shown in Fig. 4. The proposed topology offers lesser power loss in each switching devices compared to other topologies. Fig.5 shows the number of switch count versus voltage levels. The proposed asymmetrical configuration shows the greater enhancement in the number of levels. The comparison of number of dc sources versus voltage levels is shown in Fig.6

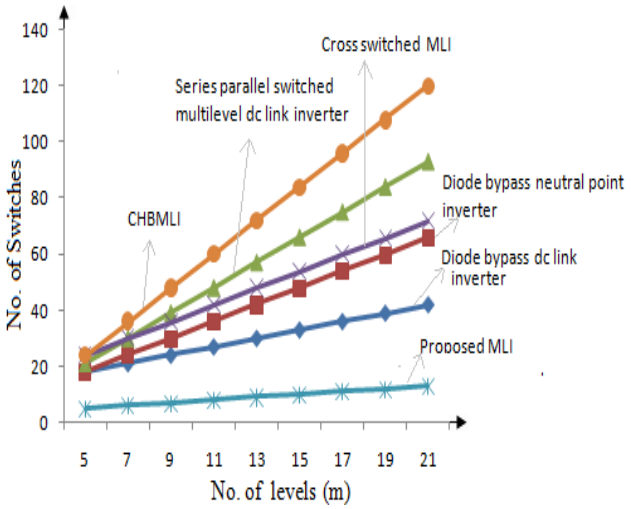


Fig.4 Comparison of switch count against voltage levels.

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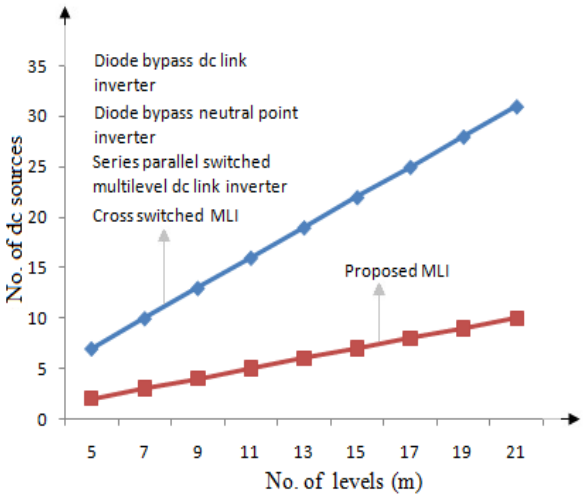


Fig.5 Comparison of dc sources required against voltage levels.

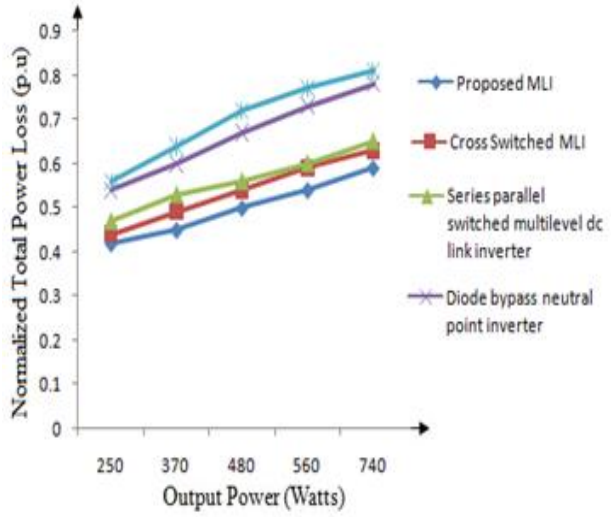


Fig.6 Comparison of total power loss against output power.

4. Simulation Results

The proposed topology is simulated for seven level output in Matlab R2013b with simulation specifications: V_{dc1}= 100V, V_{dc2}= 200V, switching frequency of 2 kHz and star connected RL load of 150Ω and 106mH in each phase respectively. The PWM required to trigger the switches using the methodology shown in Fig. 3. The simulated three phase voltage waveform (V_{AN}, V_{BN} and V_{CN}) are shown in Fig. 7. The corresponding line voltage waveform (V_{AB}, V_{BC} and V_{CA}) along with phase current waveform are depicted in Figs. 8 and 9 respectively

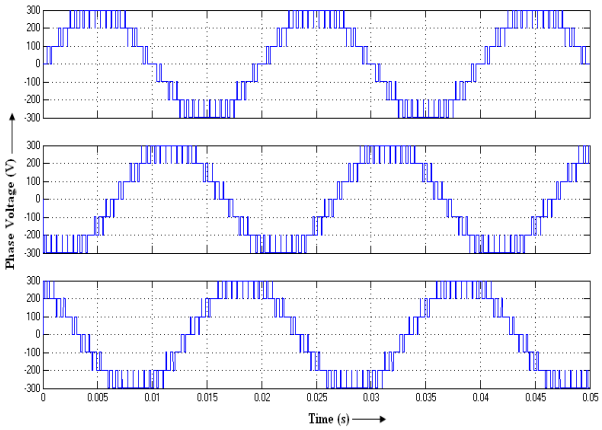


Fig.7 Phase voltage waveform.

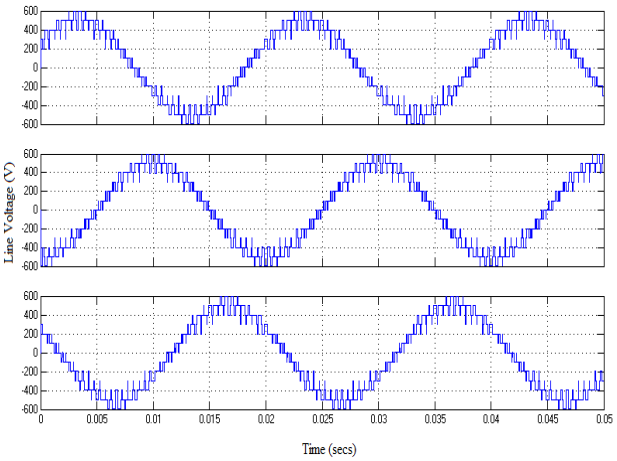


Fig.8 Line voltage waveform.

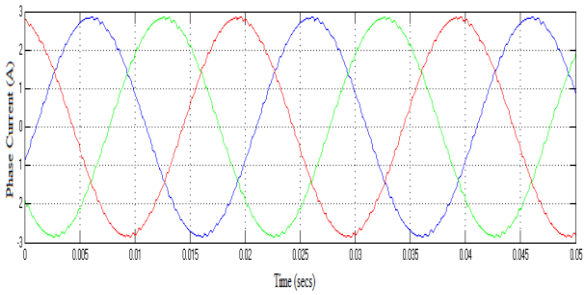


Fig.9 Phase current waveform.

5. Harware Result

The seven level inverter is constructed for per phase and its prototype set up is shown in fig. The switching pulses are generated using Xilinx Spartan- 3A/3A FPGA controller. The fig depicts the phase voltage waveform of asymmetrical configurations. The experimental results shows the feasibility of the topology with simulation results and its usage in practical circuits and forge a new dimension for the use of MLIs.

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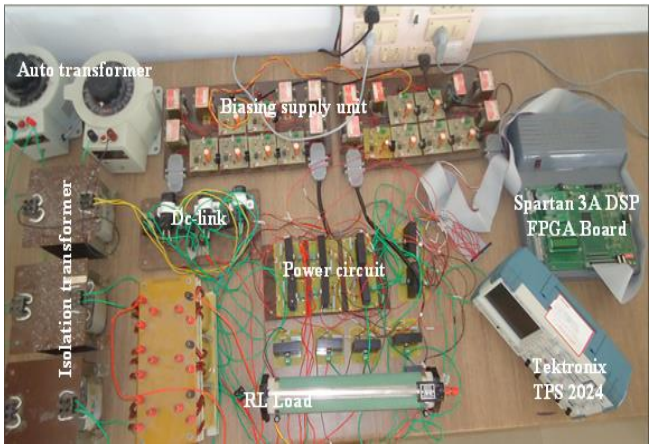


Fig.10 Hardware setup

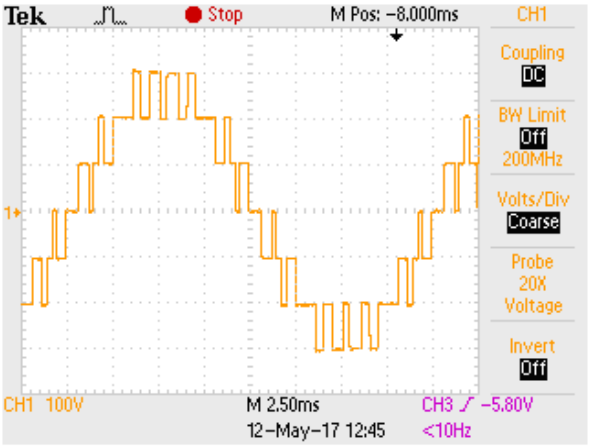


Fig.11 Output Voltage waveform for per phase

5. Conclusion

A new three phase asymmetrical multilevel inverter topology has been proposed with an objective to offer reduced number of dc sources and switching devices for a given number of levels. The proposed has the advantage of only two switches conducting in each level transition of output voltage and has lesser power loss. The performance of the proposed topology is proven through simulation and analytical studies

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