AN ENHANCED CARBON NANOTUBE FIELD EFFECT TRANSISTOR FOR VLSI CIRCUIT DESIGNING IN NANO TECHNOLOGY

P. Prakash[a*], K. Mohana Sundaram[b], M. Anto Bennet[c]

[a]Research Scholar, Department of Electrical and Electronics Engineering, Vel Tech Multi Tech Dr. Rangarajan Dr. Sakunthala Engineering College, Chennai-62. E-mail: mp.prakash09@gmail.com
[b]Professor, Department of Electrical and Electronics Engineering, Vel Tech Multi Tech Dr. Rangarajan Dr. Sakunthala Engineering College, Chennai-62. E-mail: kumohanasundaram@gmail.com
[c]Professor, Department of Electronics and Communication Engineering, Vel Tech, Chennai-62. E-mail: bennetmab@gmail.com

Abstract— *In the recent days, Complementary Metal Oxide Semiconductor (CMOS) is one of the most widely used technologies that is used to attain high density Very Large Scale Integration (VLSI) circuits with high energy efficiency. Reducing the size of the components that are used to design the circuit is an important and demanding task. For this purpose, some of the architectures and frameworks are designed in the existing works. But, it has some major drawbacks such as, increased area, higher power consumption, and required large number of transistors. In order to overcome these issues, this paper introduced a new design architecture based on the Nano technology. The main intention of this work is to reduce the size of the components that are used in the VLSI circuit design, and to increase the overall performance of the proposed system. After initializing the parameters, the P-type and N-type channels and the size of the transistors are estimated based on the layout design. Then, the number of components and its size are reduced in the proposed Enhanced Carbon Nanotube Field Effect Transistors (ECNFET) design. After that, the library is generated and the filtering is applied to eliminate the noise in the circuit. The novel concept of this paper is it modified the traditional structure of CNFET with reduced number of transistors. In experiments, the proposed architecture is evaluated in terms of performance and is compared with the traditional circuits to prove the betterment of the ECNFET.*

Keywords— *Complementary Metal Oxide Semiconductor (CMOS), Enhanced CarbonNanotube Field Effect Transistors (ECNFET), N-Type and P-Type Channels and Layout Design.*

1. Introduction

CARBON Nanotube Field Effect Transistors (CNTFET) is one of the widely used technology for future nanoelectronics[1, 2]. In the last decades, the silicon transistor devices have been decreased drastically due to its critical dimension. So, some research activities focused on identifying an alternative to enable the improvement in density and performance of electronics information system. It includes metal gate electrode, constant gate dielectric, double gate FET, and strained-Si FET. The high dielectric constant materials provide an efficient charge injection and reduce the direct tunneling current leakage. When compared to these electronics, the Carbon Nanotubes (CN)[3, 4] are more useful due to its important characteristics:

- Capability of adapting the desired threshold voltage.
- One dimensional (1- dim) character.

BUPT

Moreover, it exhibits metallic as well as the semiconducting character, and then it attains the fine control of the tube diameter. The quantization of electron and hole states can occur in only one dimensional sub band[5]. Thus, it reduces the phase space, probability of back scattering with a high conductivity of CN. If the semiconducting CN are used in a FET geometry, the confinement can help to control the off-state of the transistor [6, 7].

2. Problem Description

The main focus of the Nano technology is the miniature design of gates and circuits to reduce the size of chip. The supply voltages and threshold voltages are reduced by using the advanced CMOS technology[8] for designing the low power circuits. Moreover, the reduction in the threshold voltage results in the increase of leakage current. The CMOS devices possess high noise immunity and low static power consumption[9]. As one of the transistors of the pair is always in off condition, it draws significant power during the switching ofon and off states. Subsequently, the CMOS devices do not produce so much of waste heat. Moreover, CMOS allows a high density of logic functions to be mapped on a chip, so it became the most widely used technology of VLSI chip manufacturing. Due to the low voltage, this technique disconnects the switching block from power supply line and ground line, whenever the circuit is in idle mode. To overcome these issues, this work focuses to design a new FET layout, namely, Enhanced CNFET (ECNFET) for reducing the area occupied and power consumption. Also, the nanometer technology is also implemented in VLSI logical architectures[10]. Further, it is implemented in the logical circuits such as inverter, adders, flip flops and counters.

3. Objectives

Based on the problem description, this research work has the following objectives:

- An Enhanced CNFET is developed in the layout architecture by specifying the channel parameter of FET architecture.
- To perform the logical operation in the circuits, the proposed design is presented as a library.
- To drive the transistor element with high voltage (MHz), the sizing is sufficiently reduced.
- To attain a minimum delay rate with increased operating frequency, the FET is optimized with the standard established CMOS technology.
- To provide the better results compared than the traditional CNTFET, the VLSI circuit is designed based on the n-type and p-type transistors.

4. Organization

The rest of the paper is structured as follows: Section II reviews the existing frameworks and architectures that are related to design of VLSI circuit using nanoelectronics. Section III illustrates the clear description about the proposed ECNFET architecture. Section IV evaluates the results of both existing and proposed architectures using different performance parameters. Finally, Section V concludes the paper and some enhancement that will be implemented in future.

5. Related Works

This section reviews some of the existing architectures and frameworks that are related to low power design circuits in VLSI.

Roohi, et al [11]suggested a Domain Wall Nano Magnet (DWNM) based device to attain a highly scalable current mode. The main aim of this architecture design was to reduce the power consumption and delay consumption at various operating temperatures. Here, the SPICE circuit simulator was utilized to verify the model of DWNM based Full Adder (FA) design. Based on the input current and temperature, the Power Delay Product (PDP) of the DWNM-FA was estimated. Also, the functionality of the circuit was verified by using the following parameters: area, thickness of oxide surface, gilbert damping factor, thickness of free layer, polarization, saturation

BUPT

magnetization, threshold current density, out of plane anisotropy and uniaxial anisotropy field. However, this design has some drawbacks that include low performance, scalability and increased complexity. *Moaiyeri, et al*[12]designed a new ternary serial adder by employing the positive, negative, and standard ternary logics. The aim of this paper was to reduce the required amount of devices during the design of serial adder. In this work, a single full adder and a flip flop were used to add every two arbitrary large numbers in the ternary serial adder. Moreover, a D-flip flop was used to save the carrier signal. The parameters used on the CNTFET model were as follows:

- Physical channel length
- Mean free path
- Sub lithographic pitch
- Thickness of high k-top gate electric
- Dielectric constant of Substrate

The advantage of this paper was, the utilized static ternary flip flop structure in the circuit do not required any additional supply voltage. The major disadvantages of this paper were, it has increased power consumption, delay consumption, and number of devices. *Labrado and Thapliyal* [13] designed a single layer Quantum-dot Cellular Automata (QCA) for deliberating some basic arithmetic circuits. This designing circuit consists of full adder, full subtractor, 4-bit ripple carry adder, and 4-bit ripple borrow subtractor. *Bahadori, et al* [14] introduced a Carry Skip Adder (CSKA) structure to reduce the energy consumption of digital circuits. In this paper, the features of CSLA were utilized to reduce the delay of the circuits by implementing the CMOS logic. They were able to increase the speed while keeping the area and power under control.Moreover, the suggested structure has the capability of implementing the simple carry skip logics. Here, the power consumption was reduced by employing the variable latency feature of the structure. Based on the slack time, the amount of power and energy savings was functioned.

Kagaris[15] recommended a Computer Aided Design (CAD) synthesis tool to reduce the required number of transistors in the circuitry. Here, a CAD tool, namely, MOTO-X was employed to reduce the transistors under a user specified bound because the reduction in the number of transistors could automatically reduce the power and delay consumption. The disadvantage of this paper was, it required to resynthesize the sub-circuits of a given circuit. *Mehrabani and Eshghi*[16]have suggested a carbon nanotube field effect transistor device to reduce the power, delay and energy consumption. Here, the PDP was used to validate the performance of the designed VLSI circuit. In this paper, the SPICE simulation tool was used to evaluate the performance of the suggested architecture. For this purpose, some of the parameters that include physical channel length, intrinsic CNT channel, length of region, high k-top gate dielectric material, and capacitance between the channel region and substrate. *Nabavi, et al*[17] suggested an optimum pMOS to nMOS width ratio for designing the CMOS circuit with no extra cost. This structure includes the following steps:

- Maximum current over capacitance ratio was identified.
- An analytical expression was derived by reducing the delay of an inverter.
- Various CMOs logic gates were simulated in the sub threshold region.

The main intention of this work was to attain the maximum speed in sub threshold operation. The parameters considered in the CMOS design were, propagation delay, energy and energy delay product.

Karthikeyan, et al[18] suggested a CNTFET technology to analyze the performance of MAC unit in VLSI. In this design, a high speed and low PDP based full adder was presented with only two transistors. From the paper, it was observed that, the arithmetic circuits could be more useful in the VLSI systems, when compared to the other circuitry designs. The advantage of this architecture was, it reduced the power consumption

while maintaining the high update rate. *Almudever and Rubio* [19] analyzed the impacts of CNTFET technology based on the density fluctuations and non-uniform inter CNT spacing. The factors such as CNT diameter, the presence of metallic CNTs and the doping fluctuations were the main sources of the CNTFET manufacturing process. The advantages of this paper were, it attained low metal to CNT contact resistance and increased CNT density. *Pudi and Sridharan*[20] introduced a ripple carry and Brent-Kung adders with low complexity for designing Quantum dot Cellular Automata (QCA). The main intention of this paper was, it reduced the new of majority logics and applied it on the multi-bit adders. Here, the binary states were determined based on the locations of electrons. The functionality of QCA layout was verified by using the coherence vector simulation engine.

Sharad, et al [21] developed a spin based neuron model to attain low power consumption, high speed and high integration density. In this paper, a spin based neuron synapse modules were interconnected through charge mode signaling by using the CMOS technology. Moreover, a physics based simulation framework was utilized to simulate the spin based neuron synapse units. The major advantage of this paper was, the suggested framework was more suitable for low power consumption circuit design. *Moaiyeri, et al* [22] presented a low power Multiple Valued Logic (MVL) for multi nano devices. Based on the conventional COMS architecture, the binary gates were inherently utilized with the simple structures. The main aim of this paper was to improve the manufacturability and feasibility of the circuit design. The major drawback of this design was, it was unsuitable for the current and upcoming technologies that include high static power dissipation, large off chip resistors and the utilization of multiple supply voltages. *Deng, et al* [23] introduced a low power Magnetic Full Adder (MFA) to improve the power efficiency and die area. Here, the switching mechanism, namely, Spin Transfer Torque (STT) was employed to increase the writing speed and power efficiency. The main aim of this paper was to solve the communication bottleneck between the separated logic module and memory block. Also, a Pre-Charge Sense Amplifier (PCSA) was used in this work to evaluate the logic results on the outputs. However, this framework has some main drawbacks that include, it was not suitable for power saving and the heating devices consumed more area. *Kaizerman, et al* [24]structured a low power Dual Mode Logic (DML) to attain high albeit with increased power dissipation. In this design, the gate was operated in two stages:

- Precharge
- Evaluation

The output was charged to low or high based on the topology of DML gate during the precharge phase. Then, the output was evaluated at the gate inputs in the evaluation phase. Here, two parameters such as Static Noise Margin (SNM) and Logical Level (LL) analysis. The disadvantages of this framework were as follows: crosstalk noise, susceptibility to glitches, and charge sharing. *Mirzaee, et al* [25] utilized new ternary adders to generate the binary signals based on the logic style. The efficiency of new designs were examined by performing extensive analyses. Here, the CNTFET was used to form the circuit due to the special characteristics of ternary circuit. Moreover, the power, area and delay were directly influenced in this circuit for performance evaluation. The disadvantage of this architecture was, it has very large number of transistors. *Motaman, et al* [26]investigated the challenges of VLSI circuit design, which includes bitcell layout, head positioning, utilization factor of the nanowire, shift latency and shift power. The operations such as read, write, head and shift selection were performed during the bitcell design. Moreover, the area and latency were optimized by identifying the appropriate the read/write head size. Here, a shift circuit and write driver were developed for boosting the current. Then, increased energy

efficiency was attained with the help of cache segregation method. *Bhattacharyya, et al* [27] introduced a hybrid 1-bit full adder to analyze the performance of low power high speed circuits. The main aim of this paper was to optimize the power, delay and PDP with reduced energy consumption. In this paper, the power consumption of the hybrid full adder was categorized into two types, which include static power and dynamic short circuit power. The major limitation of this paper was, high input capacitance and required more number of buffers.

In this survey, the advantages and disadvantages of various circuit designing architectures are analyzed with its advantages and disadvantages. But, it mainly lacks with some drawbacks that include the followings:

- High power and area consumption
- It is not applicable for the combinational circuits
- Produces erroneous output
- Number of transistors are high
- Power dissipation

In order to overcome these issues, the proposed work aims to develop a Field Effect Transistor (FET) with reduced area and power consumption.

6. Proposed Method

This section presents the detailed description of the proposed Enhanced Carbon Nanotube Field Effect Transistor (ECNFET) based VLSI circuit design architecture. The main intention of this paper is to reduce the size of nano meter with increased operating frequency and reduced delay. The flow of the proposed system is shown in Fig 1.

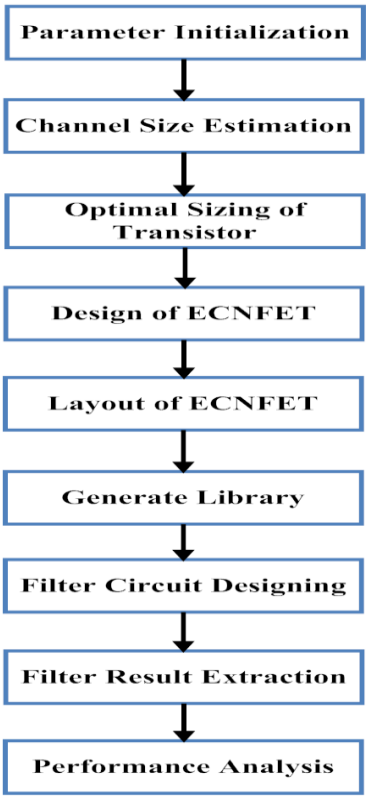


Fig 1. Overall flow of the proposed architecture design

At first, the parameters such as amount of substrate usage, P-well size, channel size, gate size and doping level are given as the input. After that, the size of the channel and its width are optimized, and then the proposed ECNFET transistor device is designed with optimized materials. The layout design of the proposed transistor is extracted and it is created as a library file. Furthermore, the filter is designed for eliminating the harmonics in the proposed device. Finally, the measures such as delay, operating frequency, and size of device are used to evaluate the performance of the proposed architecture.

6.1. Channel Estimation

After initializing the parameters, the size of n-type and p-type channels are estimated based on its layout design. The proposed ECNFET is the most widely used FET that finds an extensive use in VLSI circuits.Typically, the technological circuit

BUPT

design requires the transistor channel is capacitively coupled with the insulated gates and FETs. The PCNFET and NCNFET channels are shown in Fig 2, in which the voltmeter and ammeter is connected with the circuit resistance.

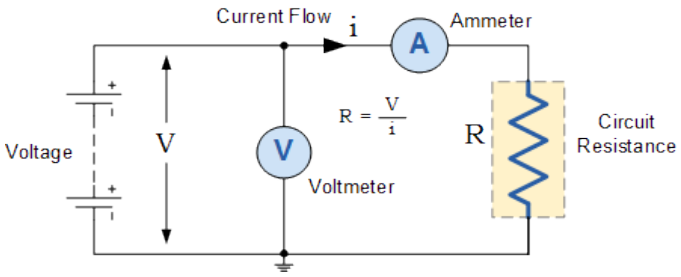


Fig 2. Characteristics of the proposed PCNFET and NCNFET

6.2 Optimal Sizing of Transistor

After estimating the channels, the size of the PCNFET and NCNFET transistors are estimated, which are inherent in any CMOS process. Typically, in the PNP transistor, the N type material is inserted between two P type region of emitter and collector, so it has three terminals such as emitter, base, and collector. Similarly, the P type material is inserted between two N type materials in the NPN transistor. These transistors are an important semiconductor device due to its applications in electronics and amplification of a signal. So, the PNP and NPN are the three terminal device that contains two junctions. The two junctions of each transistor havethree different modes of operation based on the biasing condition of forward or reverse. In the active mode of the operation, the transistor is used as an amplifier, where both junctions are differently biased. Then, the emitter base junction has to be forward biased and the collector base junction has to be reverse biased. The other two modes are saturation and cutoff, which are used during the switching operations. In saturation mode, both the emitter and collector base junctions are forward biased, and in the cutoff mode, both junctions are reverse biased. Moreover, these transistors find an immense use in digital circuits during the logic operations; also it is used as a discrete component in Integrated Circuits (ICs). So, it is important to reduce the size of these transistors in the VLSI design.

6.3 Circuit Designing

The power consumption in CMOS circuits is related to the signal transitions and stems from transistors, wires, and short circuit currents. So, reducing the required amount of power is an important task in circuit designing. For this purpose, this work proposed a new design, namely, ECNFET with reduced number of components, which is visually depicted in Fig 3. In this circuit, the carbon nanotube is inserted in between the source and drain.

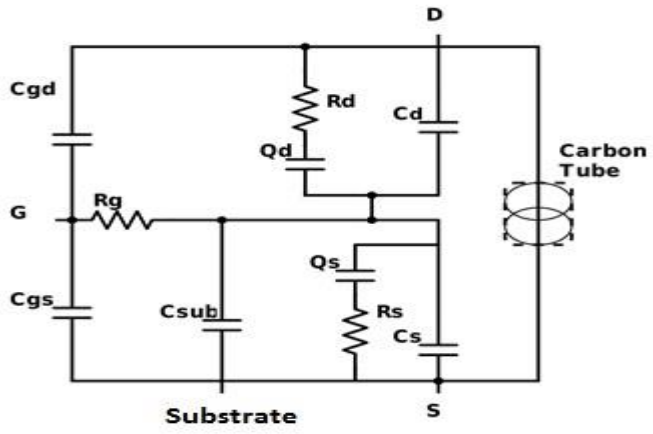


Fig 3. Layout of ECNFET

Here, the output resistance can be represented as follows:

At saturation level, $V_{gd} < V_{th}$ *or* $V_{ds} > V_{ds(sat)}$

$$R = \frac{1}{\lambda * I_{ds}} \qquad (1)$$

$$I_{ds} = \frac{1}{2}\left(\mu_p \times C_{ox} \times \frac{W}{L}\right)\left(V_{gs} - V_{th}\right)^2 \quad (2)$$

At linear level, $V_{gd} > V_{th}$ *or* $V_{ds} < V_{ds(sat)} = V_{gs} - V_{th}$

$$R = \frac{1}{\left[\mu_p \times C_{ox} \times \left(\frac{W}{L}\right) \times (V_{gs} - V_{th})\right]} \quad (3)$$

$$I_{ds} = \left(\mu_p \times C_{ox} \times \frac{W}{L}\right)\left[\left(V_{gs} - V_{th}\right) - \frac{1}{2}V_{ds}\right]V_{ds} \quad (4)$$

Where, λ represents the channel length Modulation parameter, V_{gs} is the gate to source voltage, V_{ds} represents the drain to source voltage, L indicates the length, W is the width, I_d indicates the drain current, C_{ox} is the capacitance per unit area, V_{th} represents threshold voltage, and $\mu_p = 550$ is an effective mobility of holes. After estimating the output resistance, the threshold voltage of the CNT channel is calculated as follows:

$$V_{th} = \frac{E_g}{2e} = \frac{\sqrt{3}}{3} \times \frac{aV_\pi}{eD_{CNT}} \quad (5)$$

$$D_{CNT} = \frac{(\sqrt{3}a_0)}{\pi} \times \sqrt{n^2 + nm + m^2} \quad (6)$$

Where, a = 2.49 Å // Å is the carbon to carbon atom distance;

a_0 = 1.42 nm // (n, m) – Integer pairs called as chirality vector;

V_π = 3.033 eV;

$e = 1.602176 \times 10^{-19}$ // e is the unit electron charge;

Here, the grapheme sheet wrapped is represented based on the pair of indices n, m, which denotes the number of unit vector along two directions in the honey comb crystal lattice of grapheme. If, m = 0, the nanotubes are termed as zigzag; for instance, n is 19 and m is 0:

$$D_{CNT} = \frac{\left(\sqrt{3} \times 1.42\right)}{\pi} \times \sqrt{19^2 + 0 + 0} = 14.9nm$$

$$V_{th} = \frac{\sqrt{3}}{3} \times \frac{2.49 \times 3.033}{14.9 \times 1.602176} = 0.1827V$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

Where, $\varepsilon_{ox} = 3.45 \times 10^{-13}$ and t_{ox} is the oxide thickness.

$$t_{ox} = 422.4$$

$$C_{ox} = \frac{\varepsilon}{t_{ox}} = \frac{3.45 \times 10^{-13}}{422.4} = 0.816fF$$

The total gate capacitance, $C_g = \frac{\partial Q}{\partial V_g}$

Channel Length Modulation parameter, $\lambda = \sqrt{\left(\frac{\varepsilon_{nt}}{\varepsilon_{ox}}\right) d_{nt} t_{ox}}$

Where, $\varepsilon_{nt} = 1$ indicates the dielectric permittivity of the nanotube, ε_{ox} is the dielectric permittivity of the gate oxide, d_{nt} represents the diameter of nanotube, d_{ox} indicates the diameter of gate oxide:

$$\lambda = \sqrt{\left(\frac{1}{3.45}\right) \times 1.4878 \times 422.4} = 13.4966$$

$$I_{ds} = \frac{1}{2}\left(550 \times 0.816 \times \frac{12.3}{8}\right)(0.2 - 0.1827)^2 = 0.1033nA$$

$$R = \frac{1}{550 \times 0.816 \times \frac{12.3}{8} \times (1.5 - 0.1827)} = 0.04\ m\Omega$$

6.4 Filtering

After designing the circuit, the filtering process is applied to remove the harmonics and noise. The main intention of filtering is to eliminate the unwanted parts of the signals and to extract the useful parts (i.e. frequency range) of the signal. Generally, there are two types of filtering techniques such as analog and digital are used for circuit designing in which the analog filters utilizes some electronic circuits that are made from the components of resistors and capacitors. Consequently, the digital filters use a digital processor to perform the numerical calculations on sampled values of a signal. The major advantages of filtering are, high selectivity and it requires only fewer coefficients.

7. Performance Analysis

This section evaluates the results of the proposed ECNFET architecture using different performance measures that include VI characteristics, VC characteristics, DC characteristics, On-off current ratio, Power Delay Product (PDP), operating frequency, short channel effect, and voltage gain.

7.1 VI Characteristics

Fig 4(a) & 4(b) show the VI characteristics using 2D & 3D illustration respectively.This is estimated by using equation (2)& equation (4). From the results, it is observed that Ids saturates at 0.7V.

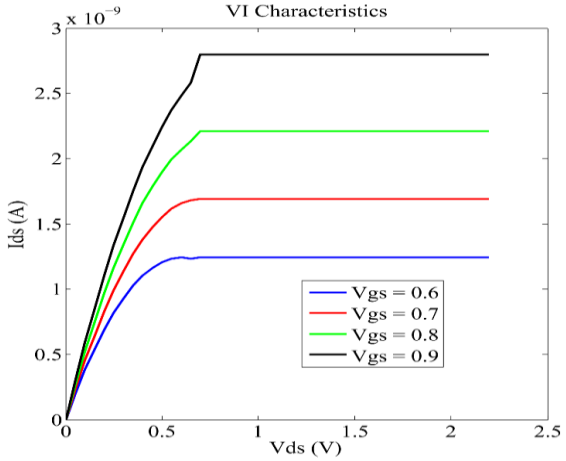


Fig 4(a). VI Characteristics

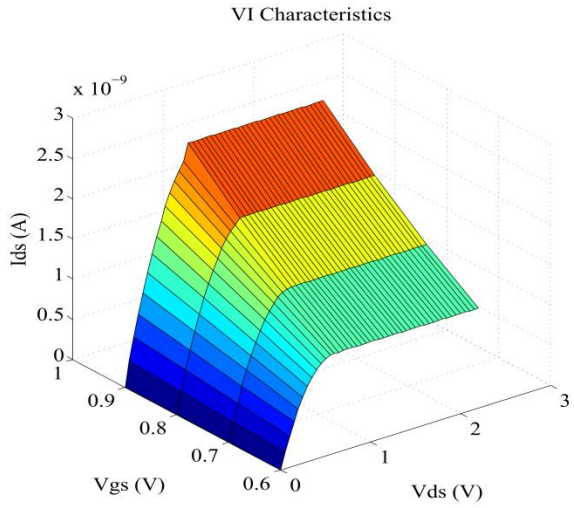


Fig 4(b). VI Characteristics (3D Illustration)

7.2 VC Characteristics

Fig 5 shows the characteristics of VC with respect to the gate to source voltage V_{gs} and capacitance C. The estimation of capacitance is illustrated in equation (7), where Q indicates the charge of electron and V represents the voltage.

$$\text{Capacitance, } C = \frac{\Delta Q}{\Delta V} \qquad (7)$$

Where, Q ≃ 1.602×10^{-19}Coulombs.

From the graph, it is observed that the capacitance value is linearly decreased by increasing the gate to source voltage.

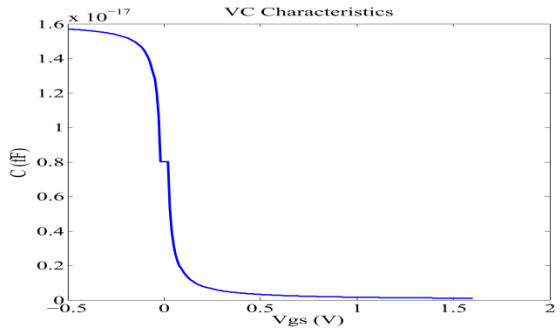


Fig 5. VC Characteristics

BUPT

7.3 DC Characteristics

Fig 6 shows the DC characteristics of an inverterwith respect to varying time in terms of nano seconds and voltage. The DC characteristics is mainly calculated based on the threshold and saturation. Also, it estimates the overall current peak value of the circuit.

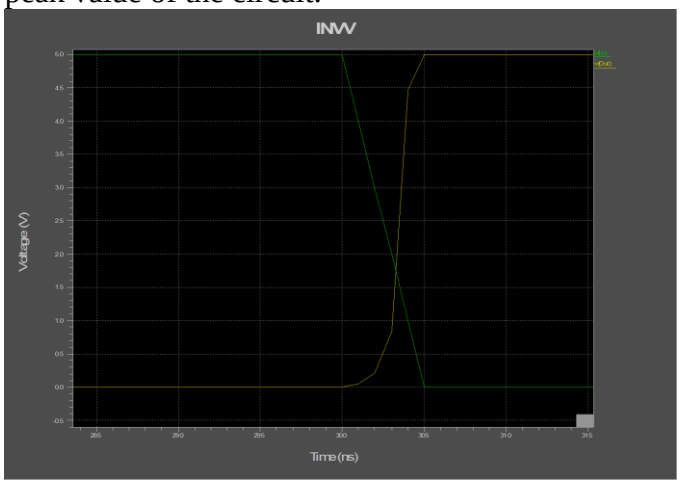


Fig 6. DC characteristics

7.4 On-Off Current Ratio

Fig 7 shows the on-off current ratio of the ECNFET circuit, which is calculated based on the gate to source voltage and current. Moreover, it is used to identify whether the switch is on or off. If the input is on, the current ratio will be high, if it is off, the current ratio will be equal, but it should not be high. The on-off ratio is estimated as follows:

$$I_{ON} = 100 \times \frac{W}{L} \times 10^{\frac{(V_{gs}-V_{th})}{S}}$$

$$Where\ S = \eta \times V_{th} \times \ln 10$$

Put $\eta = 1.5$, for varying V_{gs}=0.5V, 1V, 1.5V

We obtain $I_{ON} = 520nA, 3.5\mu A, 241\mu A$ respectively.

$$I_{off}(nA) = 100 \times \frac{W}{L} \times 10^{-\frac{V_{th}}{S}}$$

$$= 100 \times \frac{12.3}{8} \times 10^{-\frac{0.1827}{0.1}}$$

$$= 2.2899(nA)$$

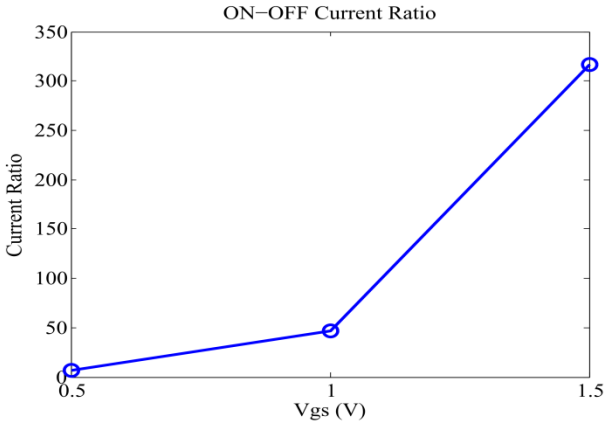


Fig 7. On-Off current ratio

7.5 Power Delay Product (PDP)

The Power Delay Product (PDP) is defined as the amount of energy, which is the product of average power and gate delay. Fig 8 shows the PDP of the proposed ECNFET circuit, where the x-axis represents the drain voltage and y-axis represents the PDP. It is calculated as follows:

$$PDP = Power \times Delay \qquad (8)$$

From the results, it is observed that the PDP is gradually increased with the increase in the drain voltage.

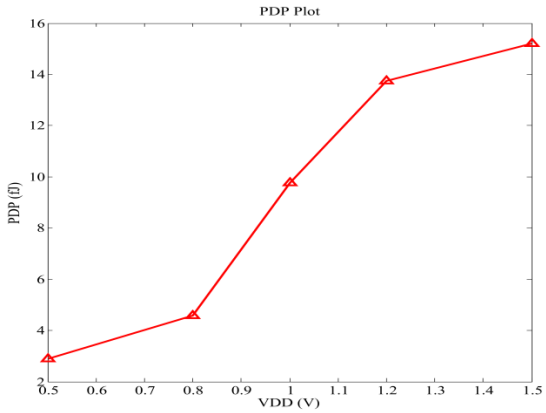


Fig 8. Power delay product

BUPT

7.6 Operating Frequency

Operating frequency can be increased based on the amount of time, if the frequency is increased, the delay will be reduced. Fig 9 shows the operating frequency of the proposed ECNFET circuit with respect to delay and frequency, where the x-axis represents the drain voltage and the y-axis represents the delay in terms of nano seconds. It is calculated as follows:

$$Operating\ Frequency = \frac{1}{Delay}\ Hz \quad (9)$$

From the analysis, it is observed that the delay will be gradually decreased with the increase in drain voltage.

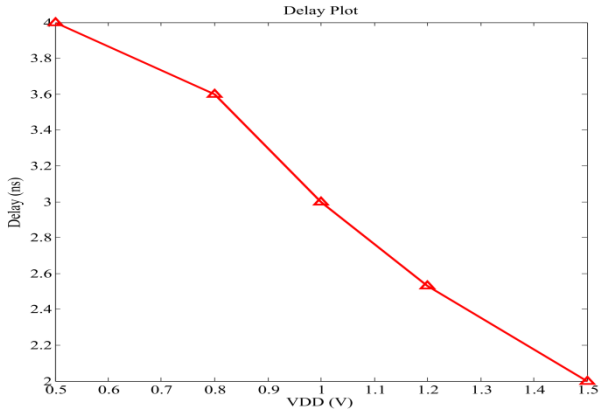


Fig 9 (a). Drain voltage Vs delay

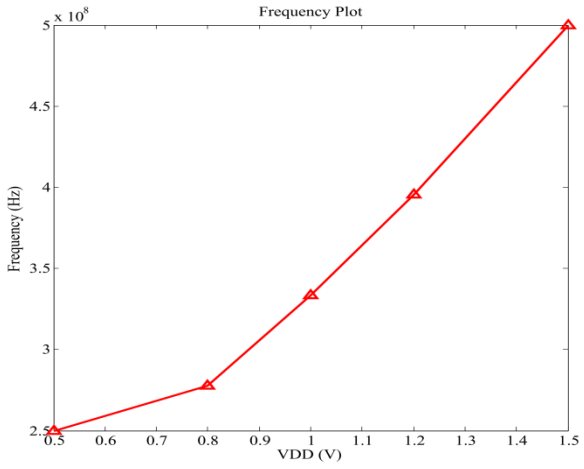


Fig 9 (b). Drain voltage Vs frequency

7.7 Short Channel Effect

In this design, the p-type and n-type channels are used, in which the channel length is same based on the value of magnitude. Moreover, the depletion layer will differ for the source and drain. Fig 10 shows the short channel effect of the proposed ECNFET circuit, where the x-axis represents the gate to source voltage, and the y-axis represents the current of drain source. From the analysis, it is observed that the current is automatically increased with the increase in the gate to source voltage.

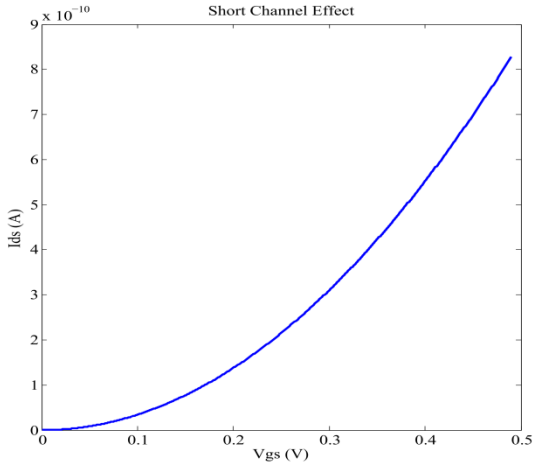


Fig 10. Short channel effect

7.8 Leakage Current

The leakage current is estimated as follows:

$$I_{leak} = I_0 \times 10^{\frac{[V_{gs}-V_{th}]}{S}} \quad (10)$$

Where,

$$Initial\ Current, I_0 = \frac{W}{L}\mu_0 C_{ox} V_{th}^2 e^{1.8} \quad (11)$$

$$S = \eta \times V_{th} \times ln10 (12)$$

$$I_0 = \frac{12.3}{8} \times 550 \times 0.816 \times 10^{-15} \times (0.1827)^2 \times e^{1.8} = 0.13934\ pA$$

$$S = 1.5 \times 0.1827 \times ln10 = 0.61$$

$$I_{leak} = 0.13934 \times 10^{\frac{0.2-0.1827}{0.61}} = 0.1489\ pA$$

7.9 Drain Induced Barrier Lowering (DIBA)

The drain induced barrier lowering is calculated as follows:

$$DIBL = -\left(\frac{V_{th}^{DD} - V_{th}^{low}}{V_{DD} - V_{D}^{low}}\right) \quad (13)$$

$$DIBL = -\left(\frac{0.014 - 0.1827}{1 - 0.4}\right) = 0.2812$$

7.10 Voltage Gain

Voltage gain is defined as the ratio of output and the input, which is generally represented in terms of A_v. Fig 11 shows the voltage gain level of the proposed ECNFET circuit with respect to the time in terms of nano seconds and the voltage. From the analysis, it is evaluated that the voltage gain is increased to $A_v = 0.8\,V$.

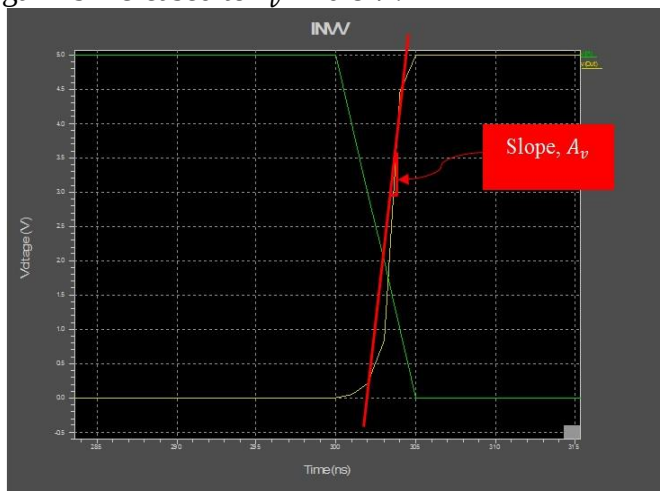


Fig 11. Voltage gain level.

7.11 Transconductance

The transconductance is the measure of output current of a device to the input voltage across the device. Higher transconductance results in terms of higher gain. The transconductance is calculated as follows:

$$g_m = \frac{\mu\left(\frac{C_g}{L}\right)}{\frac{V_{ds}}{L}} \quad (14)$$

$$g_m = 2.2028$$

8. Conclusion and Future Work

This paper presented a new circuit designing architecture, namely, ECNFET with reduced number of components using nano technology. The main intention of this paper is to reduce the size of nano meter, required number of transistors, area consumption, and power consumption. Initially, the parameters are initialized with the thresholds, and then size of the p-type and n-type channelsis estimated. After that, the optimal sizing of transistors such as NCNFET and PCNFET is performed for improving the performance becausereduction in the size of the transistor results in the reduced area consumption, power consumption, and delay as well. Then, the processor functions are stored in the library, based on these, the filtering process is applied on the circuit in order to eliminate the noise like frequency mismatching. Finally, the filtering results are extracted and its performance is evaluated to prove the betterment of the proposed design. The results are evaluated and compared in terms of PDP, operating frequency, short channel effect, and voltage gain. From the analysis, it is observed that the proposed design provides the better results compared than the other circuitries.

In future, this work will be enhanced by designing the VLSI circuit with reduced temperature level.

REFERENCES

[1] Cao Q, Han SJ, Penumatcha AV, Frank MM, Tulevski GS, Tersoff J, Haensch WE. Origins and characteristics of the threshold voltage variability of quasiballistic single-walled carbon nanotube field-effect transistors. ACS nano. 2015 Feb 9;9(2):1936-44.

[2] Kim SH, Song W, Jung MW, Kang MA, Kim K, Chang SJ, Lee SS, Lim J, Hwang J, Myung S, An KS. Carbon nanotube and graphene hybrid thin film for transparent electrodes and field effect transistors.

BUPT

Advanced Materials. 2014 Jul 1;26(25):4247-52.
[3] De Volder MF, Tawfick SH, Baughman RH, Hart AJ. Carbon nanotubes: present and future commercial applications. science. 2013 Feb 1;339(6119):535-9.
[4] Brady GJ, Joo Y, Wu MY, Shea MJ, Gopalan P, Arnold MS. Polyfluorene-sorted, carbon nanotube array field-effect transistors with increased current density and high on/off ratio. ACS nano. 2014 Nov 13;8(11):11614-21.
[5] Hu Z, Tulevski GS, Hannon JB, Afzali A, Liehr M, Park H. Variability and reliability analysis in self-assembled multichannel carbon nanotube field-effect transistors. Applied Physics Letters. 2015 Jun 15;106(24):243106.
[6] Qiu C, Zhang Z, Zhong D, Si J, Yang Y, Peng LM. Carbon nanotube feedback-gate field-effect transistor: Suppressing current leakage and increasing on/off ratio. Acs Nano. 2015 Jan 2;9(1):969-77.
[7] Tramble A, Burns P, Hayden S, Moten R, Xiao Z, Camino F. Fabrication of high-performance carbon nanotube field-effect transistors (CNTFETs) and CNTFET-based electronic circuits with semiconductors as the source/drain contact materials. InIon Implantation Technology (IIT), 2014 20th International Conference on 2014 Jun 26 (pp. 1-3). IEEE.
[8] Bao W, Cai X, Kim D, Sridhara K, Fuhrer MS. High mobility ambipolar MoS2 field-effect transistors: Substrate and dielectric effects. Applied Physics Letters. 2013 Jan 28;102(4):042104.
[9] Van NH, Lee JH, Sohn JI, Cha SN, Whang D, Kim JM, Kang DJ. High performance Si nanowire field-effect-transistors based on a CMOS inverter with tunable threshold voltage. Nanoscale. 2014;6(10):5479-83.
[10] Saha SK. Compact MOSFET modeling for process variability-aware VLSI circuit design. IEEE Access. 2014;2:104-15.
[11] Roohi A, Zand R, DeMara RF. A tunable majority gate-based full adder using current-induced domain wall nanomagnets. IEEE Transactions on Magnetics. 2016 Aug;52(8):1-7.
[12] Moaiyeri MH, Nasiri M, Khastoo N. An efficient ternary serial adder based on carbon nanotube FETs. Engineering Science and Technology, an International Journal. 2016 Mar 31;19(1):271-8.
[13] Labrado C, Thapliyal H. Design of adder and subtractor circuits in majority logic-based field-coupled QCA nanocomputing. Electronics Letters. 2016 Feb 5;52(6):464-6.
[14] Bahadori M, Kamal M, Afzali-Kusha A, Pedram M. High-speed and energy-efficient carry skip adder operating under a wide range of supply voltage levels. IEEE transactions on very large scale integration (vlsi) systems. 2016 Feb;24(2):421-33.
[15] Kagaris D. MOTO-X: a multiple-output transistor-level synthesis CAD tool. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. 2016 Jan;35(1):114-27.
[16] Mehrabani YS, Eshghi M. Noise and Process Variation Tolerant, Low-Power, High-Speed, and Low-Energy Full Adders in CNFET Technology. IEEE Transactions on Very Large Scale Integration (VLSI) Systems. 2016 Nov;24(11):3268-81.
[17] Nabavi M, Ramezankhani F, Shams M. Optimum pMOS-to-nMOS Width Ratio for Efficient Subthreshold CMOS Circuits. IEEE Transactions on Electron Devices. 2016 Mar;63(3):916-24.
[18] Karthikeyan KV, Babu R, Mathan N, Karthick B. Performance analysis of an efficient MAC unit using CNTFET technology. Materials Today: Proceedings. 2016 Dec 31;3(6):2525-31.
[19] Almudever CG, Rubio A. Variability and reliability analysis of CNFET technology: Impact of manufacturing imperfections. Microelectronics Reliability. 2015 Feb 28;55(2):358-66.

[20] Pudi V, Sridharan K. Low complexity design of ripple carry and Brent–Kung adders in QCA. IEEE Transactions on Nanotechnology. 2012 Jan;11(1):105-19.

[21] Sharad M, Augustine C, Panagopoulos G, Roy K. Spin-based neuron model with domain-wall magnets as synapse. IEEE Transactions on Nanotechnology. 2012 Jul;11(4):843-53.

[22] Moaiyeri MH, Mirzaee RF, Doostaregan A, Navi K, Hashemipour O. A universal method for designing low-power carbon nanotube FET-based multiple-valued logic circuits. IET Computers & Digital Techniques. 2013 Jul 1;7(4):167-81.

[23] Deng E, Zhang Y, Klein JO, Ravelsona D, Chappert C, Zhao W. Low power magnetic full-adder based on spin transfer torque MRAM. IEEE transactions on magnetics. 2013 Sep;49(9):4982-7.

[24] Kaizerman A, Fisher S, Fish A. Subthreshold dual mode logic. IEEE Transactions on Very Large Scale Integration (VLSI) Systems. 2013 May;21(5):979-83.

[25] Mirzaee RF, Navi K, Bagherzadeh N. High-efficient circuits for ternary addition. VLSI Design. 2014 Jan 1;2014:10.

[26] Motaman S, Iyengar AS, Ghosh S. Domain wall memory-layout, circuit and synergistic systems. IEEE Transactions on Nanotechnology. 2015 Mar;14(2):282-91.

[27] Bhattacharyya P, Kundu B, Ghosh S, Kumar V, Dandapat A. Performance analysis of a low-power high-speed hybrid 1-bit full adder circuit. IEEE Transactions on very large scale integration (VLSI) systems. 2015 Oct;23(10):2001-8.