A NOVEL DDS ARCHITECTURE FOR DYNAMIC RECONFIGURABLE THREE PHASE INDUCTION MOTOR DRIVE

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Abstract: *This paper presents a novel Direct Digital Synthesis (DDS) architecture based dynamic Reconfigurable Pulse Width Modulated (RPWM) variable frequency drive. The proposed architecture employs DDS based waveform generator to get a highly stable reference sine wave that reduces the hardware complexity and improves the system robustness. The architecture incorporates two switching strategies - Sine Pulse Width Modulation (SPWM) for lower Total Harmonic Distortion (THD) below 25 Hz and Space Vector Pulse Width Modulation (SVPWM) beyond 25 Hz. The proposed architecture incorporate a simplified dynamic reconfiguration strategy for faster control switching compared to the existing complex dynamic partial reconfiguration algorithms. The proposed method is experimentally validated through a three phase squirrel cage induction motor interfaced with a low cost Cyclone–II™ FPGA. The dynamic reconfiguration strategy achieves a switching speed of 480 ns.*

Keywords: *Field programmable gate arrays, reconfigurable architectures, space vector pulse width modulation, total harmonic distortion and variable speed drives.*

1. Introduction

The reconfigurable architectures have become a well-known and established research area, producing interesting as well as important results in both embedded and power converter systems. Reconfigurable architectures have blurred the gap between software and hardware, opening a new domain of unseen applications and opportunities.

Rapid development of the industrial power conditioning equipment in the past decade has opened up much scope for the automation industry in power electronics. The power electronics industry has immensely benefitted from the availability of rich software / hardware resources, lower cost, and higher speed in FPGA based system design. The design cycle of the power converters has considerably decreased due to the sophisticated software tool support from the FPGA vendors and also due to the availability of smart power modules from different power semiconductor manufacturers. The use of DDS for the generation of reference sine wave has considerably reduced the hardware complexity and will be an inevitable module in the future digital control of power converters [1]-[5].

A typical Electric Variable Speed Drives (EVSD) system consists of three basic components mainly electric motor, power converter, and control system. The power converter controls the power flow from AC mains to the motor by appropriate control of power semiconductor switches [6]-[8]. Variable speed drives are commonly used for achieving energy savings in buildings, usually by controlling pumps and fans that are part of the Heating, Ventilation and Air Conditioning (HVAC) system [9]. Different architectures of variable speed drives which result in efficient implantation is still a hot topic of research.

The existing dynamic reconfiguration methods [10] require expensive software tools and involve complex design steps for its implementation. The conventional speed control methods uses analog oscillator circuits for the reference sine wave generation which has frequency stability error. This paper addresses these problems in the design and development of an FPGA based three phase, three level DDS based Reconfigurable Pulse Width Modulation controller (DDS-RPWM) in a low-cost Altera Cyclone–II FPGA. The proposed DDS-RPWM controller achieves very high reconfiguration speed and implements the design using conventional low cost software design tool. The DDS based reference sine waveform generation used in the proposed method considerably reduces the hardware complexity and provides frequency stability. The SPWM control algorithm shows lower THD% at lower modulation indices compared to SVPWM control algorithm. The

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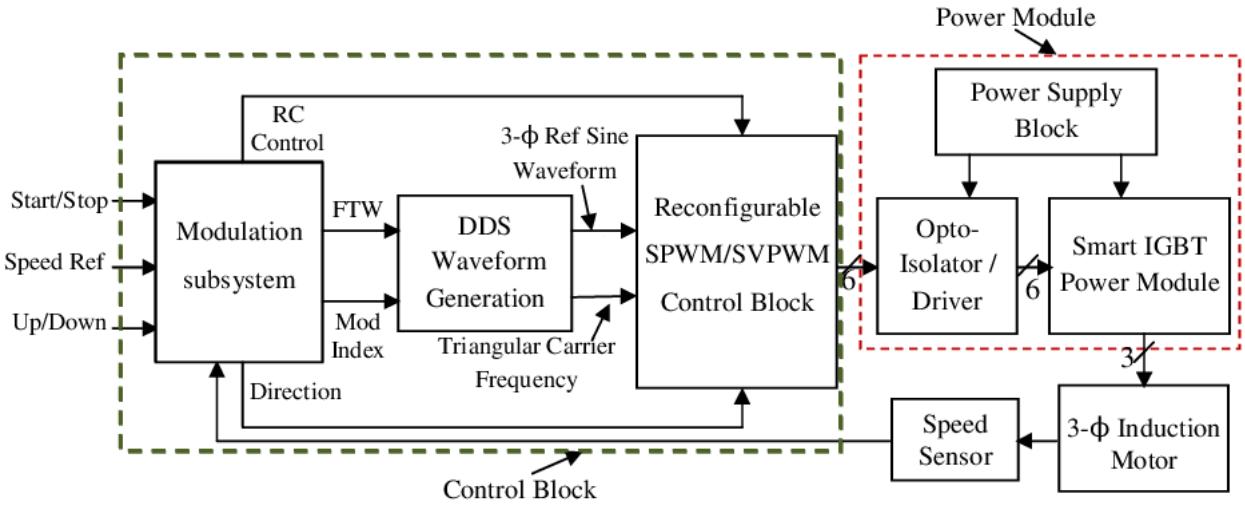


Figure 1. Proposed architecture of the dynamically reconfigurable PWM controller.

SVPWM algorithm provides lower THD% and higher DC bus utilization at higher modulation indexes. The proposed work explores advantages of these two control algorithm by a high speed dynamic reconfiguration. The rest of the paper is organized as follows: section II describes the DDS-RPWM controller architecture based on a DDS sine waveform synthesis; section III discusses the scalar speed control of induction motor drives; and section IV presents the detailed hardware implementation results using smart power module and section V summarizes the conclusions.

2 DDS Reconfigurable pwm controller architecture

The elaborate architecture of proposed DDS-RPWM controller suitable for reconfiguration is as depicted in Figure 1. The controller has the following three functional blocks: Control block, Power Module, and three phase induction motor. The primary functional unit, namely control block has three sub-blocks: Modulation sub-block, DDS waveform generator and reconfigurable sub-module. The modulation sub-block generates necessary control signals to implement the constant V/f speed control algorithm for the three phase induction motor drive. Based on the reference speed command and feedback from the speed sensor, modulation sub-block generates the necessary control signals such as Modulation İndex (MI), Frequency Tuning Word (FTW), Reconfiguration Control (RC Ctrl) and direction for achieving the desired speed pattern. The DDS based waveform generator block generates highly stable three phase variable frequency reference sine waveform and high frequency triangular carrier required for the PWM generation. The reconfigurable control block implements the dynamic reconfiguration of SPWM and SVPWM control algorithm based on the command issued from the modulation sub-block. The functional unit, namely control block is implemented in low cost Cyclone-II FPGA.

The power module block consists of three sub-blocks: Power supply block, opto-isolator/driver, and three phase smart IGBT power module. The power module interfaces the control algorithm from FPGA to three phase squirrel cage induction motor through opto-isolators. An overview of the power module is described in the experimental set-up in section 4.

2.1 DDS Based Waveform Generation Module

The basic block diagram of DDS based sine waveform generator is as shown in Figure 2. The DDS function block has two distinct sub-blocks, namely a phase accumulator and a phase to waveform converter [1-5]. The frequency of the sine wave depends on the rate at which the frequency tuning word is changed. The

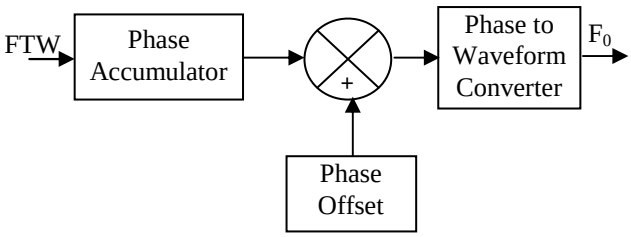


Figure 2. Direct digital synthesis block diagram.

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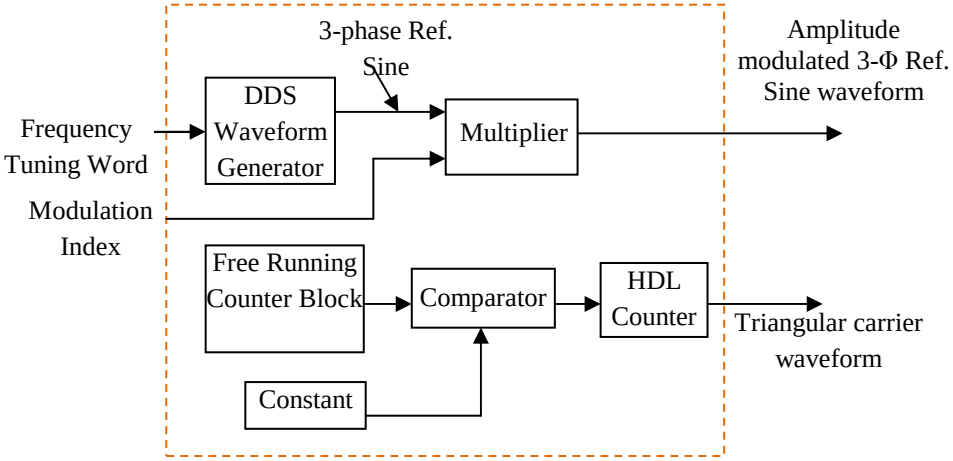


Figure 3. DDS sine and Triangle waveform generation block diagram.

phase to waveform converter is implemented using a sine Look-Up Table (LUT). The phase accumulator generates a succession of addresses at the rate of FTW that is transformed into the desired waveform by using a sine LUT. The 120 degree phase shifted reference sine waveform is generated by adding an appropriate phase offset value to the phase accumulator output. The output frequency of the DDS module is given by Equation (1)

$$F_o = \frac{F_S}{2^N} M \qquad (1)$$

Where F_S the DDS is master clock frequency; M is the frequency tuning word and N is the width of the phase accumulator expressed in number of bits.

The frequency resolution of the DDS module is obtained by setting $M = 1$ in Equation (1) and is given by the equation (2). The frequency resolution of the sine waveform is designed to 0.1 Hz. The frequency range of the sine waveform is set to 2 Hz to 65 Hz.

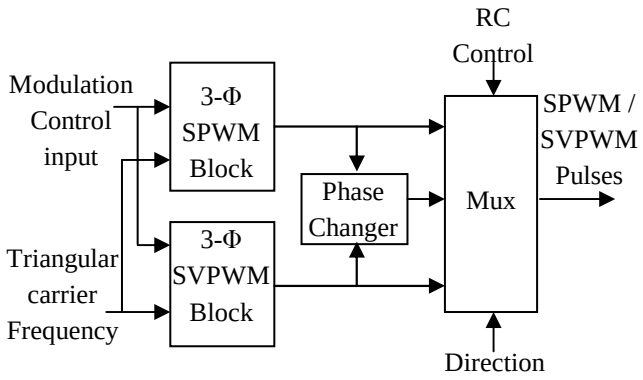


Figure 4. Reconfiguration and direction control block diagram.

$$F_o(\min) = \frac{F_S}{2^N} \qquad (2)$$

The high frequency triangular carrier is generated using a free running counter block and a Hardware Description Language (HDL) counter block as shown in Figure 3. The triangular carrier frequency is related to the DDS clock frequency, as per the equation (3)

$$F_{cr} = \frac{F_S}{2^{L+1}} \qquad (3)$$

Where L is the word length of the counter. The HDL counter block in the Simulink up-counts until the direction input to the HDL counter becomes one. The direction input to the counter is obtained from the comparator block. The triangular waveform generated from the HDL counter is appropriately scaled to set the amplitude between 0 and 1. The modulation index of the SPWM and SVPWM is controlled by scaling the amplitude of the sine wave generated from the DDS block.

2.2 Dynamic Reconfiguration

The reconfigurable control block shown in Figure 4 consists of four sub-blocks: SPWM block, SVPWM block, phase changer and a Multiplexer (Mux). The sine modulation input is applied to SPWM and SVPWM blocks simultaneously. The three phase SPWM and SVPWM pulses are fed to the phase changer block and multiplexer block. The phase changer block swaps the gate pulse sequence of phase R and phase B for speed reversal of the three phase induction motor. The RC

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Table I. Selection logic for control algorithm and direction of rotation of motor.

RC Ctrl input	Direction input	Control Algorithm Selected	Direction of rotation of motor
0	0	SPWM	Clock-wise
0	1	SPWM	Counter clock-wise
1	0	SVPWM	Clock-wise
1	1	SVPWM	Counter clock-wise

Ctrl signal which is generated from the modulation sub-block, will determine which control algorithm is fed to the three phase induction motor drive. The motor will rotate in clock-wise or counter clock-wise depending on whether the direction input is logic zero or one.

The selection of SPWM/SVPWM control logic and the direction of rotation of motor are derived as per the truth table shown in Table I The control algorithms SPWM and SVPWM are implemented as a separate Verilog module and are triggered using 'RC Ctrl' pulse issued from the modulation sub-system. The proposed method implements the reconfigurable module inside the FPGA chip itself. This method improved the speed of reconfiguration compared to the existing methods [10]-[11].

2.3 Carrier Based Space Vector PWM Generation

The SVPWM module used in the proposed controller is the simplified model of the carrier based space vector modulation as reported in the literature [12]-[16]. This model does not require any sector identification and it minimizes the computational requirements for the SVPWM. Since computational requirements are minimum for this SVPWM model, FPGA implementation is highly efficient.

3 Speed control of induction motor drive

The speed control of induction motor can be broadly classified into scalar control methods and vector control methods [17]-[20]. The popular scalar speed control methods include stator voltage control, constant V/f control; slip control, rotor resistance control etc. The proposed DDS-RPWM controller uses the constant V/f based scalar control of induction motor drive. The induction motor used in this model is a 375 watt, 2 poles, and three phase squirrel cage induction motor.

The stator voltage applied to the three phase induction motor is sinusoidal. Then, at steady-state,

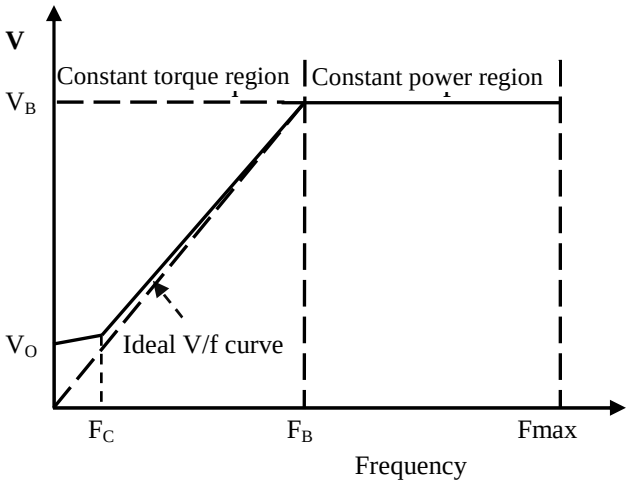


Figure 5. The stator voltage *vs.* frequency curve of speed control of Induction motor.

stator voltage V_S, stator frequency ω, and stator flux ϕ_S is related as per the Equation (4)

$$V_s \approx \omega\tilde{\phi}_s \tag{4}$$

$$\therefore \phi_s = \frac{V_s}{\omega} = \frac{1}{2\pi}\left(\frac{V_s}{f}\right) \tag{5}$$

The Electro-mechanic Torque (T_e) developed by the motor is given by the equation (6); where p is number of poles and $\tilde{i}_s$ is the stator current vector.

$$T_e = k(\tilde{\phi}_s \otimes \tilde{i}_s) = \frac{3p}{4}\left|\tilde{\phi}_s\right|\left|\tilde{i}_s\right|\sin\theta \tag{6}$$

From Equations (5) & (6), if $\left(\frac{V_s}{f}\right)$ remains constant, stator flux remains constant and the torque is independent of the supply frequency. The relationship between stator voltage and frequency under the $\left(\frac{V}{f}\right)$ principle remains constant and the torque is independent of the supply frequency as given in Figure 5. Let V_B and F_B be the rated stator voltage and rated speed of the motor respectively. An initial offset voltage VO is applied to compensate the voltage drop across the stator resistance at low operating frequency ($\leq F_c$) as shown in Figure 5. The synchronous speed of the motor, N_s, is related to stator frequency, f, and number of poles, p, as per the Equation (7).

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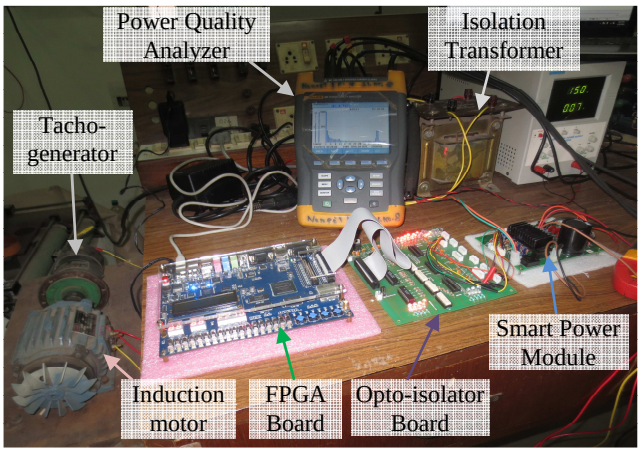


Figure 6. Experimental set-up of DDS-RPWM controller.

$$N_s = \frac{120\,f}{p} \qquad (7)$$

4 Results and discussion

The subsection-4.1 describes the development of the proto-type of the proposed controller. The subsection-4.2 analyses the experimental results. The V/f scalar speed control method is used for the speed control of three phase induction motor.

4.1 Experimental Setup

This section describes the development of the proto-type. The experimental setup shown in Figure 6 has two main units, namely control unit and power module.

The control unit consists of a low-cost cyclone-II based DE2 FPGA board. The control algorithm is implemented in Verilog HDL code. The control pulses generated from the FPGA board is fed into an opto-isolator board for protection and fault-identification.

The power circuit consists of the smart power module, full bridge rectifier with capacitor filter and inductive proximity sensor. The smart power module FSBB20CH60C from Fairchild Semiconductor Corporation is used for the implementation of the three phase full bridge inverter module. A tacho-generator is mounted on the shaft of the motor for speed measurement. An inductive proximity sensor is used for the speed measurement and feedback. The DC bus voltage is generated from a single phase 230 V utility supplies by using a full bridge rectifier module followed by a DC bus filtering capacitor. The power module is isolated from the utility supply point by using an isolation transformer.

4.2 Experimental results

The proposed DDS-RPWM controller is tested in hardware using the proto-type power module which is designed as discussed in the previous section. The various types of speed response of the controller are presented in this section. The DDS based waveform generation block and control algorithms implemented in cyclone-II FPGA are presented in this section.

4.2.1 Step-Speed Forward Response

The reference speed is changed from 0 to 360 rpm at 3.75 s and again a step speed change from 360 to 650 rpm is applied at 8.5 s. At 13.5 s and at 18.5 s a step decrease in speed (360 rpm & 0 rpm respectively) is

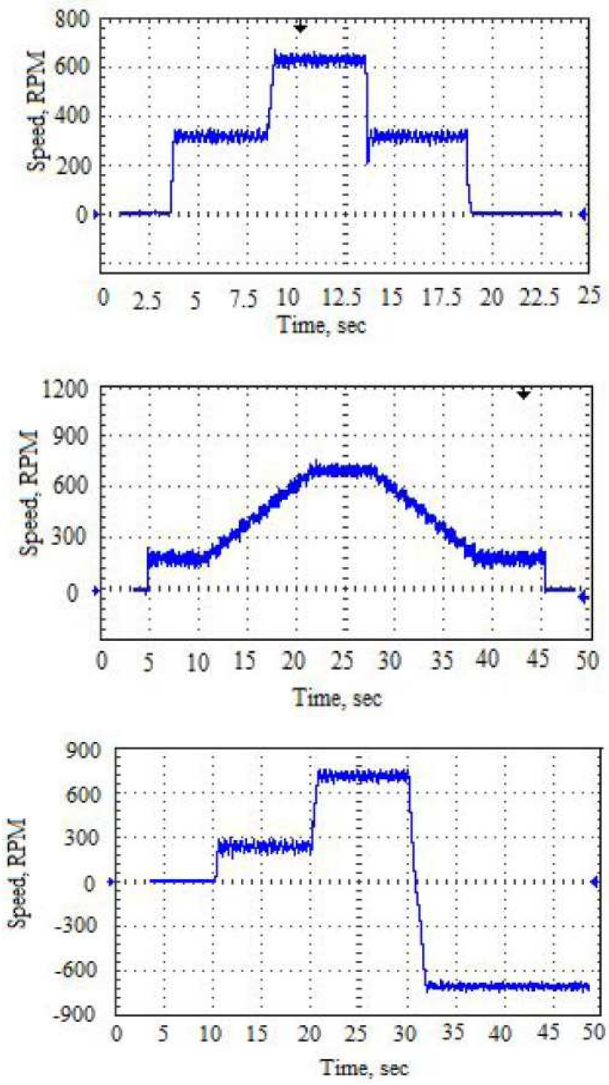


Figure 7. Experimental results for the DDS-RPWM controller under different speed profile, reference speed (black) and measured speed (blue): (a) step-speed forward response, (b) step & ramp speed forward response, (c) step-speed reverse response.

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again applied. The actual rotor speed measured (Nr') and reference rotor speed (Nr) are shown in Figure 7 (a). From the experimental results, it has been observed that the measured speed closely matches with the reference speed.

4.2.2 Step and Ramp-Speed Forward Response

The performance of the drive is experimentally verified by a combination of step and ramp speed forward mode of operation and the results are presented in Figure 7 (b). The experimental result (Nr') closely matches with the reference speed command (Nr).

4.2.3 Step-Speed Reverses Response

The reference speed command is changed in a combination of step forward and reverse speed as shown in Figure 7 (c). The experimental results (Nr') slightly deviated from the reference speed (Nr) during the step reverse command due to the flux reversal and the inertia of the motor.

4.2.4 THD% analysis of SPWM, SVPWM, and DDS-RPWM

The THD% analysis of SPWM, SVPWM and the proposed method under different frequencies are summarized in Table 2 which clearly shows the advantage of the proposed algorithm over the conventional SPWM and SVPWM algorithms. The THD% is low for SPWM for frequencies up to 25 Hz and above 25 Hz; SVPWM shows better THD% performance. The proposed method utilizes this feature to get a better THD% performance by reconfiguring between SPWM and SVPWM control algorithms.

4.2.5 V_{Rrms} vs. Frequency under various control scheme

The Root Mean Square (RMS) output voltage (R Phase) under various control algorithms at different operating frequency is as shown in Table 3. The controller is set in SPWM, SVPWM, and in DDS-RPWM mode to measure the output voltage. The proposed method shows 15.5% improvement in output voltage when compared to SPWM method. This is due to the higher DC bus utilization when the controller is operated in SVPWM method.

4.2.6 Reconfigurable Control Switching

The reconfigurable control switching between SPWM and SVPWM is shown in Figure 8 (a) to 8 (d). The reconfiguration time (Δx) from SPWM to SVPWM is measured to be 470 ns obtained from Figure 8 (b). Similarly, reconfiguration time (Δx) from SVPWM to SPWM is found to be 490 ns as per the Figure 8 (c). The control signal from the modulation sub-block 'RC Ctrl' signal triggers the reconfiguration and V_R, V_Y, and V_B are the gate pulses from R, Y and B phase respectively.

Table 2. Experimental THD % vs. frequency for SPWM, SVPWM, and proposed method.

Frequency (Hz)	SPWM	SVPWM	Proposed method (DDS-RPWM)
2	35	47	35
5	22	37	22
10	15	25	15
15	14	22	14
20	11	19	11
25	7.9	8	7.9
30	7.2	4.8	4.8
35	7	6.4	6.4
40	5.6	3.8	3.8
50	5.8	5.2	5.2

Table 3. V_R (rms) vs. frequencies for SPWM, SVPWM, and proposed method.

Frequency (Hz)	V_R (rms) (V)					
	SPWM		SVPWM		Proposed Method (DDS-RPWM)	
	Simulation	Experimental	Simulation	Experimental	Simulation	Experimental
2	18.40	20.20	21.30	23.50	18.40	20.20
5	18.40	20.40	21.20	23.60	18.40	20.40
10	36.40	39.50	42.00	45.50	36.40	39.50
20	74.00	77.80	85.50	88.50	74.00	77.80
25	94.60	96.20	109.20	110.80	94.60	96.20
30	113.20	115.60	131.10	133.70	131.10	133.70
40	154.80	157.70	179.80	182.30	179.80	182.30
50	198.90	200.30	232.40	231.50	232.40	231.50

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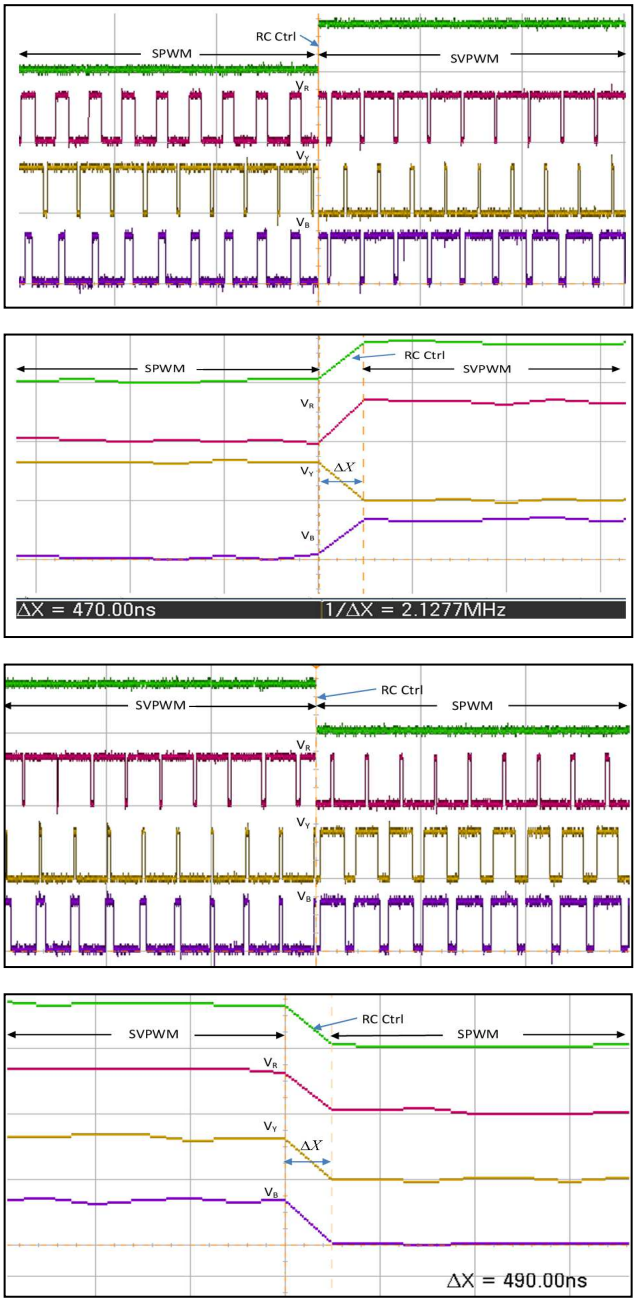


Figure 8. Experimental three phase gate pulses (V_R, V_Y, and V_B) of IGBT smart power module plotted against reconfigurable control signal (RC Ctrl) from FPGA: (a) reconfigurable control switching from SPWM to SVPWM, (b) Transition time from SPWM to SVPWM, (c) reconfigurable control switching from SVPWM to SPWM, and (d) Transition time from SVPWM to SPWM.

The FPGA resource summary of the SPWM, SVPWM and the proposed DDS-RPWM control algorithm are summarized in Table IV. It is evident that the total resource utilization of the DDS-RPWM (20%) is much less than the total resources of SPWM and SVPWM put together (36%).

Control algorithms		FPGA Resources utilized		
		Dedicated logic registers (33216)	Multipliers (70)	Total Combinational logic (33216)
SPWM	A*	13 (<1%)	0	5423 (16%)
	B†	103 (<1%)	10 (14%)	294 (<1%)
	C#	158 (<1%)	16 (23%)	5791 (17%)
SVPWM	A	13 (<1%)	0	5423 (16%)
	B	103 (<1%)	10 (14%)	294 (<1%)
	C	158 (<1%)	40 (57%)	6463 (19%)
Proposed DDS-RPWM	A	294 (<1%)	0	5465 (16%)
	B	103 (<1%)	10 (14%)	294 (<1%)
	C	158 (<1%)	40 (57%)	6490 (20%)

Table 4. Resource summary of SPWM, SVPWM, and DDS-RPWM modules

A* – DDS Sine Module; B† – Modulation Sub Module;

C# –Total Resources.

The proposed work is compared with the existing work reported in the literature as shown in Table V. The most important feature of the proposed work is the time taken for the reconfiguration. Another important feature of this system is that it requires only low cost hardware and software tools. This makes the proposed dynamic reconfiguration is an attractive alternative to existing dynamic partial reconfiguration. The proposed work proves the practicality of the dynamic reconfiguration without using any expensive tool or hardware for FPGA implementation. The time required for reconfiguration is measured as 480 ns which is much faster than the existing method. The whole system is designed as a discrete fixed step model in Simulink and then converted to Verilog HDL code using HDL Coder tool [21]-[23]. The proposed method completely automates the system design and reduces the design complexity as this method does not require any expensive tool or hardware.

5 Conclusions

In this paper, we have described a novel implementation of DDS based dynamic reconfigurable PWM Controller for three phase induction motor drive

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on a low cost Cyclone-II FPGA. The DDS based reference sine wave oscillator reduces the hardware count and hence system complexity.

Table V. Comparison of the proposed work with existing work

Parameters	A RTR FPGA based Drive Controller for Electrical Drive [10]	Proposed Method (DDS-RPWM)
FPGA used	Xilinx Virtex-II Device: XC2V1000	Altera Cyclone-II Device: EP2C35F672C6
FPGA cost	High	Very Low
Reconfiguration time	(0.973 ms) high	(480 ns) Very low
Partial bit-stream required or not	Yes	Not required
Type of reconfiguration	Run Time Partial Reconfiguration	Run Time Reconfiguration (Dynamic reconfiguration)
Reconfiguration tool cost	High cost tool is required*	Lower end FPGA Board (Altera Cyclone-II) with low cost compilation tool† only required.
Design complexity	Very High, since complex design flow that involves configuration pre-fetching to reduce partial reconfiguration time.	Easy to design, since it follows the conventional system design flow

* Xilinx PlanAhead partial reconfiguration tool license is required; †Altera Quartus-II 9.1version.

A high speed dynamic reconfigurable PWM controller that utilizes the advantages of two popular PWM controls algorithms, namely SPWM and SVPWM to improve the THD performance, was developed. The proposed design attains dynamic reconfiguration in 480 ns which is much faster than the existing dynamic partial reconfigurable PWM controller architectures. The proposed design achieves 15% reduction in THD% compared to SVPWM below 25 Hz and 2.4% reduction in THD% compared to SPWM beyond 25 Hz. Different speed patterns such as step, ramp, step reverse and combination of step & ramp are performed using the proposed controller and the reference speed matches with the experimental results closely. Further, the controller performance is experimentally validated with a 375 watt, three phase induction motor using the most popular scalar V/f speed control method.

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