A NEW MULTILEVEL INVERTER TOPOLOGY TO INTEGRATE WIND-SOLAR HYBRID SYSTEM WITHOUT A COMMON DC BUS

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Abstract: *Multilevel level inverters are becoming widely popular due to their capability to synthesize medium or high voltage at its terminal with matured low voltage components. Cascaded H-Bridge(CHB) inverter is one of the three basic topologies of multilevel inverter family known for its modularity. The conventional H-Bridge topology comprises of a basic unit with single independent source and four switches. This makes the topology bulky for higher voltage levels and steps. In this paper a new basic unit for cascaded H- bridge multilevel inverter has been proposed. The modularity of the proposed basic unit can be utilized to integrate wind and solar generation systems without a common DC bus. Its performance is compared with the other multilevel inverter topologies available in the literature in the aspects of required number of components. The Total harmonic Distortion (THD) in the output voltage, Conversion losses and efficiency are estimated and compared with a conventional CHB topology. The basic unit in symmetric mode has been simulated using MATLAB Simulink software package and the obtained results are justified with a hardware prototype.*

Key words: *Multilevel inverter, wind-solar hybrid systems, Cascaded inverter,DC-bus.*

1. Introduction

A multilevel inverter can synthesize a near sinusoidal voltage wave at the output with multiple independent dc sources in the input [1,2]. The extent of sinusoidness in the terminal voltage is based on the number of independent dc voltage sources used [3]. There are three classical multilevel inverter topologies they are, 1. Neutral Clamped Multilevel Inverter (NPC-MLI), 2. Flying Capacitor Multilevel Inverter (FC-MLI), and Cascaded H-Bridge Inverter (CHB-MLI) [4].

In NPC-MLI topology a common dc bus with even number of capacitors is used to synthesize sinusoidal voltage at the terminals. The number of capacitors will be chosen based on the required number of levels. Clamping diodes are connected between the switch pairs. If the number of levels is 'n', then there will be (n-1) switch pairs in the topology. Thus the number of diodes required increases rapidly if the required number of levels in the output voltage is high. The power rating of the switches are uneven in this topology and also there is a possibility of voltage unbalance between the capacitors connected on either side of the common dc bus. This makes the topology unpractical for medium and high power applications [5].

The FC-MLI topology utilizes capacitors in the place of diodes used in a NPC-MLI. The presence of higher number of capacitors provides high ride through capability during the event of faults. The switching of FC-MLI is very flexible when compared to NPC –MLI because a given voltage level can be obtained using different switching combinations. Also, this topology can control both real and reactive power flow. However, the higher number capacitors make the circuit bulky and the control scheme difficult [6]

The cascaded H-Bridge inverters employ independent dc sources instead of capacitors and clamping diodes. Each independent dc source with the corresponding H-Bridge is a full bridge converter. Any number of such modules can be connected based on the desired number of levels required in the terminal voltage. This attribute makes the topology highly modular and attractive for power conversion in solar PV generation systems. However the number of switches increases when the number of levels increases [7].

At present, researchers are focused on reducing the number of switches required for CHB-MLI without losing its modularity. A novel H-Bridge structure is proposed in [8]. The proposed structure can be cascaded to obtain any number of levels. Each basic structure comprises of 2 sources and 6

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switches. Even though this is one switch less per source when compared to the conventional cascaded H-Bridge inverter, the number of components required will increase drastically for higher number of voltage levels and this makes the circuit complex. A basic unit with reduced switch count is proposed in [9], but all the switches used in the topology are bidirectional which increases the conduction losses. A structure similar to the one presented in [8] is suggested in [10], here instead of two sources, one source along with two capacitors, three controllable switches and four diodes are used in each structure. Cascading this structure can enable one to get desired steps in the terminal voltage. But the presence of capacitors in each structure imposes possibility of voltage balancing issues and the diodes can make the controllability of circuit tedious. In the topology suggested in [11], the number of required switches is greatly reduced when compared to the structures discussed above. But, in this structure the switches other than that in the H-bridge are bidirectional. This increases the number of IGBTs or diodes required as the output level increases.

In this paper a new basic unit with reduced switch counts when compared to the above said topologies is presented and its application to integrate renewable energy sources is also suggested. A common DC Bus based Cascaded H-Bridge(CHB) multilevel inverter topology discussed in [12] is shown in the Fig.1

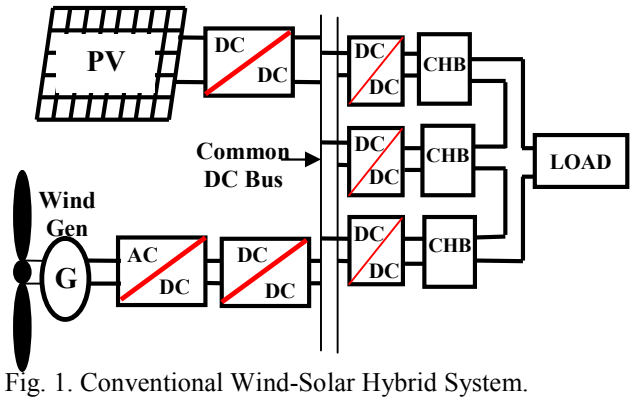


Fig. 1. Conventional Wind-Solar Hybrid System.

The output of the solar PV system and the wind generator is intermittent due to changing solar irradiance and wind velocity respectively. The influence of this intermittency is nullified using rectifier and dc-dc converter circuits [13]. The fixed dc voltage from the terminals of dc-d converter is fed to a common dc bus and this dc voltage is then converted in to AC voltage using an inverter. The number of output voltage levels will be based on the number of CHB units cascaded. If there are 'n' CHB units, then the number of levels will be 2n+1

The proposed multilevel inverter can integrate the wind and solar energy systems without a common dc bus as shown in the Fig.2

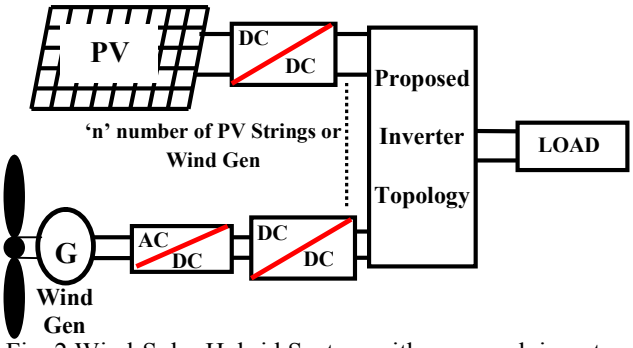


Fig. 2.Wind-Solar Hybrid System with proposed inverter.

In the structure shown in Fig. 2 the necessity of dc bus can be eliminated. Also, the output from each renewable energy generation system can be converted in to independent dc sources and the levels obtained in the output voltage will be proportional to number of such independent sources available. Since the H-bridge units and the DC-DC converters after the DC bus are eliminated, the number of switching components employed in the topology is very low and thus the cost reduces drastically.

2. The Proposed Topology

The proposed basic unit for CHB-MLI topology is depicted in Fig.1.

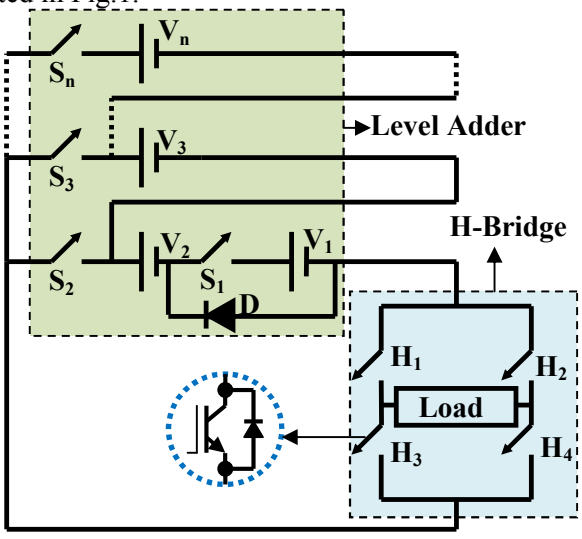


Fig. 3. Proposed basic unit for CHB-MLI topology.

The basic unit comprises of a H-bridge which enables polarity reversal and a level adder circuit comprising of independent voltage sources and the controlling switches as shown in Fig.3. The proposed

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basic unit can be operated in two modes Viz.,

i) Symmetric mode
ii) Asymmetric mode

3. Symmetric Mode

In symmetric mode of operation the magnitude of all the voltage sources are equal. That is

$$V_1 = V_2 = V_3 = \ldots\ldots\ldots = V_n = V_{dc} \quad (1)$$

For the given number of sources 'n' the required number of IGBTs, driver circuits required and diodes are represented in equations 1,2, and 3 respectively.

$$N_{IGBT} = n + 4 \quad (2)$$

$$N_{drivers} = n + 4 \quad (3)$$

$$N_{diode} = 1 \quad (4)$$

From equations 1 and 2, the total number of solid state switches required including diode can be written as in equation 4

$$N_{switch} = n + 5 \quad (5)$$

The number of level generated from the given 'n' sources will be as in equation 5

$$N_{level} = 2n + 1 \quad (6)$$

The standing voltage across the switches in level adder, switches across the H-Bridge, and across the diode can be determined using the equations 6, 7, and 8

$$V_{s-\max} = nV_{dc} \quad (7)$$

$$V_{H-\max} = 4nV_{dc} \quad (8)$$

$$V_D = V_{dc} \quad (9)$$

Therefore the total standing voltage in the circuit can be given as

$$V_{O-\max} = (5n+1)V_{dc} \quad (10)$$

4. Circuit Operation for a symmetric 9-level MLI

Using the above equations 1-6, a nine level MLI can be obtained with four voltage sources of magnitude V_{dc}, a diode, and eight IGBTs. The nine levels of voltage synthesized are + V_{dc} , +$2V_{dc}$, +3 V_{dc} , +$4V_{dc}$, 0 , -V_{dc} , -$2V_{dc}$, -$3V_{dc}$, -$4V_{dc}$. The circuit operation during positive half cycle can be understood from the Fig. 4a, 4b, 4c and 4d and the Table 1.

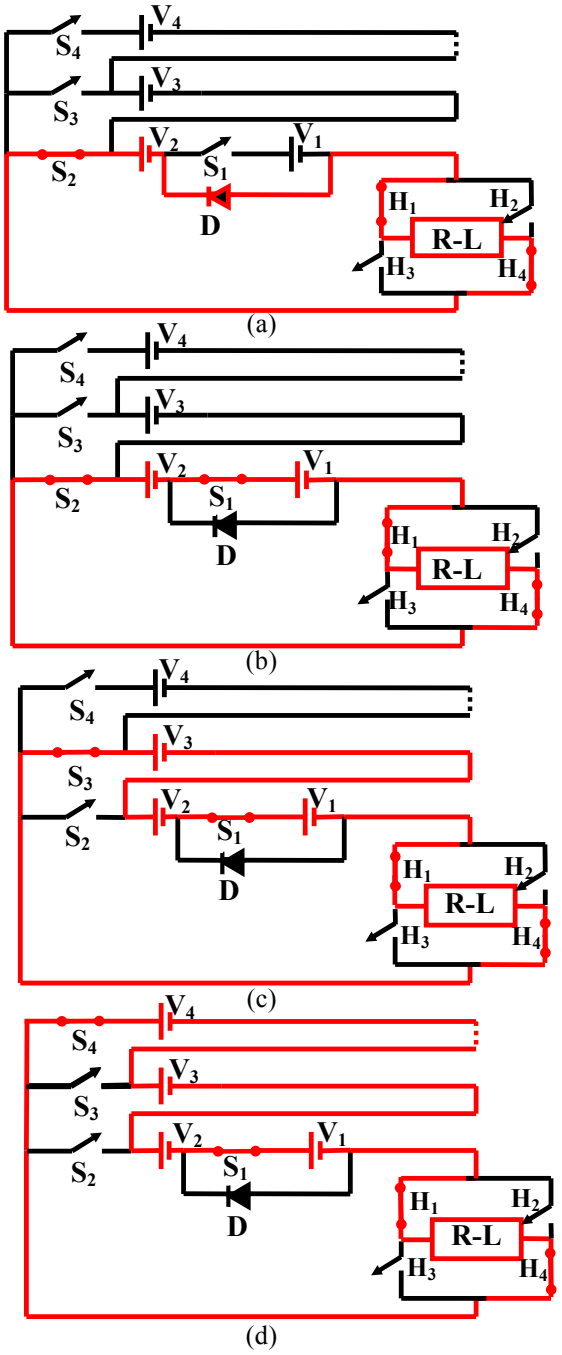


Fig. 4. Circuit operation of proposed nine level MLI (a) +V_{dc} (b) +$2V_{dc}$ (c) +$3V_{dc}$ (d) +$4V_{dc}$.

Table 1
Switches conducting for different level of voltages

S.No	Conducting Switches in level adder	Conducting Switches in H-bridge	Voltage level obtained
1	S_2	H_1, H_4	+V_{dc}
2	S_2,S_1	H_1, H_4	+$2V_{dc}$
3	S_3,S_1	H_1, H_4	+$3V_{dc}$
4	S_3,S_1	H_1, H_4	+$4V_{dc}$

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The voltages $-V_{dc}$, $-2V_{dc}$, $-3V_{dc}$, $-4V_{dc}$, can be obtained by switching the same switches used for the corresponding positive voltage level in the level ladder and the polarity reversal can be achieved by turning ON the switches H_2 and H_3 in the H-bridge instead of H_1 and H_4. By turning on the above said switches sequentially with a suitable control scheme, the output waveform obtained will be like the one shown in Fig. 5.

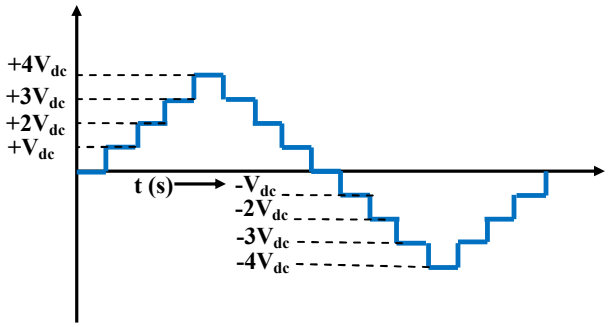


Fig. 5. Model Output Voltage Waveform.

Practically, the switches in the level adder and the H-bridge can with stand only up to certain voltage level, due to their limited voltage rating. This symmetric basic unit can be cascaded with any number of similar units for high voltage applications as shown in the Fig. 6.

The cascaded topology comprises of 'k' basic units with 'n' number of voltage sources in each basic structure. In symmetric mode if magnitude of all the voltage sources are assumed to be equal as shown below,

$$V_{11} = V_{12} = V_{13} = ... = V_{1n} = V_{dc} \quad (11)$$

$$V_{21} = V_{22} = V_{23} = ... = V_{2n} = V_{dc} \quad (12)$$

Until

$$V_{k1} = V_{k2} = V_{k3} = ... = V_{kn} = V_{dc} \quad (13)$$

then the attainable output voltage can be computed as

$$V_{out} = k \times n V_{dc} \quad (14)$$

The standing voltage across the entire circuit can e given as

$$V_{O-\max} = k \times \left[(5n+1) V_{dc} \right] \quad (15)$$

5. Comparison of circuit components for symmetric topology

For the given 'n' number of sources, the components required for the proposed topology is compared with the references [9], [10], [11], and conventional CHB-MLI and tabulated in Table 2. From the Table 2 it can be understood that the proposed topology requires less number of components for the given number of sources 'n'. The number of components required for topology discussed in reference 11 is only marginally high when compared to the proposed topology. But, in that topology the switches other than that in H-bridge

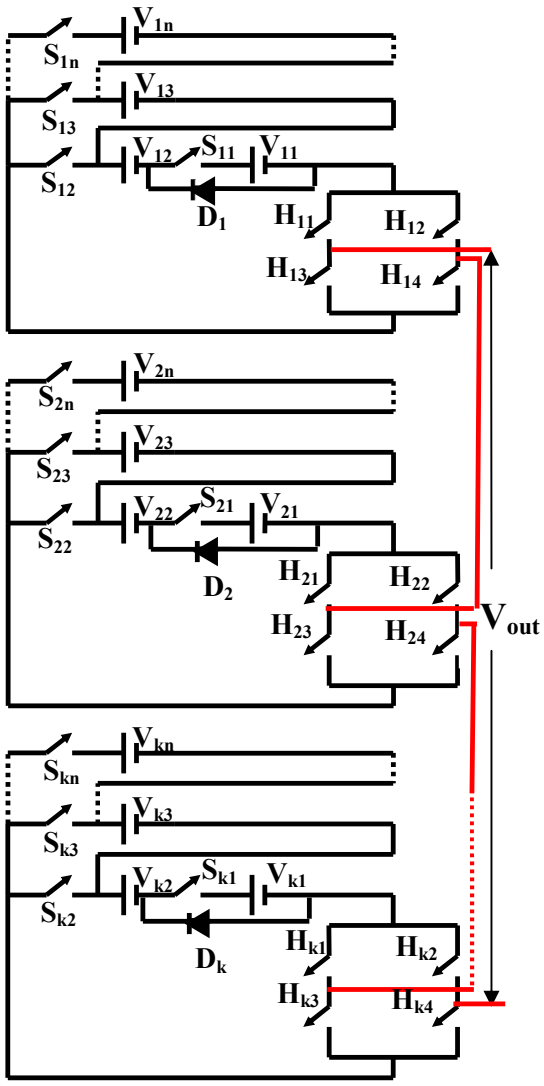


Fig. 6. Cascaded structure of proposed topology.

Table 2
Comparison of Number of sources Vs Circuit components

Topology	Required number of			
	IGBT	Gate driver	diode	capacitor
Proposed	$n+4$	$n+4$	1	0
Ref 9	$2(n-1)+4$	$(n-1)+4$	0	0
Ref 10	$3n$	$3n$	$4n$	$2n$
Ref 11	$n+6$	$n+6$	0	0
CHB-MLI	$4n$	$4n$	0	0

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are bi-directional switches. That is they require two IGBTs per switch or four diodes additionally for each switch. Thus, the components required for the proposed topology is comprehensively less when compared to the topologies presented in recent literature.

The quality of output voltage delivered at the terminals of any multilevel inverter is directly proportional to the number of levels or voltage steps in the wave. In Fig. 7 the required number of IGBTs for different levels is analyzed and from the Fig.6 it can be concluded that to generate a given number of levels in the terminal voltage, the proposed basic unit requires lesser number of IGBTs.

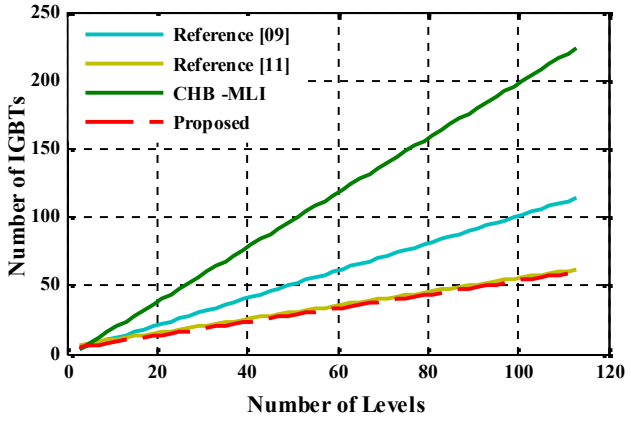


Fig. 7. Number of IGBTs required Vs Number of Levels.

6. Simulation of a 9-level prototype

The proposed inverter topology is simulated using MATLAB/ Simulink software package. The magnitude of individual independent voltage source V_{dc}=21 V , The internal resistance of the IGBT is considered as 0.1micro ohm. The resistance of the connected load is 110Ω and. The load inductance has been considered as 30 mH

A nearest level modulation PWM scheme is used for controlling the proposed topology. The reference frequency is considered as 50 Hz and the pulses for different levels are generated by comparing the reference sine wave with a constant nearest to the desired level [14]. The simulation circuit used for generating pulse pattern is shown in Fig.8.

The Fig.8 portrays the pulses given to one of the switches in the level adder circuit and a switch in H-bridge circuit. The switches in the level adder are triggered twice in every half cycle. For example the pulse shown in Fig.9a is given to the switch S_3, which is conducting twice in a half-cycle to generate the level $+3V_{dc}$. The switches in H-bridge are conducting for a whole half-cycle and turned off for another half cycle as shown in Fig.9b. The pulse shown in Fig.8b is fed to switch H_1 in the H-bridge so that it is turned ON during positive half cycle and zero state and turned off during negative half cycle. Here the magnitude of independent voltage sources has been assumed as 21 V and there are 4 such sources used.

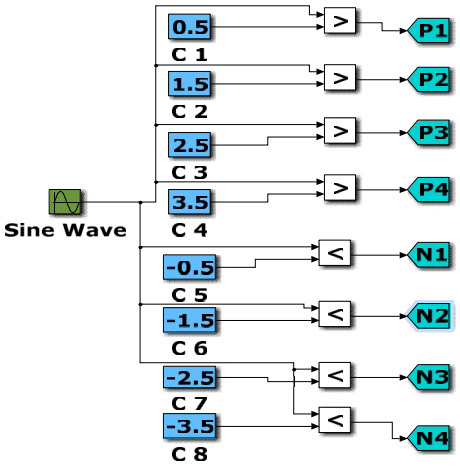
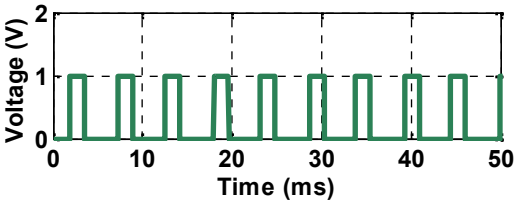
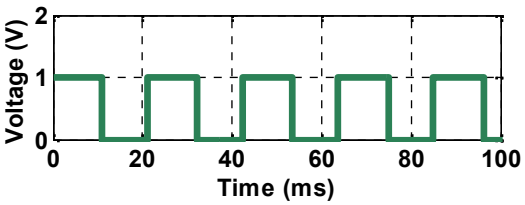


Fig. 8. Simulation circuit for pulse generation



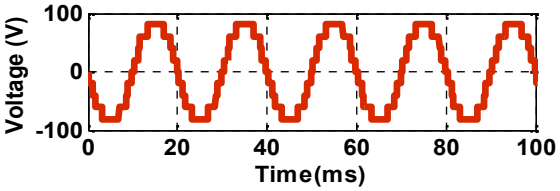
(a)



(b)

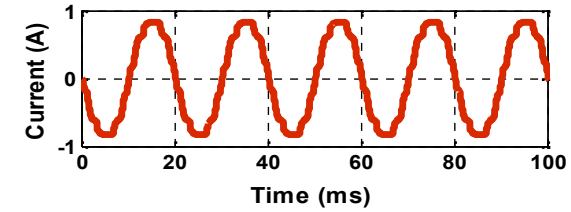
Fig 9. Pulses given (a) level adder switch
(b) H-bridge switch.

For a load resistance and load inductance of 110Ω and 30 mH , the peak value of terminal voltage will be 84V and the current through the load will be 0.8 A. The same can be observed in the Fig. 10a and Fig. 10b. The voltage THD of the inverter's terminal voltage is obtained as 9.54 %

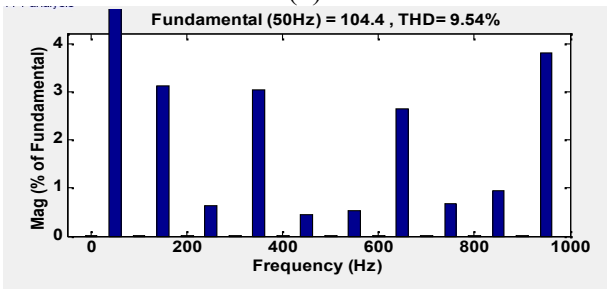


(a)

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(b)



(c)

Fig.10. Simulation results (a) terminal voltage (b) load current (c) Voltage THD.

7. Evaluation of Losses

The Switching frequency of a practical switch is limited as it requires a finite turn-on ($T_{s\text{-}on}$) and turn-off times ($T_{s\text{-}off}$). Also, there will be a reverse current flow during OFF state and a forward voltage drop during the ON state. Due to these reasons a practical switch experiences a conduction loss during the on-state because of the internal resistance of switch and switching loss during the switching transitions $T_{s\text{-}on}$ and $T_{s\text{-}off}$ as shown in the Fig.10. [15] The average power loss across a switch is based on its switching cycle. The linear approximation of average power loss over one switching instant for a practical switch is shown in the Fig.11 [16]. The instantaneous current can be represented as in equations 16, 17, and 18 and the instantaneous value of voltage can be calculated in a similar way.

$$i(t) = \frac{T}{T_{s-on}}\left(I_c - I_{leakage}\right) + I_{leakage} \qquad (16)$$

$$for\ 0 \le T \le T_{s-on}$$

$$i(t) = I_c \qquad (17)$$

$$for\ T_{s-on} \le T \le T_{s-off}$$

$$i(t) = -\frac{T - T_{total}}{T_{s-on}}\left(I_c - I_{leakage}\right) + I_{leakage}$$

$$for\ T_{total} - T_{s-off} \le T \le T_{total} \qquad (18)$$

The average power loss over one conduction period can be derived as

$$P_{average} = \frac{1}{T_{total}} \int_0^{T_{total}} v(t) \times i(t)\, dt \qquad (19)$$

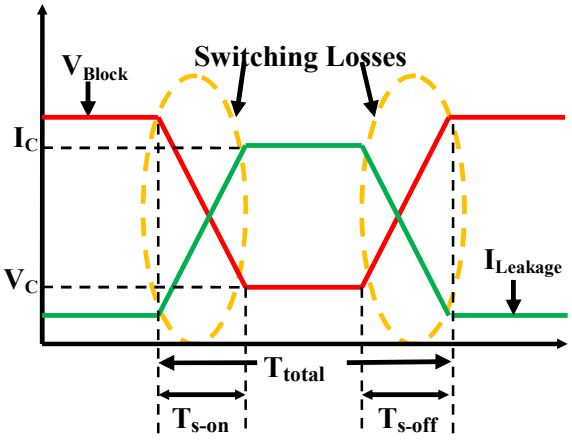


Fig.11. Linear approximation of current and voltage switching of a practical switch.

On substituting the instantaneous value of currents obtained in equations 16, 17, and 18 and the corresponding value of voltages in equation 19 and simplifying the two loss components conduction loss and switching loss can be derived as [16]

$$= \frac{V_{BLOCK} I_c}{T_{total}}\left(\frac{T_{s-on} + T_{s-off}}{6}\right) + \frac{V_c I_c}{T_{total}}\left(T_{total} - T_{s-off} - T_{s-on}\right) \qquad (20)$$

8. Switching Losses

In Switch S_3 for a blocking voltage V_{BLOCK} = 21V, conduction current I_c = 0.8A, $T_{s\text{-}off}$ = 18µs ,$T_{s\text{-}on}$=10µs and T_{total}= 4ms; The switching loss can be calculated using the first component in equation 20 [15,16].

$$P_{switching} = \frac{V_{BLOCK} I_c}{T_{total}}\left(\frac{T_{s-on} + T_{s-off}}{6}\right) \qquad (21)$$

$$P_{Switching} = \frac{21 \times 0.8}{4 \times 10^{-3}}\left(\frac{28 \times 10^{-6}}{6}\right) \qquad (22)$$

$$= 0.0196\text{W}$$

The average power dissipated in the IGBT S_3 per switching instant is 0.0196 W. The total switching loss can be obtained by multiplying the loss per switching instant with number of switching instants.

9. Conduction losses

The conduction current causes dissipation of power in the IGBT's internal resistance resulting in conduction losses [16]. In the Fig.12 it is observed that the voltage drop across the switch during the conduction period is 1V and the conduction current is 0.8 A.

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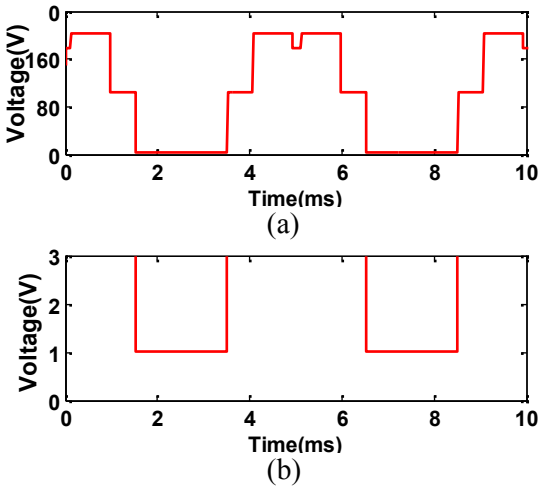


Fig. 12. Voltage Blocked across switch S3 and its zoomed view

With the above said values of $T_{s\text{-}on}$, $T_{s\text{-}off}$, T_{total} and a conduction current I_c the conduction loss across the switch S_3 can be calculated using equation 20 as

$$P_{Conduction} = \frac{V_C I_C}{T_{total}}\left(T_{total} - T_{s-off} - T_{s-on}\right) \qquad (23)$$

$$P_{Conduction} = \frac{1\times 1}{4\times 10^{-3}}\left(\left(4\times 10^{-3}\right)-\left(18\times 10^{-6}\right)-\left(10\times 10^{-6}\right)\right) \qquad (24)$$

The average conduction loss in switch S_3 is 0.794 W. Similarly the switching and conduction losses across other switches are calculated and the total switching and conduction losses are obtained as 0.04396 W and 2.4314 W respectively. The efficiency can be calculated using equation 25

$$\eta = \frac{P_{load}}{P_{in} + P_{loss}} \qquad (25)$$

Here the output power is 32.11 W, from the losses calculated above and the output power, the input power is 34.58 W. This gives an efficiency of 93%. In the common DC bus based topology discussed in [16], the efficiency is only 91 %, due to the higher number of switches in the conduction path.

10. Experimental verification

In order to verify the simulation results an experimental prototype in symmetric mode with the ratings given in Table 3 have been fabricated. The nine level output voltage obtained experimentally and the corresponding load current waveform are shown in Fig.13. In the highlighted area of Fig.14 the rms voltage, current and the experimental voltage THD can be observed. The experimental THD 10.534 % is very nearer to the simulated example.

Table 3
Hardware Specification

Sl.No	Component	Rating
1	RL Load	R=100 Ohm L=35mH
2	IGBT-Model, No:BUP 400D	V_{CE}=600V, I_c=22A
3	Gate Driver Circuits	Drive up to I_c=150A and V_{CE}=1200V
4	Pulse Generator	FPGA Spartan XE3S250E
5	$V_1=V_2=V_3=V_4$=20 V	V_{out}=80 V_{peak}

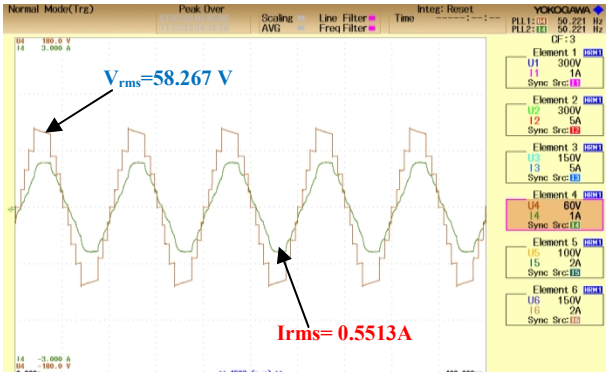


Fig.13. Experimental 9-Level output voltage and load current

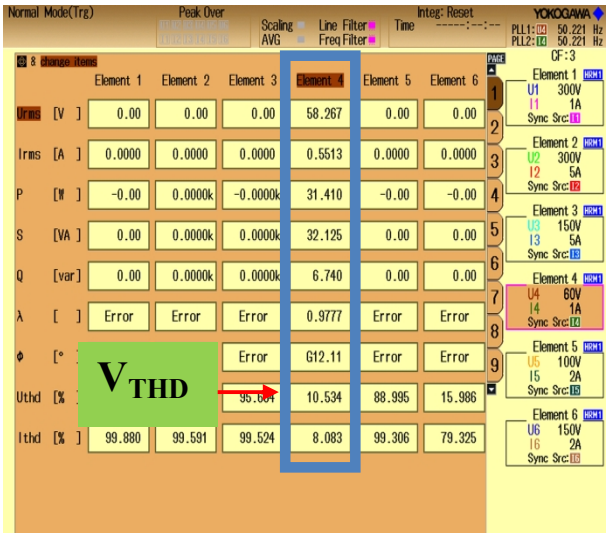


Fig.14. Experimental Voltage THD obtained

The common DC bus topology in [16] requires switch gears which can handle very high voltage levels and other necessary high voltage accessories. But, the proposed basic unit can deliver higher voltage levels with a set of low voltage sources and corresponding LV accessories, Further the number of switching components to synthesize nine levels is

seventeen in Common DC bus based topology and the ZA-MLI topology requires only Eleven Switching components. The cost comparison is given in Table 4

Table 4
Cost Comparison

For a 1kW system synthesizing nine levels,	Number of Switching Components	Cost
Reference [12] (With Common DC Bus)	17	91.97 USD@ (5.41 USD per IGBT)
Proposed Topology (Without Common DC Bus)	11	59.41 USD @ (5.41 USD per IGBT)

11. Conclusion

A new multilevel inverter topology has been proposed in this paper which is suitable for integration of wind and solar energy systems without a common DC bus. The inverter is capable of operating in both symmetric and asymmetric mode. The equations to determine the number of components and levels are derived for both symmetric and asymmetric modes. A detailed performance study of the inverter has been done with a nine level simulation and experimental prototypes. From the analysis it has been confirmed that for the given number of sources and required number of levels, the proposed topology needs less number of components when compared to similar available topologies in the literature and its efficiency is 2 % higher when compared to the common DC bus based topology. The result obtained from the experimental prototype coincides well with its simulated counterpart.

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