Evaluation Methods for Incorporating Non-Deterministic Characteristics in PWM Strategy of Induction Motor Drives and FPGA Based Experimental Implementation

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Abstract –The primary advantages of non-deterministic pulse width modulation (PWM) strategies are that the harmonic power in the output voltage is spreaded over wider range in the frequency spectrum and does not get grouped at definite frequencies. This absence of distinct dominant harmonics results generally in reduction of acoustic noise and torque ripples in the drives. The effectiveness in acoustic noise reduction is contingent on how efficiently the non-deterministic characteristics (randomness) are being incorporated in the PWM strategy. This paper proposes two dissimilar approaches to integrate the randomness in the PWM suitable for induction motor drive. Primarily, a Pseudo Random Binary Sequence (PRBS) bit based random carrier PWM (RCPWM) is deliberated. Then, a comprehensive investigation of performance of random pulse position pulse width modulation (RPPPWM) is worked out. A comprehensive simulation study on performance characteristics such as harmonic spectrum, total harmonic distortion (THD), harmonic spread factor (HSF) and power density spectrum, are presented for conventional sinusoidal PWM (SPWM), RCPWM and RPPPWM. The results are validated through the prototype VSI designed. The implemented pulse width modulators using a SPARTAN-6 field programmable gate array (FPGA) (XC6SLX45) device corroborate the simulation study and hint the triumphing one.

Keywords: Field programmable gate array (FPGA), harmonic spread factor (HSF), power density spectrum, random carrier pulse width modulation (RCPWM), random pulse position pulse width modulation (RPPPWM), total harmonic distortion (THD) and voltage source inverter (VSI).

1. INTRODUCTION

The prominence and the exploitation of voltage source inverters (VSIs) are developing unprecedentedly in industrial applications. The theory involved in pulse width modulation (PWM) technique, which is employed to attain the required output voltage and quality in the load side of the inverter, decides the competence of the drive system. PWM-VSI has developed as a dominant technology in today's industrial environment [1]-[5]. An enormous number of PWM switching pattern generators have been developed over the last four decades to encounter the requirements, primarily, distortion free output waveforms i.e. lower total harmonic distortion (THD), development of larger fundamental component, upholding the linearity between fundamental and modulation index (M_a) etc. [6]-[10]. Even though the performance requirements diverge with the applications, the requirements of VSI based drives are noticed prominently. The performance and the quality of output waveforms can be improved through an ingenious PWM theory [11]-[12]. An imperative advantage of random (nondeterministic) pulse width modulation (RPWM) techniques is non-repetitive spectral characteristics of the output waveforms without energy concentration at distinct harmonics [13]-[15].

Moreover, this period is outstanding due to the revolution of technological possibilities in the field of digital electronic control by micro controller, digital signal processor (DSP), complex programmable logic devices (CPLD), field programmable gate array (FPGA) and application specific integrated circuit (ASIC) technologies [16]-[17]. Among all these likelihoods, FPGA is a good candidate having the advantage of the flexibility in the programming solution and the efficiency of a specific architecture with higher integration density and higher speed. The FPGA technology delivers the programmable system-on-chip (PSoC) environments for designing modern digital ASIC controllers for specific applications.

A.M.Trzynadlowski *et al.,* have developed a RPWM technique to reduce acoustic noise and mechanical vibration [18]. The random switching is based on a uniform probability density function. The preeminence of the RPWM techniques over the deterministic PWM methods is studied. Thomas G. Habetler and Deepakraj M. Divan have introduced an acoustic noise reduction option using a randomly modulated carrier [19]. The randomly modulated carrier is compared with reference waveform to produce the RPWM pulses. In this technique, random signal is used as the modulating function, the effects of its magnitude and varying speed (or bandwidth) on the inverter output harmonic distributed characteristics are analyzed.

The design and development of dynamic partially reconfigurable PWM (DPRPWM) controller for three-phase VSIs in a single Xilinx Spartan 3 XCS400PQ208 FPGA has been developed [20]. A structure of FPGA-based three-level space vector modulation (SVM) inverter has been proposed [21]. The SVM algorithm for three-level

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inverter is described, including the approach to calculate the dwell times of each switching state using volt-second characteristic, the algorithm for determining the space vector location and the principle for selecting switching sequences to generate symmetrical PWM output waves. The standard design flow of FPGA implementation and the functional block diagram of FPGA realization are given. Five-phase sinusoidal PWM signal generator at fast sampling frequency using one-chip programmable gate array has been realized.

It is presented that the generation of sinusoidal PWM using FPGA can achieve switching frequency of the inverter at 40 kHz that may raise potential for excellent drive performances [22]. A FPGA based speed control IC for three-phase induction motor drives have been presented [23]. The sinusoidal PWM (SPWM) is realized on a single FPGA chip from Xilinx Inc. to deliver controlling switching pulses for inverter block.

Even though the industrial society has understood the PWM persuaded torque ripples and acoustic noises, the lack of systematic evaluation of existing PWM techniques break further verdicts. The analog platform is inappropriate to non-deterministic PWM methods because of their nature. A flexible, reprogrammable digital platform could solve this issue. In this paper, a methodical study on performance characteristics such as harmonic spectrum, total harmonic distortion (THD), harmonic spread factor (HSF) and power density spectrum, are presented for both conventional SPWM and the two developed RPWM methods. A FPGA based implementation and validation of Pseudo Random Binary Sequence (PRBS) bit based random carrier PWM (RCPWM) and random pulse position pulse width modulation (RPPPWM) for the three-phase VSI fed induction motor drive, are presented.

The results are validated through the prototype VSI designed. The proposed RPWM architectures have been designed using the Very High Speed Integrated Circuit (VHSIC) Hardware Description Language (VHDL). The functional simulation of the architecture has been carried out using the tool Modelsim 6.3. The Register Transfer Level (RTL) level verification and implementation are done using the synthesize tool Xilinx ISE 13.2. The designed architectures have been configured to the SPARTAN-6 FPGA (XC6SLX45) device.

2. INTEGRATION OF RANDOMNESS IN SPWM

2.1 Random Carrier RPWM

In RCPWM, the randomness is added in the initial stage of the pulse generation. The carrier is synthesized from two different carriers and the synthesizing process involves the randomness. Fig.1 shows the randomized triangular carrier generation and also the complete RPWM system. As shown in Fig.1, the triangular carrier with fixed frequency 'f_{c+}' and the triangular carriers with fixed frequency (same as 'f_{c+}') but opposite phase 'f_{c-}' are given as input to the 2×1 multiplexer. The randomized triangular carrier 'f_R' can be obtained randomly selecting the f_{c+} and f_{c-} by the PRBS bits 0 or 1 obtained using the linear feedback shift register (LFSR).

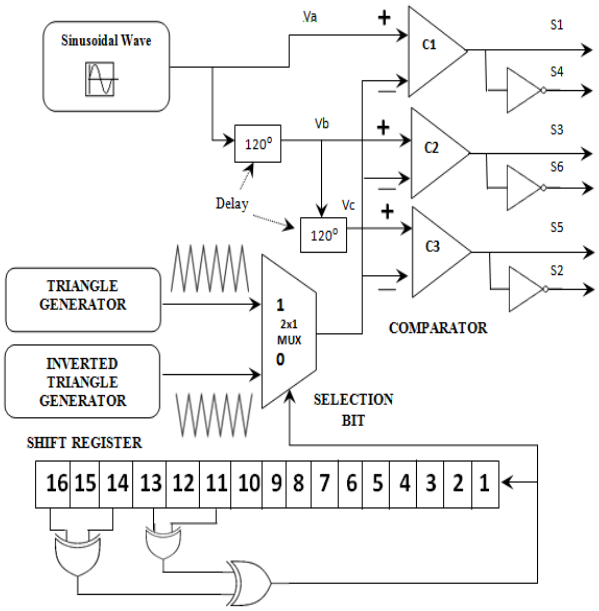


Fig.1. Random Carrier PWM

In order to obtain the random bit for selecting the winning triangle and synthesize a highly randomized carrier, a winning sequential digital circuit with large number of distinct states (bigger repetition cycle) is required. This is because the randomness does not rely only on two distinct carriers but also on the sequential pattern used for selection. LFSR is the best solution to offer the above requirement (more randomness) [24-26]. The principle of LFSR is based on the logical operation of several bits of a digital number and is commonly known as pseudo PWM code generator in communication systems [26]. In this study, 16 bits LFSR with a feedback of four tapings is used and the feedback causes the register to loop through repetitive sequences of pseudo-random value. The choice of taps determines how many values there are in a given sequence before the sequence repeats. The optimum tapping bit numbers are used for logical XOR operation (Bits 4, 5 and 6, 8). Repetition also depends upon the length of LFSR and the clock frequency used. Lastly, the winning triangle carrier cycle based resultant carrier f_R is compared with sinusoidal reference to get the gating pulses.

2.2 Random Pulse Position Scheme

The randomness can also be integrated in the pulse position instead at the carrier cycles. The resultant RPPPWM also spreads voltage and current harmonics over a wide frequency range by incorporating randomness in the switching pulse positions. Fig.2 illustrates the fixed switching frequency RPPPWM scheme, which consists of logical circuits and random bits generator. Here, the fixed frequency triangular carrier and its inverted form (180 degree shifted) are considered like previous assimilation. While the gating pulses are generated separately for both the types of carrier, and hence pulses of two groups are available viz. (P_1-P_3) and (Q_1 to Q_3). The selection among these two groups is done using a select signal,

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pseudorandom binary sequence (PRBS) bits.

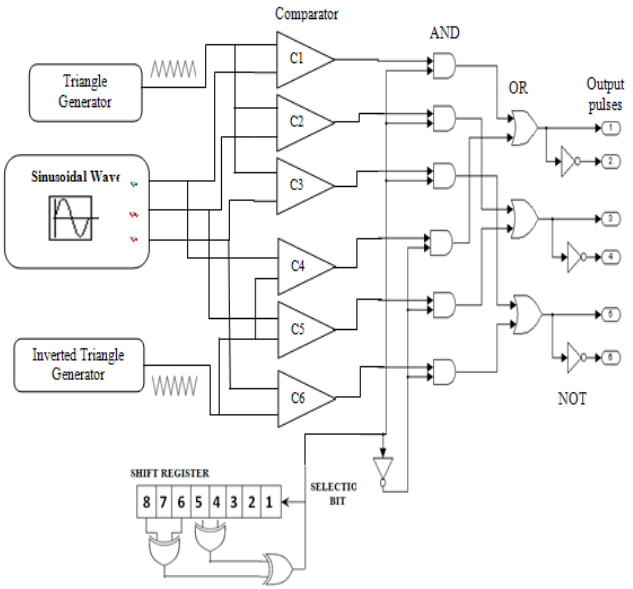


Fig.2. Fixed switching frequency with random pulse position scheme

If the PRBS bit is 1, pulses (P_1-P_3) are selected else (Q_1 to Q_3) and the selected output pulses are marked as 1, 3 & 5 in Fig.2. Once the group is selected then lingering pulses 2, 4 & 6 are generated by inverting 1, 3 & 5.

3. SIMULATION STUDY

The simulation study is performed in MATLAB/Simulink software with ODE Solver ode23tb. A three-phase VSI inverter with three-phase squirrel cage induction motor (0.75 kW) is considered. The input dc voltage (V_{dc}) is 415 V and the output frequency is taken as 50 Hz. The switching frequency of SPWM is 3 kHz while the RPWM strategies employ ±3 kHz.

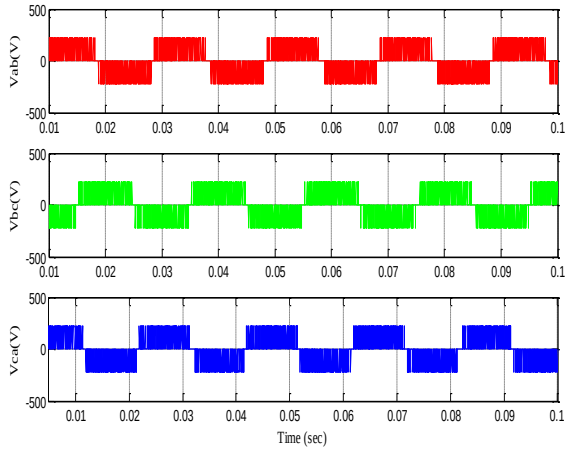


Fig. 3. Simulated line-line voltage waveform for Ma=0.8

The line voltage and current waveforms resulted from SPWM are illustrated in Fig.3 and Fig.4 respectively for modulation index, M_a=0.8. The output voltage is three level pulsed waveform with rectangular envelop as expected. The current waveform is closer to sinusoidal due to the filtering action of stator winding inductors. The results prove the fundamental characteristics of SPWM. M_a controls the fundamental component value (V_1) of output voltage. When the M_a value is increased the V_1 value also increases. The THD has inverse relation with both M_a and V_1. When M_a is increased, THD decreases. The value of HSF also has inverse relation with M_a. For the M_a value of 0.2, the HSF is 8.3 and it falls around 5 when M_a is raised to 1.

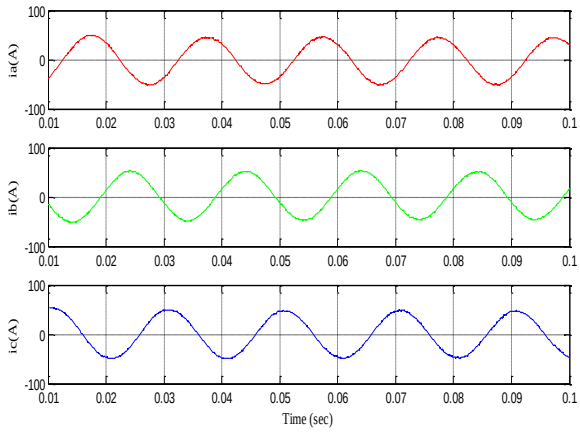


Fig. 4. Simulated line current waveform for Ma=0.8

All the general characteristics of SPWM are also possessed by the RCPWM. Also there are no significant changes at V_1 and THD values, while the HSF values are meritorious in RPWM methods. For example at M_a value of 0.2, the HSF is 41% lesser in RCPWM than SPWM while 42% lesser in RPPWM. Throughout the working range of M_a, the RCPWM and RPPWM offer similar value or little enhanced values for V1 while lesser value for the THD.

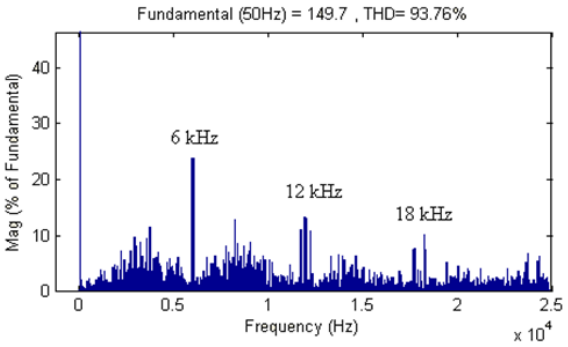


Fig. 5. Spectrum of output voltage

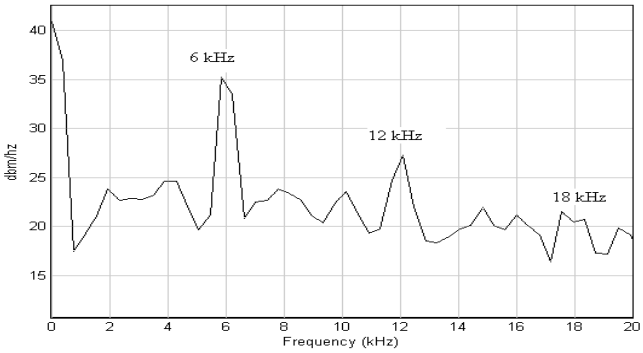


Fig. 6. Power spectral density for Ma= 0.8

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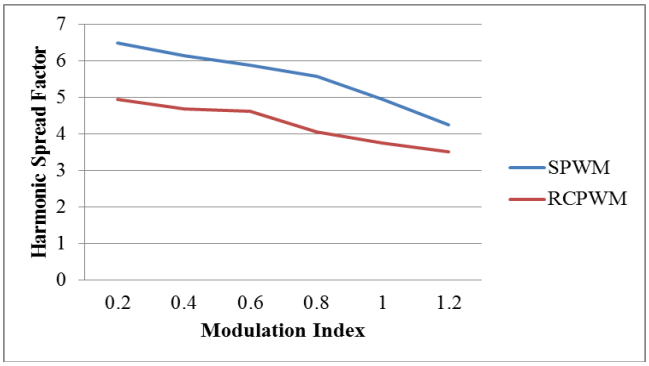


Fig. 7. HSF and Modulation Index- SPWM and RCPWM

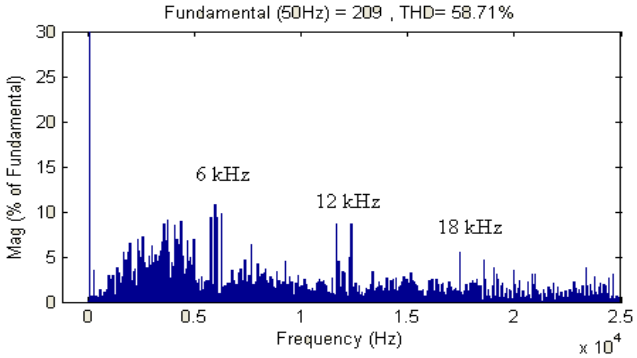


Fig. 8. Spectrum of output voltage (Ma=1.2)

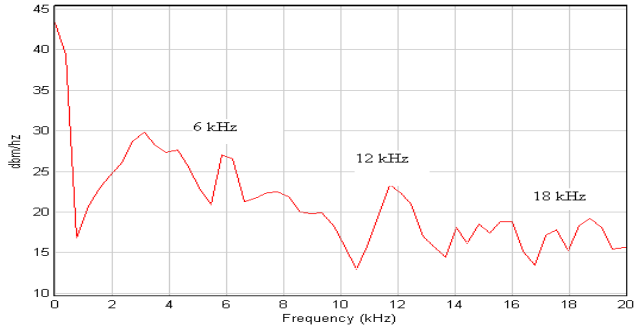


Fig. 9. Power spectral density (PSD) (Ma= 1.2)

Fig.5 illustrates the output spectrum output voltage for the RCPWM and the power density spectrum (PSD) is depicted in Fig.6. The curve drawn in Fig.7 exhibits the modulation depth dependency of HSF. Archetypal harmonic spectrum and PDS of RPPPWM are presented for Ma=1.2 in Fig.8 and Fig.9 respectively. The distortion (deviation of any waveform from the sinusoidal waveform in shape) can be better indicated/marked using the index THD. This formula is suitable for both voltage as well as current waveforms.

$$THD = \sqrt{\frac{V^2_{2(rms)} + V^2_{3(rms)} + \ldots + V^2_{n(rms)}}{V^2_{1(rms)}}} \qquad (1)$$

Where, V_1 is the RMS value of fundamental component of the output voltage of the VSI, V_2 is the RMS value of second harmonics and so on. For evaluating the harmonic spread effect of the different any PWM strategy, a simple quality indicator would be useful. For this purpose, the concept of statistical deviation can be employed and the HSF is defined as follows,

$$HSF = \sqrt{\frac{1}{N}\sum_{K=0}^{N}(H_j - H_0)^2} \qquad (2)$$

$$H_0 = \sum_{j>1}^{N}(H_j) \qquad (3)$$

Where, 'Hj' is amplitude of j^{th} harmonics, 'H_0' is average value of all 'N' harmonics. Table 1 compares sinusoidal, random carrier (RC) and random position (RP) PWM methods in terms of V_1, THD and HSF. From the results, it is understood that both RC and RPP PWM methods offer lesser HSF than the conventional SPWM. The performance of the RPPPWM is little better than the RCPWM.

Table 1.Comparison of SPWM, RCPWM and RPPPWM

M_a	V_1(V)			THD %			HSF		
	Sine	RC	RPP	Sine	RC	RPP	Sine	RC	RPP
0.2	74	75	76	242	241	241	8.3	4.9	4.8
0.4	136	137	140	168	168	166	6.1	4.7	4.4
0.6	211	211	213	123	122	121	5.9	4.6	4.3
0.8	293	294	294	90	89	89	5.6	4.1	4.0
1.0	366	367	368	66	66	66	5.2	3.7	3.6
1.2	394	395	400	59	58	56	5.0	3.5	3.2

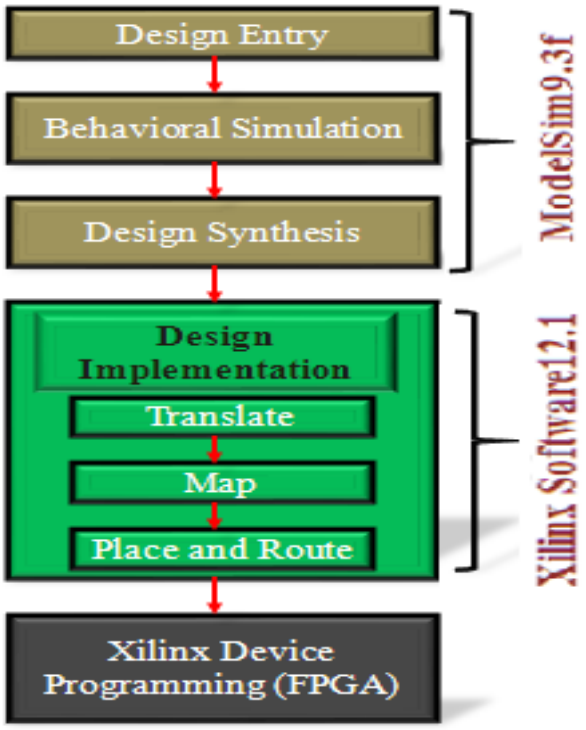


Fig.10. The involvements of Modelsim and Xilinx tools

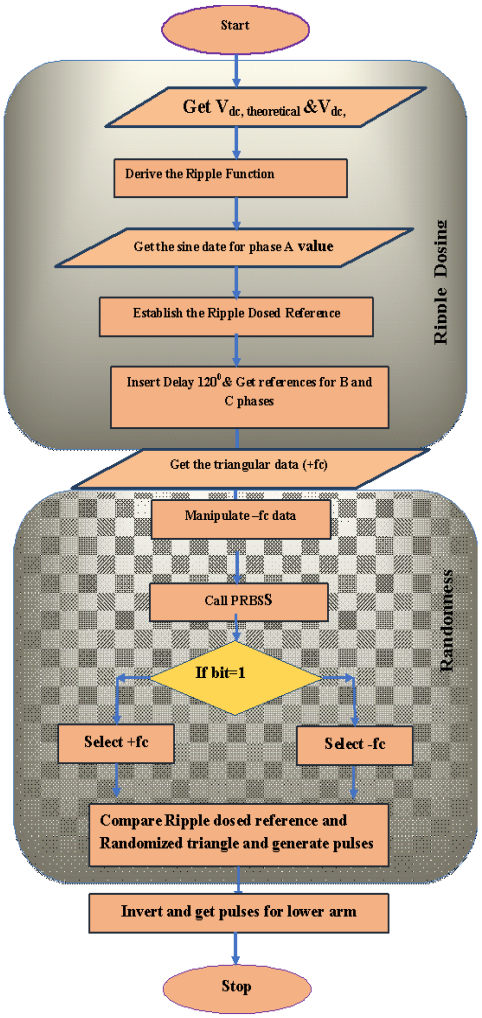


Fig. 11. Implementation of RCPWM

4. HARDWARE IMPLEMENTATION

The proposed RPWM architectures are designed using the VHDL language. The functional simulation of the architecture is carried out using the tool, Modelsim 6.3. The RTL level verification and implementation are done using the synthesize tool Xilinx ISE 13.2. Then the designed architectures are configured to the SPARTAN-6 FPGA (XC6SLX45) device [27]-[29]. The functionality of each block in the architecture is simulated thoroughly using the Modelsim software. The involvement of Modelsim and Xilinx software tools are detailed in the Fig.10 as a flow chart.

The algorithm involved in the RCPWM implementation is diagrammed in Fig.11. The triangular data is initialized first and inverse triangular data is derived from it. This conserves the resources and also does not involve any inaccuracy as 'fc+' and 'fc-' both are identical but 'fc-' is inversed form of 'fc+'. From the fed sine reference data of 'A' phase, datum for the 'B' and 'C' phases are derived. The references for 'B' and 'C' phases are just phase delayed versions of 'A'. The next step is selection between 'fc+' and 'fc-', which accomplished by a binary select input. If the bit is '1', 'fc+' is selected else 'fc-' is selected.

The spreading ability and the HSF value depend on how the select bit is randomized. The so called LSFR sequence select between the carriers and its comparison with the reference result in required pulses for the VSI. The step involved in getting PRBS is indicated in Fig.12.

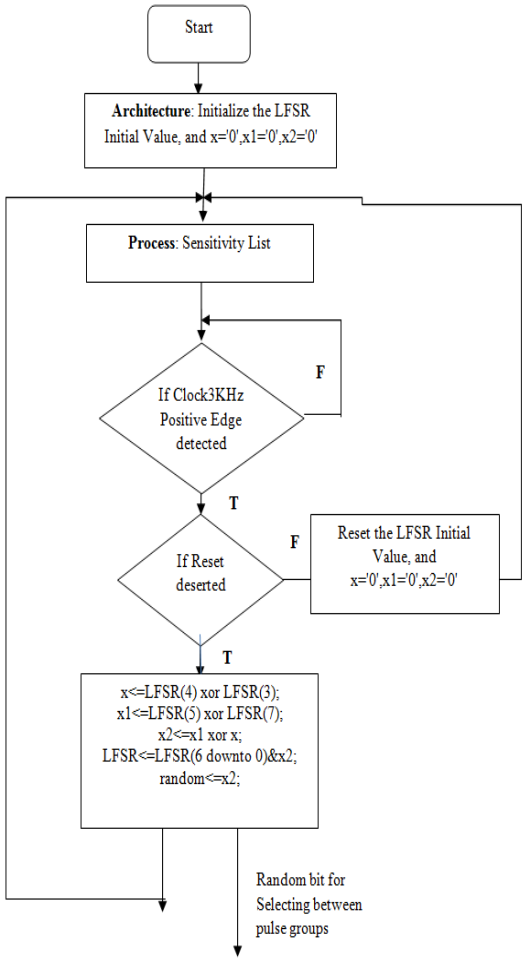


Fig. 12. Generating PRBS

The simulated VHDL Design of the RCPWM architecture is synthesized using Xilinx ISE software. The RTL verification and logic implementation of the design are carried out here. The corresponding synthesis results are shown in Fig.13 and Fig.14. The gating pulses generated for the modulation index 0.8 (RPPPWM) is presented in Fig.15 and the complete timing analysis is presented in Fig.16.The power estimation for the designed architecture is done using the Xilinx power estimator tool (Xpower Estimator (XPE)-14.1). The power estimation report for the RCPWM design is generated and shown in Fig.17 and the temperature dependency of the On-Chip power also analyzed as illustrated in Fig.18.

The synthesized design of RCPWM and RPPPWM architectures are downloaded to the FPGA Spartan 6 device (XC6SLX45) with the help of device programming software "DIGILENT ADEPT". The configured FPGA device with proposed architecture is tested in the laboratory. The output line to line voltage and current are shown in Fig.19. The close similarity between simulation study and

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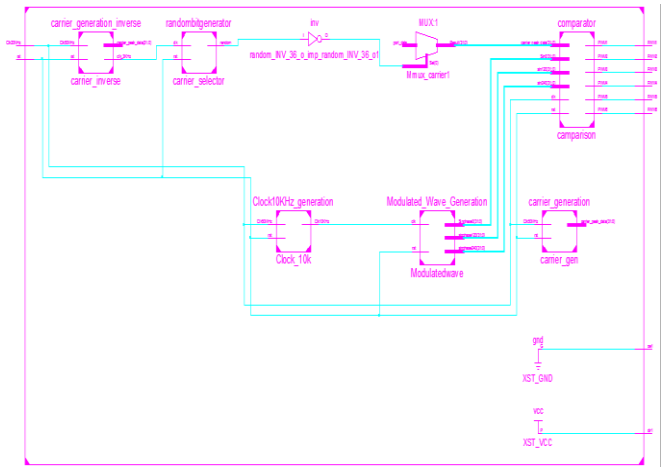


Fig. 13. RTL Diagram for RPWM 8-bit PRBS

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	325	30064	1%
Number of Slice LUTs	793	15032	5%
Number of fully used LUT-FF pairs	228	890	25%
Number of bonded IOBs	10	186	5%
Number of BUFG / BUFG CTRLs	5	16	31%
Number of DSP48A1s	3	38	7%

Fig. 14. Device utilization summary-RCPWM

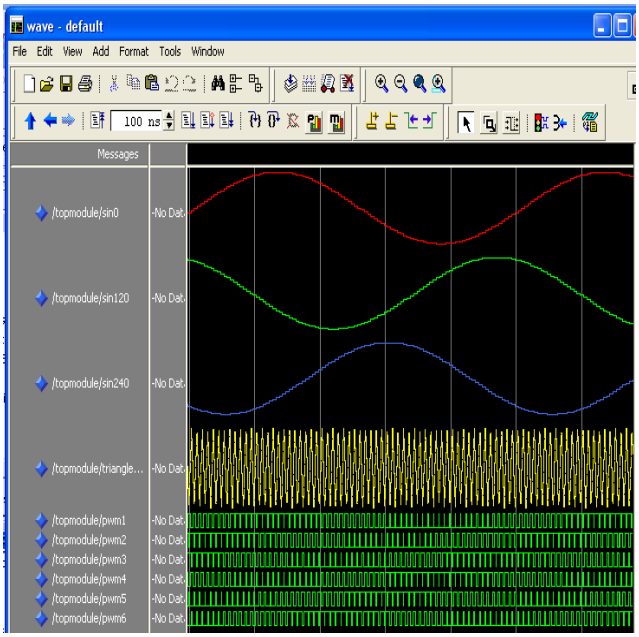


Fig. 15. Gating scheme output pulses in Modelsim window

laboratory implementation is evidenced in Fig.20 and Fig.21, which are simulation and hardware harmonic spectra. The typical gate pulses for M_a value of 0.8 is shown in Fig.22. Representative spectrum obtained in laboratory testing for RPPPWM is illustrated in Fig.23 for M_a=1.2.

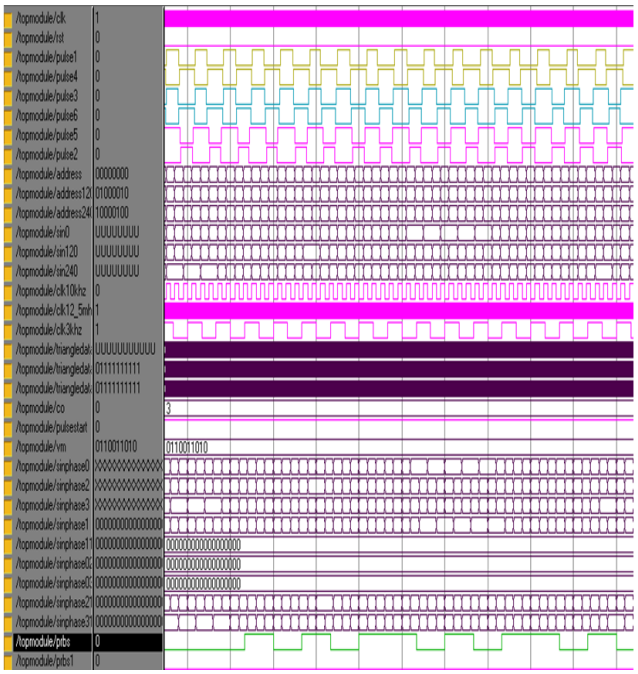


Fig. 16. Complete timing analysis

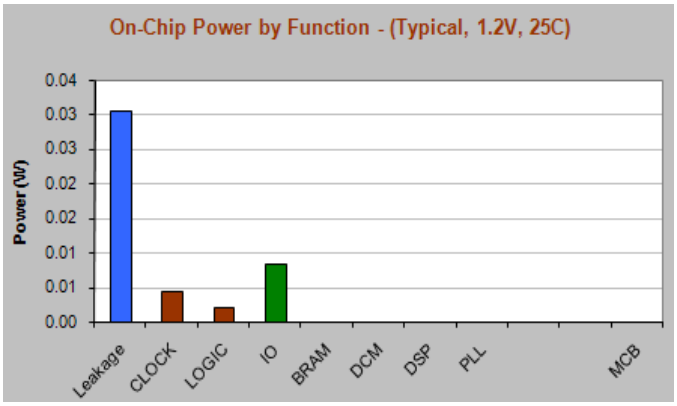


Fig. 17. Power estimation report

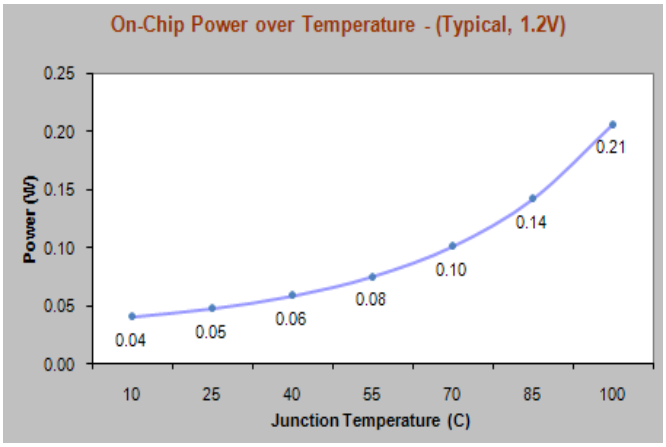


Fig. 18. Temperature dependency of power

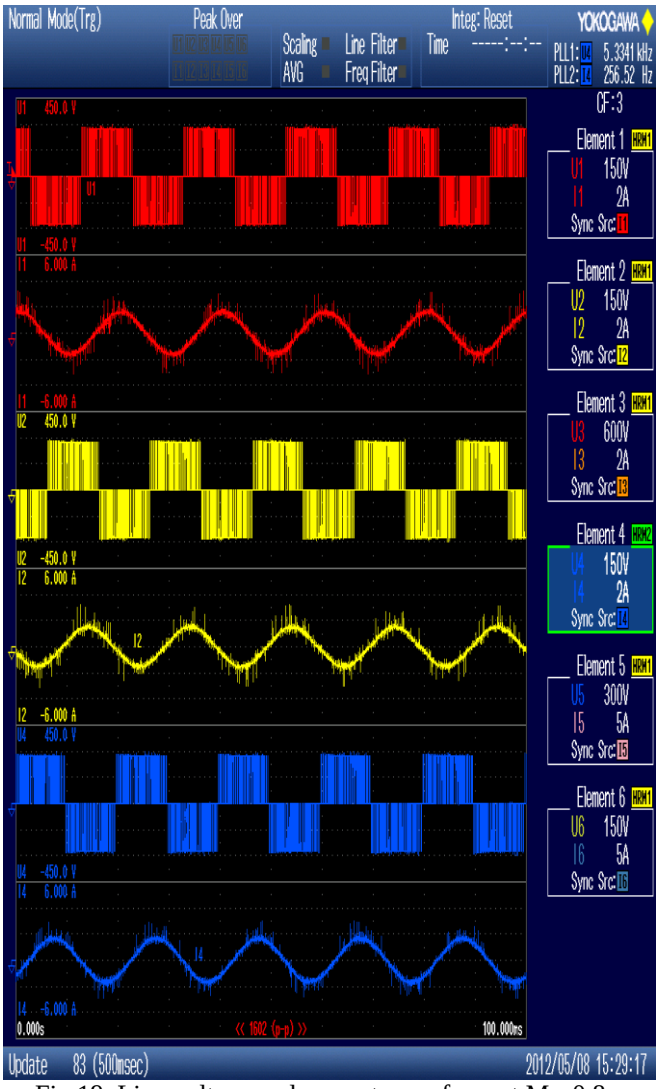


Fig.19. Line voltage and current waveform at M_a=0.8

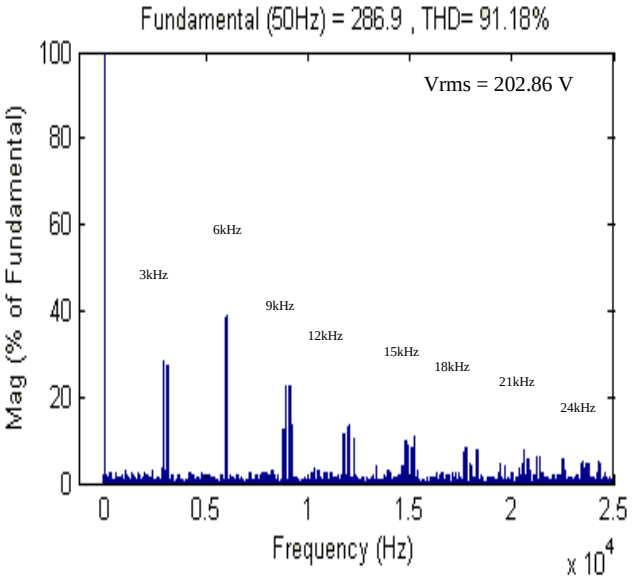


Fig. 20. MATLAB Simulation Results

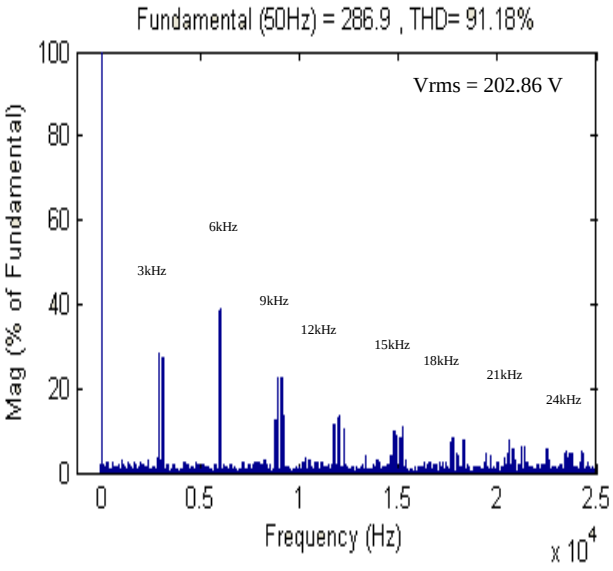


Fig.21 Hardware Results

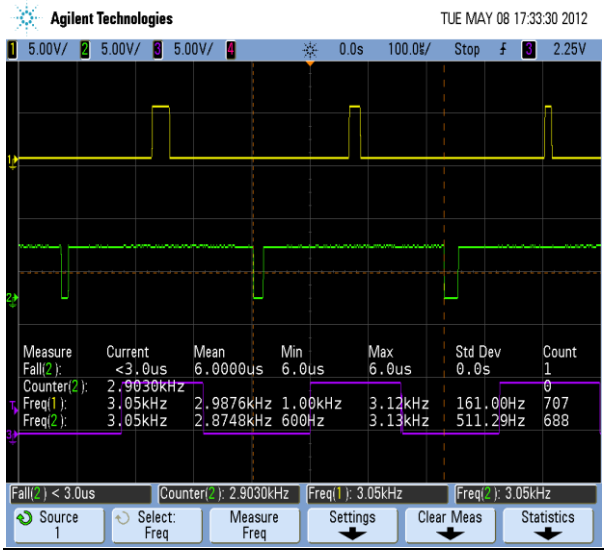


Fig.22**.** Gate pulses for Ma=0.8

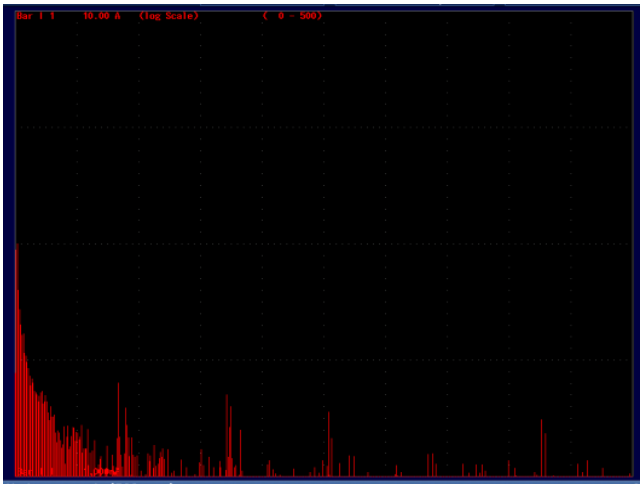


Fig.23. Representative Spectrum for Ma=1.2



Fig. 24. Experimental setup

5. CONCLUSION

Induction motors are mainly employed in industrial processes and become dominant adjustable speed drive (ASD). The performance of the induction drive depends largely on PWM techniques employed. Existing PWM strategies and research directions are aiming at improving the basic indices viz. fundamental component enhancement, THD minimization etc. They are employing constant frequency carrier and called as deterministic PWM strategies. Their main drawback is clustering of harmonic power in the output voltage harmonic spectrum and hence causing the acoustic noises in the drives. The non-deterministic methods (RPWM) can improve the harmonic spreading nature of the drive over the wide frequency range (i.e. reduced HSF). This paper develops two ways to assimilate the randomness in the PWM strategy viz. RCPWM and RPPWM. The developed methods along with the conventional SPWM are studied thoroughly for V_1, THD and HSF. Finally, all the above three methods are tested in the laboratory using a coded architecture in FPGA SPARTAN-6 XC6SLX45. The harmonic power spreading ability of the RPWM strategies along with the SPWM is validated in the hardware testing. The RCPWM and RPPWM offer marginal improvement in the output voltage, reduction THD and huge suppression of HSF than the SPWM for the entire working range.

Appendix

Power (P)……..0.75kW
Line- Line Voltage (VL)…….……..415 V
Frequency (f)……..…..50 Hz
Stator Resistance (Rs) ……..…435Ω
Stator Inductance (Ls) ……5839H
Rotor Resistance (Rr)……...1.395Ω
Rotor Inductance (Lr)……...0.005839H
Inertia (J)…….……....0.0131Kg.m^2
Friction factor……...0.0029N.m.s
Pole Pairs…….…2

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