Procedural design of a CMOS current conveyor

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**Abstract – This paper presents a new procedural design sequence for the design of a CMOS current conveyor. It is based on the structured design approach and consists in circuit partitioning, derivation of the specifications for each basic analog structure, and step-by-step design. BSIM2EKV converter is presented and EKV model is used for hand calculations. PAD (Procedural Analog Design) tool is used for validation. CCII step-by-step design is presented. Simulations (for verification and fine-tuning) using Mentor Graphics tools are presented.
Keywords: current conveyor, EKV model, PAD tool.**

I. INTRODUCTION

Research in ASIC go in the direction of low-voltage (LV), low-power (LP) designs. In this area, traditional voltage-mode techniques are going to be substituted by current-mode approach. Current-mode circuits overcome the gain-bandwidth product limitation, do not require high voltage gains and have good performance in term of speed, bandwidth and accuracy. The current-conveyor (CC) can be considered the basic circuit block. All the active devices can be made by connecting one or two CC [1].
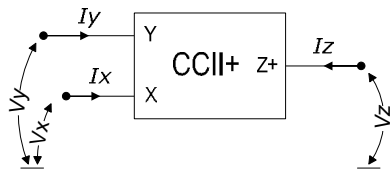

Fig.1. Second-generation current-conveyor symbol

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \Rightarrow \begin{cases} i_y = 0 \\ i_z = \pm i_x \\ v_x = v_y \end{cases} \quad (1)$$

Matrix (1) represents second-generation current conveyor (CCII) complete description.

The objective of this paper is to present a new and quick way to design current conveyors. The procedural design sequence for the design of a CCII (Fig.2.) is introduced.
Since the simulators are not design tools, the transistors sizes must be obtained by hand-calculation,

and only then confirmed by simulator. Therefore, a small number of model parameters with physical meaning and hierarchical model structure are important advantages. In this way, it became possible to approximate model equations, without a great loss of accuracy [2]. For hand calculations it is necessary to have a model suitable for transistor level design. The most suitable for this is EKV model developed at EPFL (Ecole Polytechnique Federale de Lausanne) [2]. EKV model facilitates the use of g_m/I_D based methodologies for sizing the transistors [3]. The transistor-level design approach presented in this paper is based on the choice of the inversion factor (IF) whose calculation requires the intrinsic EKV model parameters [4].
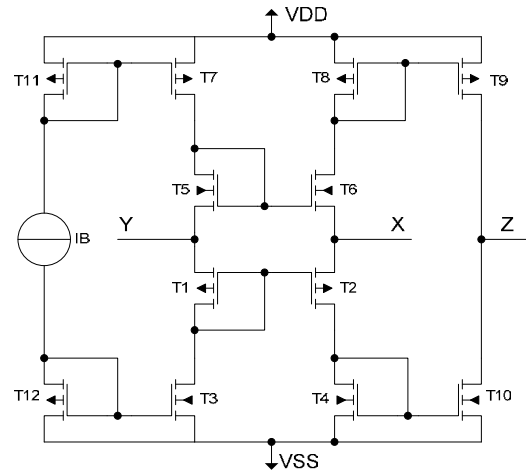

Fig.2. Bidirectional CCII topology

BSIM2EKV converter provides a way to obtain EKV model from industrial standard BSIM models. The author extracted EKV model parameters using BSIM2EKV based on HIT-KIT design kits from Austriamicrosystems foundry (design kits provided through Europractice). (HIT-KIT contains BSIM3 models for 0.35μm CMOS technology provided for Mentor Graphics tools).
PAD tool is a design environment dedicated to the design of analog circuits aiming to optimize design and quality by finding good tradeoffs. This interactive tool allows step-by-step design of analog cells by using guidelines for each analog topology.

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A CCII new step-by-step design approach is presented base on structured design. This paragraph will contained also derivation of the specifications for each basic analog block. In this way starting from current conveyor main specification we will obtain specifications for each component block and finally the low level CMOS structure. Based on the inversion factor and g_m/I_D methodology is presented an easier way to size the transistors that previous known [5].

Last section presents simulation results and comparison with hand calculations. It is used here only on step iteration hand-calculation/simulation and the results are very close. Design time is reduced considerably.

II. EKV MODELS

A. *EKV Models*

The EKV model has been developed at EPFL as a charge-based physical model. There are two versions 2.6 and 3.0. The first one is dedicated to the design of LV and LP analog circuits using submicron CMOS technologies. Version 3.0 is the most recent version and includes modeling effects for RF circuit design. Version 3.0 is validated for nanometer technologies down to 65nm [2]. EKV is a continuous and compact model showing a good accuracy, even though it has a small number of parameters. It respects the intrinsic source/drain symmetry, introduces the inversion factor as a transistor parameter, and shows the correct behavior in all inversion regions. There are only 22 parameters for EKV model instead of more then 400 in BSIM models [6]. BSIM model, even recognize to be the industrial standard has modeling problems and errors for some regions and operating points and is overcome by newest and modern models like SP2001 ansd EKV. To get good models BSIM uses a lot of binning parameters.

B. *EKV models extraction method*

Even EKV is known to be an accurate and more and more used model most of Ic foundries didn't provide EKV parameters for their processes. For an analog designer there is a simple way to obtain EKV parameters from BSIM models, using BSIM2EKV tools. Even not very accurate and needing some fittings, parameters extracted by BSIM2EKV can be used to design analog circuits based on g_m/I_D methodology.
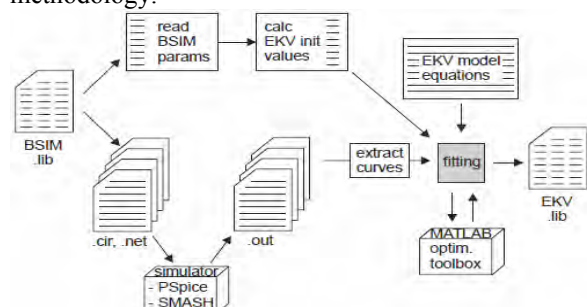

Fig.3. BSIM to EKV extraction concept

Author use a 0.35μm CMOS technology standard files (provided by Austriamicrosystems through Europractice) and a PSpice simulator to obtain some of the model parameter. Some other parameters are directly extracted from BSIM3v3 model files. Fig.3 presents the extraction concept.

III. PAD TOOL

PAD tool is a chart-based design CAD tool that allows step-by-step design of analog cells. The two main purposes of the PAD tool are to reduce expert analog designers' development time and help to hand on analog knowledge to system level designer.
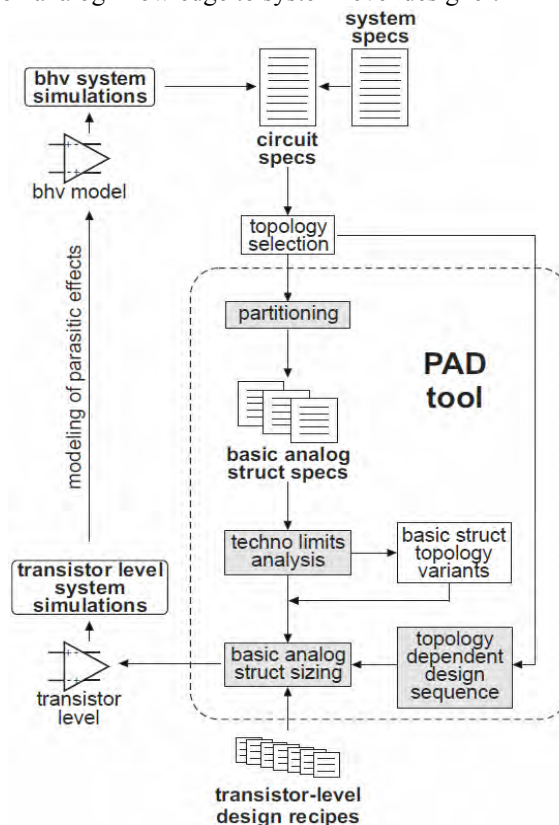

Fig.4. Analog design flow based on the structured design approach and the use of the PAD tool

The present version of PAD covers the procedural design of transconductance amplifiers (OTAs) and different operational amplifiers topologies but also permit to design nMOS/pMOS transistors individually, mirror structure and differential pair [2]. At each step, the user modifies interactively one subset of design parameters and observes the effect on other circuit parameters. At the end, an optimized design is ready for simulation (verification and fine-tuning). The analog basic structures calculator embedded in PAD uses the complete set of equations of the EKV MOS model, which links the equations for weak and strong inversion in a continuous way.

The advantage of using PAD and EKV models stands for very quick analog design over other methods (presented in [9] and [10]).
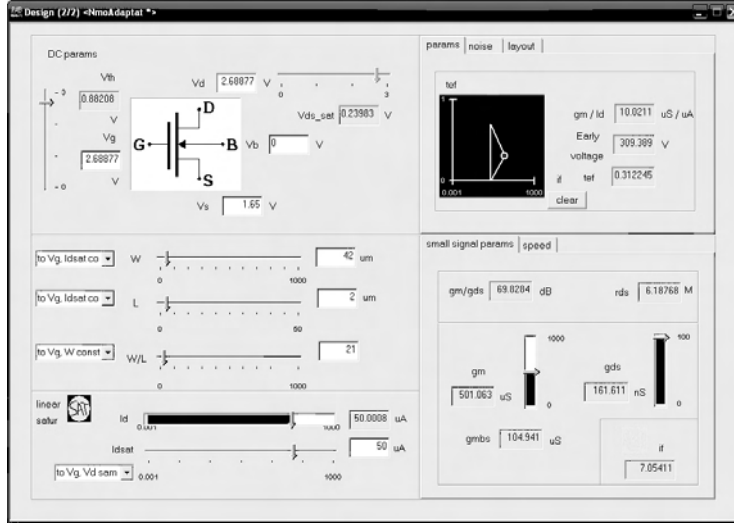
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Fig.5. PAD – nMOS transistor sizing

The short time of design comes from quick sizing of transistor based on requirements (no need to manipulate MOS equations) and from the small numbers of iteration hand-calculation/ simulation. Hand-calculations are very close with simulations.

III. PROCEDURAL DESIGN SCENARIO FOR A CURRENT-CONVEYOR

A new method for designing current conveyors is presented here. The basic concept consists in analog cell partitioning into the basic analog structures and sizing of these basic analog structures in a predefined procedural design sequence. The procedural design sequence implies few steps: circuit partitioning, derivation of the specifications, procedural design steps and local optimizations.
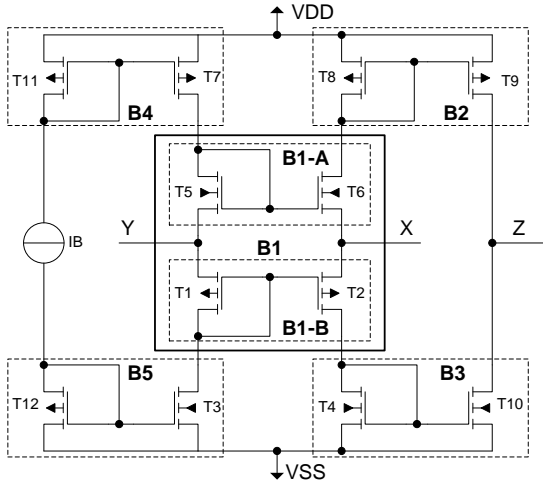

Fig.6. Current conveyor partitioned into basic analog structure

Fig.6 shows a partitioned CCII into basic analog structures – current mirrors. Blocks B2-B5 are simple current mirrors. B1 is a translinear loop formed by two quasi-current mirrors. B1-A and B1-B have the structure of current mirrors but in this circuit acts like complementary voltage follower. For operating point

(OP) CCII can be considered to be formed by 6 simple current mirrors.

The voltage input maxim range for Y port can be defined by:

$$V_{Y\,max} = VDD - V_{sat7} - V_{gs5} \qquad (2)$$

$$V_{Y\,min} = VSS + V_{sat3} + V_{gs1} \qquad (3)$$

The same equations can be derived for X voltage input:

$$V_{X\,max} = VDD - V_{sat6} - V_{gs8} \qquad (4)$$

$$V_{X\,min} = VSS + V_{sat2} + V_{gs4} \qquad (5)$$

With an X input current $i_X \neq 0$ the voltage range of the voltage follower is reduced because there must be room for the gate-source voltage of T6 or T2 within the supply voltage limits [11].

The linear input range of current on port X is determined by the operation of the translinear loop. So, writing the loop equations reveals:

$$I_{D2} = I_{D6} + i_X \qquad (6)$$

$$V_{gs5} + |V_{gs1}| = V_{gs6} + |V_{gs2}| \qquad (7)$$

Consider that all transistors operate under the saturation condition, equation (7) can be resolved in order to the currents I_{D2} and I_{D6}, resulting:

$$I_{D2,6} = kI_B\left(1 \mp \frac{i_X}{4kI_B}\right)^2 \qquad (8)$$

where I_B is the bias current and k is an aspect ratio between the dimensions of the transistors T5 (T1) and T6 (T2). This result is valid only for values of i_X between $-4kI_B$ and $+4kI_B$: these are the maximum values of the input current where the conveyor maintains a linear gain dependence on the input current [12].

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The current conveyor must fulfill matrix presented in (1) but a real conveyor will always have non 0 and non 1 coefficients. The real CCII matrix is presented in (9):

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1-\varepsilon_V & 0 & 0 \\ 0 & \pm(1-\varepsilon_i) & 0 \end{bmatrix}\begin{bmatrix} v_Y \\ i_X \\ v_Z \end{bmatrix} \Rightarrow \begin{cases} i_Y = 0 \\ i_Z = \pm i_X \\ v_X = v_Y \end{cases} \quad (9)$$

By analyzing the operation of the CCII in Fig.6 in the linear region for small signals, we get the approximate expressions for the errors in mirroring input currents (ε_i) and voltages (ε_v) [7]:

$$i_Z = i_X(1-\varepsilon_i) \quad (10)$$

$$\varepsilon_i \approx \frac{\left(1-\dfrac{g_{m10}}{g_{m4}}\right)g_{m2} + \left(1-\dfrac{g_{m9}}{g_{m8}}\right)g_{m6}}{g_{m2} + g_{m6}} \quad (11)$$

$$v_X = v_Y(1-\varepsilon_V) \quad (12)$$

$$\varepsilon_v \approx \frac{g_{ds2} + g_{ds6} + \dfrac{g_{m2}}{g_{m1}}g_{ds3} + \dfrac{g_{m6}}{g_{m5}}g_{ds7}}{g_{m2} + g_{m6}} \quad (13)$$

Other very important CC characteristics are the inputs and outputs resistances R_X, R_Y and R_Z [1]:

$$R_X \cong \frac{1}{g_{m2} + g_{m6}} \quad (14)$$

$$R_Y = \left(\frac{r_{o5}}{1+g_{m5}r_{o5}} + r_{o7}\right) || \left(\frac{r_{o1}}{1+g_{m1}r_{o1}} + r_{o3}\right) \quad (15)$$

$$R_Z = \frac{r_{o9} \cdot r_{o10}}{r_{o9} + r_{o10}} \quad (16)$$

From (2)-(5) extension of voltage input range on Y impose V_{sat} and V_{gs} very small. Equation (8) imposes IB based on maximum input current required by specifications. From (11), (13) and (14) g_{m2} and g_{m6} must be as big as possible. Equation (11) require $g_{m10}=g_{m4}$ and $g_{m9}=g_{m8}$. Output conductance for each transistor must be very small (11) (13) (15) (16).
Requirements for blocks:
B3 and B2:
- g_m for all transistors equal
- V_{gs} small for diode connected transistors
- g_{ds} small for all transistors
- small capacitance (output and input) for bandwidth
- very small current mismatch
B4 and B5:
- g_{ds} small for all transistors
- V_{sat} small for transistors
- very small current mismatch
B1-A and B1-B:
- g_m for all transistors very large
- V_{gs} small for diode connected transistors
- V_{sat} small for transistors

- small capacitance (output and input) for bandwidth

Each block can be design alone now. g_m/I_D methodology allow to choose the operation region of the transistor which best fit the requirements. V_{sat} small suggest to use *IF<10* (weak or moderate inversion). A big g_m requires also weak or moderate inversion: *IF<10*. On the other side a very good matching requires transistor working in strong inversion, *IF>10* and a good one in moderate inversion *1<IF<10*.
Most of the transistors in proposed CCII must have a small $g_{ds} \rightarrow$ channel length L must be large. A large L reduces the operating frequency by increasing the capacitance. For an *L* between L_{min} and *10*L_{min}* the frequency is not drastically affected. For analog circuits always is recommended to use *L>5*L_{min}*.

V. SIMULATIONS AND RESULTS

Biasing current is *IB*=50µA and based on (8) allow a ±200µA input current range on X port.
Using the considerations presented in paragraph III we choose for our CCII all transistors working in moderate inversion *IF=7* and *L=2µ*.
Based on *IB*, *L* and *IF* we got *W*, g_m, V_{sat} and V_{gs} for transistors using PAD.
Same results can be obtained using equations:

$$V_{sat} = V_t \cdot (2\sqrt{IF} + 4) \quad (17)$$

$$\frac{g_m}{I_{Dsat}} = \frac{1}{nV_t} \cdot \frac{1}{\dfrac{1}{2} + \sqrt{IF + \dfrac{1}{4}}} \quad (18)$$

$$g_{ds} = \frac{I_d}{V_A} \quad (19)$$

where V_t - thermal voltage, n – slope factor (1.25 for this technology), V_A – Early voltage.
PAD is not a simulator but a calculator. Unfortunately PAD has a problem with estimating the g_{ds} of the transistor.
From (19) results that we need V_A to obtain g_{ds}. At present no simple reasonably accurate hand prediction for Early voltage is available because of the complexities associated with dependencies on *IF, L*, and V_{ds} [8]. The prediction of V_A is further complicated by the possibility of DIBL and hot-electron components in addition to the always present channel length modulation component. For these reasons, MOS drain–source conductance g_{ds}, represented here using V_A, is the most difficult of the small-signal parameters to predict, having a long history of modeling errors, well known to experienced designers.
Instead, a set of measured values from simulations will be presented for the 0.35CMOS AMS process available. These measurements will then be displayed as values of V_A as a function of channel length *L* and V_{ds} over inversion factor *IF*.
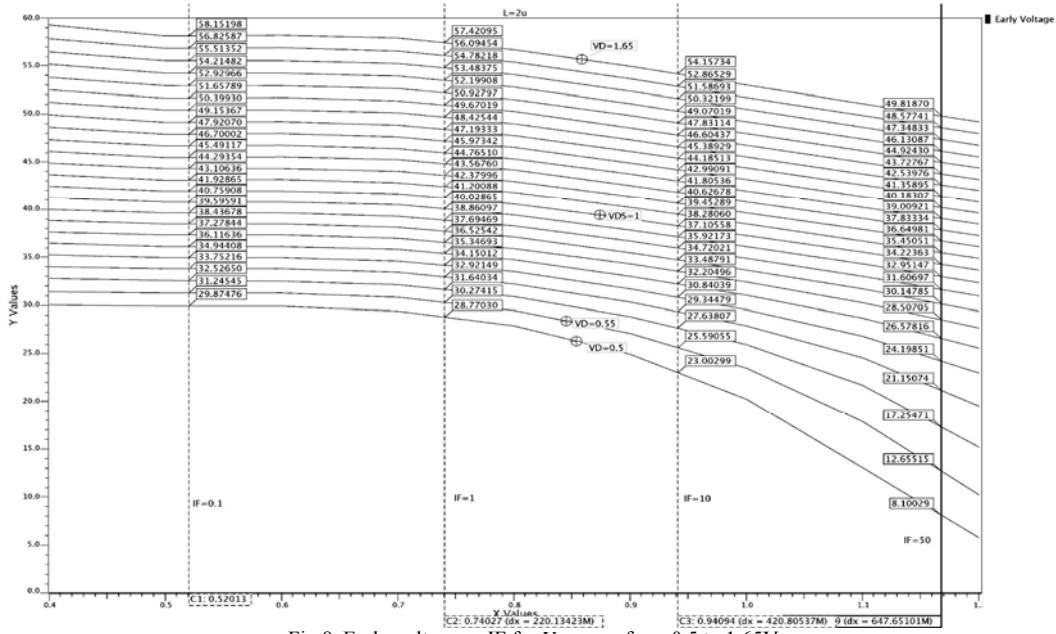
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Fig.8. Early voltage vs IF for V_{ds} range from 0.5 to 1.65V

The measurement methodology considers multiple, fixed values of V_{ds} that correspond more closely to the required design choices. This measurement methodology permit the designer to estimate V_A near the level of inversion, channel length, and V_{ds} actually used. Fig.8 shows the measurement results of the V_A for a pMOS transistor with $L=2\mu$ and V_{ds} from 0.5 to 1.65V with a step of 0.05V. Similar measurements were extracted for another value of L and also for nMOS. These operations consume some time but must be done only once – for the first time working with a new technology process.

From charts like in Fig.8 it is possible to estimate g_{ds} for each transistor in CCII, for chosen L and IF and for V_{ds} in circuit.

Table 1. Aspect ratios of transistors

Transistors	W [μ]	L [μ]
nMOS M1, M3, M6, M8, M10, M12	40	2
pMOS M2, M4, M5, M7, M9, M11	148	2

After simulations results that hand-calculations errors are small, less than 10%. For some conditions is possible to get hand calculation error even 20%. Errors are small comparing with other hand-calculation methodology. The biggest advantage is the reduced time required for design.
The simulation was performed using Mentor Graphics simulator – Eldo.
Fig. 9 presents the voltages transfer from Y port to X port. A very good voltage-following action can be observed over the wide voltage range: -630mV to 630mV with an error less than 1%.
Fig. 10 presents the voltage bandwidth between Y and X. The bandwidth is 78MHz with a load $R_{Xload}=50k\Omega$ and $C_{Xload}=1pF$.
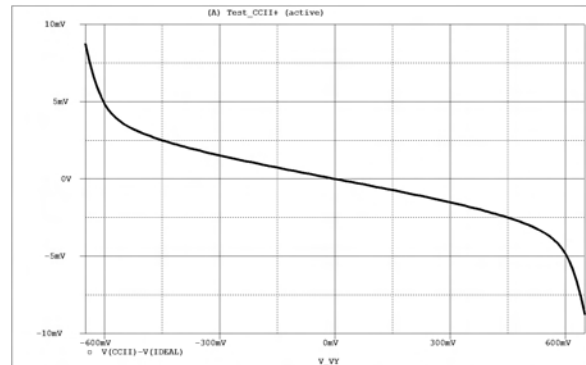

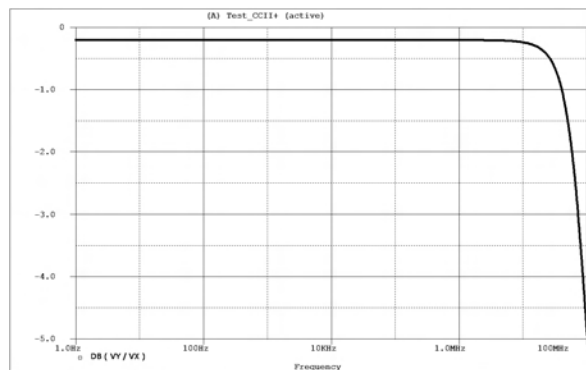Fig.9. The voltage input-output characteristic between ports Y and X

Fig.10 Frequency response of voltage gain between Y and X

Voltage transient analysis with a 100mV peak input voltage is presented in Fig. 11. Because of internal, parasitic series resistor R_X the output voltage is reduced. R_{Xload} and R_X represent a voltage divider.
Current transfer between port X and port Z ($R_{Zload}=10k\Omega$ and $C_{Zload}=1pF$) is excellent: current input range -190μA to 170μA with less than 1% error. Current range is in good accordance with theoretical one from relation (8). Frequency response in current from port X to Z is presented in Fig. 12.
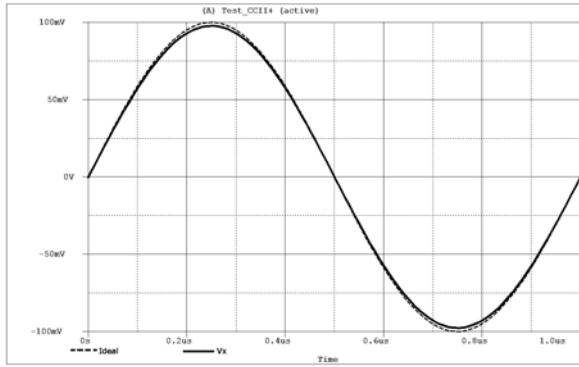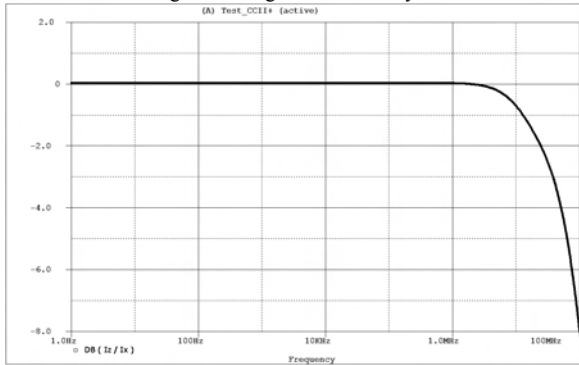
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Fig.11. Voltage transient analysis

Fig.12. Frequency response of current gain
between X and Z port

Other important features of the CCII are inputs and output impedance. Fig.13 presents simulated impedances for Y and Z ports. All of them have resistive component at low frequencies and capacitive component at high frequencies. Z_X presents also a small inductive component. The values of resistance and capacitance are presented in Table 2.
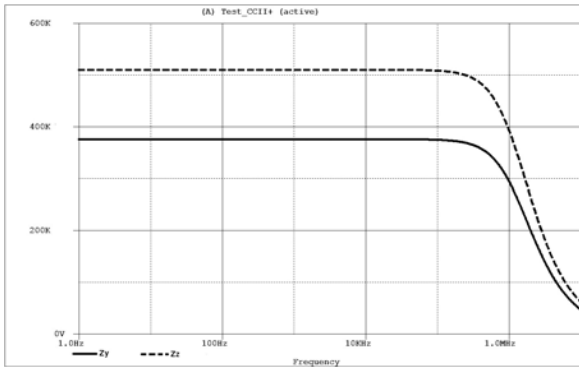

Fig.15. Impedance Z_Y and Z_Z against frequency

Table 2. CCII performance

Technology	0.35μ CMOS AMS
Supply voltage	±1.65V
Bias current	50μA
Current gain (1-ε_i)	0.975
Voltage gain (1- ε_v)	0.977
Current bandwidth	37.8MHz
Voltage Bandwidth	78.6MHz
Input impedance $R_Y//C_Y$	376kΩ ‖ 335fF
Output impedance $R_Z//C_Z$	510kΩ ‖ 259fF
Input resistance R_X	905Ω
Voltage input range	-630mv – +630mv
Current input range	-190 μA - +170 μA

VI. CONCLUSION

The paper presents a new approach to design CCIIs. The structured analog design procedure is applied to current conveyor. The circuit is partitioned in basic analog blocks – simple current mirrors and each transistor in block is size using g_m/I_D methodology. For speeding up the design time a calculator is used – PAD. Analog design requires always the output conductance g_{ds} of the transistor, but there is no simple and accurate hand prediction for g_{ds}. The solution is extracting the Early voltage V_A from simulations and saving like a chart as a function of channel length L and V_{ds} over inversion factor IF.
There is a good agreement between simulations and hand calculations. The design CCII has good performance in term of bandwidth, current and voltage gain and input range (see Table 2).

ACKNOWLEDGMENTS

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