Buletinul Ştiinţific al Universităţii "Politehnica" din Timişoara

Seria ELECTRONICĂ şi TELECOMUNICAŢII
TRANSACTIONS on ELECTRONICS and COMMUNICATIONS

Tom 54(68), Fascicola 2, 2009

Current-Mode Double-Simulation Sine Oscillator

Beniamin Dragoi[1], Mircea Ciugudean

Abstract – Researches on the conception and theory of an original high frequency stability and harmonic purity sine oscillator are presented. It is based on a resonant parallel circuit L‖C, whose components are simulated by the help of first-generation current conveyers (CCI). Negative impedance converter (NIC) and negative admittance/impedance converter (NAIC) are presented. Simulation results based on ideal CCIs are shown.
Keywords: current conveyor, NIC, NAIC, oscillator.

I. INTRODUCTION

Sinusoidal oscillators play an important role in instrumentation, communication and signal processing applications. A quadrature oscillator is used in some applications because provides two sinusoids with 90° phase difference. Voltage-mode operational amplifier based circuits have been shown to be very well suited for generation of sinusoidal waveforms. The simplicity in the design approach turns into a disadvantage when it is desired to generate high frequencies because the dynamic range of operation is dictated by the frequency-dependent gain of the operational amplifiers (op-amp). Current conveyors (CC) are unity gain active elements exhibiting higher linearity, wider dynamic range, better frequency performance and lower power consumption compared to their voltage mode counterparts, op-amp [1]. Few types of CC exist covering first, second and third generation CC but first generation CC (CCI) is well known for its simplicity [2].

It is known a double-simulation sine oscillator based on a resonant parallel circuit $L_{eq}\|C_{eq}$, whose components are simulated by the help of operational amplifiers [3], [4]. This oscillator has been named "the electronic quartz" because of their very high frequency stability. Using a similar principle, it is proposed here current conveyors based circuits as NIC (negative impedance converter) and NAIC (negative admittance/impedance converter) which, with ideal conditions, simulate (on one input) an equivalent inductance L_{eq} and respectively, an equivalent capacity C_{eq}. These circuits are based on first-generation CMOS current conveyers CCI+ and respectively, CCI- [5][6].

II. SIMULATION OF L AND C COMPONENTS

NIC and NAIC are implemented using first generation current conveyers (CCI) whose main characteristics are presented in definition matrix (1), input-output equations (2) and nodes impedance level (Table 1)[7].

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \cdot \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (1)$$

$$\begin{cases} I_Y = \pm I_z = I_x \\ V_x = V_Y \end{cases} \quad (2)$$

Table 1 CCI impedance levels

Node (CCI)	Impedance Level
X	0
Y	0
Z	∞

A NIC can be implemented using a CCI+, as shown in Fig.1.

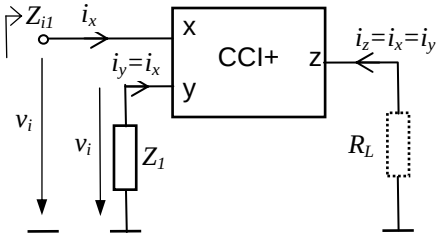

Fig.1. NIC using CCI+

Here: $$Z_{i1} = \frac{v_i}{i_x} = \frac{v_i}{i_y} = -Z_1 \quad (3)$$

and using an ideal capacitor C_1 as impedance Z_1 one obtains the NIC input impedance:

$$Z_{i1} = -\frac{1}{j\omega C_1} = j\omega \frac{1}{\omega^2 C_1} = j\omega L_{eq} \quad (4)$$

[1] Facultatea de Electronică şi Telecomunicaţii, Departamentul Electronica Aplicată, Bd. V. Pârvan Nr. 2, 300223 Timişoara, e-mail beniamin.dragoi@etc.upt.ro

with $$L_{eq} = \frac{1}{\omega^2 C_1} \quad (5)$$

By the help of a CCI- one may design a NAIC (Fig.2).

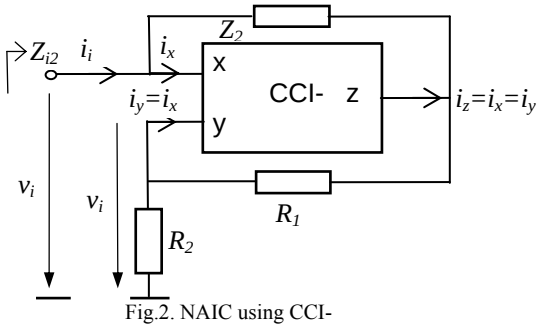

Fig.2. NAIC using CCI-

The input impedance is:

$$Z_{i2} = \frac{v_i}{i_i} = -\frac{1}{Z_2} R_1 R_2 = -Y_2 R_1 R_2 \quad (6)$$

If an ideal capacitor C_2 is used as the Z_2 impedance, then the input impedance of the NAIC will be:

$$Z_{i2} = -j\omega C_2 R_1 R_2 = \frac{\omega^2 C_2 R_1 R_2}{j\omega} \frac{1}{j\omega C_{eq}} \quad (7)$$

$$C_{eq} = \frac{1}{\omega^2 C_2 R_1 R_2} \quad (8)$$

III. DOUBLE-SIMULATION OSCILLATOR

To achieve a sine oscillator scheme, the NIC and the NAIC must be connected as shown in proposed oscillator in Fig.3.

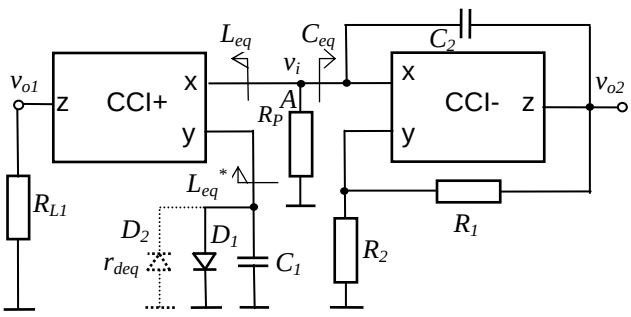

Fig.3. Current-mode double-simulation oscillator

The R_P resistor has the purpose of compensation of the negative resistance appearing to the NIC input because of the limiting diode(s) equivalent resistance r_{deq}, as the oscillation condition claims (see lather).

Using equal capacities C_1=C_2=C and resistances R_1=R_2=R the characteristic oscillator equation is obtained by an open-loop technique (Fig.4) as follows.

In Fig.4 were noted

$$Z_1 = r_{deq} \| \frac{1}{j\omega C} \qquad Z_2 = \frac{1}{j\omega C} \quad (9)$$

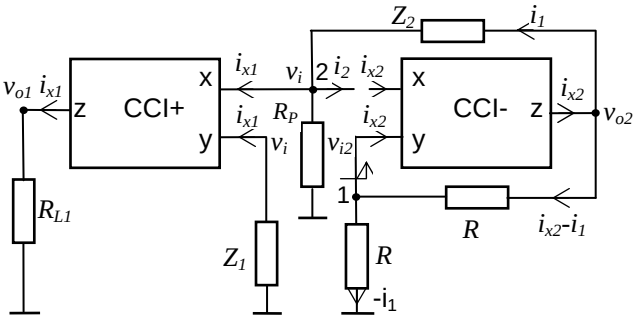

Fig.4. Oscillator open-loop

Noting i_1 - current through Z_2 impedance and the i_2 - open-loop output current, one writes the current sum in node 2

$$i_1 = i_2 + i_{x1} + \frac{v_i}{R_P} \quad (10)$$

Because $v_i = -i_{x1} Z_1$ this equation becomes

$$i_1 = i_2 + i_{x1} - i_{x1} \frac{Z_1}{R_P} \quad (11)$$

and

$$i_2 = i_1 - i_{x1}\left(1 - \frac{Z_1}{R_P}\right) \quad (12)$$

Heaving $v_i = -i_1 R = i_{x1} Z_1$ the i_1 current becomes

$$i_1 = i_{x1} \frac{Z_1}{R} \quad (13)$$

Now the (12) equation may be written

$$i_2 = i_{x1} \frac{Z_1}{R} - i_{x1}\left(1 - \frac{Z_1}{R_P}\right) = i_{x1}\left(\frac{Z_1}{R} + \frac{Z_1}{R_P} - 1\right) \quad (14)$$

The potential difference between nodes 1 and 2 is

$$v_{i2} - v_i = -(i_{x2} - i_1)R + i_1 Z_2 \quad (15)$$

and using the above formula of i_1 (13), we have

$$v_{i2} - v_i = -\left(i_{x2} - i_{x1} \frac{Z_1}{R}\right)R + i_{x1} \frac{Z_1}{R} Z_2 \quad (16)$$

$$i_{x2} R = v_i - v_{i2} + i_{x1} Z_1 + i_{x1} \frac{Z_1}{R} Z_2 \quad (17)$$

$$i_{x2} = (v_i - v_{i2}) \frac{1}{R} + i_{x1} \frac{Z_1}{R^2}(R + Z_2) \quad (18)$$

In order to the circuit oscillates when the loop closes it is necessary to have $i_2 = i_{x2}$ and $v_{i2} = v_i$, thus, from the (14) and (18) equations one obtains:

$$i_{x1}\left(\frac{Z_1}{R}+\frac{Z_1}{R_P}-1\right)=i_{x1}\frac{Z_1}{R^2}\left(R+Z_2\right) \qquad (19)$$

then, after simplification,

$$\left(\frac{Z_1}{R}+\frac{Z_1}{R_P}-1\right)=\frac{Z_1}{R^2}\left(R+Z_2\right) \qquad (20)$$

This will give the characteristic equation

$$Z_1Z_2-\frac{R^2}{R_P}Z_1+R^2=0 \qquad (21)$$

Replacing Z_1 Z_2 from (9) the characteristic equation becomes:

$$(j\omega)^2R^2C^2r_{deq}R_P+j\omega CR^2\left(R_P-r_{deq}\right)+R_Pr_{deq}=0 \qquad (22)$$

From the characteristic equation we can drive the phase oscillation condition:

$$r_{deq}=R_P \qquad (23)$$

and the amplitude oscillation condition, which conducts to frequency relation:

$$\omega_o=\frac{1}{RC} \quad \text{or} \quad f_o=\frac{1}{2\pi RC} \qquad (24)$$

Quality factor is:

$$Q=\frac{1}{R}\frac{r_{deq}R_P}{R_P-r_{deq}} \qquad (25)$$

Another way to determinate oscillation frequency is by replacing L_{eq} (5) and C_{eq} (8) in well known LC oscillators' frequency relation:

$$f_o=\frac{1}{2\pi\sqrt{L_{eq}C_{eq}}} \qquad (26)$$

Thus

$$f_o=\frac{1}{2\pi\sqrt{R_1R_2C_1C_2}} \qquad (27)$$

The (23) condition is automatically maintained thanks to the adaptive r_{deq} value [4]. This condition represents also the reciprocal compensation of the negative resistance (reflected from r_{deq}) and the positive one on the NIC x input.

D_1 and/or D_2 diodes achieve the voltage-amplitude self-regulation [4] for the input voltage v_i and so, for the output voltages v_{o1} and v_{o2} to. This is the easiest way to obtain amplitude limitation and regulation. The using of two diodes D_1 and D_2 instead only one, can decreases THD because of the symmetrical amplitude regulation. Paper [4] and work [8] show that limiting diode(s) equivalent resistance r_{deq} is:

$$r_{deq}\approx kQ^*r_{dp} \qquad (28)$$

$$\text{with} \quad k\approx\begin{cases}2.2 & use \quad D_1\\ 0.5 & use \quad D_1\ \&\ D_2\end{cases} \qquad (29)$$

Here r_{dp} is the "peak" dynamic diode resistance and is defined like the I_D/V_D characteristic slope for operating point P set by $v_{dm}=v_{im}$ (Fig.5). Q^* is the quality factor for the second resonant circuit based on $C_1||L_{eq}^*$ seen by diode(s) (not including diode) in Fig.3, where L_{eq}^* is another simulated inductance appearing on the CCI+ y input.

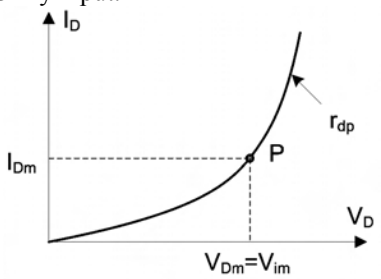

Fig.5. Diode „peak" dynamic resistance - r_{dp} - definition

This diode equivalent resistance r_{deq} has a high value thanks to a high quality factor Q^*. During normal operation moving of the P point on the I_D/V_D characteristic, changes r_{deq} and consequently total resistance in node A. If v_i amplitude increases (because $|r_{deq}|>R_P$) → P point go to the right → r_{deq} decreases until $|r_{deq}|=R_P$. If v_i amplitude decreases ($|r_{deq}|<R_P$) → P point go to the left → r_{deq} increases until $|r_{deq}|=R_P$. Always, diode(s) maintains the ideal condition $|r_{deq}|=R_P$. Thus, the quality factor of the resonant $L_{eq}\|C_{eq}$ has a value Q →∞. The oscillator frequency stability is drove then towards the RC product stability. So, using components with opposite-sign and comparable value thermal coefficients, or using a thermal compensation, one can achieve a high frequency stability with temperature variation.

By the same reason, the output voltage THD may attain a very small value. These performances may be improved by thermo-stabilizing the chip.

To obtain the phase diagram of v_i, v_{o1}, and v_{o2} voltages, it must observe that, admitting the hypothesis

$$r_{deq}>>X_C \qquad (30)$$

it can write at the y input of CCI+

$$v_i=-i_{x1}\frac{1}{j\omega_oC}=-i_{x1}\frac{R}{j}=j\cdot i_{x1}R \qquad (31)$$

$$v_{o2}=\left(i_{x2}-i_1\right)R+v_i=\left(i_{x2}-i_{x1}-i_{x2}\right)R+v_i=\\ =-i_{x1}R+v_i \qquad (32)$$

If consider the v_i phaser on the real axis then the current have a phase difference of 90° behind v_i (Fig.6). As the relation (31) shows, it can see that

$$|v_i| = |i_{x1}R| \tag{33}$$

thus, the phaser v_{o2} (32) is the sum of two equal-amplitude vectors (Fig.6) and has a phase difference of 45° before v_i .

The output voltage $v_{o1} = -i_{x1}R_{L1}$ is a collinear phaser with $-i_{x1}$ and has a phase difference of 90° before v_i.

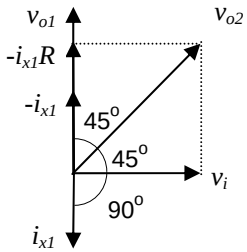

Fig.6. Oscillator phase diagram

Using the v_{o1} and v_i as output voltages the circuit becomes a quadrature oscillator. The amplitude of v_{o1} is established independently by the R_{L1} resistor value.

IV. SIMULATION RESULTS

Proposed NIC and NAIC based on ideal CCI+ and CCI- depicted in Fig.1 and Fig.2 was simulated using PSpice program. NIC using C_1=10pF simulation result is presented in Fig.7. It can be observed NIC inductive character over very wide frequency range: NIC show a 90° phase between its input voltage and current. NIC's equivalent inductance is in inverse ratio to frequency.

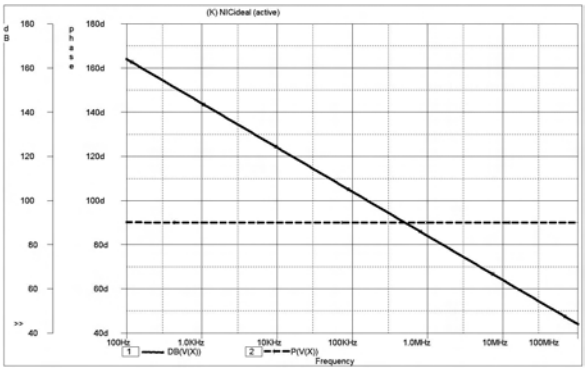

Fig.7. NIC using ideal CCI+ simulation

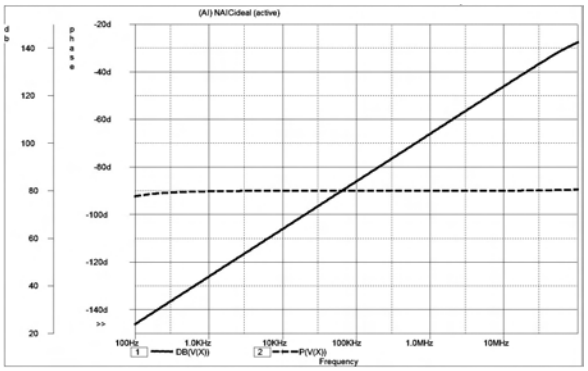

Fig.8. NAIC using ideal CCI- simulation

NAIC simulation using C_2=10pF and R_1=R_2=50kΩ is presented in Fig.8. This circuit shows a capacitive character: -90° phase between its input voltage and current. Circuit presents low phase distortions at low (under 1 kHz) and high frequency (over 50MHz). NAIC's equivalent capacitance is in inverse ratio to frequency.

Simulation of the proposed oscillator without amplitude regulation and using ideal passive componets is presented in Fig.9. In Fig.3 D_1 is replaced by a resistor R_D=R_P thus obtaining $Q\rightarrow\infty$. R_1=R_2=100kΩ, C_1=C_2=50pF, oscillation frequency is 31.847 kHz. It can be observed that circuit is a quadrature oscillator. Measured phases between v_i-v_{o2}, and v_{o1}-v_{o2} are 45° and 90° for v_i-v_{o1}.

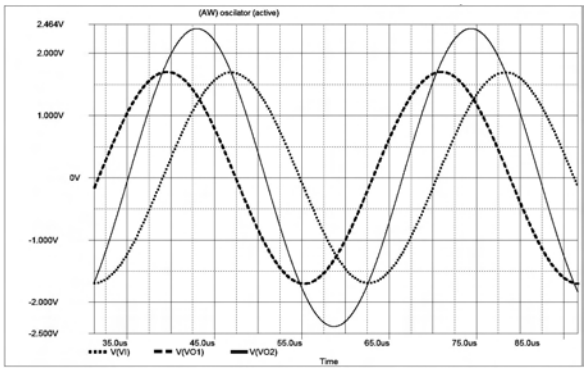

Fig.9. Oscillator with diode(s) replaced by a resistor R_D=R_P

Fig.10 presents AC simulation for oscillator without amplitude regulation. Frequency response for v_i shows $Q\rightarrow\infty$. It is impossible to measure Q=∞ but increasing simulation number of points v_i peak go up-and-up thus Q increase. Simulation presented in Fig.10 give a Q=7e+5.

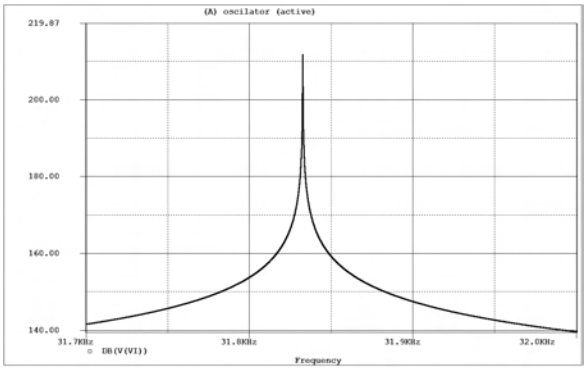

Fig.10. Oscillator with diode(s) replaced by a resistor R_D=R_P – AC simulation

Simulation of the oscillator with amplitude regulation (Fig.3) and real passive components (from 0.35µm CMOS process technology) is presented in Fig.11. D_1 and D_2 provide equivalent resistance r_{deq} and maintains the ideal condition $|r_{deq}|$=R_P for a large variation of R_P. Fig.11 shows simulation result for, C_1=C_2=10pF, R_P=3,5MΩ, R_1=R_2=100kΩ. D_1 and D_2 are diodes with W=L=20µm. C_1 and C_2 are poly1-poly2 capacitor; R_1 is poly1 resistor and R_2 is poly 2

resistor; R_P is N+ high resistance poly1 resistor. Simulated frequency is f_0= 169.026 kHz a little bit different from mathematic frequency (159.154 kHz) because of resistors parasitic capacitors.

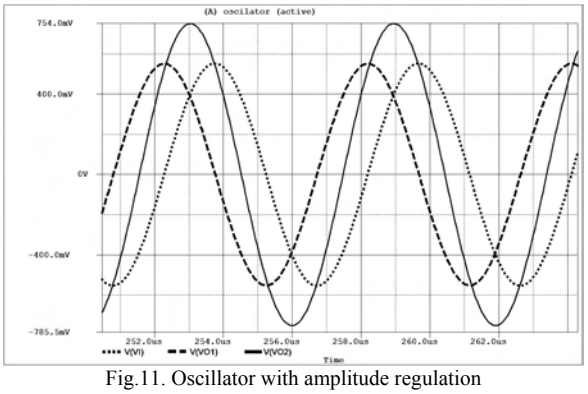

Fig.11. Oscillator with amplitude regulation

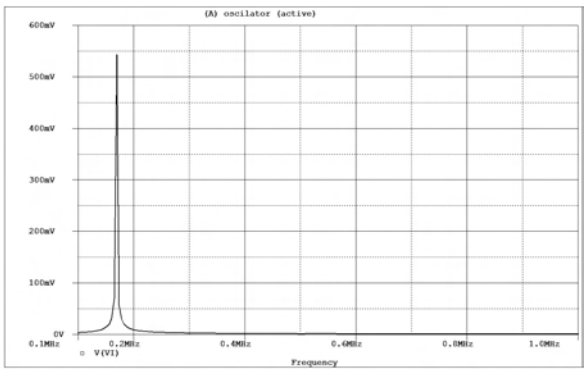

Fig.12. Frequency spectrum of the waveform in Fig.11

Fig.12 shows the frequency spectrum giving total harmonic distortion (THD) less than 0.1%.

In Fig.13 is presented frequency variation with R_2 for C_1=C_2=10pF, R_P=2.5MΩ, R_1=100kΩ. R_2 vary from 30kΩ to 300kΩ. It has been choose R_2 to be varied because it is a grounded resistor. A setting mechanism for a resistor value it is easier to be implemented if resistor is grounded. Also, is possible to use an external frequency setting resistor R_2 using only on chip pad. Higher frequency can be obtained using smaller C_1=C_2=C. Values less than 10pF are suited for IC integration.

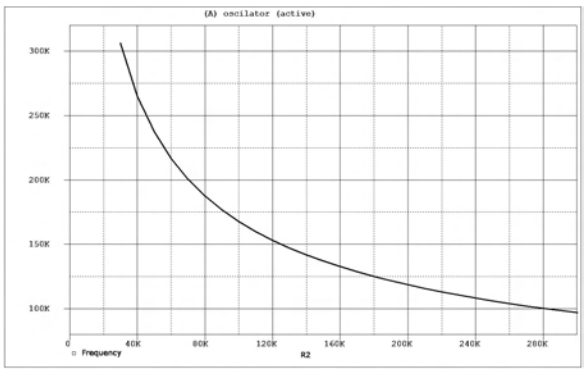

Fig.13. Variation of frequency with R_2

Fig. 14 shows frequency variation with temperature. C_1=C_2=10pF, R_P=3500kΩ, R_1=R_2=100kΩ. All components are integrated components from a 0.35μm CMOS technology. There is a maximum frequency changing of 1.1 kHz over 140° Celsius temperature range. This is about 10Hz/°C maximum, so, the maximum frequency shift is $\Delta f/(f_0\Delta T)=6.2\cdot10^{-5}$/°C

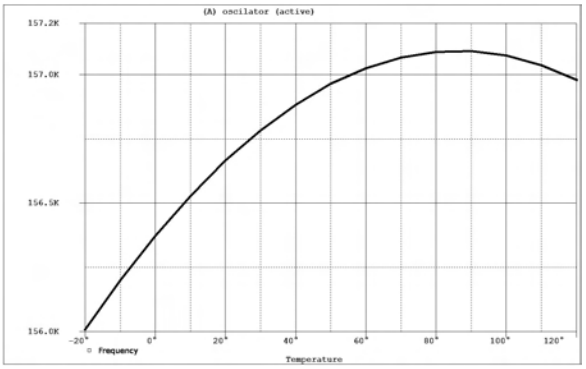

Fig.14. Variation of frequency with temperature

IV. CONCLUSION

Researches on the conception and the theory of a new high frequency stability and harmonic purity sine oscillator were presented. The oscillator is built on a resonant parallel circuit $L_{eq}\|C_{eq}$, whose components are simulated by the help of first-generation current conveyers CCI+ and CCI-.

The oscillator includes a diode amplitude regulation element, which automatically maintains the oscillation condition Q→∞. Because of this high-value quality factor the oscillator performances in frequency stability and harmonic purity are very good.

The authors aim to achieve based on this oscillator and using temperature stabilization, quartz less current-mode CMOS frequency reference. Future work will use real CCI based on CMOS transistors.

REFERENCES

[1] Yan Hui Xi, Qiao Liu, Hong Li, "Design of Multiphase Sinusoidal Oscillator based on CCCII", *Proceedings of the 6th World Congress on Inteligent Control and Automation,* 2006, Dalian, China, Vol. 1, pp: 4960 – 4962.

[2] Dragoi Beniamin, Ciugudean M.,"First Generation Selfbiased Bidirectional CMOS Current Conveyor", *Sesiunea naţională de comunicări ştiinţifice DrETC 2007*, ISBN 978-973-625-494-9, pp. 78-82.

[3] M. Ciugudean, "A Sine Oscillator with Simulated LC" *Electronic Engineering*, February 1993, pp.34-36.

[4] M. Ciugudean, Ph. Marchegay, "Double Simulation New Quadrature Sine Oscillator - the "Electronic Quartz", *Buletinul Ştiinţific al Universităţii "Politehnica" din Timişoara, Transactions on Electronics and Communications*, Tom 49(63), Fascicola 2, 2004, pp.142-146.

[5] M. T. Abuelma'atti, "New current-mode-active filters employing current conveyors", *International Journal of circuit theory and Applications*, Vol.21, No.1,1993, pp.93-99.

[6] M. T. Abuelma'atti, A.A.Al-Ghumaiz, "Novel CCI- based single-element-controlled oscillators employing grounded resistors and capacitors", *IEEE Trans. On Circuits and systems – 1*, Vol.43, Febr.1996, pp. 153-155.

[13] Ferri G., Guerrini N.C.,"Low-Voltage Low-Power CMOS Current Conveyors", Kluwer Academic Publishers, Dordrecht, 2003, ISBN 1402074867.

[8] M. Ciugudean, V. Tiponut, M. Tanase, I. Bogdanov, H. Cârstea, A. Filip, "Circuite integrate liniare. Aplicaţii" *Editura Facla*, Timişoara, 1991.