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Negative Impedance Converter Circuits for Integrated Clock Transmission Lines Loss Compensation

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Abstract – The present article presents a Negative Impedance Converter (NIC) circuit that can be used for loss compensation of lossy transmission lines integrated with standard deep submicron CMOS processes. The use of standard CMOS processes places several constraints on the required performances of the NIC circuit such as the use of low supply voltages coupled with high signal swings (which limits the number of stacked transistors in circuit branches) or the appreciable working frequency (from about 1GHz to several GHz for clock signals in modern standard CMOS technologies).

Keywords: Negative impedance converter, NIC, transmission lines loss compensation

1. INTRODUCTION

In modern CMOS VLSI circuits or SoCs (Systems on Chip) having large digital domains, the operating clock frequencies have reached and crossed the GHz limit while the silicon area taken by such systems continues steadily to grow. For these integrated devices the main design concerns are starting to shift from digital circuit synthesis (achievable with hardware description languages) to clock distribution network synthesis and until a hard limit is not reached for CMOS process (i.e. manifestation of quantum effects in nanoscale devices or the emergence of a new technology that will render CMOS obsolete) this trend will continue to pose new design challenges for the IC design engineer.

As clock frequencies and chip sizes continue to grow, the use of integrated transmission lines for clock distribution becomes more and more tempting as this technique lands itself perfectly on this trend. Unlike other approaches where higher frequencies and bigger silicon area act as opposing parameters, for transmission lines, these two factors act in tandem.

However, the problem of integrated transmission lines, as detailed in [1], [2], lies in the high losses associated with the relatively high resistance of fine metal tracks and this problem aggravates as the minimum feature size in CMOS process nodes continues to decrease.

One mean to overcome this issue, as detailed in [1] and [2], is to use some compensation schemes based on circuits simulating a negative conductance (i.e. negative impedance converter circuits – NICs) so as to cancel the effect of resistive losses. One of the advantages that derive from this loss compensation technique is the possibility to use a salphasic distribution of the clock signal as introduced in [3] and presented for VLSI systems in [2].

As the salphasic distribution technique is based on a standing wave configuration, it requires ideal or low loss transmission lines and it is important to use active loss compensations methods for integrated clock distribution networks. The very high working frequency, due to the nature of the distributed signal along the transmission lines, limits the applicable NIC architectures – i.e. circuits based on simulating a negative impedance with the aid of operational (trans)amplifiers are excluded because of the difficulties and limits that arise in designing the amplifier [4], [5]. Due to their higher frequency limit, the preferred implementations consist of cross-coupled simple stage amplifiers. These configurations can be regarded also as current conveyors [6].

However, a significant drawback of these stages is the dependence of the simulated negative impedance on circuit parameters and hence, process variations.

For instance, given equation (1) that models the behavior of a NIC circuit [1], detailed in the third chapter, the effect of the process parameters can be approximated with the aid of equation (2).

$$Z_{in} = -R - \frac{V_{GS} - V_T}{I_D} \tag{1}$$

$$Z_{in} = -R \cdot \left(1 + \frac{\Delta R}{R}\right) - \frac{V_{GS} - \left(V_T + \Delta V_T\right)}{I_D \cdot \left(1 + \frac{\Delta I_D}{I_D}\right)} \tag{2}$$

Here $\Delta R/R$, ΔV_T and $\Delta I_D/I_D$ stand for process induced variations of integrated resistor value, transistor threshold and, respectively, current gain variations. For typical deep submicron processes, these

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parameters can be as high as 15% to 25% of the nominal values, resulting thus a considerable influence on the simulated negative impedance.
The purpose of this article is to present a practical implementation of a NIC circuit able to compensate for all deviations from the ideal model.

2. LOSS COMPENSATION METHOD BASED ON NIC CIRCUITS

Considering an infinite transmission line driven by a voltage source, the potential in a cross section at distance *r* from the injection point can be expressed as [7]:

$$u(r,t) = U_0^F e^{j\omega t} e^{-\gamma r} + U_0^R e^{j\omega t} e^{\gamma r} \quad (3)$$

$$\gamma = \alpha + j\beta \quad (4)$$

where U_0^F and U_0^R represent the forward and, respectively, the reversed wave amplitudes; γ is the (complex) propagation constant with α the attenuation coefficient and β the phase constant.
As shown in [2], an integrated transmission line used in CMOS technologies presents a relatively high resistive loss that translates in a nonzero, nonneglectable α attenuation coefficient of equation (4).
Unlike in [1] where the per-unit length conductance of the line is given by transistor base currents in a bipolar process, allowing thus the use of a compensation method based on the minimization of the absolute value of the complex propagation constant, for CMOS processes, the compensation method must minimize only the attenuation coefficient. This is because the intrinsic line conductance is neglectable, due to the nature of the typical line load which consists only of MOS transistor gates. Even for nanoscale devices that have nonzero gate currents, the effect of the gate conductance is much smaller than in bipolar technologies.
It is shown in [2] that the required per-unit-length compensation conductance is given by:

$$G_{Comp} = -\frac{R_l \cdot C_l}{L_l} \quad (5)$$

In equation (5) R_l, C_l and L_l are per-unit-length line parameters. In case of a heavily loaded transmission line, the per-unit-length capacitance may be approximated with the load capacitance divided by the length of the line. In this approximation, the per-unit-length inductance depends only on the length of the transmission line [7]. With this model, and knowing the process variations for the load capacitance and line resistance, the compensation conductance may be approximated by equation (6):

$$G_{Comp} = -\frac{c_0^2}{\mu_r \cdot \varepsilon_r \cdot l} R_l \cdot C_G^2 \cdot \left(1 + \frac{\Delta R}{R}\right)\left(1 + \frac{\Delta C_G}{C_G}\right) \quad (6)$$

with l the length of the line, c_0 the speed of light in vacuum, μ_r and ε_r are the relative magnetic permeability and, respectively, the relative electric permittivity of the dielectric material (silicon dioxide) and C_G represents the load (transistor gates) capacitance.
The process induced variation for the needed compensation conductance can be as high as ±30%.
By combining this with the process variations of the simulated negative impedance as given in the first section, the total process variation of the compensation negative conductance can be as high as 45% (i.e. almost a two fold difference between the minimum and maximum negative conductance), hence it is necessary to provide some control means in order to adjust the conductance value to the needed one.
The next section studies two circuit implementations of adjustable negative impedance converters.

3. NIC CIRCUITS

The first solution seen in Fig.1.a uses a bilateral NIC ciruit similar with that of [1]. For the differential mode, this circuit configuration transforms the impedance seen between the sources of the transistors

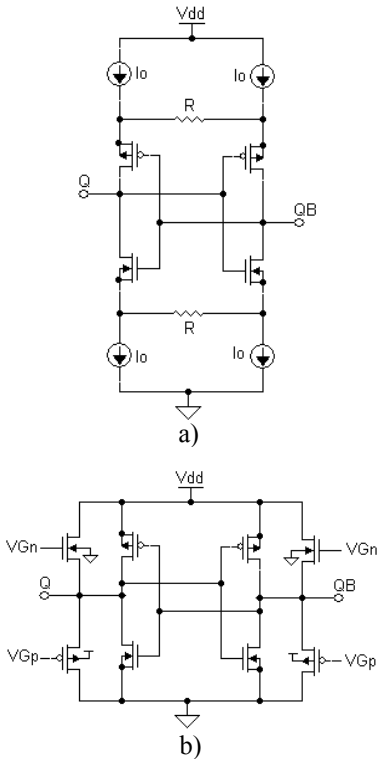

Fig. 1. Negative impedance converters

into an equivalent negative output impedance similar to that of equation (1).

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The output impedance can be adjusted by controlling either the I_0 current or by adjusting the value of the R resistor (using active resistors).
The second solution (Fig.1.b) uses a pair of cross-coupled inverters working on an equivalent load formed by source followers. In order to control the differential simulated negative impedance it is sufficient to adjust the source followers current by changing VGn and VGp voltages.
Using the small signal model of Fig. 2 for the first negative impedance converter circuit, it is possible to derive an equation for the simulated impedance.

$$\begin{aligned} u_+ &= v_{gs2} + Gm \cdot v_{gs2} \cdot R/2 \\ u_- &= v_{gs1} + Gm \cdot v_{gs1} \cdot R/2 \end{aligned} \tag{7}$$

In equation (7), *Gm* is the sum of the equivalent nMOS and pMOS *gm* transconductance for each transistor branch.

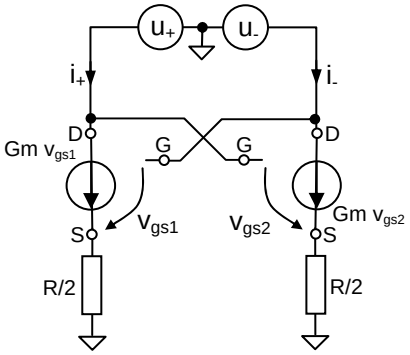

Fig. 2. Small signal model for the NIC circuit of Fig. 1a

Knowing that $i_+ = -i_-$ and that $u_{DIFF} = u_+ - u_-$, by solving the system of equations (7), the resulting expression for the negative impedance is that of equation (8):

$$Z_{in} = -\left(R + \frac{2}{Gm}\right) \tag{8}$$

Considering the transistors in saturation, this last equation can be rewritten as a function of process and operating point parameters as in equation (1) [5]. Note however that equation (1) is a simplified version of equation (9) because it considers only one type of transistors.

$$Z_{in} = -R - \frac{(V_{GSn} - V_{Tn})(V_{GSp} - V_{Tp})}{I_0(V_{GSn} + V_{GSp} - (V_{Tn} + V_{Tp}))} \tag{9}$$

Equation (9) allows one to estimate the process variations for the negative impedance since it depends directly on the transistor threshold voltages and transistor current.
Regarding the quality of this circuit, equation (9) hides the effect of component matching. It should be noted that even if the equation contains only one term in *R* or in I_0, the circuit has 2 resistors and 4 current sources, making the impact of their matching quite important (i.e. for 4 components with random variations, the net effect on the final circuit is two (i.e. square root of 4) times greater than for a single component of the same type [5]).
For the second NIC circuit, the equivalent small signal model can be found in Fig. 3.
Here again, starting form the system of equation (10), it is possible to derive the simulated negative impedance.

$$\begin{aligned} i_+ + Gm_{SF} \cdot v_{gs\_SF1} &= Gm \cdot v_{gs1} \\ i_- + Gm_{SF} \cdot v_{gs\_SF2} &= Gm \cdot v_{gs2} \end{aligned} \tag{10}$$

Noting that, again, $i_+ = -i_-$ and $u_{DIFF} = u_+ - u_-$ and replacing the gate to source voltages according to the circuit configuration, gives a simulated impedance of:

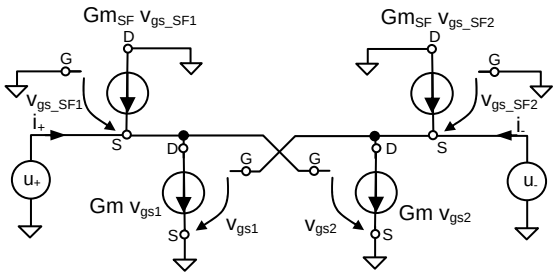

Fig. 3 Small signal model for the NIC circuit of Fig. 1b

$$Z_{in} = -\frac{2}{Gm - Gm_{SF}} \tag{11}$$

In equation (11), *Gm* stands for the sum of the transconductances of the inverter nMOS and pMOS transistors while Gm_{SF} stands for the sum of the transconductances of the source follower stages transistors.
As was done for equation (8), it is possible to rewrite the terms of equation (11) as a function of the process and operating point parameters. Note that for a correctly sized circuit, there should be no static current circulation between the source follower stages and the inverter stages. This means that it is possible to approximate the DC current of the inverter stage with I_0 and that of the source follower stage with I_{SF}.

$$Gm = I_0\left(\frac{1}{V_{GSn} - V_{Tn}} + \frac{1}{V_{GSp} - V_{Tp}}\right) \tag{12}$$

$$Gm_{SF} = I_{SF}\left(\frac{1}{V_{GSn\_SF} - V_{Tn}} + \frac{1}{V_{GSp\_SF} - V_{Tp}}\right) \tag{13}$$

An important difference that can be seen between the two circuit implementations is the sign of the simulated impedance which for the first circuit is always negative while for the second one, it depends

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on the relative transconductance magnitudes of the source followers stage and inverter stage. However, it is possible to size the stages so as to always assure that the source follower stage has a lower transconductance than the inverter stage, in all operating conditions, making the simulated impedance negative in all process corners.
Regarding the process and random variations, both circuits exhibit similar behavior. In principle, the second circuit should have a lower variation since it has fewer circuit elements, but the complexity of the controlling circuit (not shown in Fig. 1b) cancels this effect.
The main difference between the circuits is the allowable input-output voltage swing. Since the first NIC has two current sources placed in series with the main transistors, the voltage swing is limited by the overdrive voltages of the current source transistors. Even more, if the adjustment method is based on the control of the transistor transconductances, this problem is aggravated because, as the circuit current is changed, so do the transistor's overdrive voltages change. This means that for low magnitude negative impedances, for which transistor *gm*s must be large, the remaining signal voltage headroom becomes limited to only a few hundreds milivolts.
This problem does not exist for the second circuit configuration since the control of the negative impedance is achieved by adjusting the current of the source follower's stages. In this way, the effect of the controlling current on the large signal behavior of the circuit is minimized.
Another important difference is the parasitic capacitance. In order to allow reasonably large signal swings, the first circuit implementation of the negative impedance converter needs quite large transistors (for low overdrive voltages) but this translates in larger parasitic capacitances. With larger parasitic capacitance comes also a lower bandwidth compared with the second NIC circuit.
It should be noted that also the second circuit implementation suffers from several drawbacks, for instance, the need to maintain the output common mode voltage unaffected by the controlling current. This translates in a more complex circuit implementation, but this is, in general [5], [6], the price paid for better performance.
The version of Fig. 1b of the NIC circuit will be further analyzed in the next section.

4. PRACTICAL IMPLEMENTATION OF A NIC CIRCUIT

Equation (11) can be used to size the main transistors of the NIC circuit starting from the requirements regarding the simulated negative impedance and the needed variation to maintain transmission line compensation over all process corners. The process variation can be estimated based on the expected variation of the compensation conductance (this includes all the variations associated with the parameters of the integrated transmission lines) in concert with the expected variation for the negative impedance converter circuit.
Assuming a nominal compensation conductance of 200 ohms and a process variation of 150 to 300 ohms, equation (1) can be used to get the nominal values for the transistors transconductances. Another parameter needed here is the allowable compensation current variation. This is important because the transconductance is proportional with the square root of the drain current so, a too large variation for the transistor transconductance translates in an even larger variation for the transistor current. A maximum current variation of 4 times is chosen.
With all these we get the required transconductances – system of equation (14). Gm_{MAX}, Gm_{MIN}, Gm_{SF_MAX} and Gm_{SF_MIN} represent the process variations of the nominal transistor transconductances while I_{MIN} is the minimum source follower current and I_0 is the nominal source follower current.

$$\begin{aligned} |Z_{in}|_{MIN} &= \frac{2}{Gm_{MAX} - Gm_{SF\_MAX} \cdot \sqrt{I_{MIN}/I_{SF}}} \\ |Z_{in}|_{MAX} &= \frac{2}{Gm_{MIN} - Gm_{SF\_MIN} \cdot \sqrt{4I_{MIN}/I_{SF}}} \\ |Z_{in}| &= \frac{2}{Gm - Gm_{SF}} \end{aligned} \tag{14}$$

For the chosen process (a 0.13µm standard CMOS process), the process variations for the transistor transconductances is about ±20% so $Gm_{MIN} = 0.8Gm$, $Gm_{MAX} = 1.2Gm$.
With these parameters, by summing the first two equations of equation system (14), we get the ratio between the minimum and the nominal source follower current to be equal with $(1/1.4)^2$. This means that for a nominal current of 250µA, the minimum current will be 127.5µA and the maximum current will be about 510µA.
The nominal sums of transistor transconductances results $Gm \approx 27.8$mS and $Gm_{SF} \approx 7.8$mS. Assuming equal *gm* transconductances for the nMOS and pMOS transistors gives a nominal value of 13.9mS for the inverter transistors and 3.9mS for the source followers.
In the next step it is necessary to establish the nominal currents and transistor sizes.
For the source follower stage, as was already said, the chosen nominal current is 250µA and it is imposed with the aid of the control circuit. From this, using equation (15) it is possible to get the *W/L* ratio:

$$\left.\frac{W}{L}\right|_{SF} = \frac{gm_{SF}^2}{2K \cdot I_{SF}} \tag{15}$$

For the inverter stages, the nominal current is imposed by the common mode DC potential in combination with the required transconductance as in equation (16). Equation (17) determines the transistor sizes:

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$$I_0 = \frac{gm(V_{GS} - V_T)}{2} \quad (16)$$

$$\frac{W}{L} = \frac{gm}{K(V_{GS} - V_T)} \quad (17)$$

For better performance in the nominal case, the common mode DC potential is chosen to be half the supply voltage, 0.6V for a standard 0.13µm process, giving a gate to source voltage for the inverter transistors of 0.6V.

Knowing the DC operating conditions for the nominal case, the process current gain for the MOS transistors (Kn = 465µA/V^2, Kp = 76µA/V^2) and choosing the minimum length of 0.12 µm the resulting transistors widths are as follows: Wn = 15.36µm, Wp = 94µm, Wn_{SF} = 7.85µm and Wp_{SF} = 48µm. The inverter stage nominal current (one inverter) is 1.62mA.

At this point it must be said that this calculated values serve only as a reference point because the used model does not include mobility saturation or other second order effects.

Regarding the control circuit for this NIC, the circuit must allow the control of the source follower stage current without affecting the output common mode voltage. This is achieved with the aid of feedback loops that control the common mode as seen in Fig. 4.

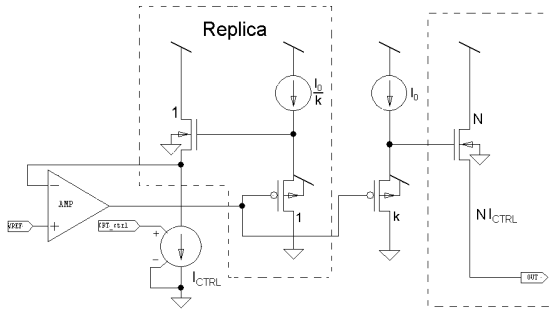

Fig. 4. Simplified circuit diagram for the NIC control circuit

Fig. 4 is a simplified version of the control circuit for better illustration of the concept as it presents only the control part for nMOS source follower (the rightmost transistor). A similar circuit must be constructed for the pMOS source follower (by changing all transistor types and the connection of the control current source).

The two inputs of this circuit are the common mode reference voltage and the control current. However, it is evident from the previous figure that these inputs do not act directly over the source followers but through a replica circuit. Basically, the replica circuit mimics the static behavior of the NIC source followers.

Analyzing the circuit of Fig. 4, it is evident that the feedback loop controls the gate of two pMOS source followers with the widths in a ratio of k. The smaller source follower, in turn, will set the gate potential for the replica source follower such as to have a desired voltage in the source terminal. By noting that the output source follower is in fact a multiple of the replica nMOS source follower, the output common mode DC potential must also be equal with that set by the feedback loop.

The simulated negative impedance is controlled by changing the current of the replica source follower. Again, because the output source follower is a multiple of the replica circuit, the output current is a multiple of the control current, allowing thus independent control of the output current and common mode voltage. The reference voltage for the common mode output potential can be e fixed voltage source independent of process variations (i.e. a band-gap source) but for better performance, it is recommended to generate this reference with a replica of the NIC circuit inverters stage. In this way, the source followers stage will output a voltage close to the voltage required by the inverter stages, minimizing the static current circulation between the stages (a condition used during the design of the negative impedance converter).

5. SIMULATION RESULTS

The circuit was simulated starting from the transistor sizes determined in the previous section. As was already said, the model neglects velocity saturation so these values should be used only as starting points. After several adjustments for transistor sizes, the final circuit behaved closed to the desired characteristics.

As it can be seen in Fig. 5, the simulated negative impedance varies from about – 164 ohms to about –290 ohms for the worst corner case.

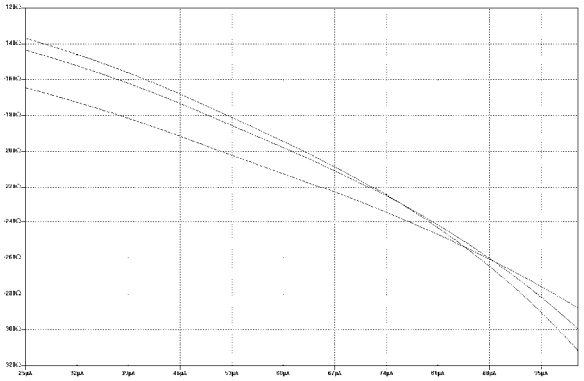

Fig. 5. Simulated variation versus controlling current of the negative impedance over process variations

It is evident from the previous figure that the controlling current is adjusted only between 25 and 100µA instead of around 125µA to about 500µA. This is because the replica circuit is 5 times smaller than the source follower stage.

Fig. 6 presents some large signal simulations. It can be seen that at 1GHz and small signal amplitudes, the NIC circuit regenerates the signal while for full swing input signal the circuit saturates at some distance to the supply lines. For these tests, the circuit was excited by a voltage source in series with a resistor.

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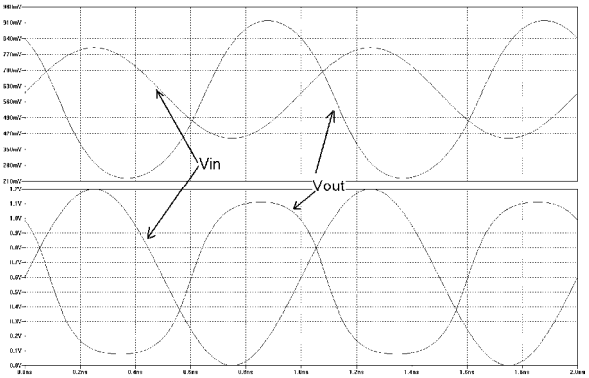

Fig. 6. NIC circuit large signal behavior

The current consumption of the final circuit was 4.65mA at 1.2V and nominal operating conditions (this figure excludes the feedback loops operational amplifiers and bias generators for the current sources used in the replica cells). For the inverter stages, the final current is 1.7mA per inverter and for the source followers is 275µA. The difference between this value and the desired 250µA is due to current multiplication errors from the replica circuit to the final source follower stages.

6. CONCLUSIONS

The present article detailed the role of a negative impedance converter circuit in integrated clock distribution networks. As circuit sizes continue to grow and as the operating frequency is in the GHz range, it becomes more attractive to use integrated transmission lines when designing clock distribution networks. However, these transmission lines suffer from substantial resistive losses due to the fine scale of the integrated traces. As was presented in the introduction and the second section on the role of NIC circuits, these losses may be compensated with the aid of simulated negative conductances, obtained with NIC circuits.

The next section compares two NIC circuit implementations. The first circuit, altough more efficient with respect to the ocupied silicon area and current consumption, suffers from reduced voltage swings and higher parasitic capacitance (which, in turn, limit the maximum operating frequency).

The second circuit deals with these last two problems by increasing the complexity of the controlling circuit (and hence larger area and current consumption) and by reducing the number of stacked transistors to a minimum of two transistors per branch.

Simulations have shown a good circuit operation, close to the requirements set in the practical implementation section.

REFERENCES

[1] Matthias Buβmann, Ulrich Langmann, *"Active Compensation of Interconnect Losses for Multi-GHz Clock distribution Networks"*, IEEE Trans. Circuits Syst. –II: Analog and digital Signal Processing, vol. 39, no.11, pp. 790 – 798, 1992

[2] Andrei Paşca, *"Probleme speciale ce apar in reţelele de distribuţie de clock"*, MSc Thesis, "Politehnica" University, Timişoara, 2006

[3] Vernon L. Chi, *"Salphasic Distribution of Clock Signals for Synchronous Systems"*, IEEE Trans. Comput., vol. 43, no. 5, pp. 597 – 602, 1994

[4] Lucian Jurca, Mircea Ciugudean, *"Circuite integrate analogice"*, Ed. Politehnica, Timişoara, 2004

[5] Behzad Razavi, *"Design of Analog CMOS Integrated Circuits"*, McGraw-Hill, 2001

[6] Chris Toumazou, Nick Battersby, Sonia Porta, *"Circuits and Systems Tutorials"*, Wiley-IEEE Press, 1995.

[7] Aldo de Sabata, *"Tehnica frecvenţelor înalte"*, Ed. Orizonturi Universitare, 2001

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