CMOS Temperature Sensors Using Peaking Current Source

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Abstract – Two new CMOS analog temperature sensors, obtained from known reference voltage sources, are presented. They are realized by two cross-connected current mirrors, one of which being a peaking source. The temperature sensor behaviour was obtained here by corresponding design, made with the goal to achieve a maximum output-voltage slope. The two circuits were conceived in 0.35μm CMOS process and realize some superior performances in comparison with known analog temperature sensors: slope of order 1.5mV/ºC, minimum supply voltage of 1.5V, small supply current, very good SR and PSRR parameters, small area on chip. The output-voltage total process variation is 2%.

Keywords: temperature sensors, CMOS analog sensors, process variation

I. INTRODUCTION

The performing smart temperature sensors are more and more used in VLSI modern systems. One may find from the publications the temperature sensors in CMOS chips constitute an important academic and industrial research subject of last 20 years. The actuality of the research in the domain of smart temperature sensors is proved by the great number of published papers, books and PhD theses.

In [2] a great number of applications, requiring the temperature sensor use, were gathered up. The domain stage of the analog temperature sensors, representing the front-end part of the smart sensors, is commented. Were presented the numerous conditions imposed to integrated temperature sensors. Based on bibliographic study (over 50 papers, books and PhD theses) one achieved, on much criteria, a more complete classification than the encountered in publications one. There too, were presented comparatively and were commented the known or estimated by the author performances of the proper (front-end) analog sensors, separately from the smart sensors. The table which presents the comparative performances of known sensors shows the fact that neither sensor fulfils simultaneously all the imposed requirements, especially that of scheme complexity and the output voltage or current process variation. This means the researches aiming sensor improvement must be continued.

Then, in [2] were presented and analyzed some known proper (front-end) analog temperature sensors, based on two cross-connected current mirrors, with their advantages and disadvantages. This type of temperature sensors has been studied thoroughly because it is just the thesis subject. Thus, have been analyzed the schemes and performances presented in [3], [4], [5], whose circuits are not very complex and include two cross-connected current mirrors. The most close as circuit structure to our work is the sensor in [4], shown in Fig. 1.
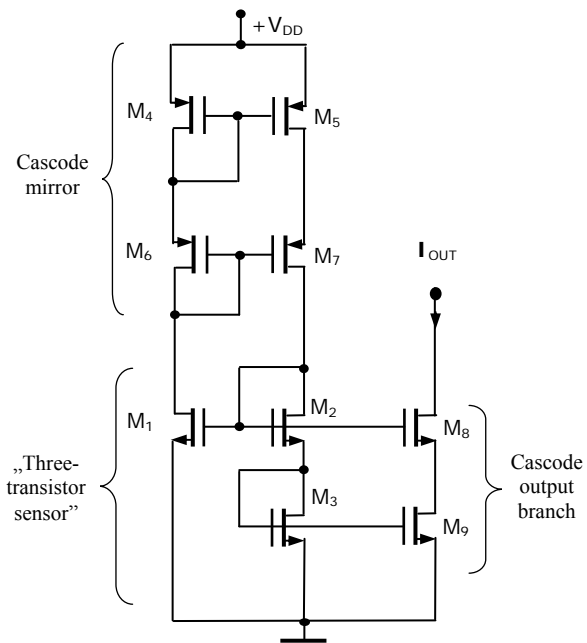

Fig. 1. Analog temperature sensor in [4]

This is a combination between a lower modified-simple mirror (M_1, M_2 and the extra diode M_3), an upper cascode mirror and a current-output cascode-configuration branch (M_8, M_9).

The scheme in Fig. 1 has the advantages:

- reduced component quantity (9 transistors) and occupied-on-chip area,

- good output-current slope (the sensor sensibility),

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- good isolation of the output against supply-voltage perturbations (thanks to cascodes).

The scheme disadvantages are:

- high supply-voltage minimum value, 5V (for CMOS-1μm process, which may be scaled),

- high nonlinearity of current-temperature characteristic,

- lack of process-variation-effect (on the output current) verification, which may be important because of V_T-voltage dependence on process parameters.

Another above-cited two schemes, [3], [5], include more complex circuits (15 transistors and 3 bias-voltage sources respectively 10 transistors and 3 bias-voltage sources).

Table 1 presents comparatively the performances of above-cited three analog temperature sensors. Some of sensor's data do not exist in the respective papers. One may see the sensor sensibility is modest or even poor, and sensible smaller as another-principle schemes or those proposed by us ourselves in [2]. Then, some of these schemes have higher complexity and nonlinearity. Some performances are obtained by cascode configurations.

It may be observed, one not yet disposes of an analog circuit which fulfils all the requirements imposed to front-end temperature sensors in the smart sensors.

None of these schemes use the Wilson-peaking or Widlar-peaking configuration, proposed in this work. Our sensor schemes or another close to this, have not been encountered in literature with the destination of temperature sensor but with that of current or voltage references [1], [6], [7].

The basic idea to achieving the two sensors started from known identical reference voltage source schemes [1] which were designed here so the output voltage has a strong temperature linear dependency and maximum slope.

The proposed circuits consist of two classical cross-connected mirrors, where the lower mirror is a Wilson or modified-Widlar one [1] (with an extra diode on the left branch) and the upper one is a peaking mirror. The schematic uses integrated resistors whose I-order temperature coefficient is of particular type.

Section II presents the proposed Wilson-peaking temperature sensor and his performances. Section III presents the proposed Widlar-peaking one and his performances. Section IV presents the conclusions of this paper.

Table 1. Some proper-analog (front-end)-temperature-sensor performances

Ref.	CMOS process	Component number	Chip area	Sensibility (slope)	Temperature range	Nonlinearity	Process variation	V_{DDmin} / Supply current
	[μm]		μm²		°C	%	%	V / μA
[3]	0.8	27		0.7 mV/°C	-43...127	0.12		1,6 / 0,03
[4]	1	9	2800	0.08 μA/°C	10...100	±1.5		5 / 20
[5]	0.18	>20	1320	5.6 nA/°C	0...80	1.3	4	1,8 / 25

II. THE WILSON-PEAKING SENSOR

The circuit, shown in Fig.2, achieved by a cross-connection of a lower modified-Wilson current mirror (M_1, M_2 and R_1) and an upper peaking mirror (M_3, M_4 and R_2), is known as voltage reference [1] but, in our work, it is converted by design in a temperature sensor [2]. The output is considered not charged but the load (resistor) may be included in parallel with R_1. The output-voltage thermal-sensibility calculus and sensibility optimisation may be done in a same procedural manner as that presented in [2] but it is extremely complex because the transistors M_1 and M_4 work in weak-inversion regime.

The simulation of the Wilson-peaking sensor of Fig.2 has been done in the temperature range of -30...120ºC. To find the output-voltage maximum slope one achieved a great quantity of simulations, for different values of: R_1 and R_2 resistors and resistance temperature coefficients (type NTC and PTC resistors). The best results were obtained for: R_1=80kΩ, R_4=2.7kΩ, both of NTC type, and transistor dimensions: $L_{1,2,3,4}$=5μm, W_1=85μm, W_2=5μm, W_3=0,5μm and W_4=80μm.

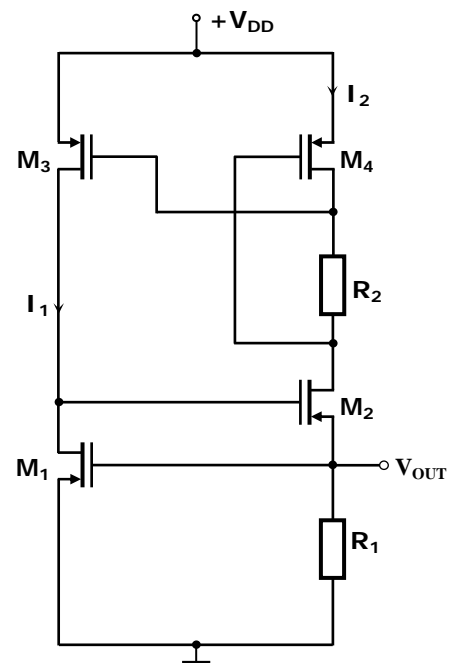Comparatively with known schemes, analysed in [2], this type of sensor presents some good performances:

Fig. 2. Wilson-peaking temperature-sensor scheme

output-voltage slope of -1.55mV/°C, nonlinearity of 0.53% (Fig.3), minimum supply voltage V_{DDmin}=1.5V (Fig.4), factors SR=811ppm/V and PSRR=67dB (at low frequency, 27°C and V_{DD}=3.5V, Fig.5), supply current of 4.8 µA, occupied-on-chip area of only 2800µm^2. One finds the analyzed circuit furnishes a negative-slope output voltage.

Especial performances were obtained as a result of simulations to process variations (for BC and WC parameters) (Fig.6). Thus, for particular resistor widths (3.14µm for R_1 and 9.45µm for R_2), one obtained an output-voltage total process variation of only 8% at 120ºC temperature.
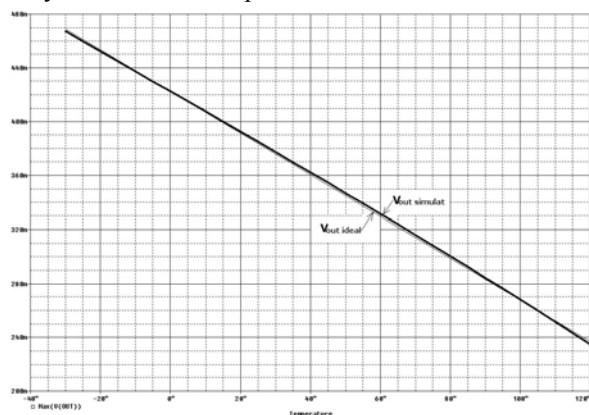
Fig. 3. Output-voltage variation against temperature for Wilson-peaking sensor
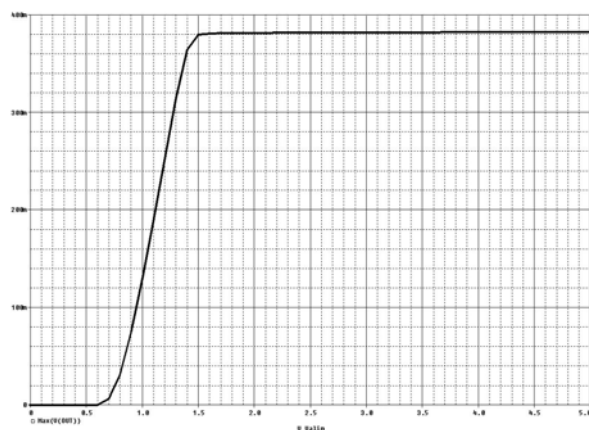

Fig. 4. Output-voltage versus supply-voltage dependency for Wilson-peaking sensor
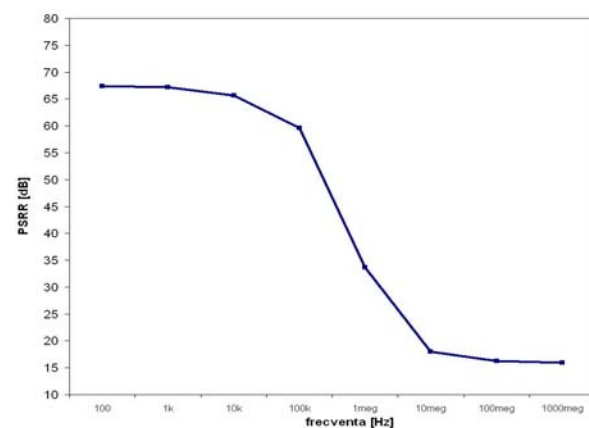

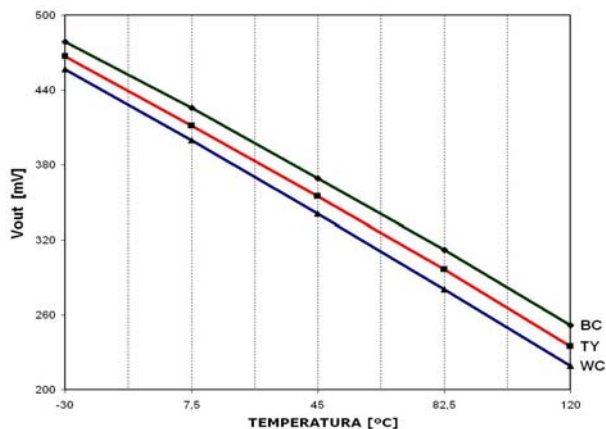Fig. 5. PSRR versus frequency dependency for the Wilson-peaking sensor

Fig.6. Process and temperature dependency of the Wilson-peaking-sensor output voltage

III. THE WIDLAR-PEAKING SENZOR

The sensor circuit, shown in Fig.7, is achieved by a lower modified-Widlar current mirror (M_1, M_2, M_5 and R_1) and an upper peaking mirror (M_3, M_4 and R_2), used as voltage reference in [1], but converted here by design in a temperature sensor [2].
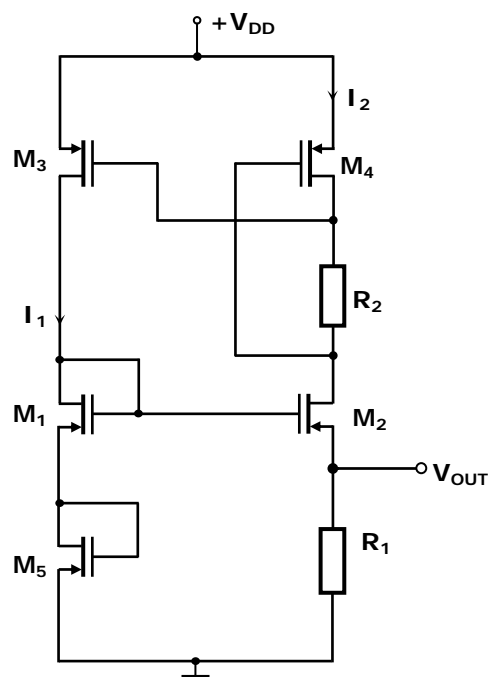

Fig. 7. Widlar-peaking temperature-sensor scheme

The output-voltage thermal-sensibility calculus and sensibility optimisation may be done in a same procedural manner as that presented in [2] but, here too, it is extremely complicated because the transistors M_1 and M_4 work in weak-inversion regime. The simulation of the Widlar-peaking sensor of Fig.7 has been done in the temperature range of -30...120ºC. To find the output-voltage maximum slope one achieved a great quantity of simulations, for different values of: R_1 and R_2 resistors and resistance temperature coefficients (type NTC and PTC resistors). The best results were obtained for:

R$_1$=60kΩ, R$_2$=2kΩ, both of NTC type, and transistor dimensions: L$_{1,2,3,4}$=5μm, W$_1$=30μm, W$_2$=80μm, W$_3$=3μm, W$_4$=95μm and W$_5$=95μm.

Comparatively with the known schemes, analysed in [2], this type of sensor presents some very good performances: output-voltage slope of -1.49mV/°C (Fig.8), nonlinearity of 0.51%, minimum supply voltage V$_{DDmin}$=1.4V (Fig.9), factors SR=5620ppm/V and PSRR=64dB (at low frequency, 27°C and V$_{DD}$=3.5V, Fig.10), supply current of 6.2μA, occupied-on-chip area of 3810μm^2. One finds the analyzed circuit furnishes a negative-slope output voltage too.
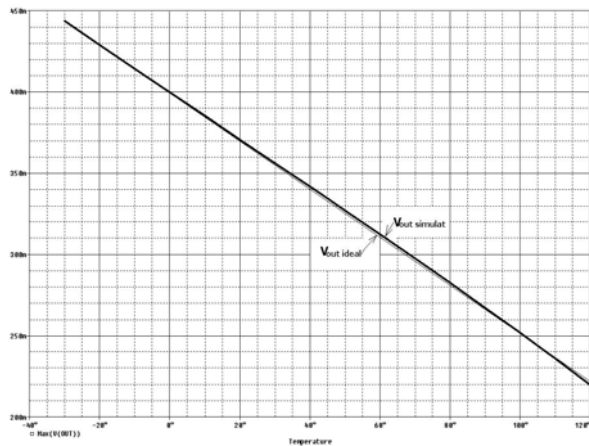

Fig.8. Output-voltage variation against temperature for Widlar-peaking sensor
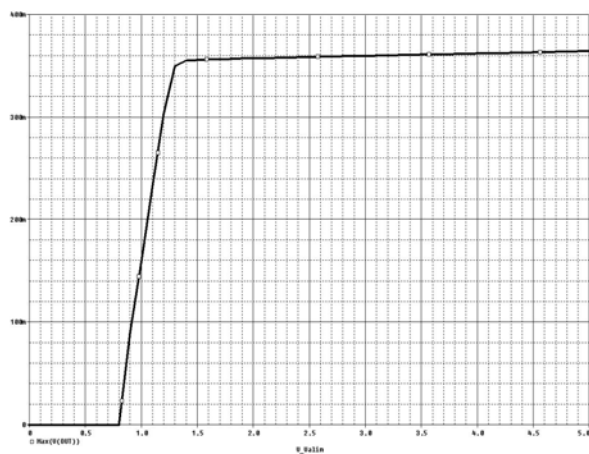

Fig.9. Output-voltage versus supply-voltage dependency for Widlar-peaking sensor

Distinct performances were obtained as a result of simulations to process variations (for BC and WC parameters). Thus, for particular resistor widths (3.52μm for R$_1$ and 4.32μm for R$_2$), one obtained an output-voltage total process variation of only 2% at 120ºC temperature (Fig.11).

At such a small process variations of the sensor output, a Monte Carlo simulation was obligatory, which considers the process geometrical errors too, especially those of transistor and resistor mismatches. From the output-voltage histogram a standard deviation σ=4,3mV results. This means, in 99.7% cases, the output-voltage deviation from the medium

value (302mV) do not exceeds 6σ=25.8mV or 8.5% (Fig.12). This is, as expected, greater than the above total process variation for BC and WC parameters.

The Monte Carlo simulation for the Widlar-peaking sensor confirms the efficiency of the output process-variation reduction technique by finding the resistor optimum widths. To diminish the standard deviation it is possible to reduce the great resistor R$_1$ value. Thus, one may decrease the 6σ quantity towards the same value as the total process variation, namely 5% [2].
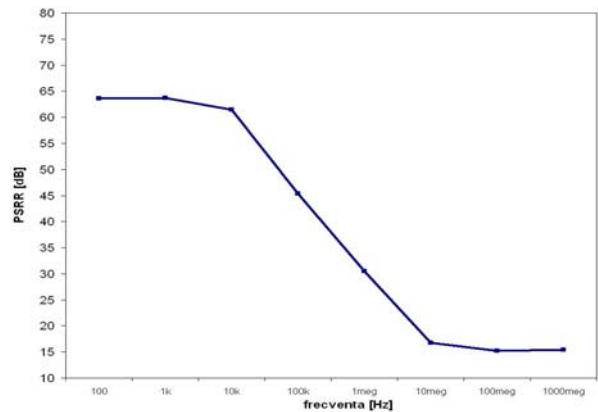

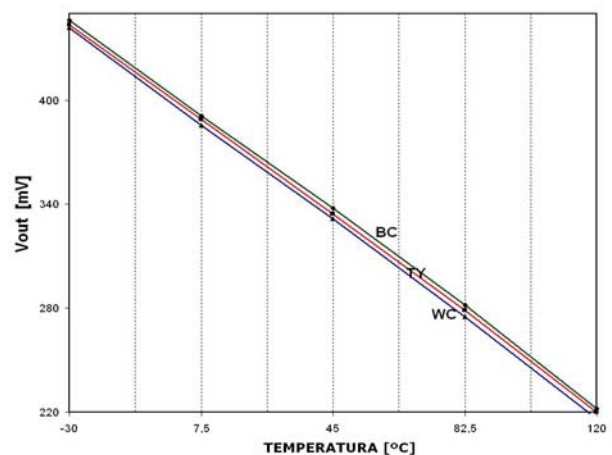Fig.10. PSRR versus frequency dependency for Widlar-peaking sensor

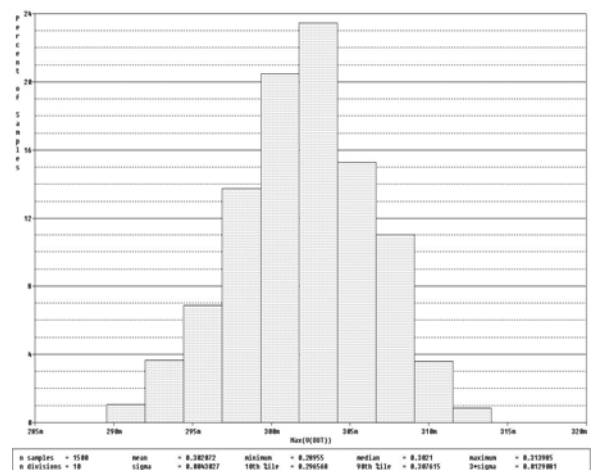Fig.11. Process and temperature dependency of the Wilson-peaking-sensor output voltage

Fig.12. Output-voltage hystogram for the Widlar-peaking sensor at 120ºC

Table 2. Comparison with front-end sensors of previous works.

Reference	Process	Component number	Area on chip	Sensitivity (slope)	Range	Nonlinearity	Process variations	PSRR	$V_{DD\,min}$/ Supply current
	µm		µm²	mV/°C	°C	%	%	dB	V / µA
[5]	0.18	>20	1320	5.6nA/°C	0...80	1.3	4		1.8/25
[8]	0.09	>14	300	1.8	30...160		4		1 /25
[9]	0.18	21	12600	0.18	-60...140	2	>6		1.6/
[10]	0.35	>35	0.5mm²	2.3*	20...120	1			3 /
This work	0.35	7	3810	-1.49	-30...120	0.51	2	64	1.4/6.2

The sign * marks the use of an amplifier to obtain a great slope.

Similar performances have been documented in literature (Table 2); however such results are based on more complex circuit, occupying extended areas on chip (consider the scaling) and having poorer linearity and process variation.

IV. CONCLUSIONS

In this work two new CMOS analog circuits, whose output voltage varies linearly with temperature, are presented. They are realized by two cross-connected current mirrors, one of which being a peaking source, known as reference voltage sources [1]. The temperature sensor behaviour was obtained here by corresponding design in 0.35 µm CMOS process [2] and using particular resistor temperature coefficients. The sensor sizing is made with the goal to obtain a maximum output-voltage slope.

It is used a very simple technique from [1], to reduce the output-voltage total process variation by finding the resistor optimum widths. This is very important because it permits to simplify the next sensor trimming circuits.

The new-sensor circuits are very simple but the obtained performances are very interesting and superior to that of much known sensors cited in references.

Thus, the Wilson-peaking sensor has some good performances: output-voltage slope of 1.55mV/°C, nonlinearity of 0.53%, minimum supply voltage V_{DDmin}=1.5V, factors SR = 810ppm/V and PSRR = 67dB (at low frequency, 27°C and V_{DD}=3.5V), supply current of 4.8 µA (at 27 ºC), occupied-on-chip area of only 2800µm², output-voltage total process variation of 8% (at 120ºC).

The Widlar-peaking sensor has some better performances: output-voltage slope of 1.49mV/°C, nonlinearity of 0.51%, minimum supply voltage V_{DDmin}=1.4V, factors SR = 2110ppm/V and PSRR = 64dB (at low frequency, 27°C and V_{DD}=3.5V), supply current of 6.2 µA (at 27 ºC), occupied-on-chip area of only 3810µm², output-voltage total process variation of 2% (at 120ºC).

The Monte Carlo simulation for the Widlar-peaking sensor confirms the efficiency of the output process-variation reduction technique by finding the resistor optimum widths.

Similar performances have been documented in literature; however such results are based on more complex circuits, occupying larger areas on chip and having poorer linearity and process variation.

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